1. **Create new folder in desktop. Open the new terminal from the same folder.**

2. For sourcing the script file
⇨ **csh**
⇨ **source /home/installs/cshrc**

3. For creating library file
⇨ **gedit cds.lib (Define design_lib ./design.lib)**
⇨ **gedit hdl.var**
(Define WORK design_lib
Define NCELABOPTS –messages)
mkdir design.lib

shift : wq

⇨ **gedit filename.v** (To create Verilog file in vi editor)
⇨ **gedit file_testbench.v** (To create Verilog Testbench file in vi editor)
⇨ **ncvlog filename.v –mess** (compile the code)
⇨ **ncvlog file_testbench.v –mess** (compile the testbench code)

patest

⇨ **ncelab testbench module name –access +rwc -mess** (to elaborate)
⇨ **ncsim testbench module name -gui** (to simulate)

patest R ↵ on patest Send to w/f window
Run button

5. For Synthesis

For Combinational circuits

genus -gui

//Reading the library files
read_lib /home/installs/FOUNDRY/digital/45nm/dig/lib/slow.lib

```
read_hdl filename.v

elaborate

//sdc file (Need to write for all input and output ports which are there in the program)
set_input_delay -max 0.2   [get_ports "i/p"]
set_input_delay -max 0.2   [get_ports "i/p"]
set_output_delay -max 0.2 [get_ports "o/p"]
```

```
set_db syn_generic_effort medium
set_db syn_map_effort medium
set_db syn_opt_effort medium
syn_generic  // Translation: converts program to basic gates
syn_map   // Mapping: converts logic to basic gates
syn_opt //optimization
```



```
set_output_delay -max 0.2 [get_ports "o/p"]
set_output_delay -max 0.2 [get_ports "o/p"]

// if d
/ a

set_db syn_generic_effort medium
set_db syn_map_effort medium
set_db syn_opt_effort medium
syn_generic        // Translation: converts program to basic gates
syn_map            // Mapping: converts logic to basic gates
syn_opt            //optimization
report_power >filename_report.rpt
report_area >filename_area.rpt
report_gates >filename_gates.rpt
report_timing -unconstrained >filename_timing.rpt
gui_show
```

For Sequential Circuit

genus
//Reading the library files
read_lib /home/installs/FOUNDRY/digital/45nm/dig/lib/slow.lib ///PATH OF LIBRARY FILE

//2-lef files need to be copied

set_db lef_library {/home/installs/FOUNDRY/digital/45nm/dig/lef/gsclib045_macro.lef /home/installs/FOUNDRY/digital/45nm/dig/lef/gsclib045_tech.lef}
read_hdl filename.v
elaborate

//sdc file
create_clock -name clk -period 2 -waveform {0 1} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 0.2 [get_ports "i/p"] -clock [get_clocks "clk"]
set_input_delay -max 0.2 [get_ports "i/p"] -clock [get_clocks "clk"]
set_input_delay -max 0.2 [get_ports "i/p"]
set_input_delay -max 0.2 [get_ports "i/p"]