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A SURVEY OF LOW-VOLTAGE LOW-POWER TECHNIQUES AND CHALLENGES FOR CMOS DIGITAL CIRCUITS

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Low-power design is an important research in recent years. A huge amount of papers in the open literature until now were proposed to deal with various low-power issues, including technology innovation, circuit/logic design techniques, algorithm realization, and architecture/system selection. Due to the high-energy electron effect and reliability consideration, it is necessary to further reduce the supply voltage of integrated circuit in CMOS sub-micro technologies. However, it is hard to get a whole view for various low-power low-voltage techniques in a short time. In this paper, the motivations and challenges of CMOS low-voltage low-power circuit are addressed. Various design methodologies are surveyed and summarized in whole. The paper attempts to quickly give readers a full-view conception in low-voltage low-power CMOS system design.

Keywords: Low voltage; low power; LVLP.

1. Introduction

Consumer electronics such as multimedia players, portable electrical equipments, and outdoor measuring/test devices are commonly used today. More portable computers, biomedical units,[1] and mobile phones have become an important means in human life. The lighter weight and longer available time of these devices are essential requirements. As a result, design of low-voltage operation and low-power consumption are necessary. Furthermore, CMOS technologies are continuously scaled down to embed more transistors within a small chip area by process innovations. This means that the lateral-and-vertical dimension of transistor is getting more thin and compact than previous technology. The improvements of operating

speed, cost reduction, and SoC (system-on-a-chip) physical realization are outstanding, but at the expense of a great impact on reliability and leakage current. Due to the hot-electron effect and device reliable issues, the voltage supply of the integrated circuit is needed to further reduce. Therefore, design of low-voltage low-power (LVLP) CMOS circuits in a sub-micro technology for today's requirements is important and useful. Many papers in open literature and text books are published to describe the LVLP techniques.[2−45] References 31−33 are devoted to power reduction for memory design, while Refs. 34−36 focus on low-power FPGA design. These various techniques are based on different viewpoints: fabrication technology, circuit design, logic realization, data code representations, architecture selection, and algorithm/function implementation methodologies. It is difficult and impractical to describe all these sophisticated techniques in detail within a limited page length. In this paper, however, we attempt to summarize some important techniques for LVLP chip designs especially for CMOS sub-micro technologies. In addition, motivation and challenges of LVLP design are described to extend the generality of the paper. We expect that the related material summarized in this paper is useful for any IC designer interesting in low-voltage low-power design.

The paper is organized as follows. Section 2 describes the motivation of LVLP circuit in sub-micro technologies. The obstacles and challenges of LVLP CMOS circuit design are then described in Sec. 3. Section 4 points out various LVLP design methodologies. A variety of design techniques are systematically explained. Finally, a brief conclusion is given.

2. Motivation of LVLP Design

There are many reasons to explain why the low-power design is necessary. It is obvious that sustained consumption of more energy will make a great deep and far impact on environment. It is abnormal for drastic climate, drought, and flood occurring frequently in recent years. Most importantly, the "energy" in the earth is limited. Based on electrical viewpoint, how to effectively reduce the power consumption and improve the energy efficiency are still hot and popular researches.

(1) Portable/mobile requirement: more functions of commercial products are progressively integrated in a single chip. Today, system-on-a-chip (SoC) is feasible and realistic. In order to enhance the convenience in use, more commercial products are manufactured in portable type and with smaller volume. As a result, low-power design is necessary to extend the available working time of these products. Looking forward to have a long available time of portable devices may be an initial motivation of low-power circuits. Currently, low-power design is an essential and key requirement for design of portable device.

(2) Weight consideration: traditionally, supply voltage 12 V, 9 V, 5 V, or 3 V is commonly used in electronic devices. Due to the 1.5 V battery unit cell still used,

many cells are respectively cascaded in an equipment to attain the corresponding required supply voltage. Obviously, the weight of device is increased going along with the number of battery cells. It is annoying that portable product has a heavy weight.

(3) Reliability: since semiconductor fabrication is continuously improving via thinner oxides, reduced device size, smaller line-to-line space, and so forth, supply voltage is necessary to scaled down to improve device "reliability". The "reliability" issue is the main reason to drive the circuit in low-voltage operation. Under the condition of a fixed voltage supply, both the intensities of vertical electrical field and lateral electrical field are increased when CMOS transistors are scaled down. When electrical field is increased, the carrier (free electron or hole) in channel will be in high energy state, which is abbreviated as "hot electron". The higher energy carrier will impact the fixed atom existed in channel interface or oxide–semiconductor interface. As a result, more mobile electron–hole pairs are generated to induce gate/substrate leakage current. It is a major source of power consumption in sub-micro CMOS circuits. In addition, some of the high-energy carriers trapped into the interface of oxide–semiconductor result in the variation of threshold voltage.

(4) Temperature and heat considerations: an improper temperature will make great impact on semiconductor's characteristic. Many circuit parameters such as reverse-biased saturation current (I_o), threshold voltage (V_T), carrier mobility (u), intrinsic concentration (n_i) are sensitive to temperature variation. When circuits operate in high power consumption, the average temperature of whole chip will be raised. Due to the temperature gradient existed in the chip, the variations of different parameters result in current fluctuation. This effect is an iterative procedure until the bias-point saturation or chip burned down. The stability of the integrated circuit is strongly dependent on temperature and power consumption.

(5) IC package: in practicality, ICs are almost mounted in a printed-circuit board for system integration. In order to increase mechanical strength and protect from outer dust-and-humidity, the chips are often packaged (plastic, ceramic, or plastic compound material) and/or coated by protecting layer. However, the side effect of the package materials also isolates the heat conduction. The effect indeed increases the chip temperature. Low-power design will relieve the thermal considerations for packaged IC especially for an SoC design.

(6) Low voltage operation: in Fig. 1, the forecast of CMOS circuit for supply voltage and technologies had been reported. In this report, it predicts the trend of CMOS supply voltage and pitch dimension for MPU/ASIC design. As the CMOS technology improvement, the prediction for supply voltage will be scaled down to 0.6 V on year 2024.[46]

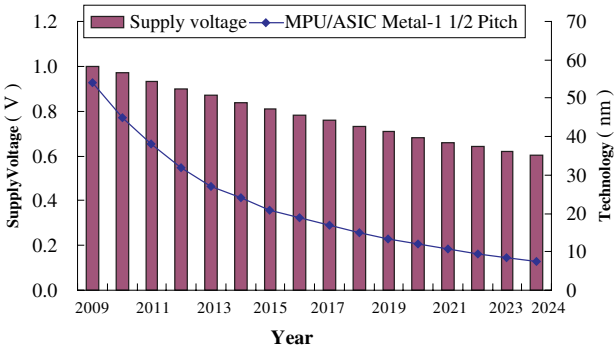

Fig. 1. A forecast of CMOS circuit for supply voltage and technologies by ITRS 2009.

3. Challenges of LVLP Design[47,48]

Sourcing from "The International Technology Roadmap for Semiconductors: 2009, Design Issues",[46] we know that current design technology faces two basic types of complexity — silicon complexity and system complexity. Silicon complexity refers to the impact of process scaling and the introduction of new materials or device/interconnect architectures. Some nonideal factors such as device parasitic, interconnect coupling, process/manufacturing variability, decreased reliability, and so forth, must be concerned and inspected. System complexity refers to exponentially increasing transistor counts enabled by smaller feature sizes and spurred by consumer demand for increased functionality, lower cost, and shorter time-to-market. Implied challenges include design for reusability, verification/test, cost-driven design, embedded software design, and design process management. Based on these considerations, some challenges directly related to CMOS circuit design are briefly summarized in this section. Due to time-to-market requirement, design of high-performance LVLP CMOS circuit within time limitation is a challenge. Notice that LV design are impacted by many factors such as electronic design automation (EDA) tools, threshold voltage V_T, driving capability, signal to noise ratio (SNR), standby/leakage current, parasitic parameters, and so on. Unfortunately, these factors are influenced by each other. Hence, the design of LVLP CMOS circuit is well-known as an optimized procedure under energy-delay trade-off.

(1) EDA tools: the simulation accuracy of IC's performance strongly depend not only on device modeling precision but also on the maturity of EDA tools. In sub-micro CMOS technology, many effects such as leakage current, interconnect delay, high-frequency device interference, gate insulator tunneling, breakdown integrity, joule heating, and electro-migration will no longer allow being negligible. The leakage current in SoC design dominates the standby power dissipation. The delay of interconnect line is comparable with (even larger than) the gate delay. In deep sub-micro CMOS technology, the cross interference between the neighbor

transistors is more serious than traditional process. Electro-migration effect degrades the circuit reliability. All these effects impact on the circuit performance to be extremely awful. In order to predict chip performance, not only foundries should give precise model parameters, but also EDA tools have to provide the accurate and efficient analysis on these related nonideal effects.

(2) Threshold voltage: a well-known first-order approximate model of MOS transistor, the drain saturation current I_{DS} is expressed as

$$I_{DS} = k(V_{GS} - V_T)^2, \quad V_{DS} \geq V_{GS} - V_T\,, \tag{1}$$

where k is a transconductance parameter and V_T is threshold voltage. The equation is no longer valid and accurate expression for sub-micro MOS operation because of some secondary-order effects such as velocity saturation, drain-induced barrier lowing (DIBL), and sub-threshold operation. Equation (1) means, however, the minimum supply voltage must be large enough to overcome the threshold voltage. The driving capability and operation speed of circuits are thus lowered when the supply voltage is reduced. For example, a transmission gate works as a turn-on switch. The minimum supply voltage of the transmission gate must be larger than $V_{Tn} + |V_{Tp}|$ for obtaining a reasonable turn-on resistance. For low-voltage CMOS design, V_T can be reduced in fabricated process by using doping impurity. However, it is not a smart solution for low power design because of non-negligible leakage current.

(3) Driving capability and parasitic capacitance: in spite of MOS transistors either operate in pinch-off saturation, velocity saturation, or sub-threshold region, obviously, reducing the supply voltage means a small drain current I_{DS}. As MOS transistor operated in strong inversion and under low supply voltage, its transconductance g_m is proportional to $\sqrt{I_{DS}}$, in company with both the driving capability and signal amplification are degraded. As a result, when a larger capacitance loading is needed to drive, the low-voltage circuit will naturally suffer from the low operating speed if without adopting any circuit compensation techniques. In addition, parasitic capacitors are usually inevitable in current silicon technology. Besides, all the MOS intrinsic capacitance, the line-to-line and line-to-transistor parasitic effects increase the switching error or coupling noise. The signal bandwidth and precision of circuit are thus diminished.

(4) Signal to noise ratio: in a digital viewpoint, the small voltage swing results in small noise margin. In analog domain, the strength of signal level is weakness due to the low supply voltage. For the reason, low-voltage operation in general often suffers from poor signal-to-noise ratio (SNR). For example, the constraint of low SNR will impact the designs of bio-amplifier used in electrooculography (EOG) and electroencephalography (EEG). The signal level in such a bio-amplifier ranged from several microvoltage to millivoltage. Another example is the design

of signal pre-amplifier used in wireless application, that is, design of low-noise amplifier (LNA).

(5) Standby/Leakage current: leakage current is a major source of power consumption especially for low threshold voltage technologies. Because V_{GS} approaches V_T, the transistor operates in sub-threshold conduction. The behavior of MOS transistor is somewhat like bipolar junction transistor (BJT), that is, current has exponential relationship with input voltage (V_{GS}). At this situation, I_D is dominated by the diffusion current. Thus, current of MOS transistor in sub-threshold conduction can be expressed as

$$I_D = I_O \exp \frac{V_{GS}}{\zeta V_t}\,, \tag{2}$$

where $\zeta > 1$ is a non-ideality factor ranging around 1.4–1.5 for modern technologies and thermal voltage $V_t = kT/q$. This means that V_{GS} approximate 80 mV decrease while I_D to be decreased by one decade. For example, when V_{GS} changes from 0.3 V to 0 V, I_D is reduced only a factor of $10^{3.75}$. In a low-threshold voltage technology, MOS transistor will not be turned off completely when $V_{GS} = 0$ V, which results in energy waste of circuit in static state. Furthermore, leakage current always exists in the reverse-biased p–n junction, and ranges in pico-amperes (about 10 pA/mil^2) at room temperature. The weight of leakage power in total power consumption is more evident in deep sub-micro CMOS technologies.

4. LVLP Methodologies

Inspection from transistor fabrication up to whole system realization, there are huge factors/parameters to be under consideration for a low-voltage low-power design. Despite various sophisticated techniques for power reduction, there are always increasing design factors such as loss of reliability, limited area/power/delay budget, lower design/fabrication costs, more flexibility, and cost testability. If we attempt to arrive at a global optimization under all controllable variables, the design work will be impracticable and heavily time-consuming. In order to reduce the complexity, it is feasible to manage these parameters under different viewpoints to make a trade-off. Therefore, in this section, we divide several LVLP methodologies for power reduction into four sub-issues: system/algorithm viewpoint, architecture viewpoint, logic/circuit design techniques, and process technology. Based on different viewpoints, efficient low-voltage, low-power methodologies are surveyed from top layer (system) to physical layer (process). In general, the sources of power consumption of modern CMOS integrated circuits are categorized as dynamic power (P_D), short-circuit power (P_{sc}), and leakage power (P_{leakage}). A well-known formula is re-expressed as

$$\begin{aligned} P_{\text{total}} &= P_D + P_{sc} + P_{\text{leakage}} \\ &= \alpha \times V_{\text{DD}}^2 \times C + V_{\text{DD}} \times \sum I_{sc} + V_{\text{DD}} \times \sum I_{\text{leakage}}\,, \end{aligned} \tag{3}$$

where α is the probability of status change (active factor, or called activity), I_{sc} is short-circuit current and, I_{leakage} is leakage current. The low-power consumption can be achieved by reductions of supply voltage V_{DD}, activity α, loading capacitance C, I_{sc}, and I_{leakage}. In addition, many approached such as threshold voltage control, new material to construct MOS transistor, or new structure for transistor had been reported in open literature for power reduction. Due to some overheads raised, we have to make more efficient trade-offs in various design domains at the same time.

4.1. *System/Algorithm viewpoint*

When a larger or complicated system is integrated in a single chip or chips set, "system/algorithm improvement" often provides a rather efficient methodology for whole power reduction. In general, the efficiency of power improvement (orders of magnitude) by system inspection is often better than the improvement (10−50% range) by physical/circuit effort solely. Given a definite specification, it is interesting that some constituted circuit blocks seem to be an over design. That is, due to critical path constraint and product's I/O standard, all non-critical blocks may operate under the fastest speed suffering from a waste of some power. Another design issue is "programmable implementation" versus "dedicated implementation" design. A system with programmability is often attractive in flexible characteristics and reprogramming capability, but with a higher energy per function than the dedicated system. The other design issues including power management mechanism, data refer to locality in algorithm design, system function and algorithm simplifications, and data reorganization[42] to reduce status transition, all are useful techniques to reduce the whole system power dissipation.

4.2. *Architecture viewpoint*

(1) Architecture partition[37,41]: referring to Eq. (3), the capacitance decreased results in reduction in power dissipation. Figure 2(a) shows a system sharing with a

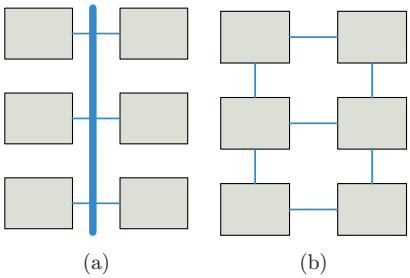

Fig. 2. Architecture partition.

common data bus for information transferred. Since the data bus is composed of many nodes connected together, it suffers from with a larger capacitance. Therefore, architecture shown in Fig. 2(a) consumes more power consumption when utilization of a single data bus to transfer information. Figure 2(b) shows that a bus topology is partitioned into "mesh" or "peer-to-peer" connection to achieve the same functionality. Obviously, the power dissipation of Fig. 2(b) is smaller than that of Fig. 2(a).

(2) Pipelined or concurrency structures: in general, lower supply voltage reduces the power consumption at the expense of low speed. The loss of speed can be compensated either by pipelined architecture or by concurrency architecture with parallel operations. Figure 3(a) shows the response time of the whole circuit working at supply voltage V_{DH} is $T_{\mathrm{a}} + T_{\mathrm{b}} + T_{\mathrm{c}}$, whereas Fig. 3(b) shows the three blocks combined with data latch "sw" working in pipelined style and with supply voltage V_{DL} ($V_{\mathrm{DL}} < V_{\mathrm{DH}}$). Due to supply voltage reduction, response time T_{1-3} is larger than $T_{\mathrm{a-c}}$. However, the design of slower response but with lower power can be compensated by the pipelined operation to keep the same throughput at the expense of hardware overheads owing to additional data latches and clock complexity as shown in Fig. 3(b).

(3) Circuit topology: more stacked MOS transistors in a dc path results in large supply voltage requirement. Due to the body effect, NMOS transistors far away the ground rail and PMOS transistors far away the V_{DD} rail result in a larger threshold voltage. In order to reduce the number of stacked MOS transistor in a digital system, by using logic restructuring, for example, we can reduce the input pin of single logic gate and reorganize its function as combination of multiple logic gates with fewer inputs. In low-voltage analog designs, circuit structure of amplifier would rather use multi-stage cascading than cascoding structure for high-gain requirement.

4.3. *Circuit design viewpoint*

(1) Voltage boost: to overcome the influence of the threshold voltage, Fig. 4 shows a conception of clock-booting technique. For $t < t_1$, switch $sw\,1$ turns on, switch $sw\,2$ turns off, and capacitor C_{boost} is charged to V_{DD}. For time $t > t_1$, the C_{boost} is boosted by through $sw\,2$ and the external pulse. Ideally, the output voltage V_{out}

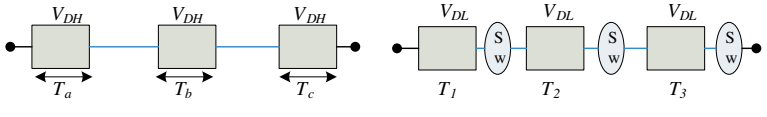

Fig. 3. Pipelined methodology.

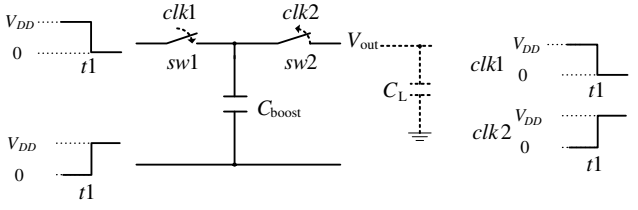

Fig. 4. Concept of voltage boost.

is $2V_{\mathrm{DD}}$. However, there are two issues to be noticed. One is the effect of parasitic and output load capacitances; the other one is how to completely transfer the $2V_{\mathrm{DD}}$ to the output node. The parasitic capacitance at $sw2$ and the load capacitance will result in charge sharing. Since the effect of the parasitic capacitances and threshold voltage drop, the real output voltage V_{out} is smaller than $2V_{\mathrm{DD}}$.

(2) Substrate bias adjustment and dynamic bias[19,20]: MOS threshold voltage can be derived as

$$|V_T| = |V_{T0}| + \frac{\sqrt{2\varepsilon_s q N_{\mathrm{imp}}}}{C_{\mathrm{ox}}} \left(\sqrt{2|\phi_p| + |V_{SB}|} - \sqrt{2|\phi_p|} \right), \tag{4}$$

where V_{T0} is the threshold voltage for $V_{SB} = 0$, ε_s is the permittivity of the silicon, N_{imp} is the density of the ion impurity in the bulk, C_{ox} is the oxide capacitance, ϕ_p is the material constant of the bulk, and V_{SB} is the bias voltage on the source–bulk junction. Some literatures indicate that source–body voltage V_{SB} can be forward biased a little about 0.1–0.3 V to enhance high speed operation.[25]

(3) Bulk-driven MOSFET[61]: for a fixed gate voltage, the magnitude of current I_D depends upon threshold V_T. By inspection of (4), V_T depends on V_{SB} bias. Intuitively, I_D may be modulated by V_{SB}. Thus, input signal can trigger the body terminal rather than conventional gate-driven. The operation is called as "bulk-driven" or "second-gate driven". Bulk-driven will efficiently reduce V_T limitation in low-voltage circuit. The advantage of bulk-driven MOS circuit reveals a wide input range. However, g_{mb} is smaller than g_m ($g_{mb} \approx 0.2{-}0.4\, g_m$), so the bulk-driving transistors often have a large device size to hold a reasonable transconductance.

(4) Dynamic logic: because of duality in PMOS and NMOS trees, input capacitance in conventional static CMOS logic is doubled. Besides the capacitance consideration, the simple CMOS inverter suffers from a short circuit current when input transition is relatively slow. Dynamic logic will be adopted to relieve the large input capacitance. However, dynamic logic generally operates in prior "precharge" phase and succeeding "evaluation" phase. Thus, the synchronization of clock must be carefully designed when multiple dynamic logics are in cooperation.

(5) Sub-threshold region[49]: sub-threshold mode, also called the weak inversion mode, based on the MOS transistors operating in the sub-threshold region is also an approach to achieve an LVLP circuit design. The sub-threshold mode circuit can provide ultimate speed/power ratio under the LVLP condition. The sub-threshold region of an MOS transistor is suitable for implementing the LVLP circuit. Nevertheless, under sub-threshold region the unity-gain bandwidth of an amplifier will be limited owing to the extremely low currents. Hence, how to overcome the problem of low direct current (DC) gain and unity-gain bandwidth is the main design issue for LVLP amplifier based on the MOS transistors operating in the sub-threshold region. Meanwhile, the bias point is difficult to design. Noise and process variation also impact the circuit operation. Focusing on digital circuit operated in sub-threshold region, many factors such as time delay increased, more sensitivity for process variation, temperature fluctuation, and noise margin degradation must be noticed in design phase.

(6) Full-swing logic: for next-generation CMOS integrated circuits, low supply voltage and low power dissipation are the trend. Some conventional low-power logics, such as pass transistor logic (PTL) and adiabatic CMOS logic circuit, have been reported for their potentials for low-power applications. However, the threshold voltage loss problem, due to PMOS poor in passing *low* signal (V_{SS}) and NMOS poor in passing *high* signal (V_{DD}), has been existed in PTL circuits. This non-full voltage-swing drawback may have limited its applications in low-voltage, low-power designs. As a result, some pull-up and/or pull-down transistors, or level restorers, must be added in PTL to compensate for threshold voltage loss. Adiabatic CMOS logic is also a low-power approach where the signal energy stored on a capacitor and recycled instead of dissipated as heat. Since adiabatic CMOS logic circuits have to use diodes, diode-connected devices, or cascade voltage switch logic circuits for the purpose of pre-charge, their outputs are not full swing. As a result, they are not appropriate for low-voltage operation unless additional compensation circuits suitable for low-voltage operation to be introduced.

Full-swing logic circuit is designed to fit the LVLP requirement with all nodes having a full-voltage swing signal, and hence it possesses the capability to operate reliably at a very-low supply voltage. This topology is advantageous in low-voltage and full-swing operation. It has better noise immunity, inherently driving capability and higher operation frequency. The full-swing logic with LVLP feature and driving capability comes with the penalty of larger transistor count than conventional PTL design and thus more expensive due to larger chip area.[51]

(7) Multiple supply voltages technique: as described in Eq. (3), power consumption in modern CMOS integrated circuits can be attributed to three main components: dynamic power, short-circuit power, and leakage power. Dynamic power is the dominant component among all, and reducing the supply voltage

will bring a quadratic improvement in the power consumption. To reduce the supply voltage is thus the most attractive and efficient way to reduce the power consumption in modern CMOS process technologies, but comes with the penalty of performance degradation. In fact, due to the increasing circuit complexity, the total power consumption of modern integrated circuits is drastically increasing even under the reduced supply voltage.

To maintain the performance of the LVLP system, multiple supply voltages (*multi-*V_{DD}) technique has been developed.[39,40] There are two schemes for implementation of *multi-*V_{DD} technique. The first one scheme, called temporal *multi-*V_{DD} technique, supports circuit with fully *high-*V_{DD} (denoted as V_{DH}) to fetch high performance in active (normal operation) mode, but provides lower supply voltages (*medium* and *low-*V_{DD}, denoted as V_{DM} and V_{DL}) to gain the low power advantage during the standby and sleep modes. In temporal *multi-*V_{DD} scheme, an additional power-circuit is required to generate the specified multiple supply voltages in corresponding modes, and the mode detector is also needed to check which operation mode is under going. The block diagram of temporal *multi-*V_{DD} scheme, shown in Fig. 5, has a power circuit to support *high-*V_{DD}, *medium-*V_{DD} and *low-*V_{DD}. The mode detector checks the operation mode of the function unit to be active, standby or sleep, and then gives a corresponding mode indication signal to power switch controller in order to pass the desired supply voltage to function (or signal processing) unit. Clock distribution block converts the clock to be the right clock frequency, and then pass it to the function unit. Level converter will shift the output of the function unit to the required voltage level for successive processing. A basic level converter, depicted in Fig. 6, can convert the low-voltage input to be a high-voltage output signal.[50]

The second one scheme called spatial *multi-*V_{DD} technique, shown in Fig. 7, provides multiple supply voltages for different signal processing units. In order to achieve high performance, the *multi-*V_{DD} is applied to units located in the critical path. Lower supply voltages (medium and low-V_{DD}) are arranged appropriately

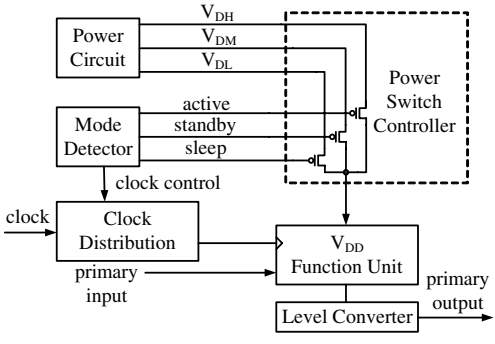

Fig. 5. Temporal *multi-*V_{DD} scheme.

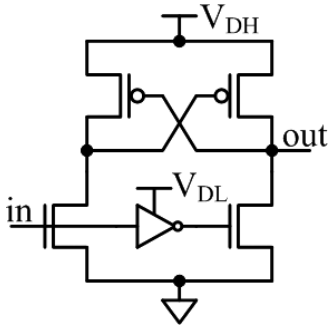

Fig. 6. Basic level converter.[50]

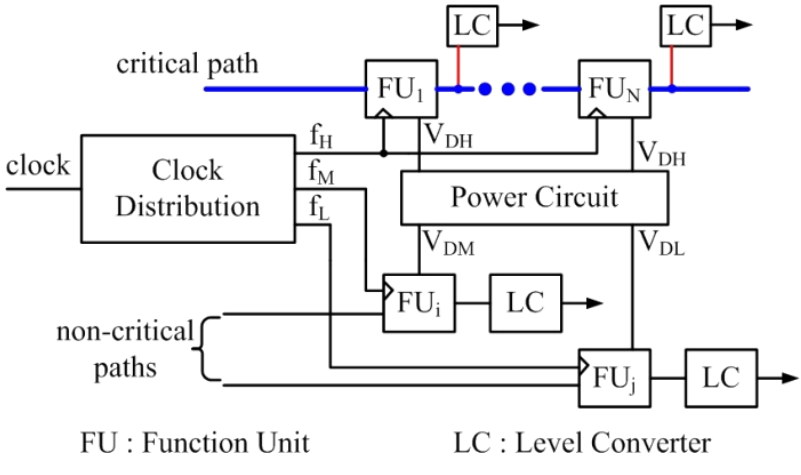

Fig. 7. Spatial *multi-*V_{DD} scheme.

for those units in noncritical paths to earn the low power dissipation. A mixed temporal and spatial *multi-*V_{DD} scheme can be implemented with more complicated design efforts and huge overheads to economize the use of energy. Anyway, to design multiple supply voltages chip, one should consider the following design issues such as multiple supply voltage clock distribution, level converters utilized to restore the standard full swing clock signal at the leaves of the low voltage clock distribution, clock skew for different supply voltage, and power distribution to eliminate the existence of hot spot.

(8) Multiple threshold voltages technique[21–24,52–54]: although sub-threshold leakage currents are not the dominant component of power consumption in modern integrated circuits, as transistor-size scaling trends going along with the low-power voltage scaling continuously becomes aggressive, sub-threshold leakage currents will turn into an increasing component and even dominate the overall

power consumption in future generations. Sub-threshold leakage current (I_{leakage}) increases exponentially with threshold voltage (V_T) and is given by

$$I_{\text{leakage}} = \frac{W}{W_0} I_0 e^{(V_{GS}-V_T)/nV_{\text{th}}}, \tag{5}$$

where W is channel width, n is the sub-threshold slop factor and lies between 1.2 and 2, and V_{th} denotes the thermal voltage. A low threshold voltage gate has high leakage power and short time delay, while a high threshold voltage gate has low leakage power and long time delay. The multiple threshold, also denoted as *multi-threshold* voltages technique provides a solution to carry out high performance benefits and low leakage power characteristics of chips.

There are two implementations, denoted as temporal and spatial schemes, for *multi-threshold* CMOS technique. The temporal *multi-threshold* scheme maintains high performance with suffering relatively larger leakage currents by using all low-V_T designs in active mode, yet still yields the low sub-threshold leakage characteristics by the arrangement of different high-V_T designs during the standby and/or sleep modes. The temporal dual-threshold scheme, shown in Fig. 8, uses all low-V_T MOS to design the function unit for improved performance, and high-V_T PMOS and NMOS as gating transistors to control the supply voltage. In active mode, the high-V_T gating transistors are turned on, the function unit based on all low-V_T MOS is connected to virtual power (V_{DV}) and ground (V_{SV}). When the circuit enters the sleep mode, the high-V_T gating transistors are turned off; the overall leakage power is bounded by extremely low sub-threshold leakage current from V_{DD} to ground (V_{SS}). The spatial *multi-threshold* scheme, shown in Fig. 9, uses different threshold voltages CMOS gates in different signal propagating paths. In order to achieve high performance and low leakage power, the implementation applies low threshold voltage gates to the critical path and makes use of high threshold voltage gates in noncritical paths. Multiple threshold voltage designs must face problems including the transistor

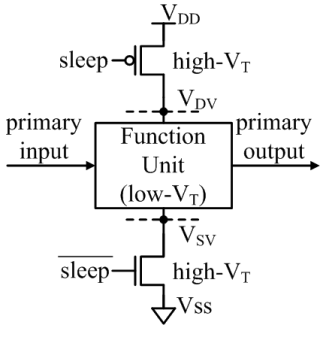

Fig. 8. Temporal multi-threshold voltages scheme.

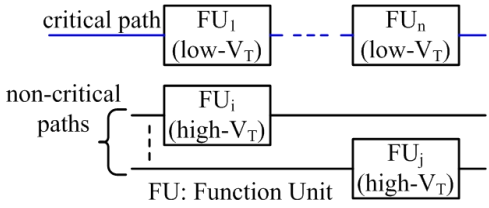

Fig. 9. Spatial multi-threshold voltage scheme.

sizing for different threshold voltages, process complexity, the performance and cost penalty, design complexity, chip area, and design for testability.

In low-power gating techniques, the clock-gating approach is well-known previous one. Power-gating CMOS logic design for LVLP chips is another effective low-power technique which maintains high active mode performance, but eliminates the standby power consumption in idle mode.[55,56] In power-gating logic gates, additional control pins are used to enable or disable the power supply of the gates. In active mode, the power-gating logic gates maintain fully power voltage supply to achieve high performance. However, during the idle mode, leakage power dissipations of the gates are extremely small due to their power-rail connections are turned off.

(9) Leakage current reduction: in CMOS nano-technologies, leakage current has become a major factor to impact low-power design. The major part of leakage current sources including reverse-biased source/drain-bulk junction leakage, gate leakage, and sub-threshold drain–source leakage must be considered. Currently, transistor with longer channel length and high threshold seems to be an effective technique to reduce the leakage power. In a 90 nm CMOS technology, the increasing of transistor channel length by 10% will approximately reduce the leakage current by 50% at the expense of increasing dynamic power by 18% (keeping W/L constant) and chip area overheads.[30] Obviously, multi-threshold scheme and reduction of supply voltage are also useful techniques to reduce leakage power. However, power consumption and circuit performance are again trade-off.

4.4. *Fabricated technology*

Some special CMOS technologies such as multiple thresholds and float-gate technologies also support capability of low-voltage design. Furthermore, silicon on insulator (SOI) technology[57] can be used to reduce the leakage current and prevent CMOS latch up. A higher permittivity ε material is also considered to replace current SiO_2 layer to build a faster and lower power transistor. One of the materials like hafnium oxide (HfO_2, with relative permittivity ε_r equals 15−30) combined with metal electrode is researching to reduce gate leakage and increase gate capacitance. However, the fabricated process is complicated and expensive than a standard

CMOS process. The other innovations in technology such as strained silicon, single-electron tunneling transistors,[58] dual-gate transistor,[59] and FinFET structure were proposed for transconductance improvement, carrier mobility increment or leakage current reduction. Micro-electromechanical systems (MEMS) technology is also developed for an ideal switch realization to completely eliminate the leakage current. A notable research in recent years, three-dimensional technology[60] (3D IC) attempts to shorten the wire length of signal propagation by using TSV (through silicon via) connection between different dies. When these process technologies reach maturity on the reliability increased, fabrication cost downed, and process yield raised, more low-power design methodologies and more new perspectives will be diversified.

5. Conclusions

In this paper, the motivation and challenges of low-voltage, low-power CMOS circuit were presented. A variety of design methodologies for LVLP were surveyed especially for sub-micro CMOS technology. From system level to physical level, we wholly discuss four issues: system/algorithm, architecture, circuit techniques, and fabricated technology viewpoints. It is impossible to review all techniques in detail within limited pages. This paper not only expects to give a complete picture in various techniques for beginners interesting in low-voltage, low-power design but also expects to give quick references for an experienced designer. Based on technology innovations and various design techniques integration, it can be anticipated that there are more optimizations and more selections in design phase to pursue an appropriate solution to meet the specification of LVLP products.

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