Harshitha Yendapally

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# Summary

* Research assistant and lab member at University of Texas, San Antonio actively looking for Internship opportunities in VLSI, embedded systems or Computer Architecture stream.
* 3.5 years of Industrial experience in Robert Bosch in designing Model based development tools with technical competence in Java plugin development, C and C++.

# Education

# Masters of Science in Electrical and Computer Engineering 3.87

# *University of Texas, San Antonio Aug’18(expected)*

# Bachelor of Engineering in Electronics and Communication Engineering 3.84

# *Osmania university April’13*

**Technical Skills**

* Languages: Verilog-HDL, System Verilog, C, C++, Core Java, Perl, ANT
* Tools: Cadence-Virtuoso, MATLAB-Simulink, Xilinx Vivado, Xilinx ISE, SDK, ASCET (Advanced Simulation and Control Engineering Tool), TPT-Time Partition Testing Tool, KEIL, Ride Microcontroller simulator, PSPICE

**Work Experience**

Senior Software Engineer

*Robert Bosch Engineering and Business Solutions Private Limited, Bangalore Aug’13-Nov’16*

* Imtone (*Aug’13-Aug’16*): Developed an automated tool and implemented algorithms for conversion of ASCET models to MATLAB models.
* Developed model based tools like ASCET Model Implementer, ASCET Backend, MATLAB Image generator. Handled all release activities like SCCM packaging, Toolbase launch, peacy and WTS server release, and UAT protocols (*Apr’14-Nov’16*).
* Developed Innovative standalone tools like Variant Reducer Testing Tool, TPT Automation Tool, Negative Sequence Call Identification Tool for testing functionality model based tools.

**Academic Projects**

* Thesis on hardware design aiming rethinking of numerical representation for Deep neural networks. *Language: System Verilog, HLS: C programming language, Tool: Cadence, Xilinx-Vivado, Xilinx-SDK*
* Onboard Encryption Algorithm circuit: Designed efficient fast processing encryption algorithm circuit.

*Language: System Verilog, HLS: C programming language, Tool: Xilinx-Vivado, Xilinx-SDK*

* Embedded light sensing system on Zybo Board: PmodALS module is configured and switches are used according to priority levels which aids in power efficient circuits design.

*Language: System Verilog, HLS: C programming language, Tool: Xilinx-Vivado, Xilinx-SDK*

* Out-of-Order Execution based on Simple Scalar Tool set: CPU performance is increased significantly by designing architectural level algorithm to temporarily suspend thread with high occupancy of physical register file.

*Simulator: M-Sim SMT,Language:C*

**Accomplishments**

* Certified as “Recognition for Technical competence” by Bosch in 2014.
* Certified by Bosch in stream of Embedded systems.
* Certified and provided with ECE Pioneer Research Scholarship by University of Texas, San Antonio.