CS22B2015 – HPC –PROFILING : MEAN SHIFT CLUSTERING

GPROF Analysis Report:

The flat profile indicates the following key hotspots in the program:

1. MeanShiftClustering :
   Time Spent: 58.92% of total runtime (2.74 seconds).

Purpose: This function is the core of the Mean Shift clustering algorithm, which is computationally expensive due to its iterative nature and distance calculations.

This is the primary bottleneck, consuming the majority of the runtime. Optimizing this function (e.g., reducing redundant calculations or parallelizing) would yield the most significant performance improvements.

2. std::pow<double, int>:

Time Spent: 25.59% of total runtime (1.19 seconds).

Purpose: This function is used for exponentiation operations, likely within the Gaussian kernel or distance calculations in the Mean Shift algorithm.

The high number of calls (599 million) indicates that exponentiation is a frequent operation. Consider optimizing or replacing this with a faster approximation if precision can be sacrificed

3. gaussianKernel:

Time Spent: 5.81% of total runtime (0.27 seconds).

Purpose: This function computes the Gaussian kernel, which is a critical part of the Mean Shift algorithm for weighting points based on their distance.

4. _init:

Time Spent: 9.68% of total runtime (0.45 seconds).

Purpose: This is an initialization function, likely related to setting up the program or libraries.

While this function takes a noticeable amount of time, it is likely a one-time setup cost and not a primary target for optimization.

Function Name	% Time	Time (s)	Calls
meanShiftClustering(Point const*, int, double, ...	58.92%	2.74	1
std::pow<double, int>(double, int)	25.59%	1.19	599,918,316
gaussianKernel(double, double)	5.81%	0.27	199,840,032
_init	9.68%	0.45	-

GCOV ANALYSIS REPORT :

File 'main.c'

Lines executed:96.88% of 96

Branches executed:100.00% of 42

Taken at least once:92.86% of 42

Calls executed:83.33% of 12

Creating 'main.c.gcov'

Lines executed:96.88% of 96

Important parts of gcov output file :

Function: gaussianKernel

- Line 16: Executed 199,840,032 times. Computes Gaussian kernel.

Function: meanShiftClustering

- Lines 49-56: Executed 199,840,032 times. Computes distances and updates centroids.

- Line 69: Executed 19,992 times. Computes centroid shifts.

- Line 101: Executed 179,118 times. Computes distances between centroids.

Function: readDataFromFile

- Line 143: Executed 9,997 times. Reads data points from file.

- Line 148: Executed 10 times. Reallocates memory for data array.

Function: main

- Line 181: Executed 1 time. Calls meanShiftClustering.

- Lines 185-187: Executed 30 times. Prints cluster centroids.

Understanding :

We can see that there are major hotspots clearly in gaussian kernel and mean shift clustering algorithm. This shows us an opportunity to parallelise parts of the important parts of algorithm in the two functions. The rest of the Line Profiling resulted insignificant.\

LIKWID – HARDWARE PROFILING

1. DEVICE TOPOLOGY

```
--------------------------------------------------------------------------------
CPU name:   Intel(R) Xeon(R) E-2224 CPU @ 3.40GHz
CPU type:   Intel Coffeelake processor
CPU stepping:    10
********************************************************************************
Hardware Thread Topology
********************************************************************************
Sockets:         1
```

```
CPU dies:         1
Cores per socket: 4
Threads per core: 1
-------------------------------------------------------------------------
------
HWThread        Thread        Core        Die        Socket
Available
0               0             0           0          0             *
1               0             1           0          0             *
2               0             2           0          0             *
3               0             3           0          0             *
-------------------------------------------------------------------------
------
Socket 0:         ( 0 1 2 3 )
-------------------------------------------------------------------------
------
*************************************************************************
******
Cache Topology
*************************************************************************
******
Level:                  1
Size:             32 kB
Cache groups:           ( 0 ) ( 1 ) ( 2 ) ( 3 )
-------------------------------------------------------------------------
------
Level:                  2
Size:             256 kB
Cache groups:           ( 0 ) ( 1 ) ( 2 ) ( 3 )
-------------------------------------------------------------------------
------
Level:                  3
Size:             8 MB
Cache groups:           ( 0 1 2 3 )
-------------------------------------------------------------------------
------
*************************************************************************
******
NUMA Topology
*************************************************************************
******
NUMA domains:           1
-------------------------------------------------------------------------
------
Domain:                 0
Processors:       ( 0 1 2 3 )
Distances:        10
```

```
Free memory:            11741.1 MB
Total memory:           15869.3 MB
--------------------------------------------------------------------------------
------
```

2. TLB DATA

```
--------------------------------------------------------------------------------
Group 1: TLB_DATA
+---------------------------------+---------+-------------+-------------+-------------+-------------+
|             Event               | Counter |  HWThread 0 |  HWThread 1 |  HWThread 2 |  HWThread 3 |
+---------------------------------+---------+-------------+-------------+-------------+-------------+
|        INSTR_RETIRED_ANY        |  FIXC0  | 11237615635 | 13360528965 | 48867840997 | 59104480595 |
|      CPU_CLK_UNHALTED_CORE      |  FIXC1  |  5215451394 |  6176532981 | 21821292910 | 26348122007 |
|       CPU_CLK_UNHALTED_REF      |  FIXC2  |  4277413886 |  4981836836 | 17293498542 | 20834480832 |
|  DTLB_LOAD_MISSES_CAUSES_A_WALK |   PMC0  |      668006 |      876599 |     1205390 |     1500435 |
| DTLB_STORE_MISSES_CAUSES_A_WALK |   PMC1  |       41338 |       49684 |       27939 |       69654 |
|   DTLB_LOAD_MISSES_WALK_ACTIVE  |   PMC2  |    31779438 |    33136447 |    30382332 |    32221809 |
|  DTLB_STORE_MISSES_WALK_ACTIVE  |   PMC3  |     1571129 |     1772759 |      836523 |     1693541 |
+---------------------------------+---------+-------------+-------------+-------------+-------------+

+-------------------------------------+---------+--------------+-------------+-------------+--------------+
|                Event                | Counter |      Sum     |     Min     |     Max     |      Avg     |
+-------------------------------------+---------+--------------+-------------+-------------+--------------+
|        INSTR_RETIRED_ANY STAT       |  FIXC0  | 132570466192 | 11237615635 | 59104480595 |  33142616548 |
|      CPU_CLK_UNHALTED_CORE STAT     |  FIXC1  |  59561399292 |  5215451394 | 26348122007 |  14890349823 |
|       CPU_CLK_UNHALTED_REF STAT     |  FIXC2  |  47387230096 |  4277413886 | 20834480832 |  11846807524 |
|  DTLB_LOAD_MISSES_CAUSES_A_WALK STAT |   PMC0  |      4250430 |      668006 |     1500435 | 1.062608e+06 |
| DTLB_STORE_MISSES_CAUSES_A_WALK STAT |   PMC1  |       188615 |       27939 |       69654 |   47153.7500 |
|   DTLB_LOAD_MISSES_WALK_ACTIVE STAT  |   PMC2  |    127520026 |    30382332 |    33136447 | 3.188001e+07 |
|  DTLB_STORE_MISSES_WALK_ACTIVE STAT  |   PMC3  |      5873952 |      836523 |     1772759 |      1468488 |
+-------------------------------------+---------+--------------+-------------+-------------+--------------+

+---------------------------------+--------------+--------------+--------------+--------------+
|             Metric              |  HWThread 0  |  HWThread 1  |  HWThread 2  |  HWThread 3  |
+---------------------------------+--------------+--------------+--------------+--------------+
|        Runtime (RDTSC) [s]      |       8.9875 |       8.9875 |       8.9875 |       8.9875 |
|        Runtime unhalted [s]     |       1.5304 |       1.8124 |       6.4030 |       7.7312 |
|            Clock [MHz]          |    4155.3791 |    4225.2780 |    4300.2890 |    4309.8982 |
|               CPI               |       0.4641 |       0.4623 |       0.4465 |       0.4458 |
|       L1 DTLB load misses       |       668006 |       876599 |      1205390 |      1500435 |
|      L1 DTLB load miss rate     |       0.0001 |       0.0001 | 2.466632e-05 | 2.538615e-05 |
| L1 DTLB load miss duration [Cyc] |      47.5736 |      37.8011 |      25.2054 |      21.4750 |
|       L1 DTLB store misses      |        41338 |        49684 |        27939 |        69654 |
|     L1 DTLB store miss rate     | 3.678538e-06 | 3.718715e-06 | 5.717257e-07 | 1.178489e-06 |
| L1 DTLB store miss duration [Cyc] |      38.0069 |      35.6807 |      29.9411 |      24.3136 |
+---------------------------------+--------------+--------------+--------------+--------------+

+-------------------------------------+-------------+-------------+-------------+-------------+
|                Metric               |      Sum    |      Min    |      Max    |      Avg    |
+-------------------------------------+-------------+-------------+-------------+-------------+
|        Runtime (RDTSC) [s] STAT     |      35.9500 |       8.9875 |       8.9875 |       8.9875 |
|        Runtime unhalted [s] STAT    |      17.4770 |       1.5304 |       7.7312 |       4.3693 |
|            Clock [MHz] STAT         |   16990.8443 |    4155.3791 |    4309.8982 |    4247.7111 |
|               CPI STAT              |       1.8187 |       0.4458 |       0.4641 |       0.4547 |
|        L1 DTLB load misses STAT     |      4250430 |       668006 |      1500435 | 1.062608e+06 |
|       L1 DTLB load miss rate STAT   |       0.0003 | 2.466632e-05 |       0.0001 |       0.0001 |
|  L1 DTLB load miss duration [Cyc] STAT |     132.0551 |      21.4750 |      47.5736 |      33.0138 |
|        L1 DTLB store misses STAT    |       188615 |       27939 |       69654 |   47153.7500 |
|      L1 DTLB store miss rate STAT   | 9.147468e-06 | 5.717257e-07 | 3.718715e-06 | 2.286867e-06 |
| L1 DTLB store miss duration [Cyc] STAT |     127.9423 |      24.3136 |      38.0069 |      31.9856 |
+-------------------------------------+-------------+-------------+-------------+-------------+
```

INFERENCE:

The TLB data indicates efficient instruction execution with a CPI around 0.45, suggesting minimal stalls. DTLB load miss rates are very low (~0.0001), implying effective memory translation, but store misses are slightly higher on some threads. The CPU clock speeds are stable, averaging around 4.2 GHz, ensuring consistent performance.

3. L3 CACHE

```
--------------------------------------------------------------------------------
Group 1: L3CACHE
+--------------------------+---------+-------------+-------------+-------------+-------------+
|          Event           | Counter |  HWThread 0 |  HWThread 1 |  HWThread 2 |  HWThread 3 |
+--------------------------+---------+-------------+-------------+-------------+-------------+
|     INSTR_RETIRED_ANY    |  FIXC0  | 46521251964 | 48320577555 | 14940180243 | 23322610804 |
|   CPU_CLK_UNHALTED_CORE  |  FIXC1  | 20793182183 | 21595461392 |  6817419927 | 10553804386 |
|   CPU_CLK_UNHALTED_REF   |  FIXC2  | 16360981844 | 16905815396 |  5356257324 |  8304668786 |
|  MEM_LOAD_RETIRED_L3_HIT |   PMC0  |     1748692 |     2121424 |     1743270 |     1525411 |
| MEM_LOAD_RETIRED_L3_MISS |   PMC1  |      211280 |      248654 |      293631 |      218241 |
|     UOPS_RETIRED_ALL     |   PMC2  | 57575138666 | 59529661242 | 18462036881 | 29012019723 |
+--------------------------+---------+-------------+-------------+-------------+-------------+

+--------------------------------+---------+--------------+-------------+-------------+--------------+
|             Event              | Counter |      Sum     |     Min     |     Max     |      Avg     |
+--------------------------------+---------+--------------+-------------+-------------+--------------+
|     INSTR_RETIRED_ANY STAT     |  FIXC0  | 133104620566 | 14940180243 | 48320577555 | 3.327616e+10 |
|   CPU_CLK_UNHALTED_CORE STAT   |  FIXC1  |  59759867888 |  6817419927 | 21595461392 |  14939966972 |
|   CPU_CLK_UNHALTED_REF STAT    |  FIXC2  |  46927723350 |  5356257324 | 16905815396 | 1.173193e+10 |
|  MEM_LOAD_RETIRED_L3_HIT STAT  |   PMC0  |      7138797 |     1525411 |     2121424 | 1.784699e+06 |
| MEM_LOAD_RETIRED_L3_MISS STAT  |   PMC1  |       971806 |      211280 |      293631 |  242951.5000 |
|     UOPS_RETIRED_ALL STAT      |   PMC2  | 164578856512 | 18462036881 | 59529661242 |  41144714128 |
+--------------------------------+---------+--------------+-------------+-------------+--------------+

+----------------------+-------------+-------------+-------------+-------------+
|        Metric        |  HWThread 0 |  HWThread 1 |  HWThread 2 |  HWThread 3 |
+----------------------+-------------+-------------+-------------+-------------+
|  Runtime (RDTSC) [s] |      8.8819 |      8.8819 |      8.8819 |      8.8819 |
| Runtime unhalted [s] |      6.1033 |      6.3388 |      2.0011 |      3.0978 |
|      Clock [MHz]     |   4329.7912 |   4351.9282 |   4336.2465 |   4329.5432 |
|          CPI         |      0.4470 |      0.4469 |      0.4563 |      0.4525 |
|    L3 request rate   | 3.404198e-05 | 3.981340e-05 |      0.0001 |      0.0001 |
|     L3 miss rate     | 3.669639e-06 | 4.176977e-06 | 1.590458e-05 | 7.522434e-06 |
|     L3 miss ratio    |      0.1078 |      0.1049 |      0.1442 |      0.1252 |
+----------------------+-------------+-------------+-------------+-------------+

+--------------------------+-------------+-------------+-------------+-------------+
|          Metric          |     Sum     |     Min     |     Max     |     Avg     |
+--------------------------+-------------+-------------+-------------+-------------+
|  Runtime (RDTSC) [s] STAT |     35.5276 |      8.8819 |      8.8819 |      8.8819 |
| Runtime unhalted [s] STAT |     17.5410 |      2.0011 |      6.3388 |      4.3853 |
|      Clock [MHz] STAT     |  17347.5091 |   4329.5432 |   4351.9282 |   4336.8773 |
|          CPI STAT         |      1.8027 |      0.4469 |      0.4563 |      0.4507 |
|    L3 request rate STAT   |      0.0003 | 3.404198e-05 |      0.0001 |      0.0001 |
|     L3 miss rate STAT     | 3.127363e-05 | 3.669639e-06 | 1.590458e-05 | 7.818408e-06 |
|     L3 miss ratio STAT    |      0.4821 |      0.1049 |      0.1442 |      0.1205 |
+--------------------------+-------------+-------------+-------------+-------------+
```

INFERENCE :

The CPI remains low (~0.45), indicating efficient execution with minimal stalls. L3 cache request and miss rates are very low, suggesting effective memory access. The CPU maintains a stable clock speed around 4.3 GHz, ensuring consistent performance across all threads.

4. L3

```
--------------------------------------------------------------------------------
Group 1: L3
+-----------------------+---------+-------------+-------------+-------------+-------------+
|         Event         | Counter |  HWThread 0 |  HWThread 1 |  HWThread 2 |  HWThread 3 |
+-----------------------+---------+-------------+-------------+-------------+-------------+
|   INSTR_RETIRED_ANY   |  FIXC0  | 14877161630 | 42516729970 | 26699974968 | 62617336817 |
| CPU_CLK_UNHALTED_CORE |  FIXC1  |  6869676368 | 18927924422 | 11994699697 | 27473946683 |
|  CPU_CLK_UNHALTED_REF |  FIXC2  |  5560959696 | 14906359404 |  9366708938 | 21525655182 |
|    L2_LINES_IN_ALL    |   PMC0  |    31641569 |    24545206 |    54202981 |   132398991 |
|     L2_TRANS_L2_WB    |   PMC1  |     2327331 |     1403029 |     3128268 |     3992350 |
+-----------------------+---------+-------------+-------------+-------------+-------------+

+---------------------------+---------+--------------+-------------+-------------+--------------+
|           Event           | Counter |      Sum     |     Min     |     Max     |      Avg     |
+---------------------------+---------+--------------+-------------+-------------+--------------+
|   INSTR_RETIRED_ANY STAT  |  FIXC0  | 146711203385 | 14877161630 | 62617336817 | 3.667780e+10 |
| CPU_CLK_UNHALTED_CORE STAT|  FIXC1  |  65266247170 |  6869676368 | 27473946683 | 1.631656e+10 |
|  CPU_CLK_UNHALTED_REF STAT|  FIXC2  |  51359683220 |  5560959696 | 21525655182 |  12839920805 |
|    L2_LINES_IN_ALL STAT   |   PMC0  |    242788747 |    24545206 |   132398991 | 6.069719e+07 |
|     L2_TRANS_L2_WB STAT   |   PMC1  |     10850978 |     1403029 |     3992350 | 2.712744e+06 |
+---------------------------+---------+--------------+-------------+-------------+--------------+

+-------------------------------+------------+------------+------------+------------+
|             Metric            | HWThread 0 | HWThread 1 | HWThread 2 | HWThread 3 |
+-------------------------------+------------+------------+------------+------------+
|      Runtime (RDTSC) [s]      |     8.8737 |     8.8737 |     8.8737 |     8.8737 |
|      Runtime unhalted [s]     |     2.0157 |     5.5539 |     3.5196 |     8.0616 |
|          Clock [MHz]          |  4210.0542 |  4327.4550 |  4364.1886 |  4349.7653 |
|              CPI              |     0.4618 |     0.4452 |     0.4492 |     0.4388 |
|  L3 load bandwidth [MBytes/s] |   228.2093 |   177.0281 |   390.9296 |   954.9048 |
|  L3 load data volume [GBytes] |     2.0251 |     1.5709 |     3.4690 |     8.4735 |
| L3 evict bandwidth [MBytes/s] |    16.7855 |    10.1191 |    22.5621 |    28.7941 |
| L3 evict data volume [GBytes] |     0.1489 |     0.0898 |     0.2002 |     0.2555 |
|    L3 bandwidth [MBytes/s]    |   244.9948 |   187.1472 |   413.4917 |   983.6990 |
|    L3 data volume [GBytes]    |     2.1740 |     1.6607 |     3.6692 |     8.7290 |
+-------------------------------+------------+------------+------------+------------+

+-----------------------------------+------------+-----------+-----------+-----------+
|              Metric               |     Sum    |    Min    |    Max    |    Avg    |
+-----------------------------------+------------+-----------+-----------+-----------+
|      Runtime (RDTSC) [s] STAT     |    35.4948 |    8.8737 |    8.8737 |    8.8737 |
|      Runtime unhalted [s] STAT    |    19.1508 |    2.0157 |    8.0616 |    4.7877 |
|          Clock [MHz] STAT         | 17251.4631 | 4210.0542 | 4364.1886 | 4312.8658 |
|              CPI STAT             |     1.7950 |    0.4388 |    0.4618 |    0.4488 |
|  L3 load bandwidth [MBytes/s] STAT|  1751.0718 |  177.0281 |  954.9048 |  437.7679 |
|  L3 load data volume [GBytes] STAT|    15.5385 |    1.5709 |    8.4735 |    3.8846 |
| L3 evict bandwidth [MBytes/s] STAT|    78.2608 |   10.1191 |   28.7941 |   19.5652 |
| L3 evict data volume [GBytes] STAT|     0.6944 |    0.0898 |    0.2555 |    0.1736 |
|    L3 bandwidth [MBytes/s] STAT   |  1829.3327 |  187.1472 |  983.6990 |  457.3332 |
|    L3 data volume [GBytes] STAT   |    16.2329 |    1.6607 |    8.7290 |    4.0582 |
+-----------------------------------+------------+-----------+-----------+-----------+
```

5. L2 – CACHE

```
--------------------------------------------------------------------------------
Group 1: L2CACHE
+-----------------------+---------+-------------+-------------+-------------+-------------+
|         Event         | Counter |  HWThread 0 |  HWThread 1 |  HWThread 2 |  HWThread 3 |
+-----------------------+---------+-------------+-------------+-------------+-------------+
|   INSTR_RETIRED_ANY   |  FIXC0  | 26562089061 | 49519106036 | 34732147932 | 46534370786 |
| CPU_CLK_UNHALTED_CORE |  FIXC1  | 11947634164 | 22020566208 | 15168968220 | 20709377385 |
|  CPU_CLK_UNHALTED_REF |  FIXC2  |  9514387376 | 17400831088 | 11826958622 | 16257733502 |
| L2_TRANS_ALL_REQUESTS |   PMC0  |   265237694 |   359073775 |   447023085 |   388013044 |
|     L2_RQSTS_MISS     |   PMC1  |    54891814 |    40242397 |   183533941 |    65815343 |
+-----------------------+---------+-------------+-------------+-------------+-------------+

+---------------------------+---------+--------------+-------------+-------------+--------------+
|           Event           | Counter |      Sum     |     Min     |     Max     |      Avg     |
+---------------------------+---------+--------------+-------------+-------------+--------------+
|   INSTR_RETIRED_ANY STAT  |  FIXC0  | 157347713815 | 26562089061 | 49519106036 | 3.933693e+10 |
| CPU_CLK_UNHALTED_CORE STAT|  FIXC1  |  69846545977 | 11947634164 | 22020566208 | 1.746164e+10 |
|  CPU_CLK_UNHALTED_REF STAT|  FIXC2  |  54999910588 |  9514387376 | 17400831088 |  13749977647 |
| L2_TRANS_ALL_REQUESTS STAT|   PMC0  |   1459347598 |   265237694 |   447023085 | 3.648369e+08 |
|     L2_RQSTS_MISS STAT    |   PMC1  |    344483495 |    40242397 |   183533941 | 8.612087e+07 |
+---------------------------+---------+--------------+-------------+-------------+--------------+

+----------------------+------------+------------+------------+------------+
|        Metric        | HWThread 0 | HWThread 1 | HWThread 2 | HWThread 3 |
+----------------------+------------+------------+------------+------------+
|  Runtime (RDTSC) [s] |     8.9257 |     8.9257 |     8.9257 |     8.9257 |
| Runtime unhalted [s] |     3.5058 |     6.4614 |     4.4510 |     6.0767 |
|      Clock [MHz]     |  4279.5880 |  4312.8004 |  4371.0305 |  4341.1812 |
|          CPI         |     0.4498 |     0.4447 |     0.4367 |     0.4450 |
|    L2 request rate   |     0.0100 |     0.0073 |     0.0129 |     0.0083 |
|     L2 miss rate     |     0.0021 |     0.0008 |     0.0053 |     0.0014 |
|     L2 miss ratio    |     0.2070 |     0.1121 |     0.4106 |     0.1696 |
+----------------------+------------+------------+------------+------------+

+---------------------------+------------+-----------+-----------+-----------+
|           Metric          |     Sum    |    Min    |    Max    |    Avg    |
+---------------------------+------------+-----------+-----------+-----------+
|  Runtime (RDTSC) [s] STAT |    35.7028 |    8.9257 |    8.9257 |    8.9257 |
| Runtime unhalted [s] STAT |    20.4949 |    3.5058 |    6.4614 |    5.1237 |
|      Clock [MHz] STAT     | 17304.6001 | 4279.5880 | 4371.0305 | 4326.1500 |
|          CPI STAT         |     1.7762 |    0.4367 |    0.4498 |    0.4441 |
|    L2 request rate STAT   |     0.0385 |    0.0073 |    0.0129 |    0.0096 |
|     L2 miss rate STAT     |     0.0096 |    0.0008 |    0.0053 |    0.0024 |
|     L2 miss ratio STAT    |     0.8993 |    0.1121 |    0.4106 |    0.2248 |
+---------------------------+------------+-----------+-----------+-----------+
```

INFERENCE :

The provided L2 cache performance data highlights the execution metrics across four hardware threads. The clock speeds average around 4326 MHz, with a CPI averaging 0.4441, indicating efficient instruction processing. L2 request rates and miss rates remain low, at an average of 0.0096 and 0.0024, respectively, signifying effective cache utilization and minimal memory access latency.

6.