Report: ASIC Implementation Flow & Comparative Synthesis Analysis

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Abstract

This report documents the complete RTL-to-GDSII flow for a 4-bit synchronous counter using the open-source OpenLane ASIC toolchain and the SKY130 PDK. It further provides a detailed comparative analysis between the results of synthesizing the same RTL design for an FPGA target (using Xilinx Vivado) and for an ASIC target.

1 Task: From Concept to Silicon

Objective was to transform a behavioral Verilog description into a GDSII file. This process involves synthesis, floor planning, placement, clock tree synthesis, routing.

1.1 The Design: `counter.v`

The core design is a simple yet fundamental digital block.

```
// A simple 4-bit synchronous counter
module counter (
    input  wire clk,
    input  wire rst_n,
    output reg [3:0] count
);
    // Behavioral description of a counter
    always @(posedge clk or negedge rst_n) begin
        if (!rst_n)
            count <= 4'b0;
        else
            count <= count + 1;
    end
endmodule
```

Listing 1: The Design: my_counter.v

1.2 The Configuration: `config.json`

The OpenLane flow is guided by a configuration file.

```
{   "PDK": "sky130A",
    "DESIGN_NAME": "counter",
    "VERILOG_FILES": "dir::src/counter.v",
    "CLOCK_PORT": "clk",
    "CLOCK_PERIOD": 10,
    "FP_CORE_UTIL": 20,
    "FP_ASPECT_RATIO": 1,
    "DIE_AREA": "0 0 200 200"
}
```

Listing 2: The Configuration: config.json

2 The ASIC Implementation Flow with OpenLane

The flow was executed interactively within the OpenLane Docker environment to observe and control each stage.

2.1 Environment Setup

- **Command:** `make mount`
- **Purpose:** Launches the Docker container with all necessary EDA tools.
- **Command:** `./flow.tcl -interactive`
- **Purpose:** Starts the interactive OpenLane shell.

2.2 Step-by-Step Execution

1. **Preparation:** `prep -design my_counter`
2. **Synthesis:** `run_synthesis`
3. **Floorplanning:** `run_floorplan`
4. **Placement:** `run_placement`
5. **Clock Tree Synthesis (CTS):** `run_cts`
6. **Routing:** `run_routing`
7. **Signoff and Verification:**
    - **DRC (Design Rule Check):** `run_magic`
    - **LVS (Layout vs. Schematic):** `run_lvs`

2.3 Final Output

The result of this entire process is the `counter.gds` file. This is a binary file containing a geometric description of every single polygon and layer that needs to be patterned onto the silicon wafer.

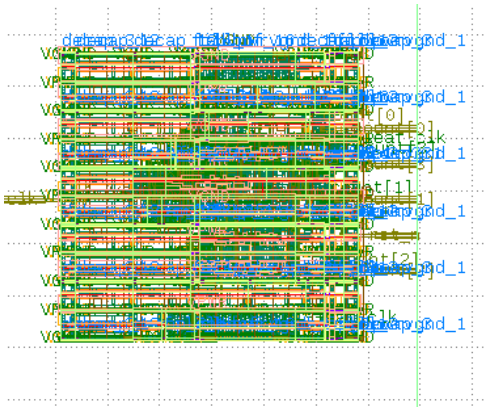

Figure 1: OpenLane GDSII Layout viewed in KLayout.

3 Timing Analysis Fundamentals

Before comparing results, it is crucial to understand key timing parameters verified by Static Timing Analysis (STA).

- **Clock Period:** The time between active clock edges (10 ns for 100 MHz).
- **Setup Time (T_{setup}):** The time data must be stable **before** the clock edge.
- **Hold Time (T_{hold}):** The time data must be stable **after** the clock edge.
- **Slack:** The difference between required and actual signal arrival time.
  - **Positive Slack:** Signal is early. Design meets timing.
  - **Negative Slack:** Signal is late. Timing violation.
- **Critical Path:** The longest combinational path between flip-flops.
- **WNS (Worst Negative Slack):** The worst setup slack. Key metric for performance.
- **WHS (Worst Hold Slack):** The worst hold slack. Key metric for correctness.

4 Comparative Synthesis Analysis: Vivado (FPGA) vs. OpenLane (ASIC)

The same RTL was synthesized with a **10 ns clock period constraint** using two different toolchains.

4.1 Vivado Synthesis Results (FPGA Flow)

Target: Xilinx Artix-7 FPGA (xc7a35tcpg236-1)

- **Resource Utilization:**
  - **Slice LUTs:** 3 (¡0.01%)
  - **Slice Registers:** 4 (¡0.01%)
  - **Bonded IOBs:** 6
- **Timing Analysis:**
  - **WNS:** +8.303 ns
  - **WHS:** +0.142 ns

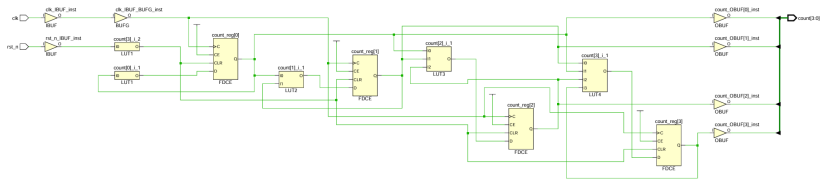

Figure 2: Vivado Post-Synthesis Schematic Diagram.

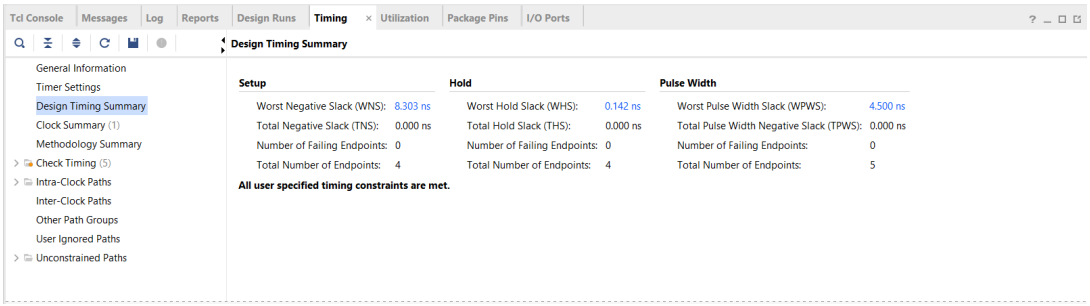

Figure 3: Vivado Timing Report excerpt showing WNS and WHS.

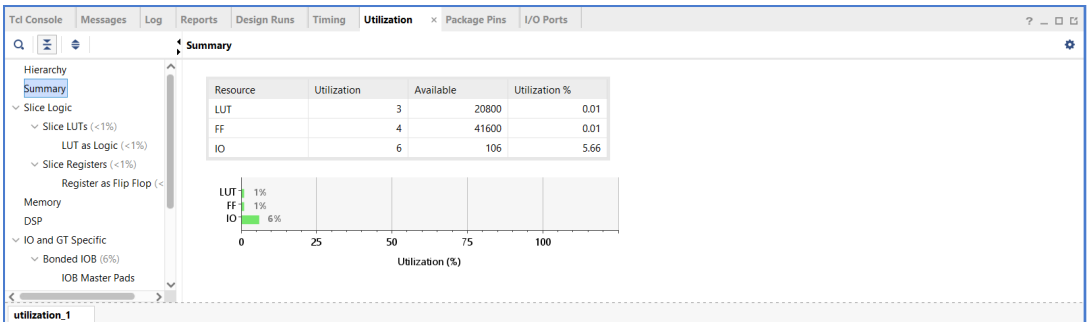

Figure 4: Vivado Utilization Report.

4.2 OpenLane Synthesis Results (ASIC Flow)

Target: SKY130A HD Standard Cell Library

- **Area Analysis:**
  - **Total Cell Area:** 163.91 μm^2
  - **Cell Count:** 10 cells
- **Timing Analysis (Pre-Layout):**
  - **WNS:** +7.17 ns
  - **WHS:** +0.32 ns

```
summary_report

=======================================================================
report_tns
=======================================================================
tns 0.00

=======================================================================
report_wns
=======================================================================
wns 0.00

=======================================================================
report_worst_slack -max (Setup)
=======================================================================
worst slack 7.17

=======================================================================
report_worst_slack -min (Hold)
=======================================================================
worst slack 0.32
summary_report_end
```

Figure 5: OpenSTA (OpenLane) Timing Report excerpt.

```
63. Printing statistics.

=== counter ===

   Number of wires:                 9
   Number of wire bits:            12
   Number of public wires:          3
   Number of public wire bits:      6
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                10
     sky130_fd_sc_hd__a21oi_2       1
     sky130_fd_sc_hd__and3_2        1
     sky130_fd_sc_hd__dfrtp_2       4
     sky130_fd_sc_hd__inv_2         1
     sky130_fd_sc_hd__nor2_2        1
     sky130_fd_sc_hd__xor2_2        2

   Chip area for module '\counter': 163.907200
```

Figure 6: OpenLane Synthesis Area Report.

4.3 Key Comparative Insights

Aspect	**Xilinx Vivado (FPGA)**	**OpenLane (ASIC)**
Target	Pre-fabricated Artix-7 FPGA	Custom SKY130 Silicon Chip
Cost Metric	**Utilization (%)** of fixed resources	**Physical Area (μm^2)** of silicon
Logic Implementation	Generic Look-Up Tables (LUTs)	**Fine-grained standard cells** (XOR, AND, NOR gates)
Performance (WNS)	**+8.303 ns**	**+7.17 ns**
Design Focus	Efficient mapping to available resources.	Optimizing for **Power, Performance, Area (PPA)**.

Table 1: FPGA vs. ASIC Synthesis Comparison

5 Inference from Results

Both the FPGA and ASIC synthesis flows successfully implemented the counter design and met the 100 MHz timing target with significant positive slack. The FPGA implementation showed slightly better timing performance (+8.303 ns WNS) using generic LUT-based architecture, while the ASIC implementation achieved efficient area usage (163.91 μm^2) through optimized standard cell selection. The results demonstrate that while both approaches are valid, the choice between FPGA and ASIC depends on the specific design priorities of performance versus area optimization.