

## Assignment - 03

A S J I

Ques ①

deadlock condition happens when two or more people (or processes) try to happen perform action at same time & the final outcome depends on who gets there first.

Because the actions overlap, the result become incorrect, inconsistent or unexpected.

ex → Two people A & B) try to withdraw money from the same ATM account at the same time.

if both check the balance (₹ 5000) before either withdraws, both think enough money exists & both may withdraw ₹ 5000 (inconsistent result)

how exclusion fixes it →

only one person can access the account ~~data~~ at a time (ATM session lock)

when A is withdrawing, B must wait.

This ensure orderly access → correct balance update.

Ques 2

Peterson's solution vs Semaphores

Aspect → Peterson's solution vs Semaphores

Implementation Complexity	pure software, harder to understand of process-prime	Simple to use with clear primitives
		waits/signals

Hardware dependency	Requires strict ordering of atomicity of load/stores → works on uniprocessors only	Requires hardware atomic instructions (Test-and-set) but works across multi- core systems
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Ques 3

Advantage of using monitors in multi-core systems :-

→ Monitors automatically provide mutual exclusion using an internal clock, so programmers don't manage semaphores manually.

Advantages :- Better safety & correctness - no issues like forgetting to release semaphore avoiding race conditions in multi-core concurrency.

Ques 4

Reader - writer starvation + preemption

How starvation occurs :-

In reader-priority RW, continuous arrival of readers may prevent writers from ever getting back the lock → writer starvation

In writer-priority RW, queue of writers may block readers indefinitely → reader starvation

Precentation method -

use fair queuing (FIFO): maintain arrival order, next request (reader or writer) is served in first-come-first serve manner. Guarantees bounded waiting

Ques 5

Drawback of removing "Hold & wait"

To prevent hold & wait, a process must request all resources at once before starting.

~~Drawback: Large resource waste → processes hold unused resource for long periods, reducing overall system utilization & causing increased waiting~~

Ques 6

ATC Traffic Control System - Case Study.

a) Critical Sections, requiring mutual exclusion + suitable IPC

In an ATC system, the following shared data structures require strict mutual exclusion  
1. Shared Radar Data Buffer  
update continuously by radar acquisition, used by flight-path calculators.

Q.

Global aircraft position Table -

contains real-time locations/altitude; accessed

by multiple processes simultaneously

### 3. Communications queue.

⇒ Messages sent to pilot must be consistent & non-conflicting

These decisions must never be corrupted as they directly impact aircraft safety.

#### Suitable IPC Mechanism -

use real-time shared memory protected by priority-inheritance mutexes or real-time message queues

- shared memory provide fast, deterministic access (important for real-time)
- priority-inheritance mutex avoids priority & ensure time-critical task (circular update) are never delayed
- message queues ensure safe, asynchronous communication for pilot messaging

b)

Deadlock detection & recovery with minimal disruption

If a deadlock occurs b/w Radar Acquisition & flight path calculation, the system cannot stop radar updates - this is safety-critical

Detection strategy →

- use a resource allocation graph (RAG) or periodic deadlock detection algorithm to detect circular wait b/w processes
- ATC system typically uses watch-dog timers  
◦ if a process does not update within a specific interval the system suspects a deadlock.

Recovery (minimum Disruption)

1. Preempt or rollback the non-critical process (flight path calculation)
2. Release its held locks/resources
3. Restart its held task & resume the flight-path calculation using the latest radar data snapshot.
4. Log the event for analysis.

This ensures

- Safety-critical real-time data collection is never interrupted.
- Flight-path calculation is done with minimal delay.
- System recovers without shutting down or losing air traffic continuity.

Ques

Given

$$A = 10, B = 5, C = 7$$

Process	Allocate	Max
P <sub>0</sub>	010	753
P <sub>1</sub>	200	322
P <sub>2</sub>	302	902
P <sub>3</sub>	311	422
P <sub>4</sub>	002	533

a) Need Matrix = Max - Allocation

Process	Need	Total Allocated
P <sub>0</sub>	743	A : 0 + 2 + 3 + 2 + 0 = 7
P <sub>1</sub>	122	B : 1 + 0 + 0 + 1 + 0 = 2
P <sub>2</sub>	600	C : 0 + 0 + 2 + 1 + 2 = 5
P <sub>3</sub>	211	
P <sub>4</sub>	631	

$$\text{Available} = \text{Total} - \text{Allocation}$$

$$A = 10 - 7 = 3$$

$$B = 5 - 2 = 3$$

$$C = 7 - 5 = 2$$

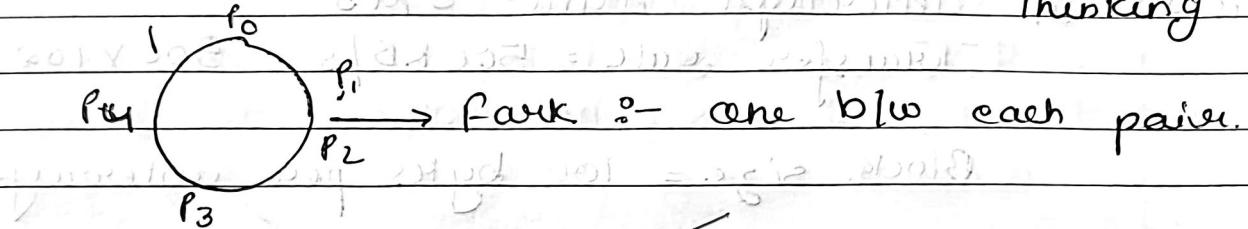
b) Safe sequence  $\Rightarrow P_1 \rightarrow P_3 \rightarrow P_0 \rightarrow P_2 \rightarrow P_4$

- c) Need of  $P_1 = (1, 2, 2)$   
 Request-  $(1, 0, 2) \leq$  Need  
 $P_1$ 's request cannot be granted immediately

Ques 7 → Dining Philosopher

5 Philosophers  
 $P_0, P_1, P_2, P_3, P_4$

Philosopher Task  
 Eating



Naive Semaphore constraints

It leads to deadlock while eating while (critical)

No eating while thinking

No thinking while eating

think();  
 wait(fork[i]);  
 wait(fork[(i+1)%5]);  
 eat();  
 signal(fork[(i+1)%5]);

Each philosopher has to pick fork on left & right, if available

Signal(fork[i]);  
 Signal(fork[i]);

every one picks fork on the left meaning all will hold the fork on their left & wait for fork in right causing a deadlock

deadlock free.

if ( $i \% 2 == 0$ ) {  
    wait (left);  
    wait (right);

    if ( $i \% 2$ )

        else {  
            wait (right);  
            wait (left);  
        }

    eat();

    signal (right()); signal (left());

Ques 8) a) Interrupt time = 5 ms

Transfer rate =  $500 \text{ KB/s} = 500 \times 10^2 \text{ B/s} = 512000 \text{ B/s}$

Block size = 100 bytes per interrupt

$$\text{Interrupt / sec} = \frac{512000}{100} = 5120$$

CPU time spent

$$5120 \times 5 \text{ ms} = 25600 \text{ ms} = 0.0256 \text{ s}$$

b)

use DMA (Direct memory access) as it transfers  
large chunks of data directly  
to memory with far fewer interrupt  
reducing its CPU utilization while  
keeping the same transfer rate