
Harshit Kumar

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Education

| Year | Degree/Examination | Institute | CGPA |
|--------------------|---|---------------|-----------|
| 2019 - 2023 (Exp.) | Ph.D. Electrical & Computer Engineering | Georgia Tech | 4.0/4.0 |
| 2014 - 2019 | B.S. & M.S. DUAL DEGREE Electronics and Electrical Communication | IIT Kharagpur | 9.04/10.0 |

Publications [\[Google Scholar\]](#)

- “BiasP: a DVFS based exploit to undermine resource allocation fairness in Linux Platforms” **Harshit Kumar**, Nikhil Chawla, and Saibal Mukhopadhyay. *ACM/IEEE ISLPED 2020*.
- “Securing IoT Devices using Dynamic Power Management: Machine Learning Approach” Nikhil Chawla, Arvind Singh, **Harshit Kumar**, Monodeep Kar, and Saibal Mukhopadhyay. *IEEE Internet of Things Journal*.
- “Towards Increasing the Difficulty of Reverse Engineering of RSFQ Circuits” **Harshit Kumar**, Tahereh Jabbari, Gleb Krylov, Kanad Basu, Eby G Friedman, and Ramesh Karri. *IEEE Transactions on Applied Superconductivity*.
- “On Finding Suitable Key-Gate Locations in Logic Encryption” Rajit Karmakar, **Harshit Kumar**, Santanu Chattopadhyay. *International Symposium on Circuits and Systems (ISCAS)-2018*.
- “Efficient Key-gate Placement And Dynamic ScanObfuscation Towards Robust Logic Encryption” Rajit Karmakar, **Harshit Kumar**, Santanu Chattopadhyay. *IEEE Transactions on Emerging Topics in Computing*.

Work Experience/Internships

Graduate Research Assistant

AUG 2019 - PRESENT

Supervisor: Prof Saibal Mukhopadhyay

GEORGIA INSTITUTE OF TECHNOLOGY, ATLANTA, GEORGIA

- Exploring the interaction of the power management infrastructure with other modules on a modern System-on-Chip from the viewpoint of device security.
- Proposed a kernel-level exploit that uses power-management as a backdoor for controlling resource allocation fairness in modern SoCs.
- Applied Bayesian inspired ML techniques for designing trustworthy hardware-based malware detectors.

Security Analysis of Superconducting Circuits

MAY 2018 - JULY 2018

Supervisor: Prof Ramesh Karri & Prof Kanad Basu

TANDON SCHOOL OF ENGINEERING, NEW YORK UNIVERSITY

- Performed security analysis of RSFQ circuits, a class of superconducting electronics, for preventing IP-Piracy.
- Developed a novel, low-overhead strategy for camouflaging RSFQ circuits which exploits similar structure of standard cells.
- Demonstrated the resilience of the aforementioned technique to SAT-based attacks by using a model-checking based attack framework.

Single Channel Speech Enhancement

MAY 2017 - JULY 2017

TATA POWER SED, BANGALORE

- Implemented a single channel speech enhancement algorithm based on the masking properties of the human auditory system.
- Incorporated a psycho-acoustically motivated spectral weighing rule to find the best trade-off between speech distortion and noise reduction.
- Achieved an increase in SNR of 9.3 dB for noisy signals having SNR of 0dB.

Other Research Experiences

Logic Encryption (BACHELOR AND MASTER’S THESIS)

SEPT 17 - APRIL 18

Supervisor: Prof Santanu Chattopadhyay, IIT Kharagpur

- Formulated a strategy, for selection of key-gate location, which enhances the security of a logically encrypted chip, preventing IP piracy and scan-based side channel attacks.
- Developed an algorithm for preventing sensitization based attacks that finds key gate locations in linear time.
- Performed comprehensive security analysis demonstrating the algorithm’s resilience against satisfiability, sensitization, and scan-based side-channel attacks.

Data Acquisition System

OCT 15 - JULY 16

Team KART, Formula SAE Team, IIT Kharagpur

- Implemented the Data Acquisition System project aimed at providing storage, wireless transmission as well as on-board real time display of vehicle data based on a 32-bit ARM Cortex M4 CPU based micro-controller.

Selected Term Projects

Computer Architecture

Spring 2020

Prof. Thomas Conte, Georgia Institute of Technology

- Designed a cache hierarchy simulator that simulates memory traces containing instruction and data addresses.
- Implemented a superscalar pipelined processor capable of performing out of order and speculative execution.
- Designed a cache-coherence simulator implementing MESI and MOESI protocol for multi-core processors.

Circuit Partitioning Using Graph Neural Networks

Spring 2020

Prof. Sung-Kyu Lim, Georgia Institute of Technology

- Implemented a deep-learning based fully differentiable approach to solve the problem of circuit partitioning using Graph Convolutional Networks.

Implementation of CORDIC Algorithm for Hyperbolic Functions

Spring 2017

Prof. Indrajit Chakrabarti, Prof. Sudip Nag, IIT Kharagpur

- RTL Design of 16-bit fixed point CORDIC algorithm for hyperbolic functions in rotation and vectoring mode with a precision of 2^{-10} in rotation and 2^{-13} in vectoring mode

High Speed Sparse Matrix Multiplier (for Feature Recognition)

Autumn 2016

Prof. Mrigank Sharad, IIT Kharagpur

- RTL Design of Multiplier using optimized parallel computation
- Optimized memory access power and speed using custom designed RAM

Positions of Responsibility

MAY 2016 - MAY 2017

Head of Electronics Subsystem

Team KART, Formula SAE Team of IIT Kharagpur

- Led a team of 6 students in developing numerous constituents of the electronic subsystem in a formula student car.

Technical Skills and Expertise

- **CAD Tools** : Cadence (Virtuoso Analog Design Environment), Synopsys (Design & IC Compiler), Pspice
- **Micro-controllers**: ARM Cortex-M, AVR, Raspberry Pi
- **Other Softwares**: Proteus, EagleCAD, Atmel Studio, Coocox IDE, Xilinx
- **Tools** : Git, LaTeX
- **Programming Languages**: C, C++, Python, MATLAB

Academic Honors and Awards

- Member of the gold winning team at the Inter-IIT Tech Meet-2018 in "Technologies for Soldier Support".
- Offered fellowship by Indian Academy of Sciences, Bengaluru, during the summers of 2017. (*Surrendered due to internship at TATA Power SED*)
- Succeeded in being among the top 35 finalists out of 1500 teams of KPIT Sparkle 2017, a national design and development innovation contest for engineering.
- Ranked among the top 0.3% students in IIT-JEE (Advanced) Examinations, 2014 (AIR- 1059).

Relevant Coursework

- **VLSI and Computer Architecture Related Courses**: Analog Electronic Circuits, Digital Electronic Circuits, Semiconductor Devices, VLSI Engineering, VLSI for Telecommunication, Architectural Design of ICs, Semiconductor Modelling, Analog VLSI, Digital VLSI, VLSI CAD, Advanced Computer Architecture, Advanced Operating Systems, Digital Systems Testing
- **Communications & Signal Processing Related Courses**: Analog Communications, Digital Communications, MIMO Communications, Network Theory, Signals and Systems, Digital Signal Processing, Introduction to Internet & Wireless Communications, Estimation & Detection Theory
- **Miscellaneous Courses**: Matrix Algebra, Probability and Stochastic Process, Mathematics I & II, Control Systems Engineering, Algorithms-I, Programming & Data Structures, Machine Intelligence & Expert System