COL216 Assignment-2 Part 1

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Report:

I have made 8 files.

1. ALU.vhd
2. register.vhd
3. dataMem.vhd
4. programMemory.vhd
5. programCounter.vhd
6. flags.vhd
7. condChecker.vhd
8. processor.vhd

1. ALU.vhd:

This is our ALU file that takes in 2 inputs what are 32 bit vectors and 1 input carry-bit. It also takes an OP code that is a 4 bit vector. It produces the necessary output as required by the selection in the form of a 32 bit output vector and a carry-out bit

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                     102     210     48.57%
# Info: Global Buffers            0      32      0.00%
# Info: LUTs                    166    63400     0.26%
# Info: CLB Slices               41    15850     0.26%
# Info: Dffs or Latches           0   126800     0.00%
# Info: Block RAMs                0      135     0.00%
# Info: DSP48E1s                  0      240     0.00%
# Info: ------------------------------------------------------------
# Info: ******************************************************
# Info: Library: work    Cell: ALU    View: Behavioral
# Info: ******************************************************
# Info:  Number of ports :                  102
# Info:  Number of nets :                   405
# Info:  Number of instances :              304
# Info:  Number of references to this view :        0 # Info: Total accumulated area :
# Info:  Number of LUTs :                   166
# Info:  Number of Primitive LUTs :         167
# Info:  Number of LUTs with LUTNM/HLUTNM :         2
# Info:  Number of MUX CARRYs :              64
# Info:  Number of accumulated instances :        401
# Info: ****************************
```

2.

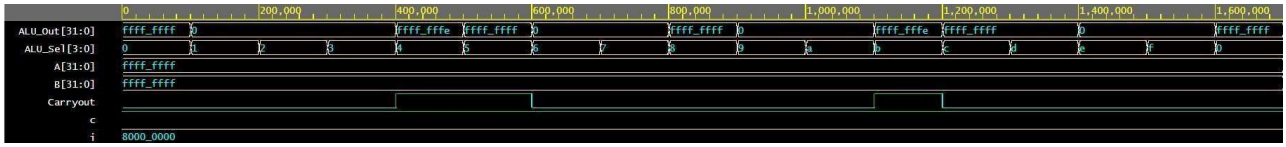

Figure 1: TestBench execution for ALU.vhd

register.vhd:

Register File contains an array of 16 std_logic_vectors of 32-bits each. Its inputs include two read addresses, one write address, one data input, one write enable and a clock. There are two data outputs on which contents of the array elements selected by read addresses are continuously available. If write enable is active, at clock edge the input data gets written in the array element selected by write address.

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                     110     210     52.38%
# Info: Global Buffers            1      32      3.12%
# Info: LUTs                     48   63400     0.08%
# Info: CLB Slices               12   15850     0.08%
# Info: Dffs or Latches           0  126800     0.00%
# Info: Block RAMs                0     135     0.00%
# Info: Distributed RAMs
# Info:    RAM32M                10
# Info:    RAM64M                2
# Info: DSP48E1s                  0     240     0.00%
# Info: ------------------------------------------------------------
# Info: ************************************************
# Info: Library: work    Cell: REG    View: BEV
# Info: ************************************************
# Info:  Number of ports :                  110
# Info:  Number of nets :                   220
# Info:  Number of instances :              111
# Info:  Number of references to this view :        0 # Info: Total accumulated area :
# Info:  Number of LUTs :                   48
# Info:  Number of Primitive LUTs :         48
# Info:    Number of LUTs as Distributed RAM :      48
# Info:  Number of accumulated instances :        123
```

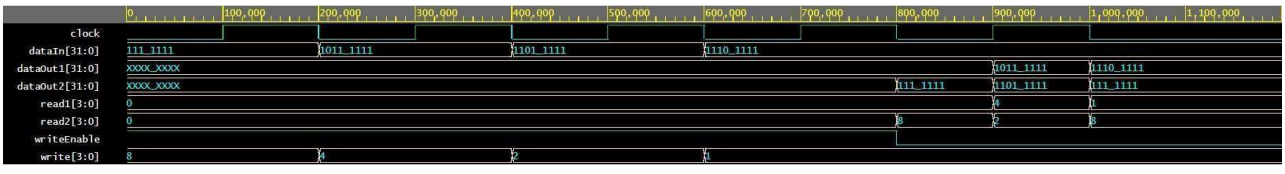

Figure 2: TestBench execution for register.vhd

3.

dataMem.vhd:

It contains an array of 64 std_logic_vectors of 32-bits. It has one read port and one write port, write is clocked whereas read is unclocked.

```
# Info: ************************************************************ # Info: Device
Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                     81      210     38.57%
# Info: Global Buffers          1       32      3.12%
# Info: LUTs                    900     63400   1.42%
# Info: CLB Slices              256     15850   1.62%
# Info: Dffs or Latches         2048    126800  1.62%
# Info: Block RAMs              0       135     0.00%
# Info: DSP48E1s                0       240     0.00%
# Info: ------------------------------------------------------------
# Info: ********************************************************
# Info: Library: work    Cell: DATA_MEMORY    View: BEV
# Info: ********************************************************
# Info:  Number of ports :                81
# Info:  Number of nets :                 162
# Info:  Number of instances :            82
# Info:  Number of references to this view :      0 # Info: Total accumulated area :
# Info:  Number of Dffs or Latches :      2048
# Info:  Number of LUTs :                 900
# Info:  Number of Primitive LUTs :       900
# Info:  Number of MUXF7 :                64
# Info:  Number of MUXF8 :                32
# Info:  Number of accumulated instances :      3126 # Info:
****************************
```

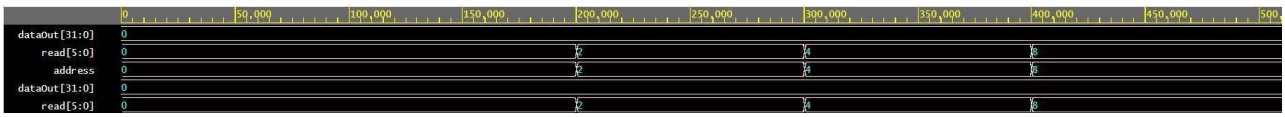

Figure 3: TestBench execution for programMemory.vhd

4.

programMemory.vhd:

It contains an array of 64 std_logic_vectors of 32-bits. It has only 1 read port.

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                     38      210     18.10%
# Info: Global Buffers          0       32      0.00%
# Info: LUTs                    0       63400   0.00%
# Info: CLB Slices              0       15850   0.00%
# Info: Dffs or Latches         0       126800  0.00%
# Info: Block RAMs              0       135     0.00%
# Info: DSP48E1s                0       240     0.00%
# Info: ------------------------------------------------------------
# Info: ************************************************************
# Info: Library: work    Cell: PROGRAM_MEMORY    View: BEV
# Info: ************************************************************
# Info:  Number of ports :                38
# Info:  Number of nets :                 33
# Info:  Number of instances :            33
# Info:  Number of references to this view :         0 # Info: Total accumulated area :
unknown
```

Results:

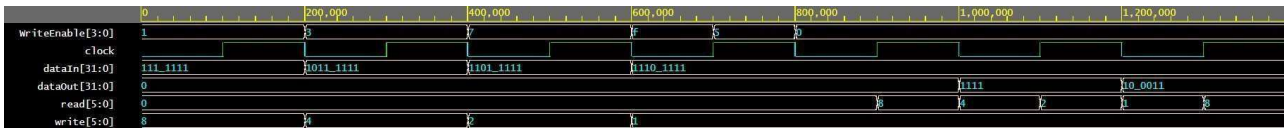

Figure 4: TestBench execution for dataMem.vhd

5.

Condition Checker

Checks whether the conditions are true according to the flags.

```
Info: Device Utilization for 7A100TCSG324
# Info: ***************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ---------------------------------------------------------------
# Info: IOs                               9       210       4.29%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              4       63400     0.01%
# Info: CLB Slices                        1       15850     0.01%
# Info: Dffs or Latches                   1       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ---------------------------------------------------------------
# Info: *******************************************************
# Info: Library: work    Cell: CondChecker    View: BEV
# Info: *******************************************************
# Info:  Number of ports :                            9
# Info:  Number of nets :                            24
# Info:  Number of instances :                       16
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of Dffs or Latches :                  1
# Info:  Number of LUTs :                             4
# Info:  Number of Primitive LUTs :                   4
# Info:  Number of accumulated instances :           16
```

6.flags.vhd

Sets the flag according to the OPCode and instructions

```
Device Utilization for 7A100TCSG324
# Info: ***************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ---------------------------------------------------------------
# Info: IOs                               106     210      50.48%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              8       63400     0.01%
# Info: CLB Slices                        2       15850     0.01%
# Info: Dffs or Latches                   4       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ---------------------------------------------------------------
# Info: *******************************************************
# Info: Library: work    Cell: Flags    View: Behavioral
# Info: *******************************************************
# Info:  Number of ports :                          106
# Info:  Number of nets :                            99
# Info:  Number of instances :                       59
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of Dffs or Latches :                  4
# Info:  Number of LUTs :                             8
# Info:  Number of Primitive LUTs :                   9
# Info:  Number of LUTs with LUTNM/HLUTNM :           2
# Info:  Number of accumulated instances :           59
# Info: ****************************
```

6.
7. ProgramCounter.vhd

Updates PC according to need

```
# Info: Device Utilization for 7A100TCSG324
# Info: ***********************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: -----------------------------------------------------------
# Info: IOs                               40      210      19.05%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              12      63400     0.02%
# Info: CLB Slices                        3       15850     0.02%
# Info: Dffs or Latches                   6       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: -----------------------------------------------------------
# Info: *********************************************************
# Info: Library: work    Cell: ProgramCounter    View: BEV
# Info: *********************************************************
# Info:  Number of ports :                            40
# Info:  Number of nets :                             60
# Info:  Number of instances :                        49
# Info:  Number of references to this view :           0
# Info: Total accumulated area :
# Info:  Number of Dffs or Latches :                   6
# Info:  Number of LUTs :                             12
# Info:  Number of Primitive LUTs :                   13
# Info:  Number of LUTs with LUTNM/HLUTNM :            2
# Info:  Number of MUX CARRYs :                        5
# Info:  Number of accumulated instances :            49
# Info: ****************************
# Info:  IO Register Mapping Report
```

8. Processor.vhd

Decoder + simulation of the entire program

```
Device Utilization for 7A100TCSG324
# Info: ***********************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: -----------------------------------------------------------
# Info: IOs                               1       210       0.48%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              0       63400     0.00%
# Info: CLB Slices                        0       15850     0.00%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: -----------------------------------------------------------
# Info: *********************************************************
# Info: Library: work    Cell: Processor    View: BEV
# Info: *********************************************************
# Info:  Number of ports :                            1
# Info:  Number of nets :                             0
# Info:  Number of instances :                        0
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of gates :                            0
# Info:  Number of accumulated instances :            0
# Info: ****************************
```