

COL216

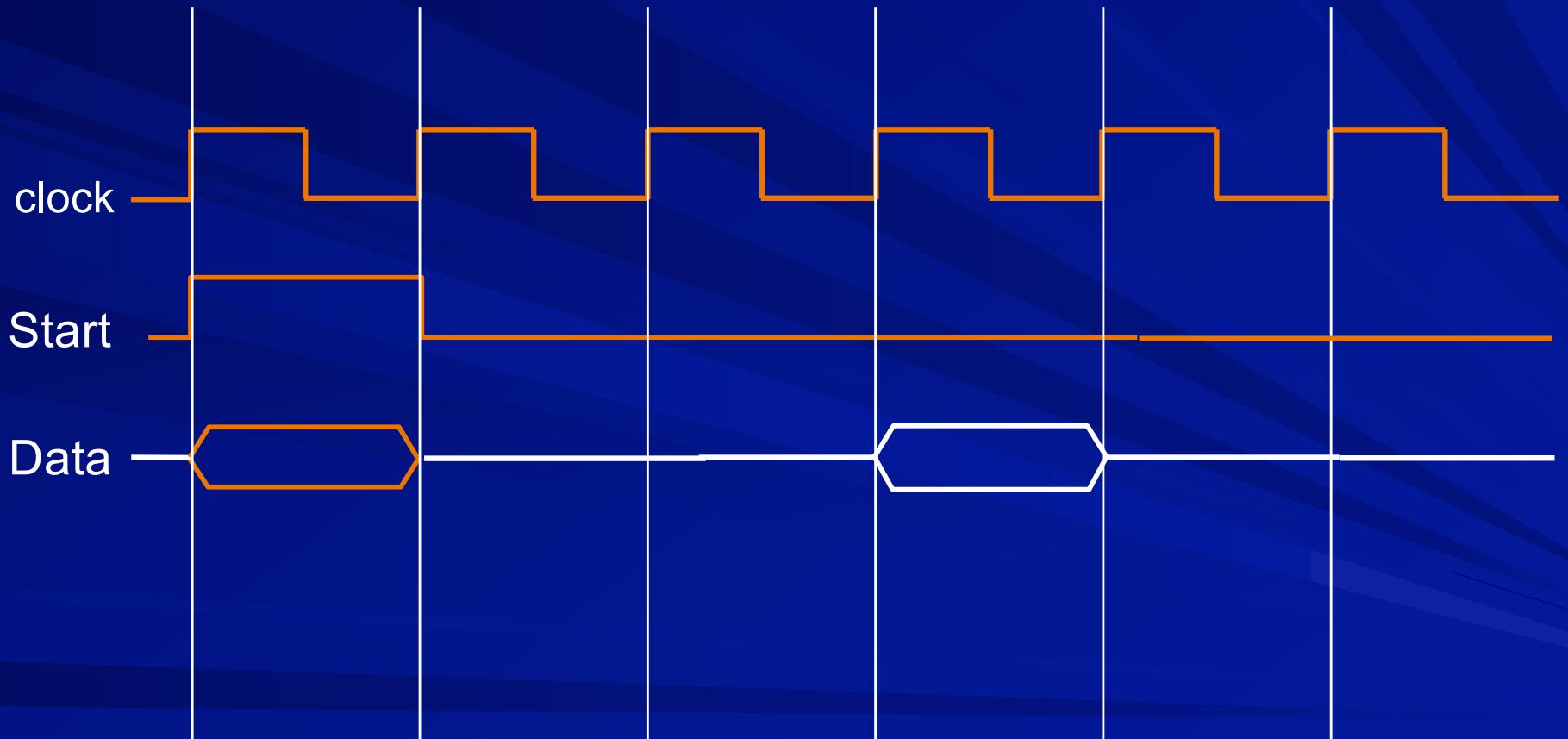
Computer Architecture

Input/Output – 5
Parallel and Serial Buses
28th March 2022

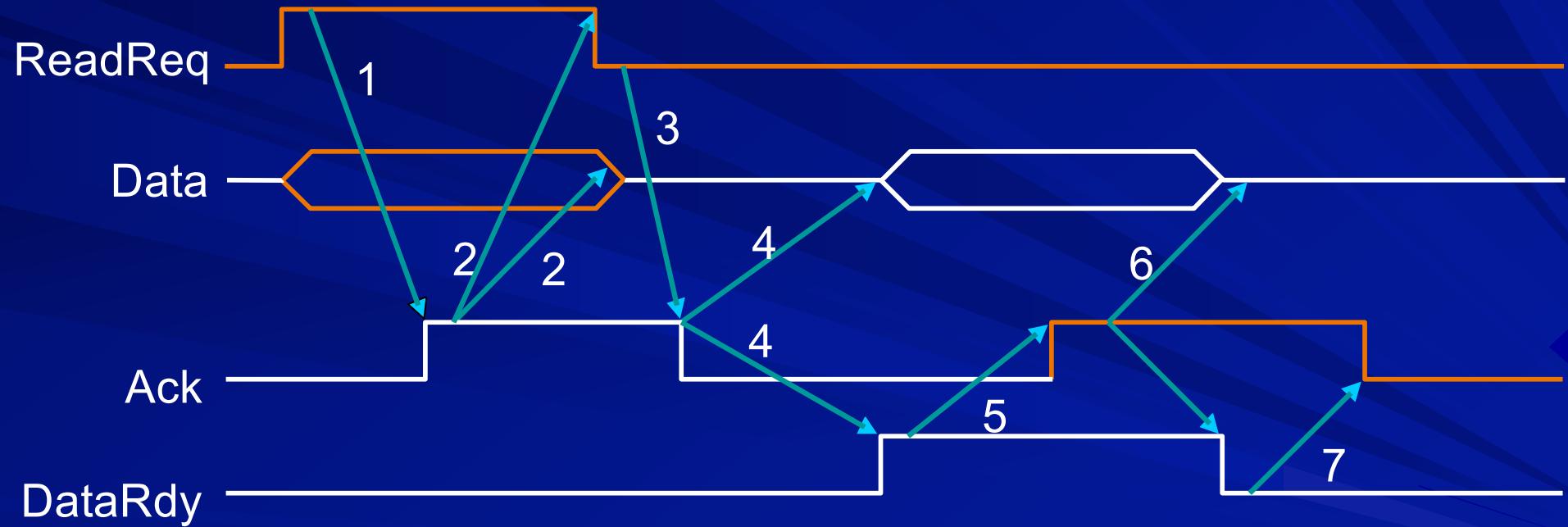
Increasing the bus bandwidth

- increase bus width
- separate data and address lines
- pipelining
- multiple word blocks
- synchronous
- split transaction

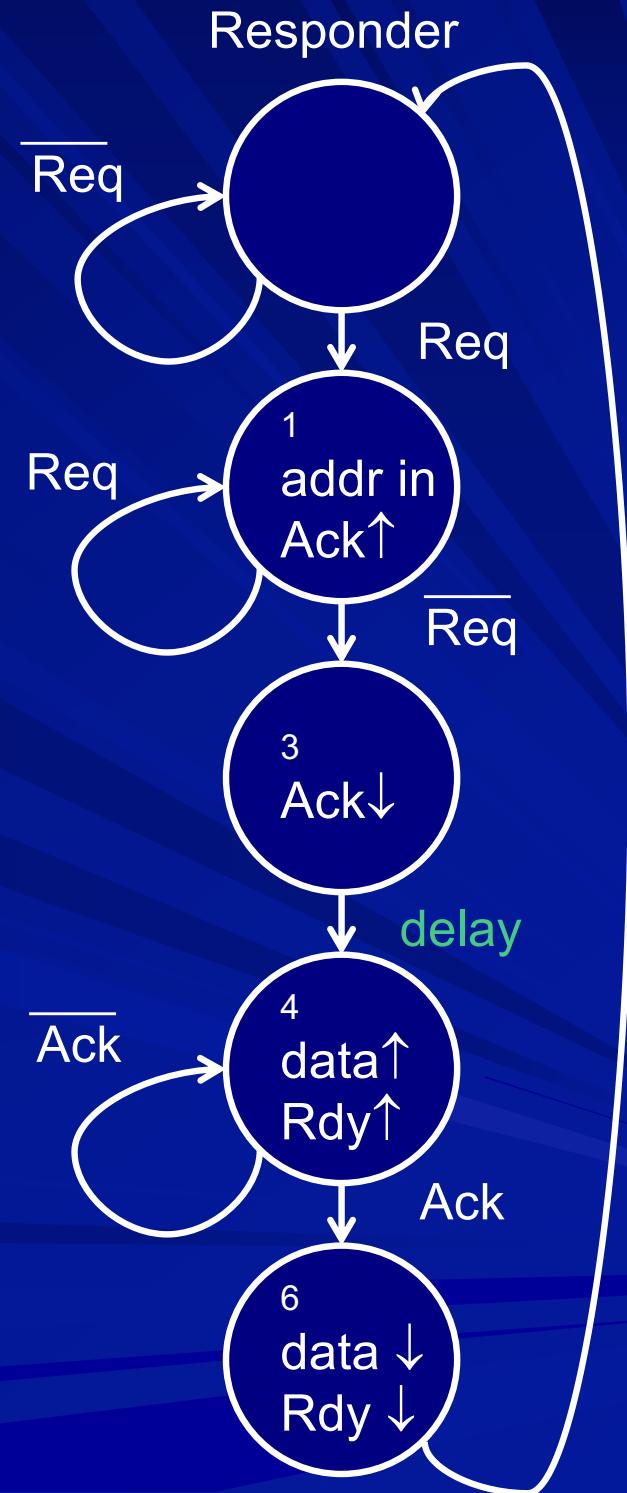
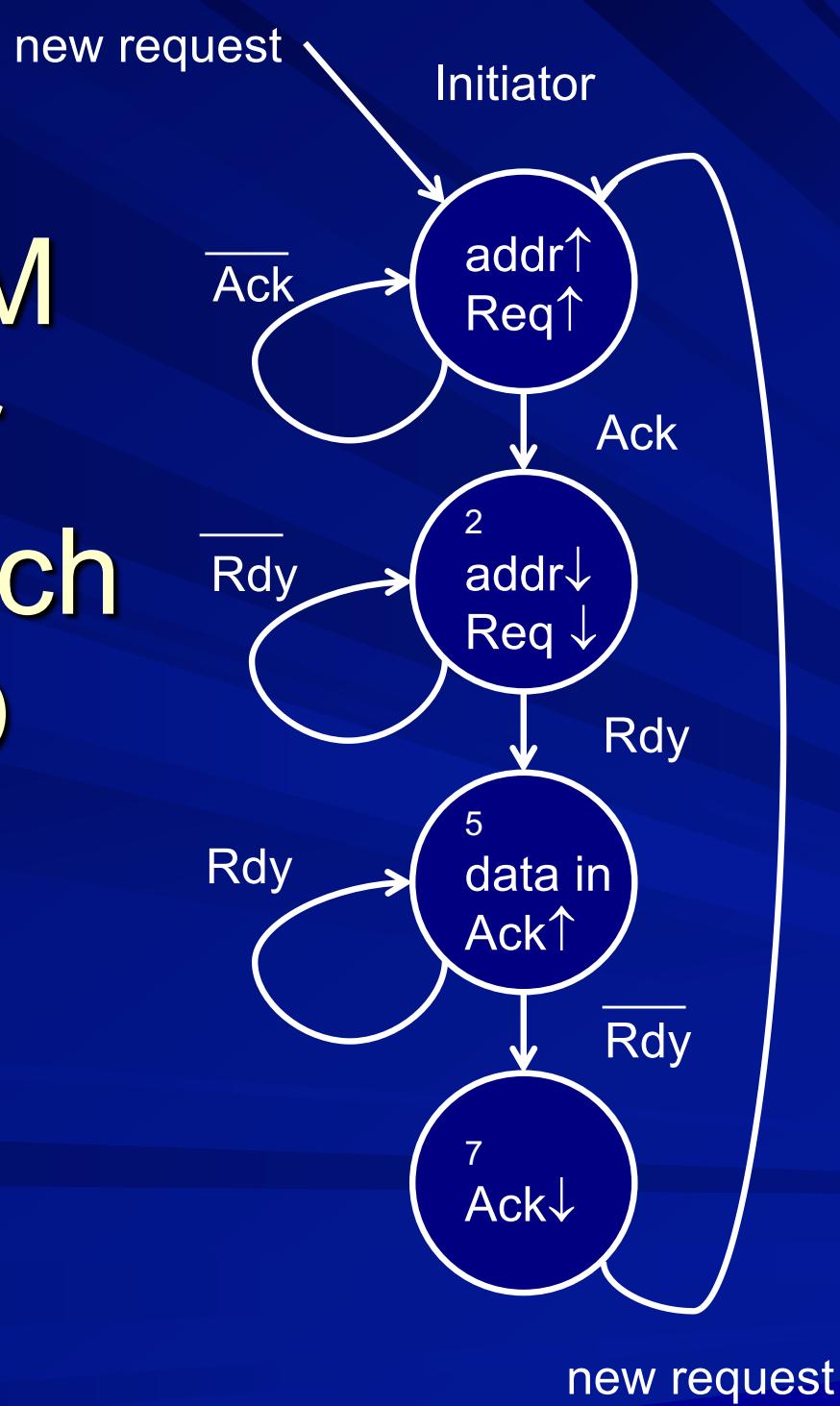
Synchronous transfer



Asynchronous handshaking



FSM for asynch I/O



Split transactions



Parallel vs Serial

■ Parallel

- multiple wires carry bits in parallel : 8-bit, 16-bit, 32-bit, 64-bit . . .
- address, read data, write data may use same wires or separate wires

■ Serial

- only one bit at a time
- read data, write data may use same wires or separate wires, no separate address wires

Series/parallel bus examples

Parallel

- ISA (Industry Standard Architecture)
- EISA (Extended ISA)
- VLB (VESA (Video Electronics Standards Association) Local Bus)
- PCI (Peripheral Component Interconnect)
- AGP (Accelerated Graphics Port)

Serial

- USB (Universal Serial Bus)
- Fire wire
- Fibre channel
- PCIe (Peripheral Component Interconnect express)
- SATA (Serial Advanced Technology Attachment)

Why serial buses?

- Serial buses are less expensive
- At high speed, keeping all the bits synchronized in parallel buses is very difficult
- Longer the signals travel, more skew is likely among the bits of parallel buses

Move from parallel to serial

PCI Bus

- PCI 1.0: 33MHz, 32-bit, peak BW 133MB/s
- PCI 2.2: 66 MHz, 64-bit, BW 533 MB/s
- PCI-X: 133MHz, 64-bit, BW 1066 MB/s
- PCI-X 2.0: 266MHz, BW 2133 MB/s

PCI-Express (serial bus), 1-16 lanes

- PCIe 1.0: 250 MB/s per lane
- PCIe 2.0: 500 MB/s per lane
- PCIe 3.0: 985 MB/s per lane

Move from parallel to serial

Parallel ATA

33 MB/s =>

66 MB/s =>

100 MB/s =>

133 MB/s

Serial ATA

150 MB/s =>

300 MB/s =>

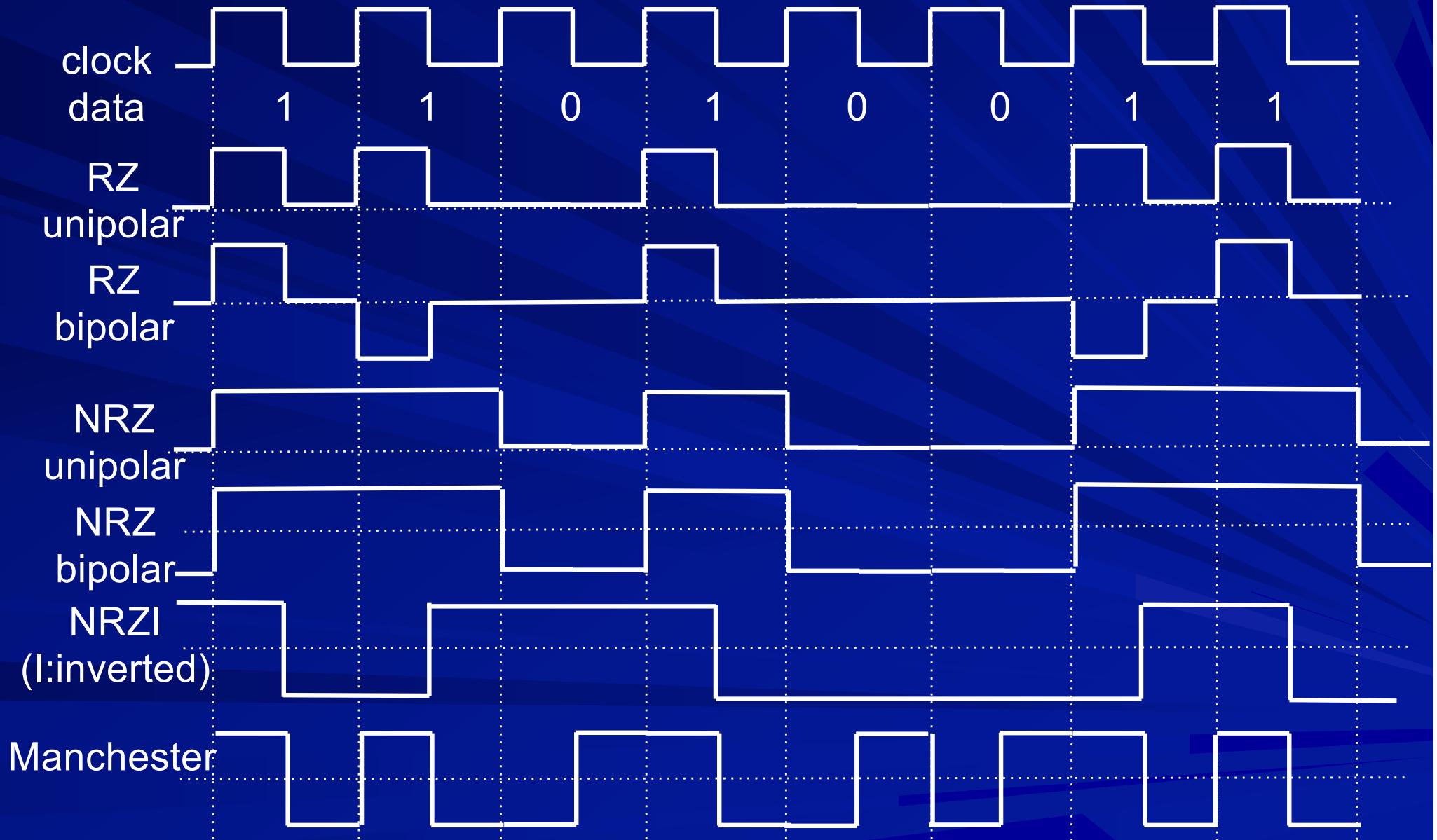
600 MB/s =>

1969 MB/s

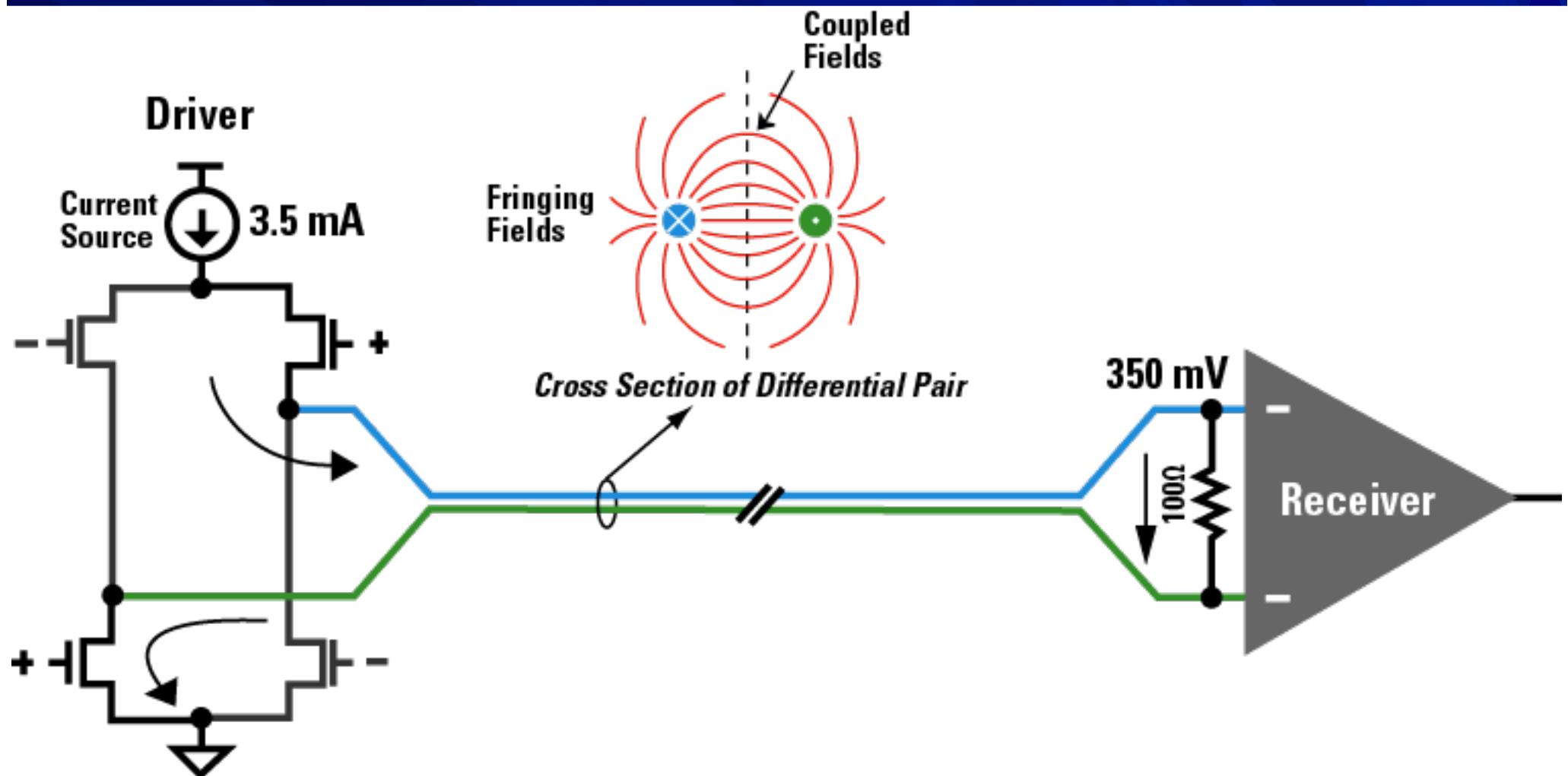
Representing bits

- Unipolar / bipolar
- Active high / active low
- Return to zero (RZ) / Non return to zero (NRZ)
- Encode using levels or transitions
- One wire / two wire (differential)

Representing bits



Low voltage differential signalling (LVDS)

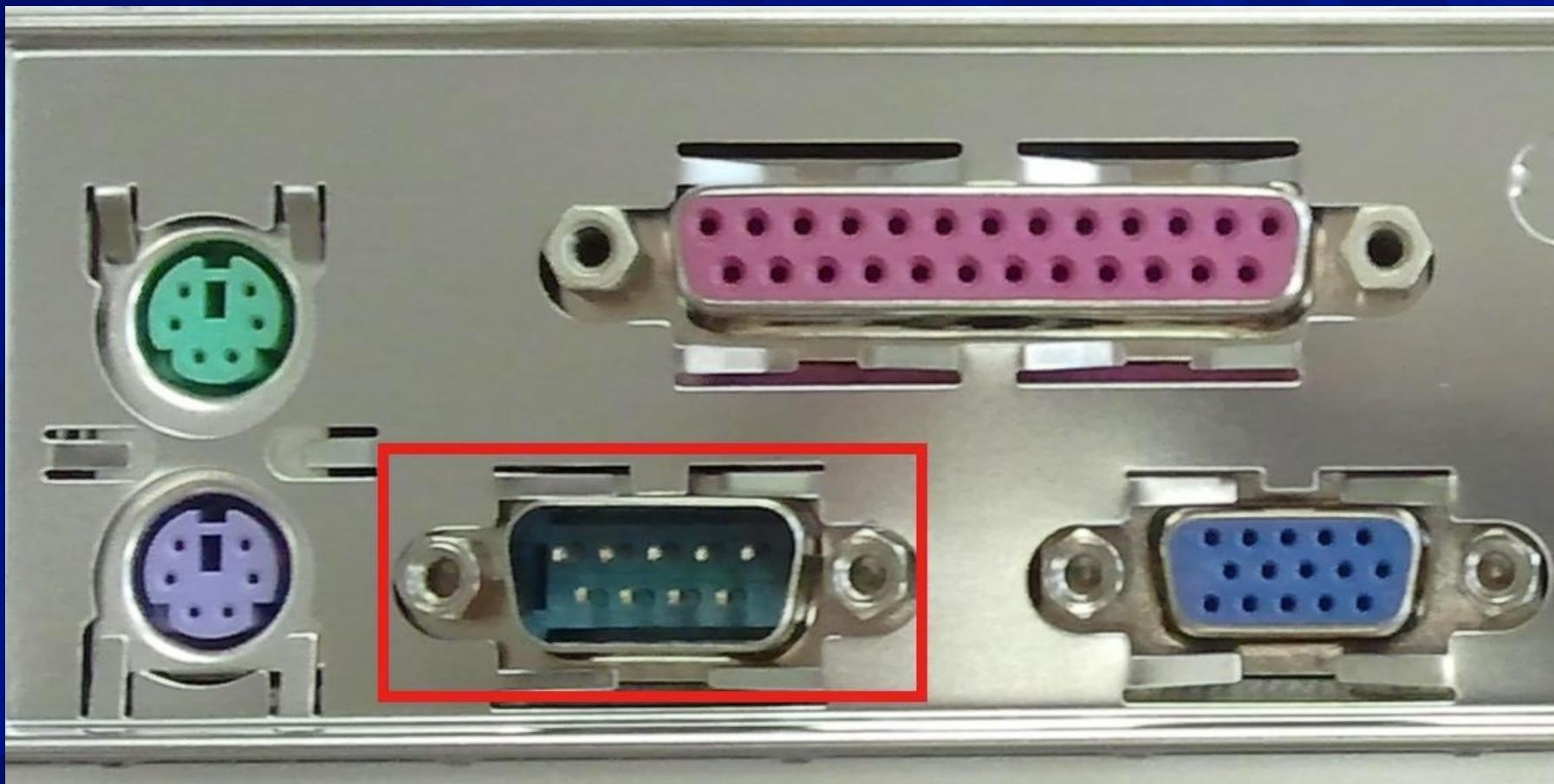


from wikipedia

Timing in serial transfer

- Synchronous
 - shared clock
 - same frequency and phase
- Mesochronous
 - transfer clock signal, separately or with data
 - same frequency but not phase
- Plesiochronous
 - locally generated clock
 - nearly same frequency, changing phase

Serial port / COM port



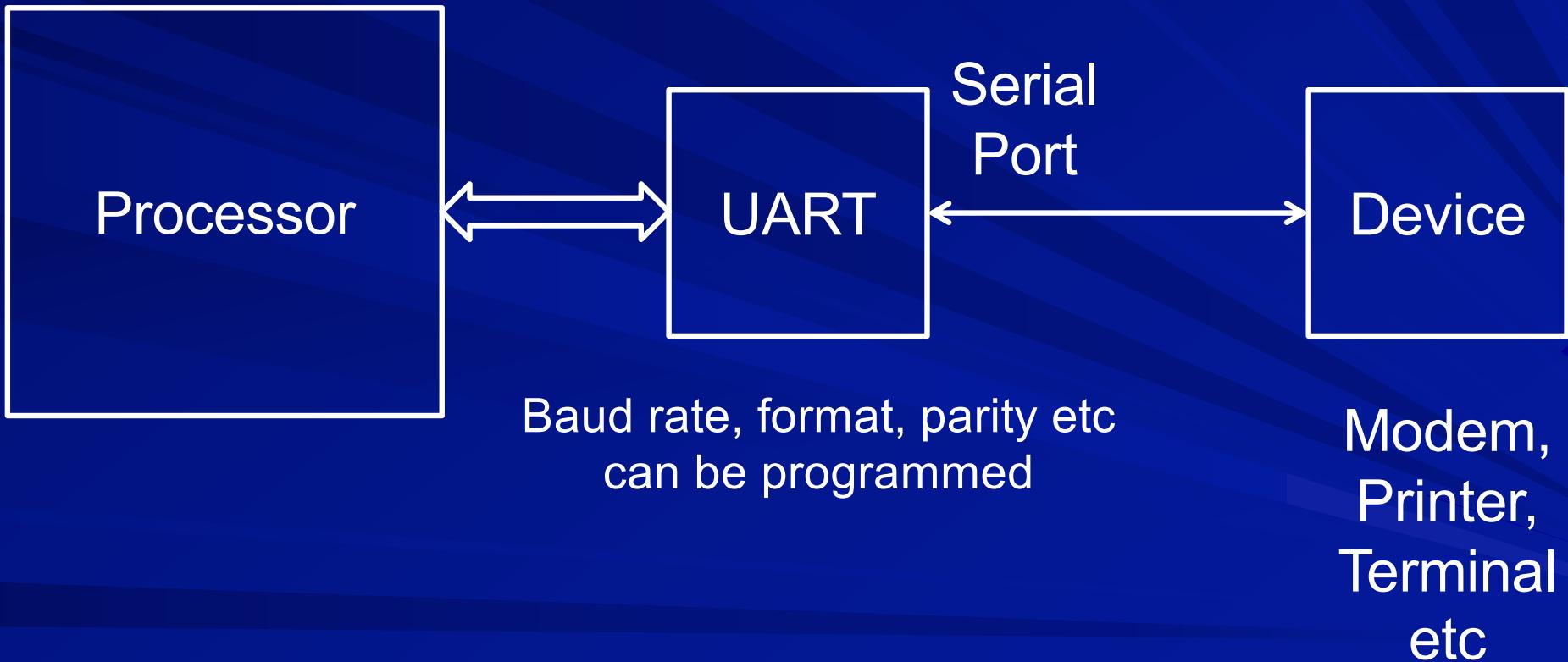
RS232 has been a common standard
75 to 115.2 K bits/s

RS232 Interface Standard



UART

(Universal Asynchronous
Receiver Transmitter)



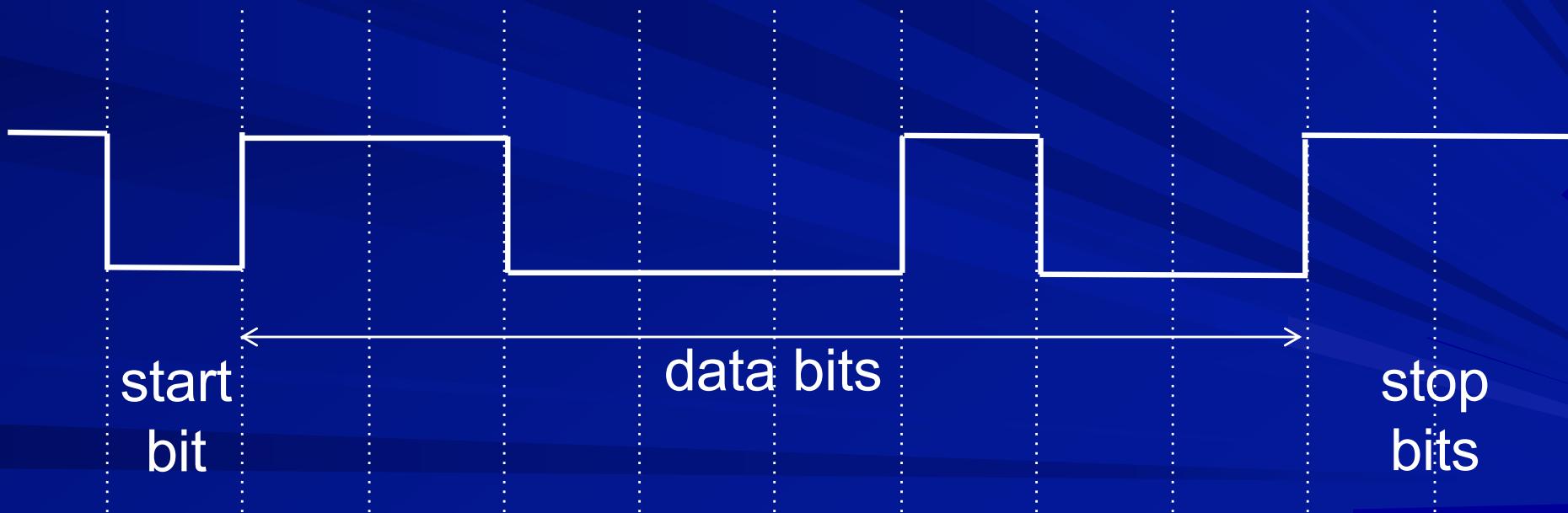
UART



Serial port: data waveform

■ Plesiochronous

- Synchronous at bit level
- Asynchronous at frame level



Data Framing



Data bits : 5 to 8

Parity : even / odd / none

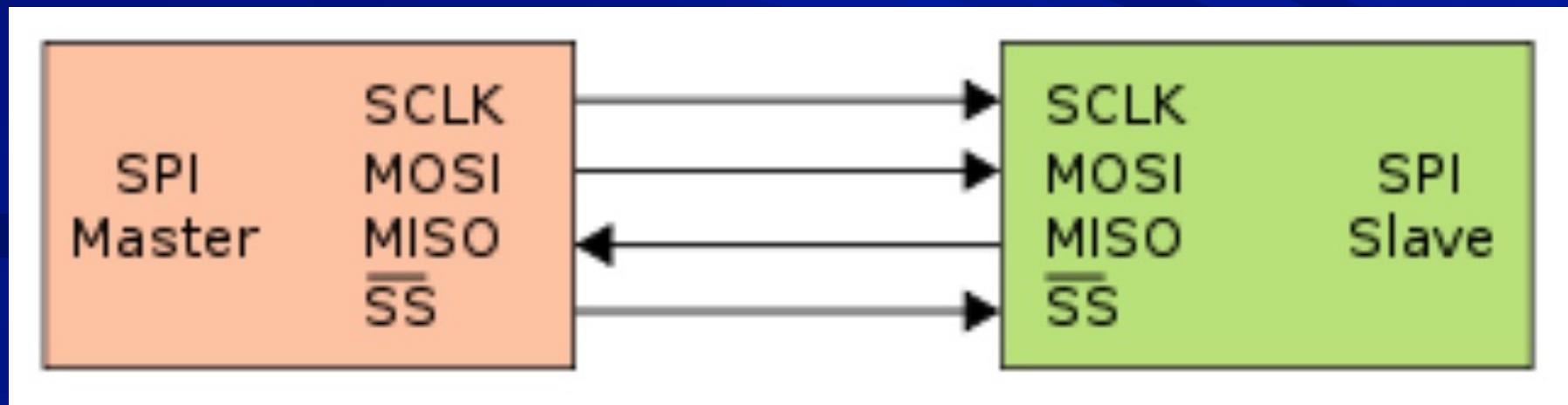
Start bits : 1

Stop bits : 1 or 2

Data rate : 300 / 600 / 1200 / 2400 / 4800 / 9600 . . .
bits/sec (bauds)

SPI : A simple serial interface

- SPI (Serial Peripheral Interface) is a synchronous serial protocol.
- Used for connecting some Pmods with BASYS-3.



SPI Signal Waveforms

