ELL100: INTRODUCTION TO ELECTRICAL ENGG.

Adder and Subtracter Circuits

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Textbook: Moris Mano's 'Digital Design':

Chapter 4.5 Binary Adder - Subtracter

Logic Circuits: Half Adder

- **Half Adder:** Sums two binary digits. Gives out sum (S) and carry (C) bits.

Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

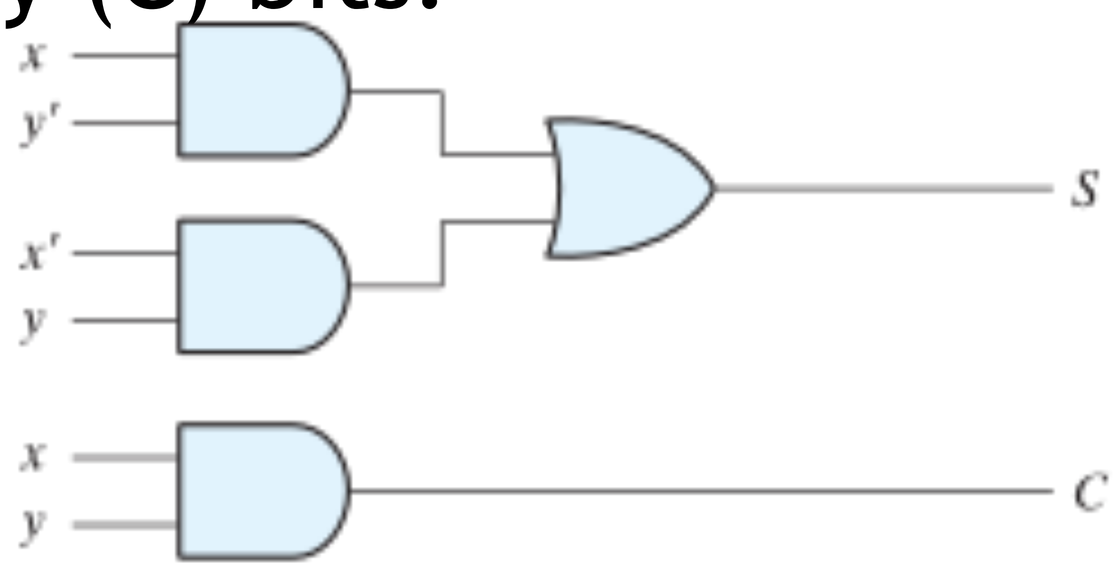
$$S = x'y + xy'$$
$$C = xy$$

Logic Circuits: Half Adder

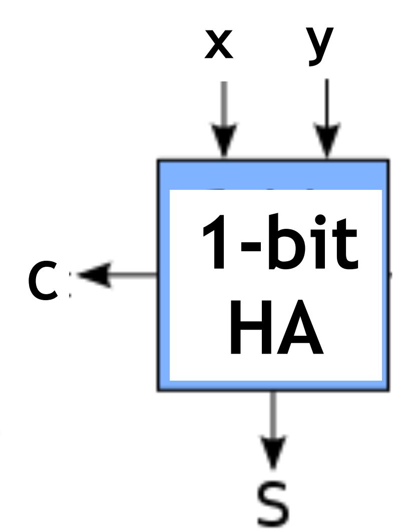
- **Half Adder:** Sums two binary digits. Gives out sum (S) and carry (C) bits.

Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



(a) $S = xy' + x'y$
$C = xy$

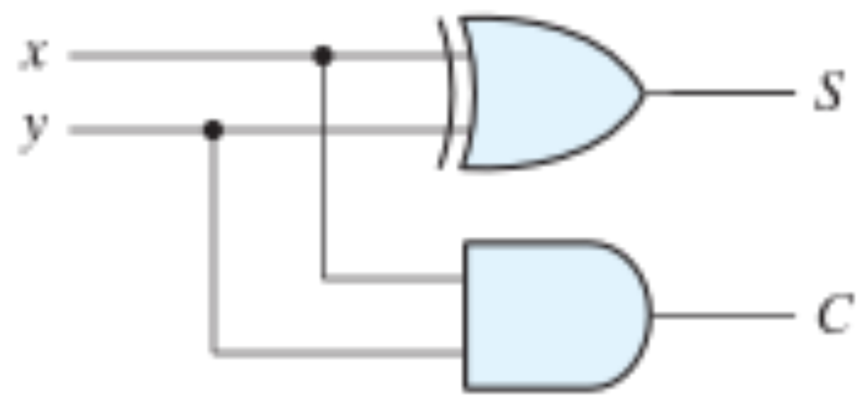


Logic Circuits: Half Adder

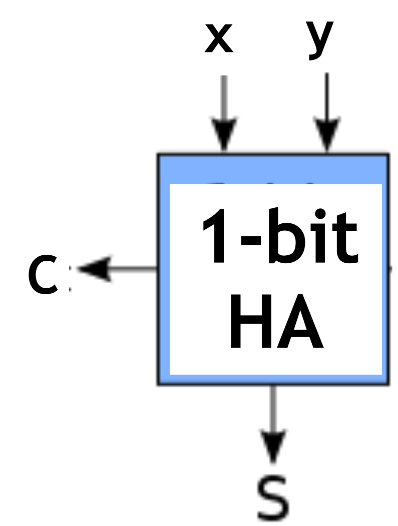
- **Half Adder:** Sums two binary digits. Gives out sum (S) and carry (C) bits.

Half Adder

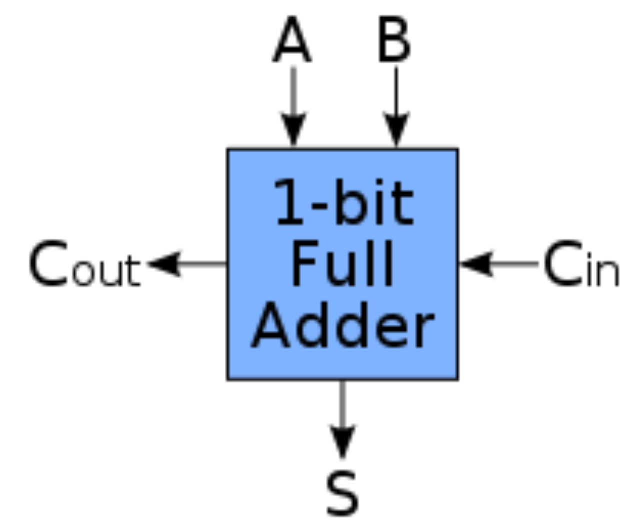
x	*y*	*C*	*S*
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



(b) $S = x \oplus y$
$C = xy$

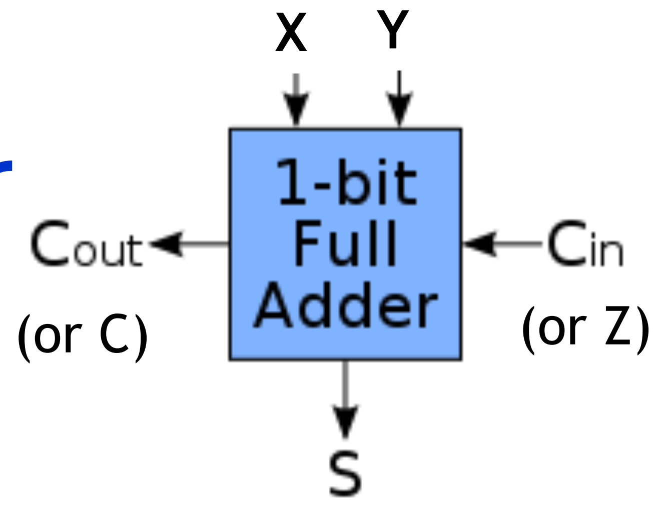


Logic Circuits: Full Adder



- **Half Adder** can only accept 2 input bits
- If two n-bit binary numbers are to be added, there can be carry-in bit also
- **Full Adder** makes provision for carry in bit

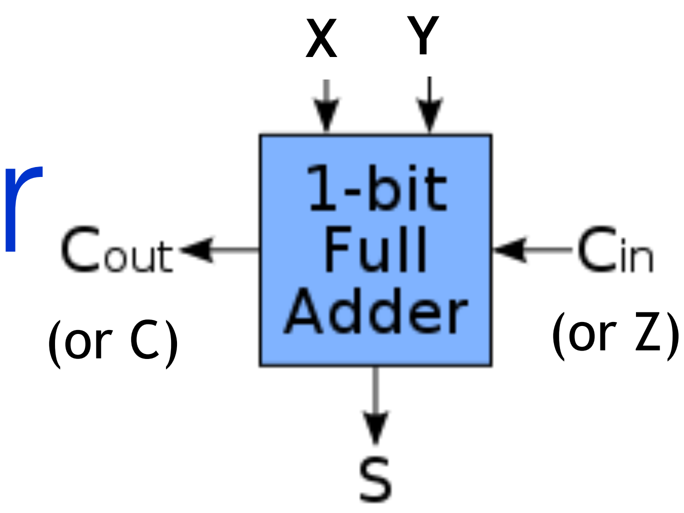
Logic Circuits: Full Adder



Full Adder

x	*y*	*z*	*C*	*S*
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Logic Circuits: Full Adder



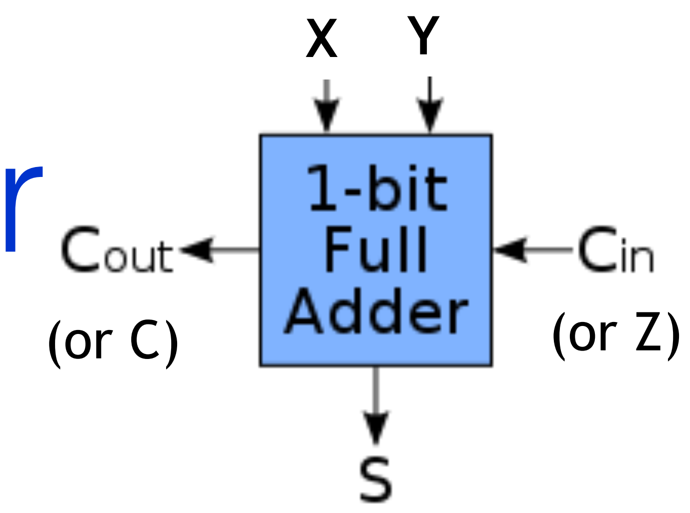
Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S = x'y'z + x'yz' + xy'z' + xyz$$

Output is 1 when an odd number of inputs are 1

Logic Circuits: Full Adder



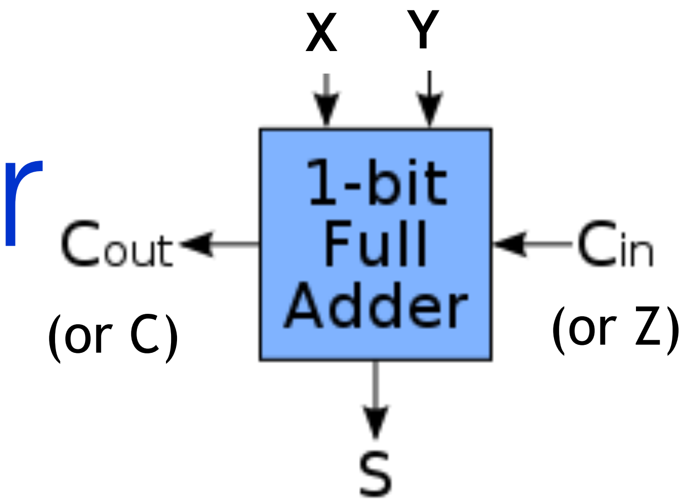
Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S = x'y'z + x'yz' + xy'z' + xyz = x \oplus y \oplus z$$
$$S = x'(y'z + yz') + x(y'z' + yz) = x'(y \oplus z) + x(y \oplus z)' = x \oplus y \oplus z$$

Distributive

Logic Circuits: Full Adder



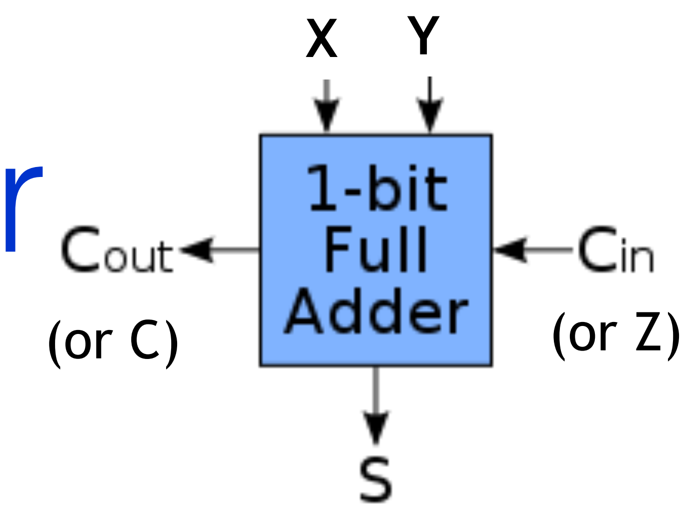
Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$C = x'yz + xy'z + xyz' + xyz$$

$$S = x'y'z + x'yz' + xy'z' + xyz = x \oplus y \oplus z$$

Logic Circuits: Full Adder



Full Adder

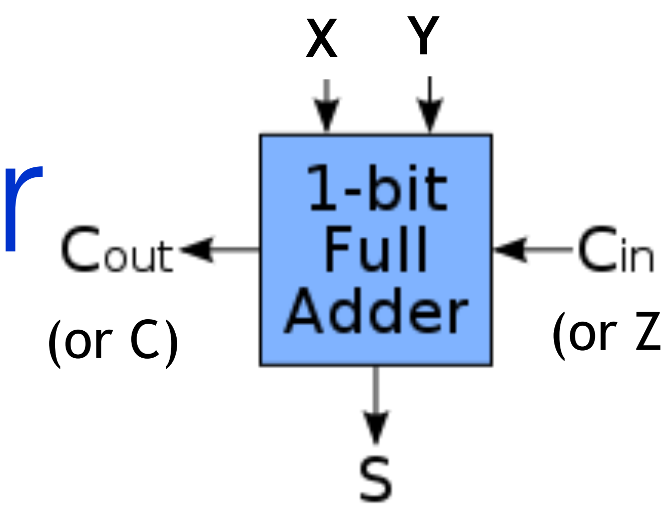
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$\begin{aligned} C &= x'yz + xy'z + xyz' + xyz \\ &= x'yz + xyz + xy'z + xyz + xyz' + xyz \end{aligned}$$

Idempotence

$$S = x'y'z + x'yz' + xy'z' + xyz = x \oplus y \oplus z$$

Logic Circuits: Full Adder



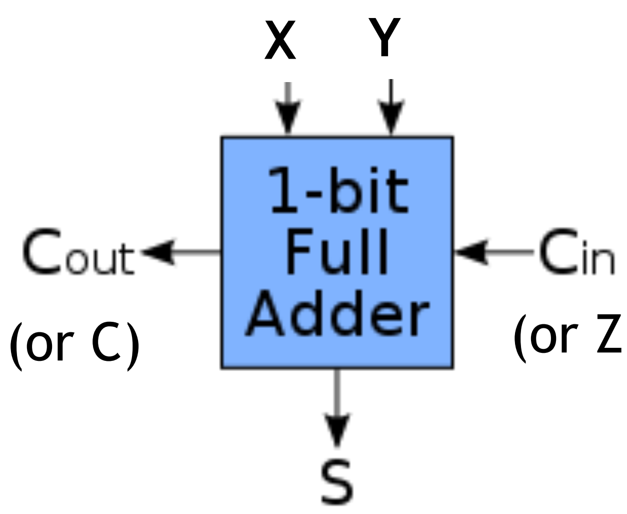
Full Adder

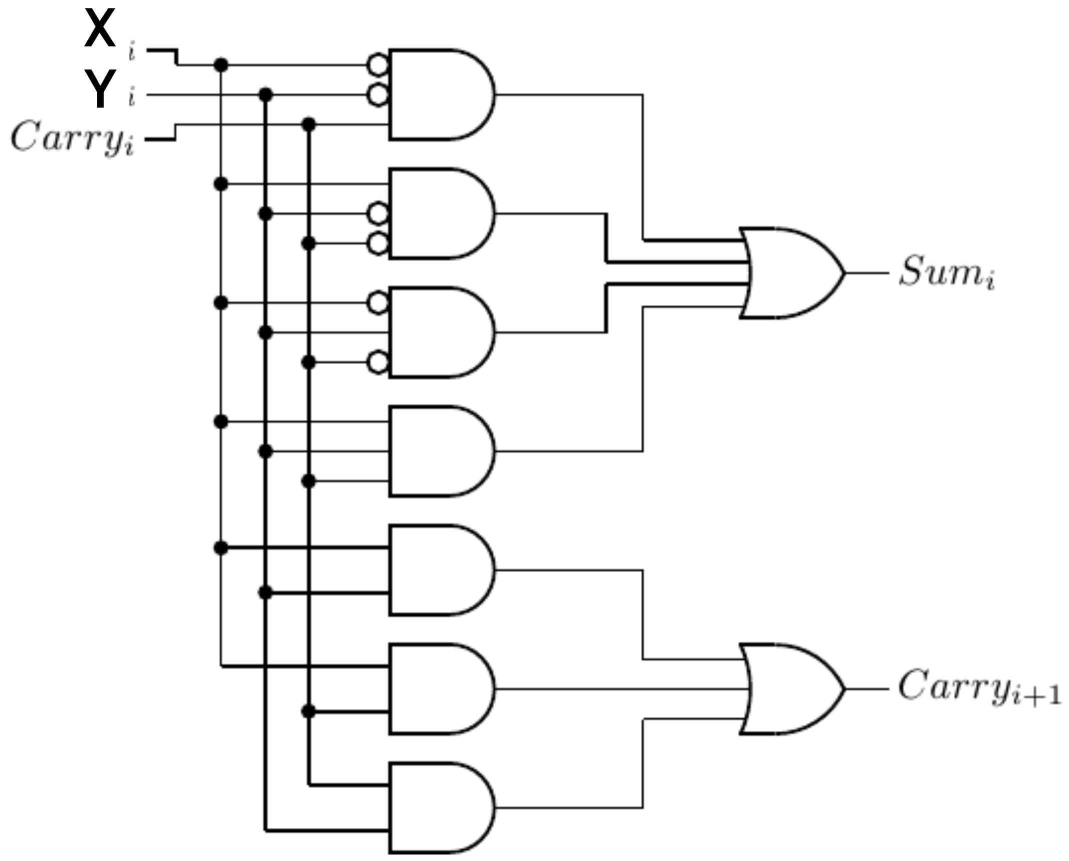
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

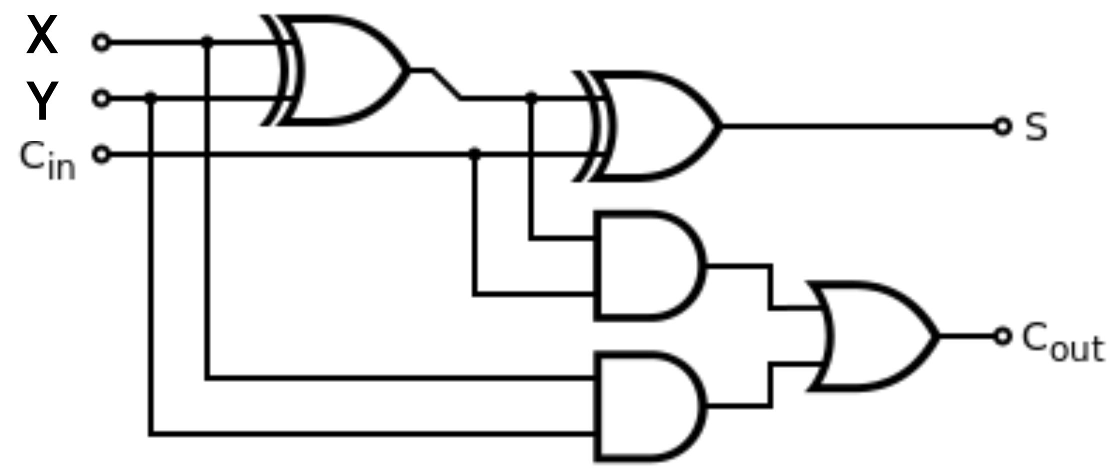
$$\begin{aligned} C &= x'yz + xy'z + xyz' + xyz \\ &= (x'+x)yz + x(y'+y)z + xy(z'+z) \quad \text{Distributive} \\ &= xy + yz + xz \quad \text{Complement} \end{aligned}$$

$$S = x'y'z + x'yz' + xy'z' + xyz = x \oplus y \oplus z$$

Full Adder: Logic Gates

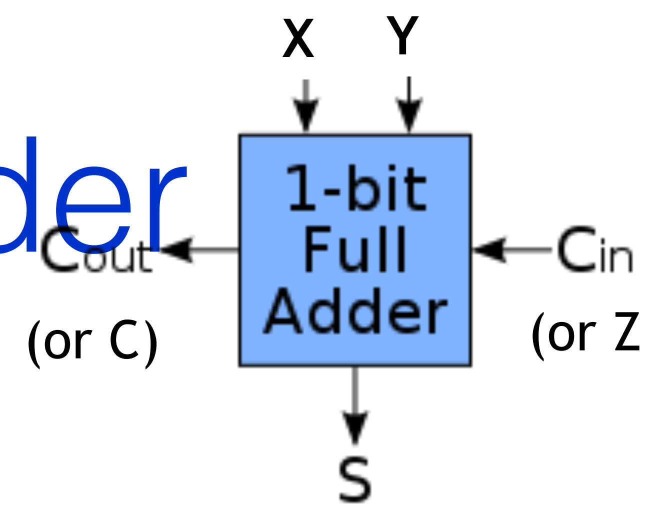






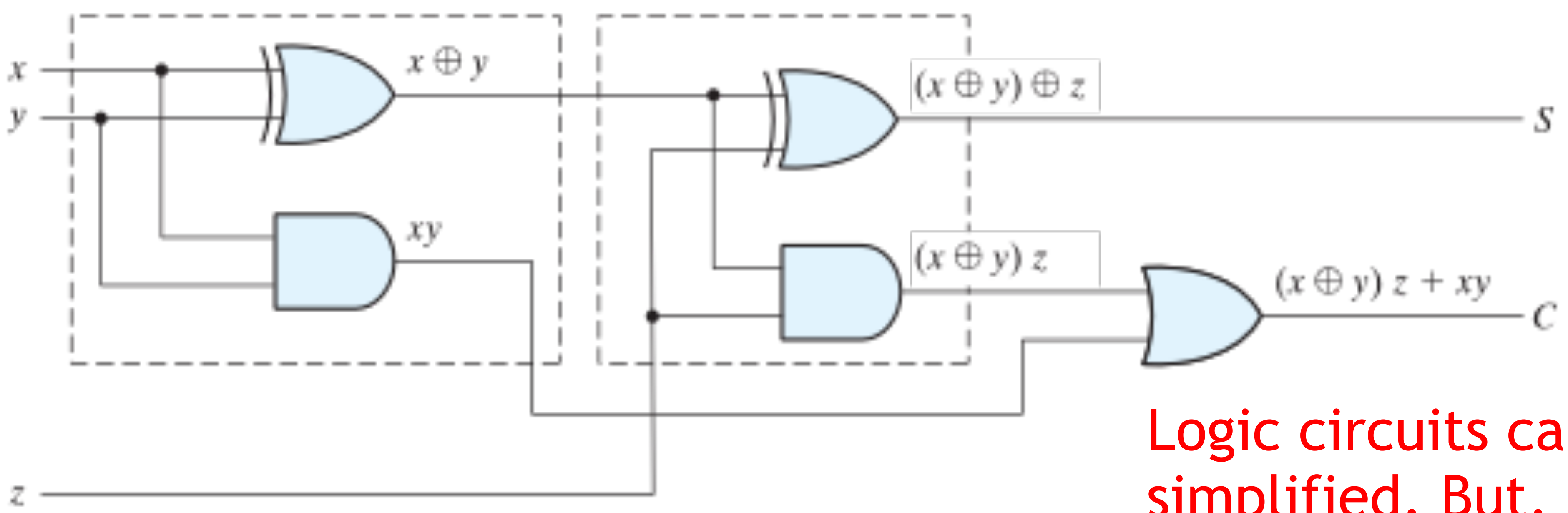
It is useful if the same logic can be implemented using lesser number of logic gates and logic levels.

Full Adder using Half Adder



$S = (x \oplus y) \oplus z$

$$\begin{aligned} C &= xy + yz + xz = xy + (x+y)z \\ &= xy + (x(y+y') + (x+x')y)z = xy + (xy + x \oplus y)z \\ &= xy + xyz + (x \oplus y)z = xy + (x \oplus y)z \end{aligned}$$



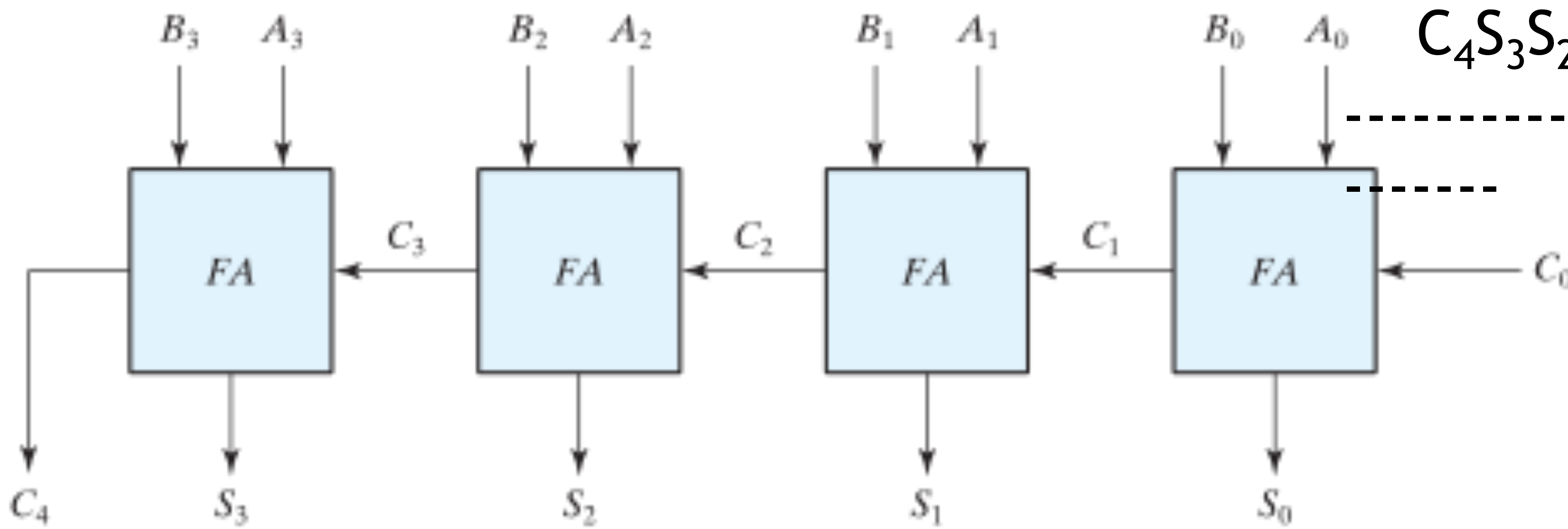
Logic circuits can be simplified. But, there should be some systematic approach.

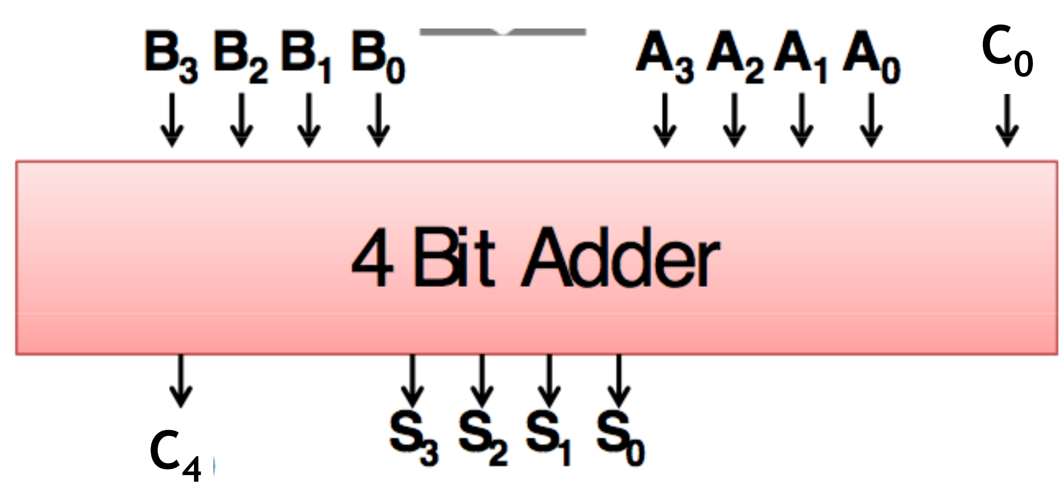
4 Bit Binary Adder

$A_3A_2A_1A_0 \leftarrow \quad C_0$

$+ \quad B_3B_2B_1B_0$

$C_4S_3S_2S_1S_0$





4 Bit Binary Adder+Subtractor

$A_3A_2A_1A_0 \leftarrow \quad C_0$

$+/-\ \ B_3B_2B_1B_0$

$C_4S_3S_2S_1S_0$

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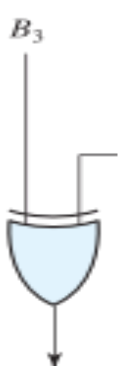
1. Need a **<u>selection bit</u>** to select between the 2 operations – ADD or SUB
2. If SUB, then first Flip all the bits of B, and find B'
3. Add B' to A (like the normal ADDER)
4. Add 1 to the Sum



Select bit (M) = 1 → Output flips B, Enable Subtract

Select bit (M) = 0 → Output=B, Enable Add