ELL100: INTRODUCTION TO ELECTRICAL ENGG.

Bipolar Junction Transistors - Characteristics and Biasing Circuits

Instructor: Debanjan Bhowmik

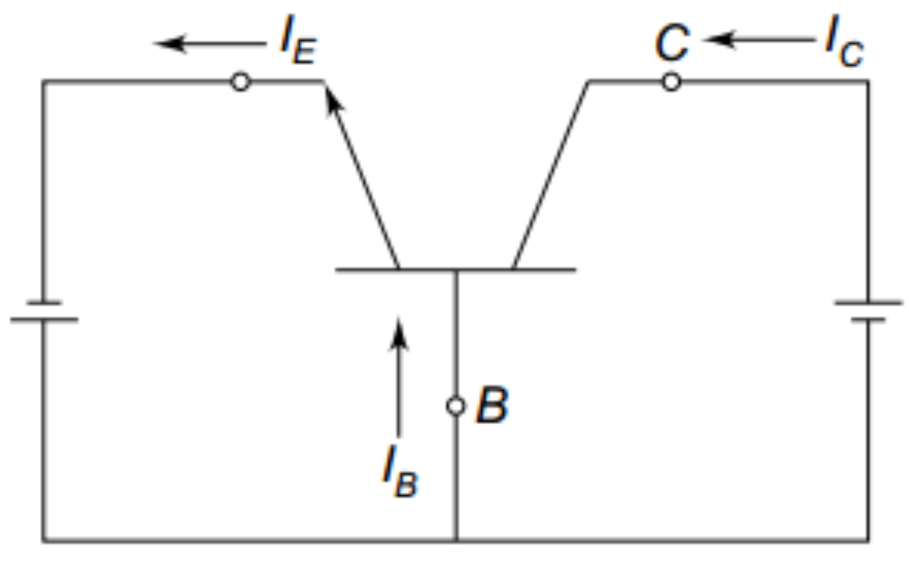
Reference: Donald Neamen's 'Electronic Circuit Analysis'
Chapter 3 (BJT)

Ideal Equivalent Circuit

I_E, I_B, I_C are the currents flowing through emitter, base and collector terminal.

Assuming no leakage I_{CBO}.

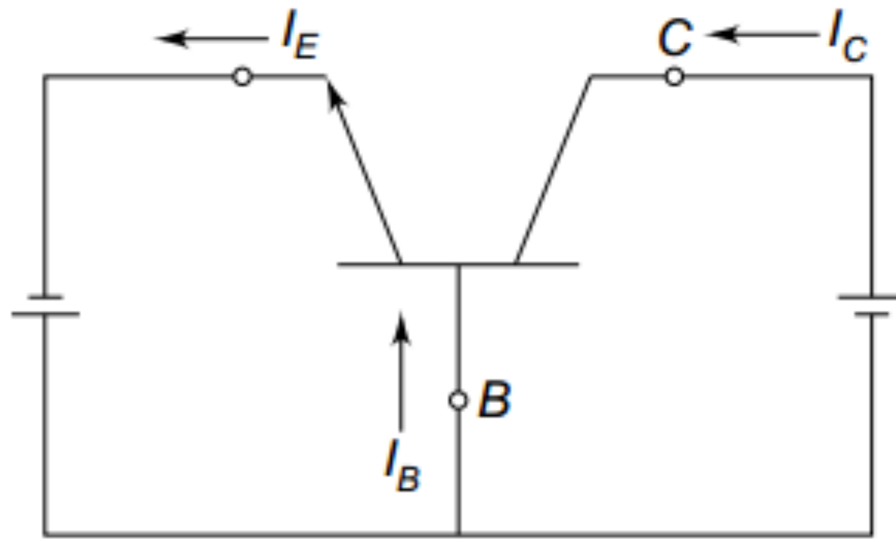
$$I_E = I_B + I_C$$



Ideal Equivalent Circuit

I_E, I_B, I_C are the currents flowing througl emitter, base and collector terminal. Assuming no leakage I_{CBO}.

$$I_E = I_B + I_C$$



$$I_C = \frac{\alpha}{1-\alpha} I_B$$

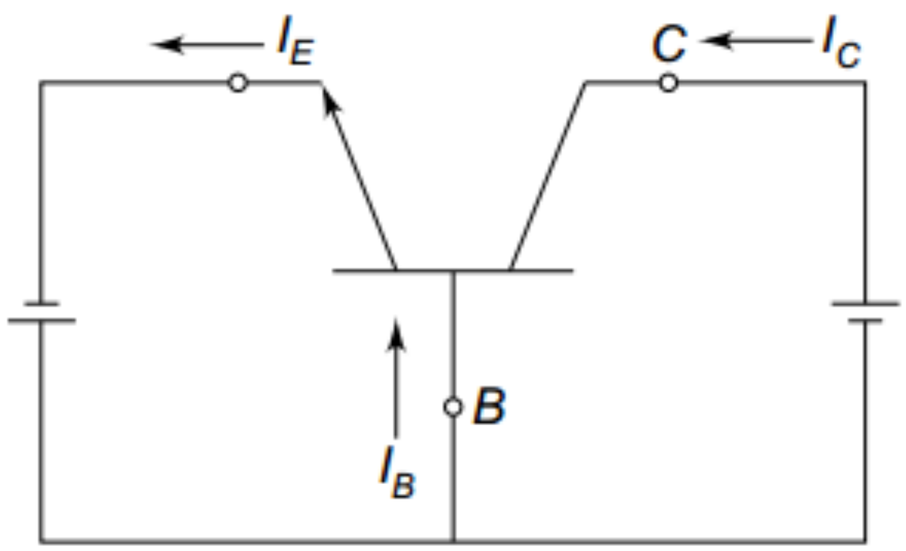
$$I_C = \beta \quad I_B$$

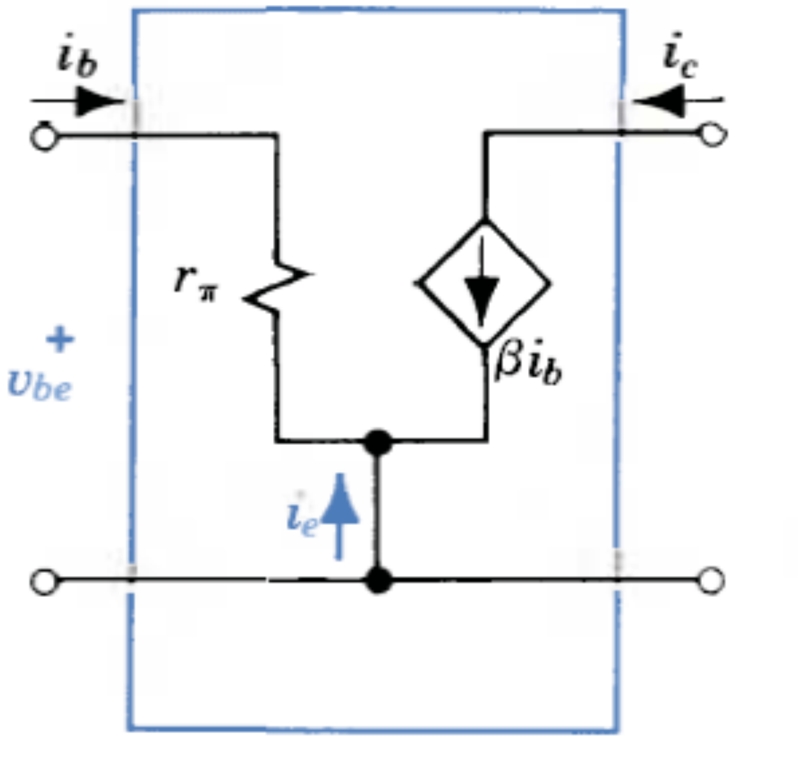
$$\beta = \frac{\alpha}{1-\alpha} = \frac{I_C}{I_B}$$

Ideal Equivalent Circuit

I_E, I_B, I_C are the currents flowing thr
emitter, base and collector terminal
Assuming no leakage I_{CBO}.

$$I_E = I_B + I_C$$





$$I_C = \frac{\alpha}{1-\alpha} I_B$$

$$I_C = \beta \quad I_B$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{I_C}{I_B}$$

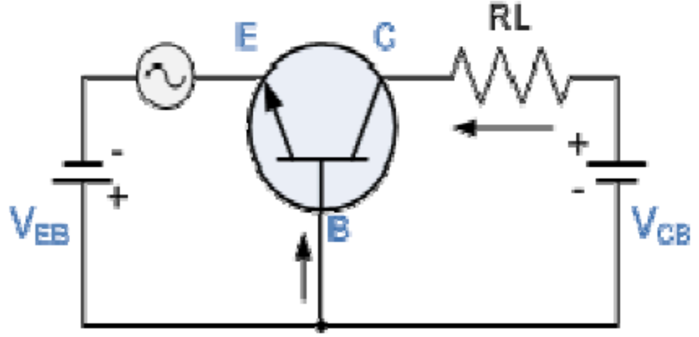
$$r_\pi = \frac{\Delta v_{be}}{\Delta i_b}$$

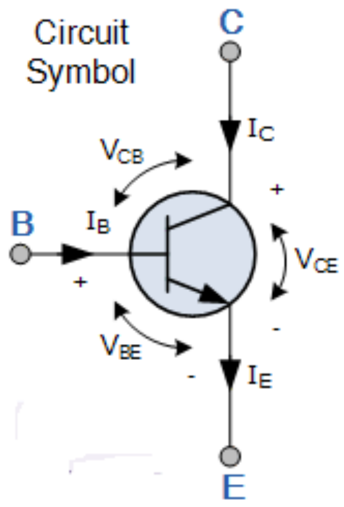
Dynamic Junction Resistance

BJT DC Behavior: Common Base Characteristics

In CB configuration, the base terminal is common to input and output voltages (npn transistor). V_{EB} is negative (input voltage), V_{CB} is positive (output voltage)

Common base configuration

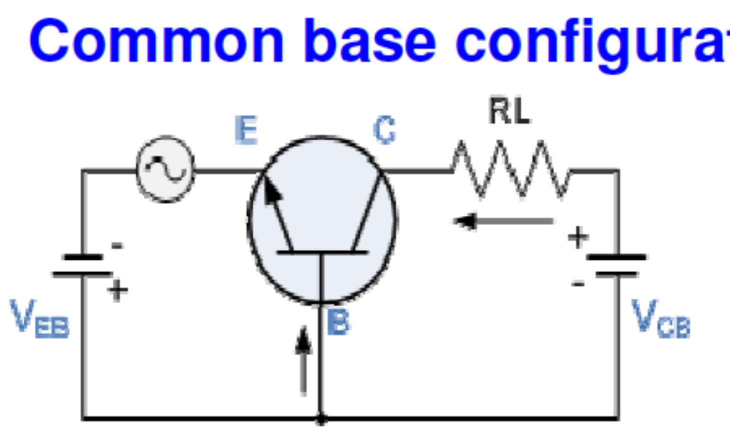


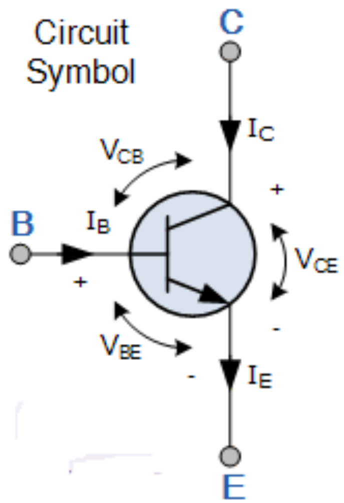


BJT DC Behavior: Common Base Characteristics

In CB configuration, the base terminal is common to input and output voltages (npn transistor). V_{EB} is negative (input voltage), V_{CB} is positive (output voltage)

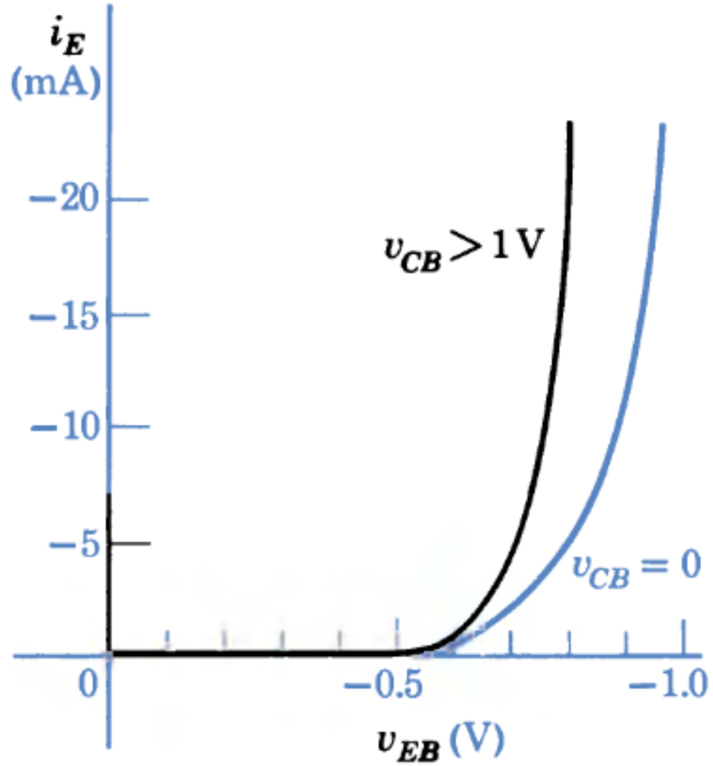
- The Emitter base combination is basically a forward biased pn junction.
- Hence, V_{EB} to I_E relation is exponential.
- Increasing the reverse bias in C-B junction improves current. (Thin base)





Input Characteristics

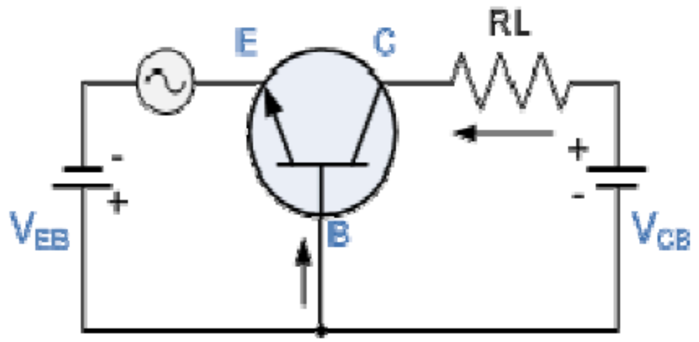
The relationship between the input voltage, V_{EB} and the input current, I_E for a constant output voltage.

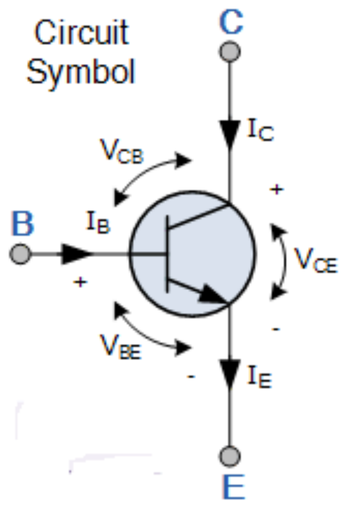


BJT DC Behavior: Common Base Characteristics

In CB configuration, the base terminal is common to input and output voltages (npn transistor). V_{EB} is negative (input voltage), V_{CB} is positive (output voltage)

Common base configuration





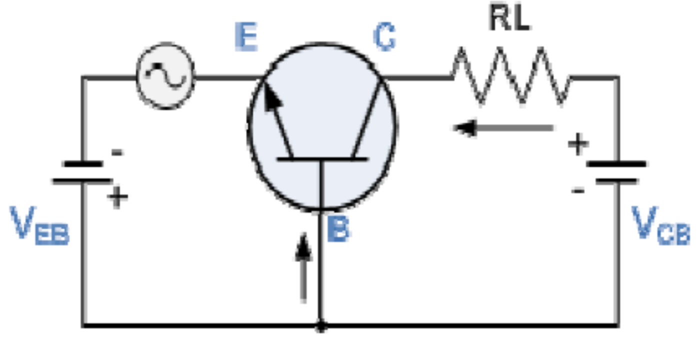
Output Characteristics

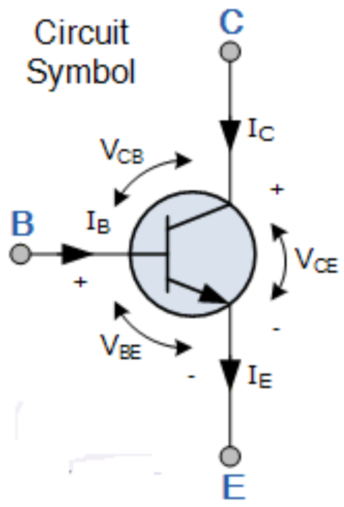
I_E is kept constant by applying a fixed input voltage V_{EB}. Then the reverse bias of V_{CB} is increased and the collector current observed for each value of V_{CB}.

BJT DC Behavior: Common Base Characteristics

In CB configuration, the base terminal is common to input and output voltages (npn transistor). V_{EB} is negative (input voltage), V_{CB} is positive (output voltage)

Common base configuration





Note that :

$I_C = \alpha I_E + I_{CBO}$

Because E-doping > C-doping some current flows even for small forward bias of C-B

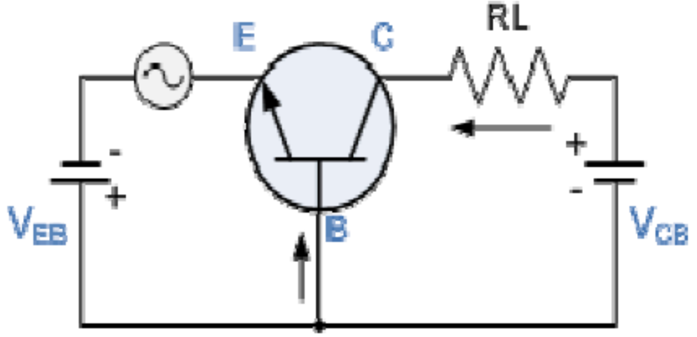
Output Characteristics

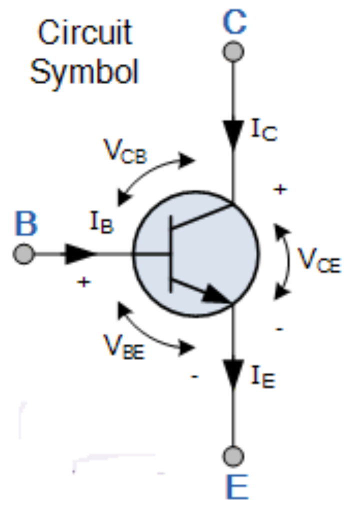
I_E is kept constant by applying a fixed input voltage V_{EB}. Then the reverse bias of V_{CB} is increased and the collector current observed for each value of V_{CB}.

BJT DC Behavior: Common Base Characteristics

In CB configuration, the base terminal is common to input and output voltages (npn transistor). V_{EB} is negative (input voltage), V_{CB} is positive (output voltage)

Common base configuration





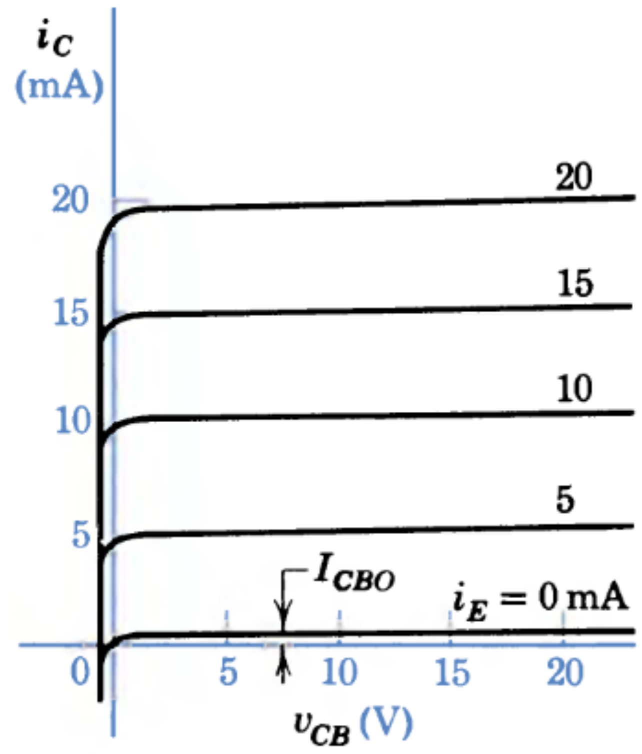
Output Characteristics

I_E is kept constant by applying a fixed input voltage V_{EB}. Then the reverse bias of V_{CB} is increased and the collector current observed for each value of V_{CB}.

Note that :

$I_C = \alpha I_E + I_{CBO}$

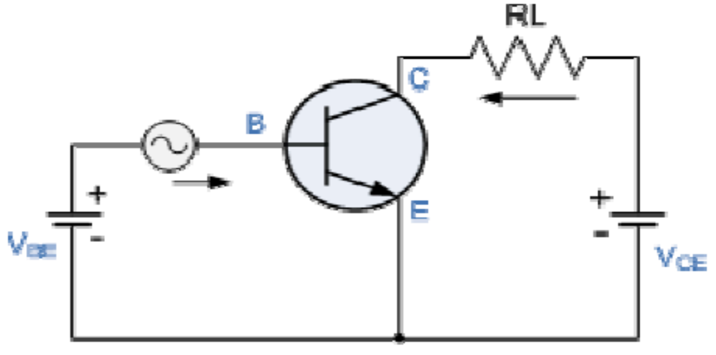
Because E-doping > C-doping some current flows even for small forward bias of C-B

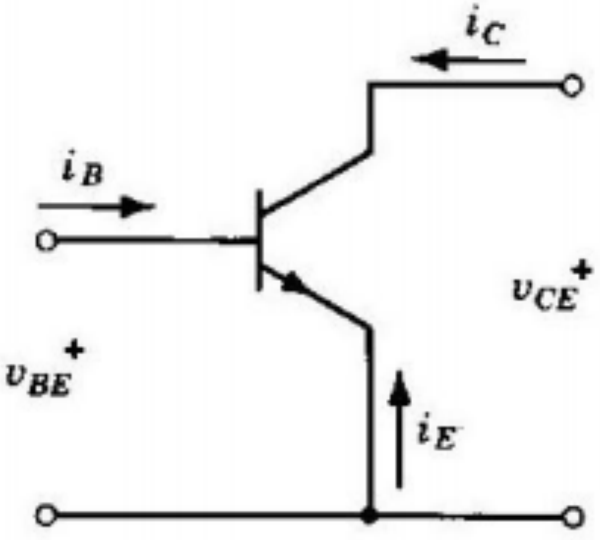


BJT DC Behavior: Common Emitter Characteristics

In CE configuration, the emitter terminal is common to input and output voltages (npn transistor).
V_{BE} is positive (input voltage)
V_{CE} is positive (output voltage)

Common emitter configuration

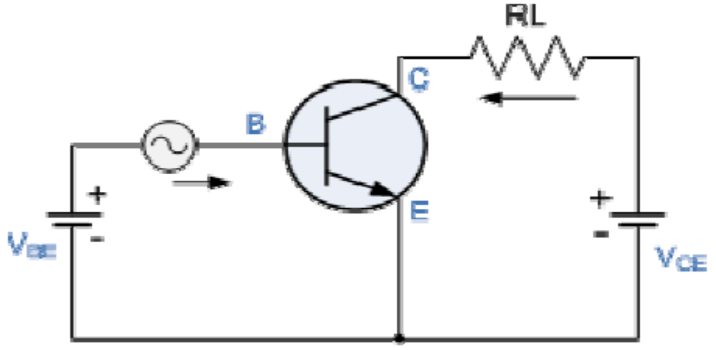


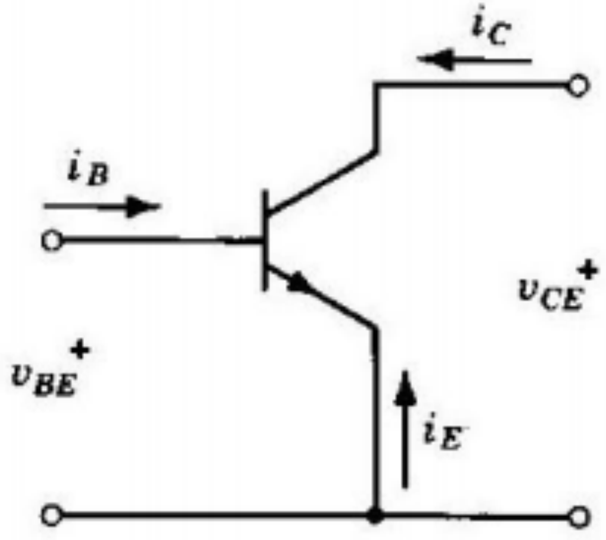


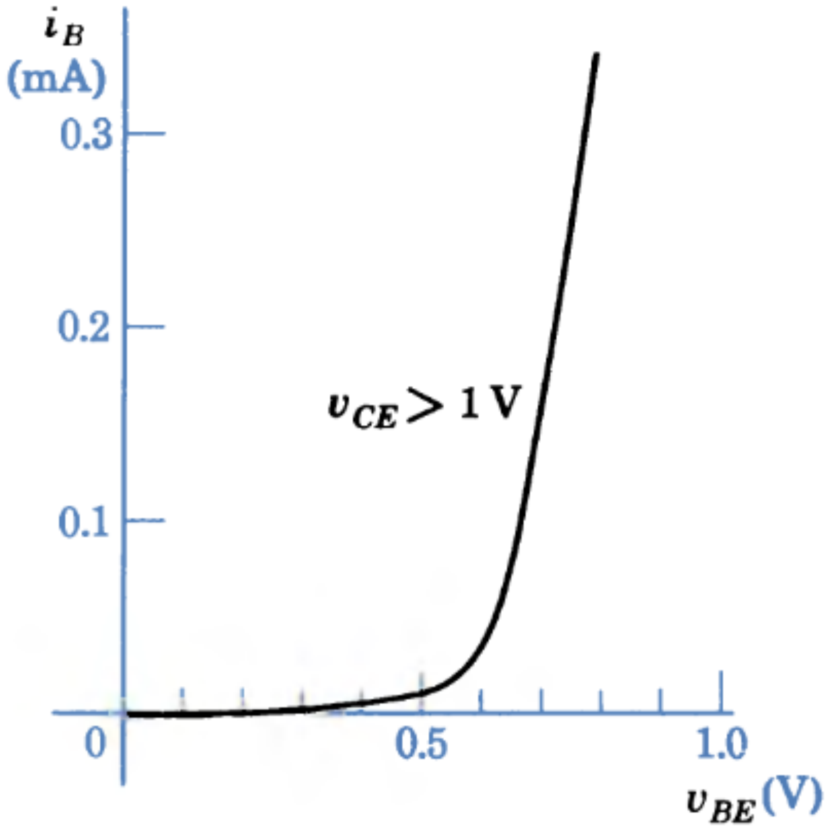
BJT DC Behavior: Common Emitter Characteristics

In CE configuration, the emitter terminal is common to input and output voltages (npn transistor).
V_{BE} is positive (input voltage)
V_{CE} is positive (output voltage)

Common emitter configuration







Input Characteristics

The input characteristics is a plot of V_{BE} vs I_B at constant V_{CE} .

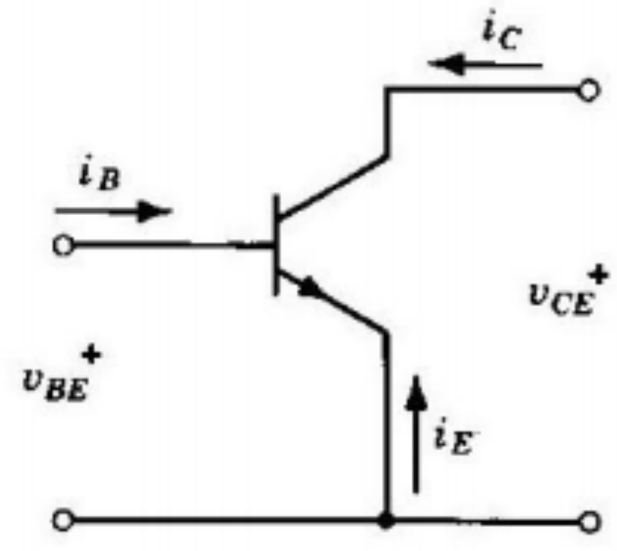
BJT DC Behavior

Common Emitter characteristics

In CE configuration, the emitter terminal is common to input and output voltages (npn transistor).
V_{BE} is positive (input voltage)
V_{CE} is positive (output voltage)

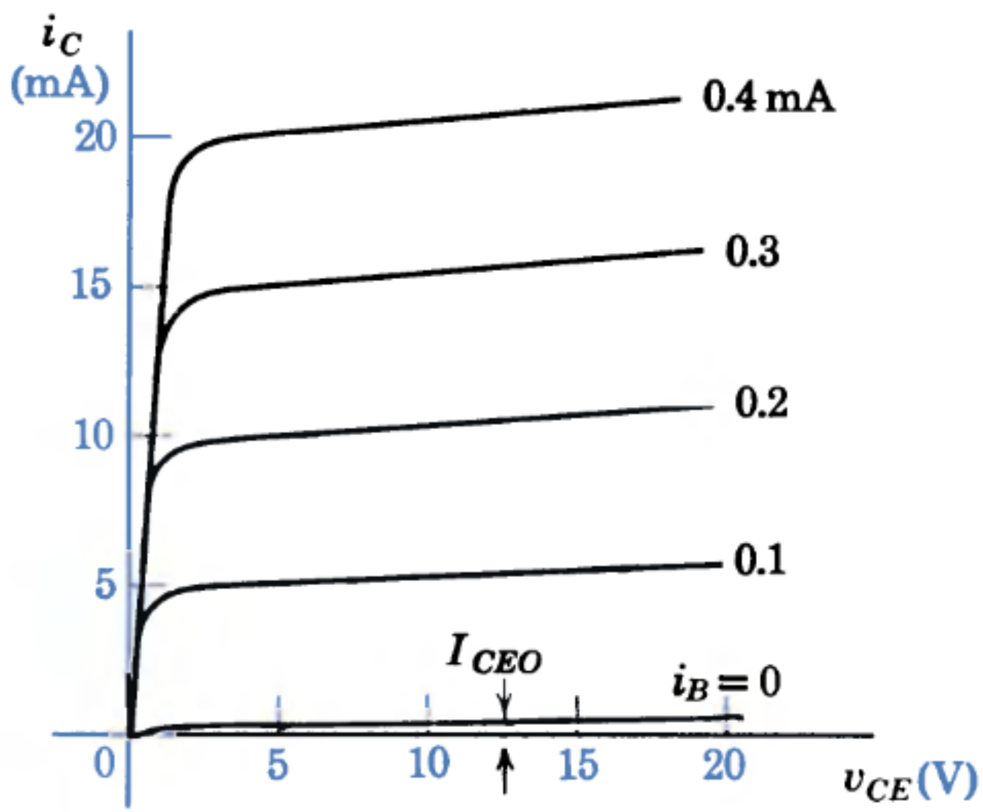
$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$I_C = \beta I_B + I_{CEO}$$

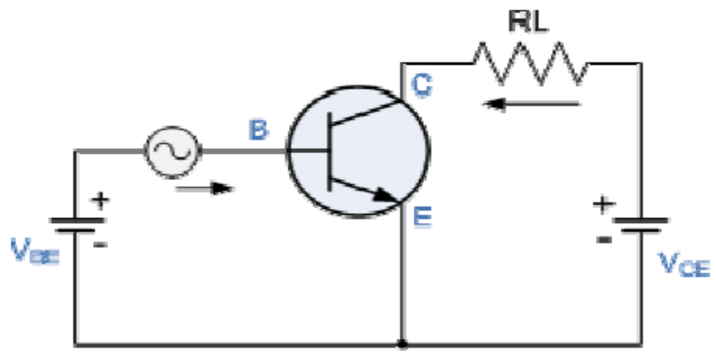


Output Characteristics

The output characteristics is a plot of I_C vs V_{CE}, for constant values of I_B.



Common emitter configuration

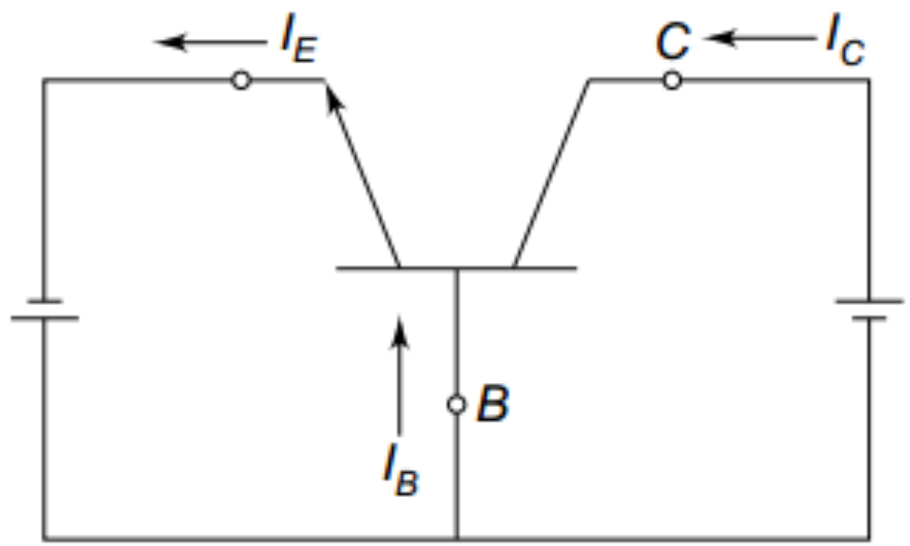


Revision of BJT currents:

$$I_E = I_B + I_C$$
$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$
$$(1-\alpha)I_C = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$



$$I_C = \beta I_B + (\beta + 1)I_{CBO}$$

β, base-to-collector current gain (assuming no leakage)

I_{CEO}, reverse saturation current in CE configuration

BJT (Ex 1)

For a transistor with $\alpha = 0.98$ and $I_{CBO} = 1nA$, calculate i_C and i_B for $i_E = 2mA$

BJT (Ex 1)

For a transistor with $\alpha = 0.98$ and $I_{CBO} = 1nA$, calculate i_C and i_B for $i_E = 2mA$

Solution:

$$i_C = \alpha i_E + I_{CB0} = (0.98 \times 2 \times 10^{-3} + 10^{-9})A = 1.96mA$$

BJT (Ex 1)

For a transistor with $\alpha = 0.98$ and $I_{CBO} = 1nA$, calculate i_C and i_B for $i_E = 2mA$

Solution:

$$i_C = \alpha i_E + I_{CB0} = (0.98 \times 2 \times 10^{-3} + 10^{-9})A = 1.96mA$$

$$i_B = i_E - i_C = (2 - 1.96)mA = 0.04mA = 40\mu A$$

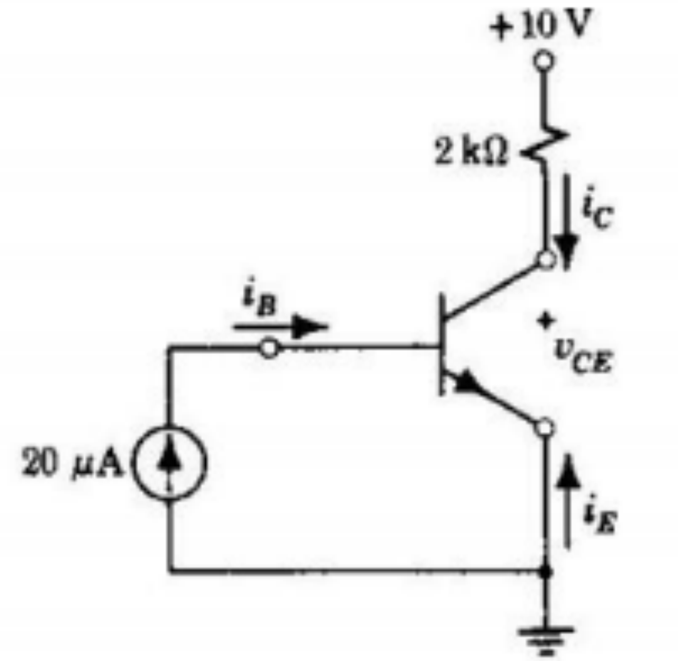
BJT (Ex 2)

A silicon npn transistor with $\alpha = 0.99$ and $I_{CBO} = 10^{-11}$ A is connected as shown in Figure. Predict i_c, i_E and v_{CE}. (Note: *It is convenient and customary in drawing electronic circuits to omit the battery, which is assumed to be connected between the +10 V terminal and ground*)

As expected for a silicon transistor. I_{CEO} is a very small part of i_C.

The emitter current is

$$i_E = -(i_B + i_C) = -(0.02 + 1.98)10^{-3} = -2 \text{ mA}$$



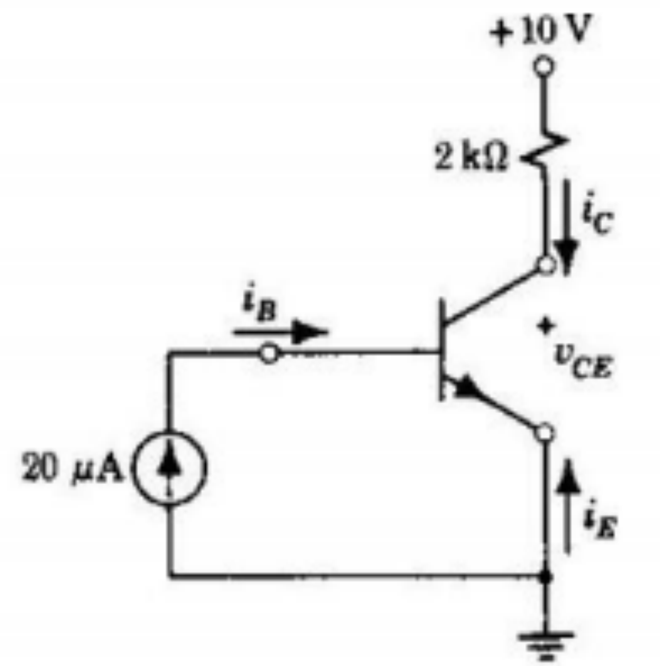
Transistor operation.

BJT (Ex 2)

A silicon npn transistor with α = 0.99 and I_{CBO} = 10^{-11} A is connected as shown in Figure. Predict i_c, i_E and v_{CE}. (Note: *It is convenient and customary in drawing electronic circuits to omit the battery, which is assumed to be connected between the +10 V terminal and ground*)

$$\beta = \frac{\alpha}{1-\alpha} = 99 \qquad I_{CEO} = (1+\beta)I_{CBO} = 1\ \text{nA}$$

$$i_C = \beta i_B + I_{CEO} = 1.98\ \text{mA}$$



Transistor operation.

As expected for a silicon transistor. I_{CEO} is a very small part of i_C.

The emitter current is

$$i_E = -(i_B + i_C) = -(0.02 + 1.98)10^{-3} = -2\ \text{mA}$$

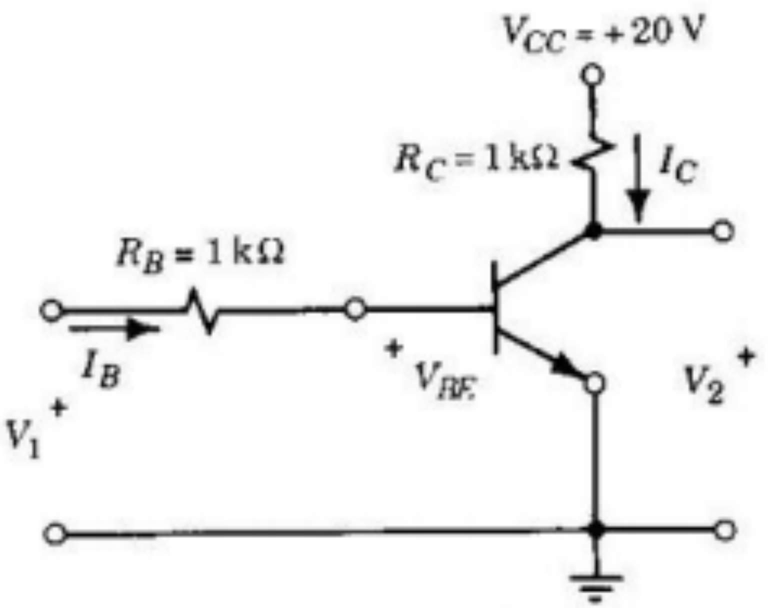
The collector–emitter voltage is

$$v_{CE} = 10 - i_C R_C \cong 10 - 2(\text{mA}) \times 2(\text{k}\Omega) = 6\ \text{V}$$

Since $v_{CB} = v_{CE} - v_{BE} \cong 6 - 0.7 = +5.3$ V, the *np* collector–base junction is reverse biased as required.

BJT (Ex 3)

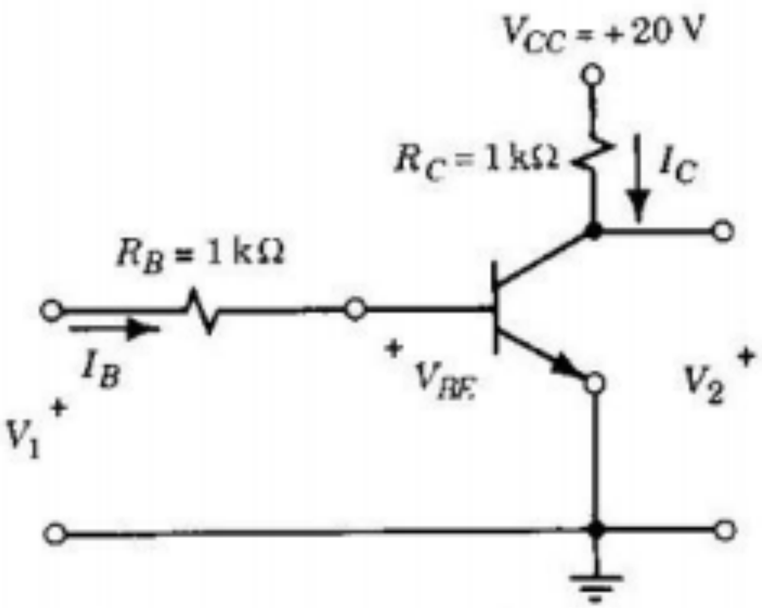
For the circuit given below, let α = 0.98, v_{BE} = 0.7 V and V_1 = 1.0 V. Find the output voltage V_2.



Transistor performance.

BJT (Ex 3)

For the circuit of given figure, let $\alpha = 0.98$, $v_{BE} = 0.7$ V and $V_1 = 1.0$ V. Find the output voltage V_2.



Transistor performance.

The current-transfer ratio β is found as

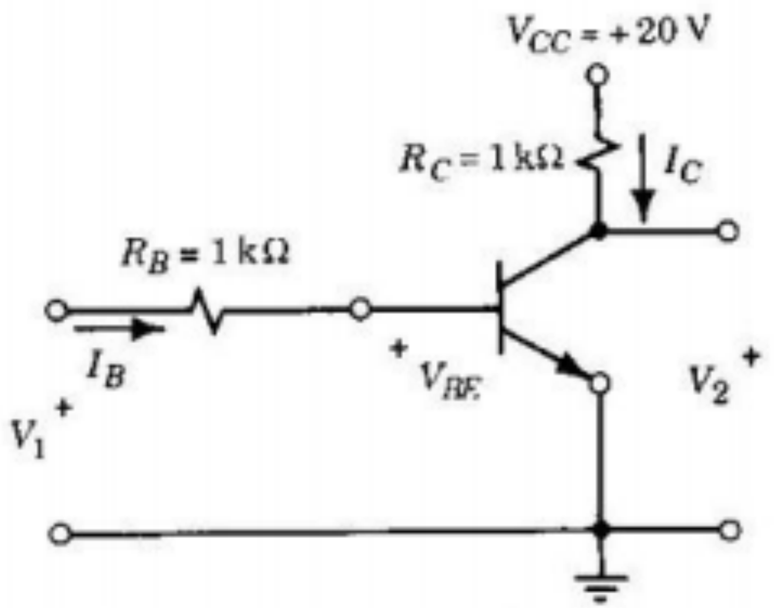
$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

Then $V_{BE} = 0.7$ V sets the device to be forward biased with the base current I_B of

$$I_B = \frac{V_1 - V_{BE}}{R_B} = \frac{1-0.7}{1000} = 0.3 \text{ mA}$$

BJT (Ex 3)

For the circuit given below, let $\alpha = 0.98$, $v_{BE} = 0.7$ V and $V_1 = 1.0$ V. Find the output voltage V_2.



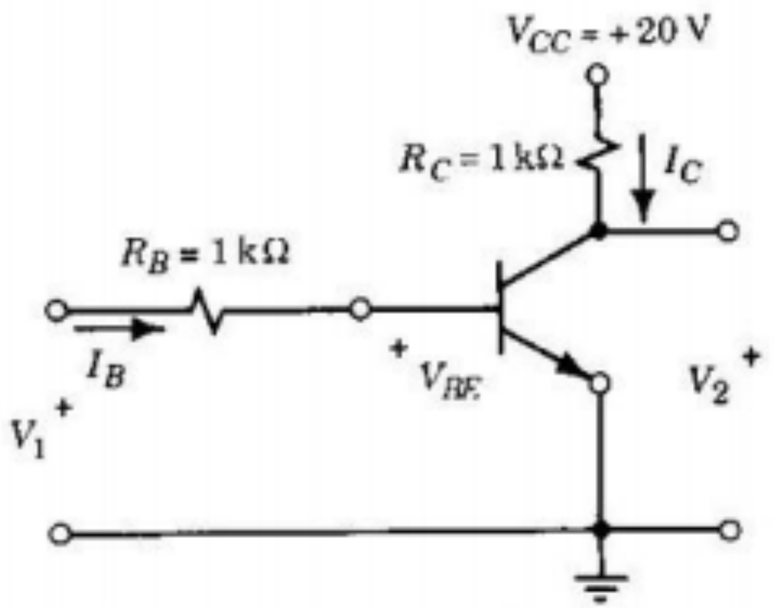
Transistor performance.

Neglecting I_{CEO}, the collector current I_C is

$$I_C = \beta I_B = 49 \times 0.3 \times 10^{-3} = 14.7 \text{ mA}$$

BJT (Ex 3)

For the circuit of given figure, let $\alpha = 0.98$, $v_{BE} = 0.7$ V and $V_1 = 1.0$ V. Find the output voltage V_2.



Transistor performance.

Neglecting I_{CEO}, the collector current I_C is

$$I_C = \beta I_B = 49 \times 0.3 \times 10^{-3} = 14.7 \text{ mA}$$

Then the output voltage is

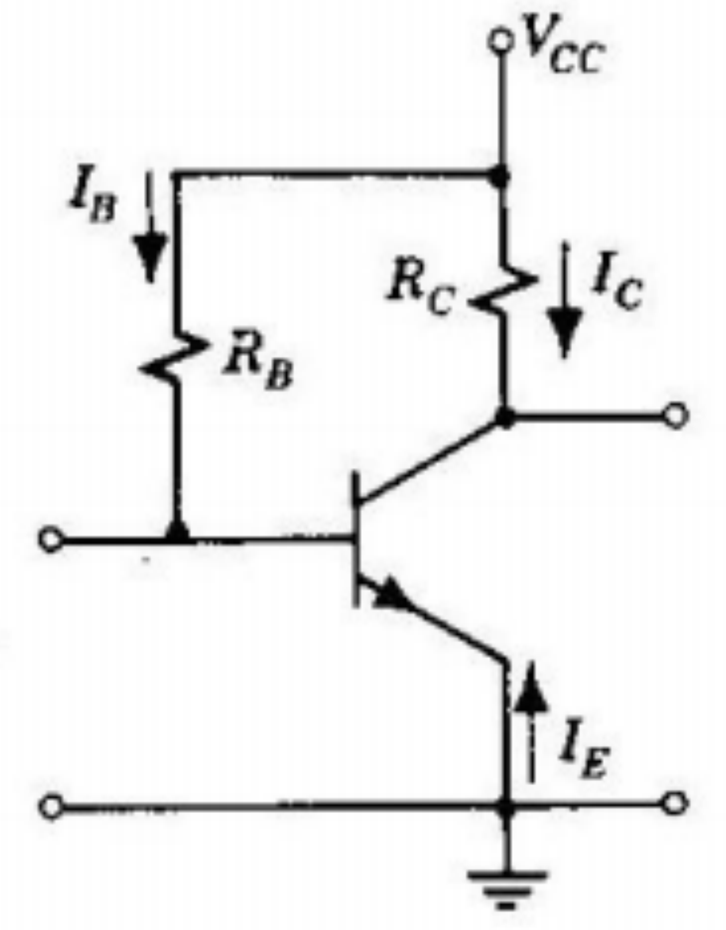
$$V_2 = V_{CC} - R_C I_C = 20 - 1000 \times 14.7 \times 10^{-3} = 5.3 \text{ V}$$

BJT Biasing Circuits

- **Objective:** Establish a proper operating point and maintain it, despite of variation of temperature and variation among individual BJTs

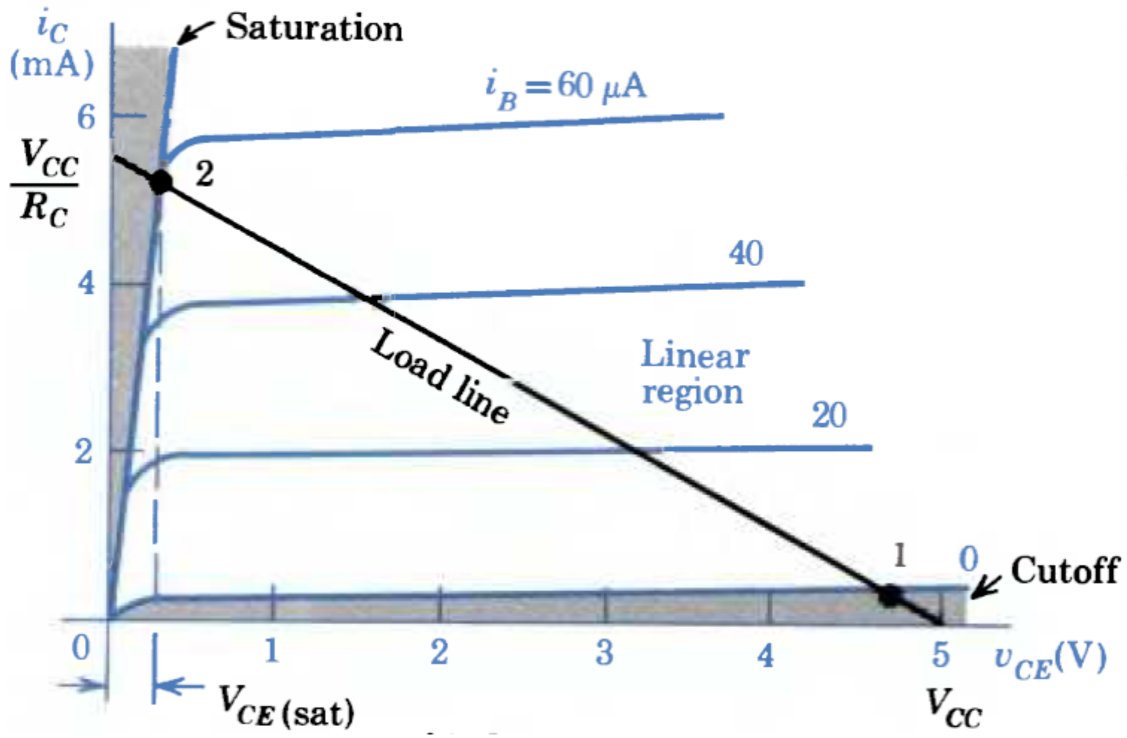
Fixed Current Bias

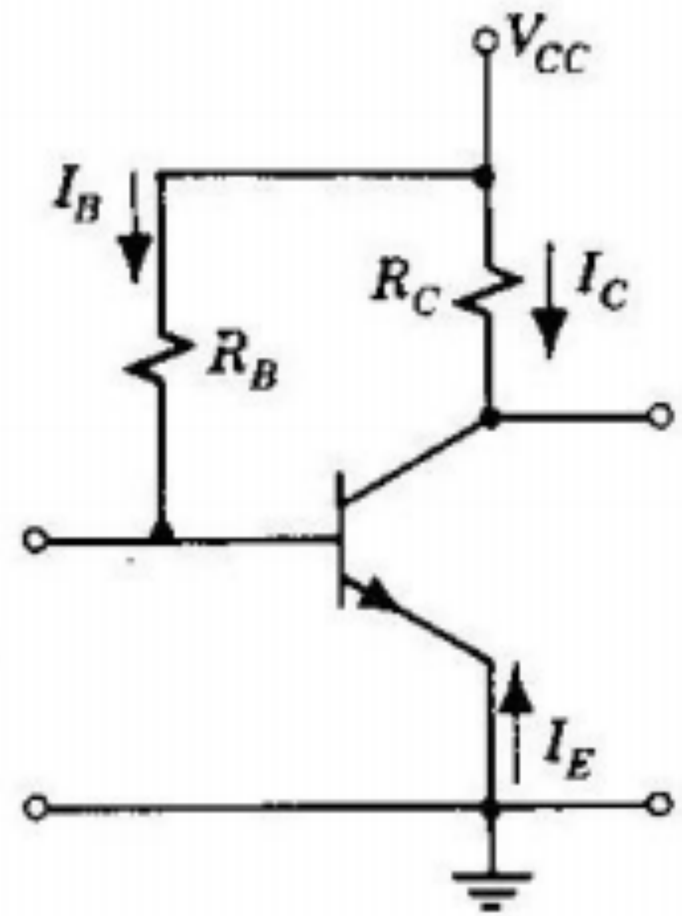
- DC base current is provided from V_{cc}.
- Since Forward biased $V_{BE} << V_{cc}$ mostly,



Fixed Current Bias

- DC base current is provided from V_{cc}.
- Since Forward biased $V_{BE} << V_{cc}$ mostly,
  - I_B is fixed
  - I_C is fixed
  - V_{CE} is fixed





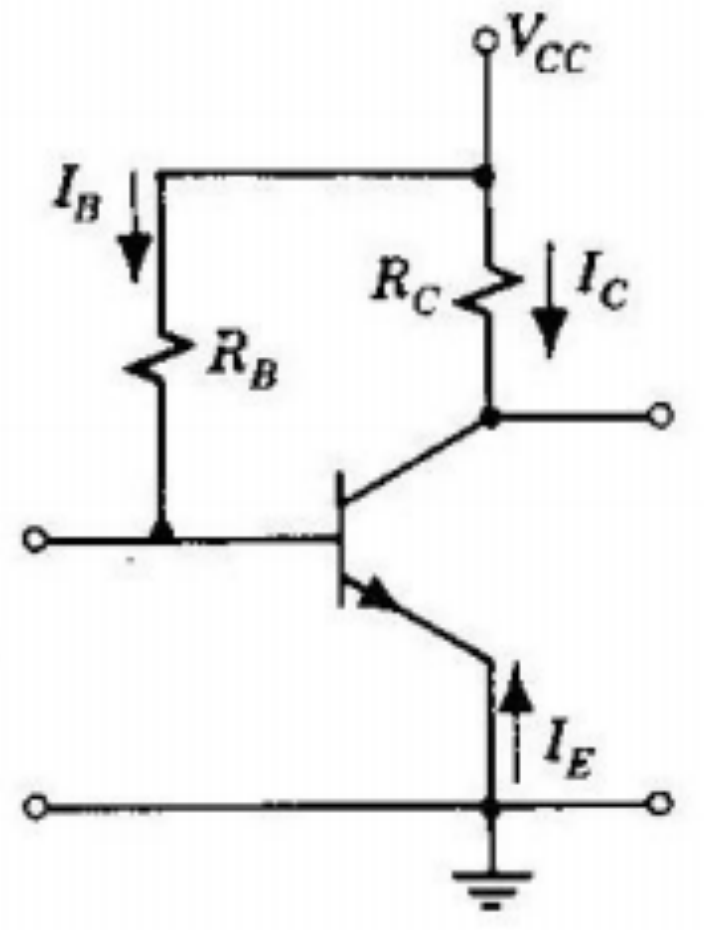
Fixed Current Bias

- DC base current is provided from V_{cc}.
- Since Forward biased $V_{BE} << V_{cc}$ mostly,

$$I_B \approx \frac{V_{CC}}{R_B}$$
$$V_{CE} = V_{CC} - R_C I_C$$

$$I_C = \beta I_B + I_{CEO}$$
$$I_C = \frac{\beta V_{CC}}{R_B} + (\beta + 1) I_{CBO}$$

$$V_{CE} = \left(1 - \beta \frac{R_C}{R_B}\right) V_{CC} - (\beta + 1) R_C I_{CBO}$$



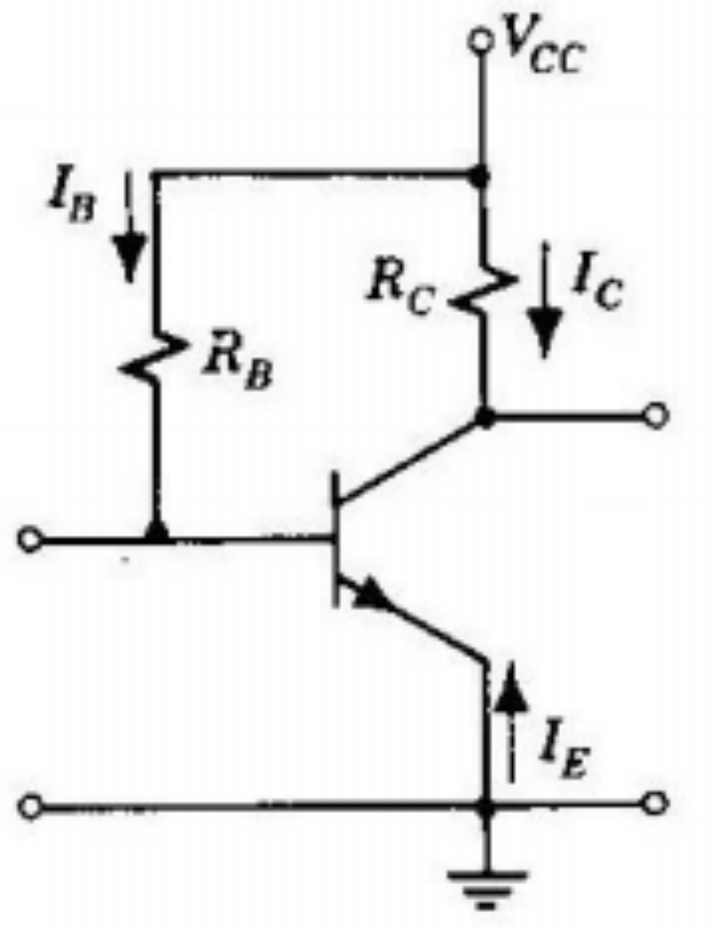
Fixed Current Bias

- DC base current is provided from V_{cc}.
- Since Forward biased $V_{BE} << V_{cc}$ mostly,

$$I_B \approx \frac{V_{CC}}{R_B}$$
$$V_{CE} = V_{CC} - R_C I_C$$

$$I_C = \beta I_B + I_{CEO}$$
$$I_C = \frac{\beta V_{CC}}{R_B} + (\beta + 1) I_{CBO}$$

$$V_{CE} = \left(1 - \beta \frac{R_C}{R_B}\right) V_{CC} - (\beta + 1) R_C I_{CBO}$$



Both output variables V_{CE} and I_C are heavily dependent on β.

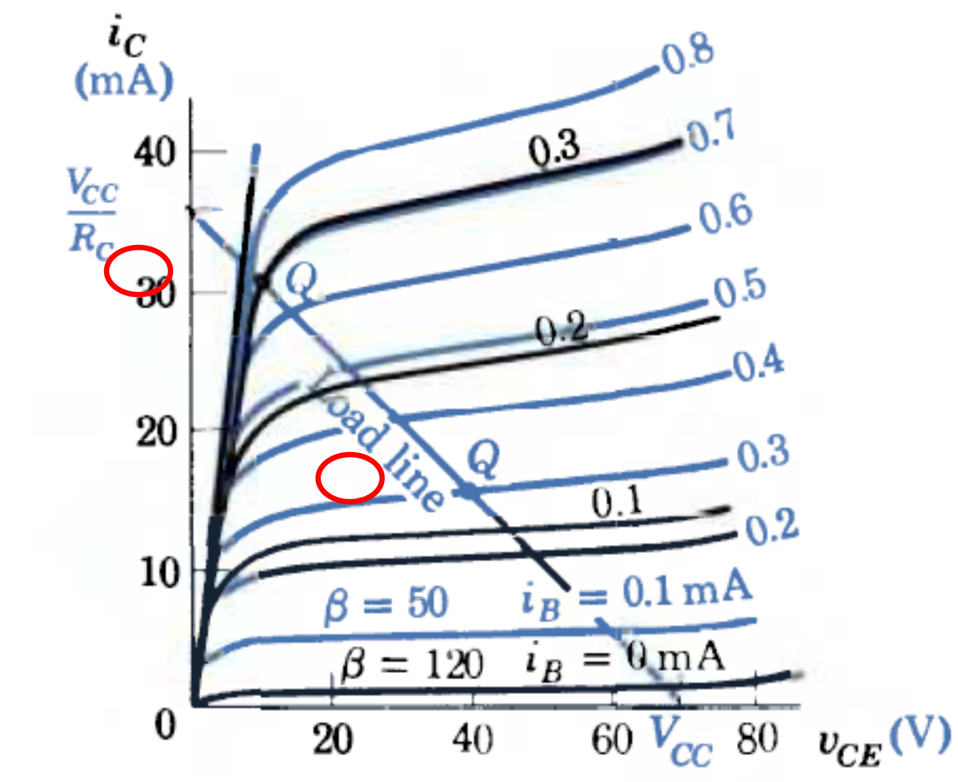
Fixed Current Bias: Problems

- Due to process variations, β may not be constant for a 'batch' of transistors.
- This means even when we know I_B from V_{CC}, I_C can vary widely.

Fixed Current Bias: Problems - 1

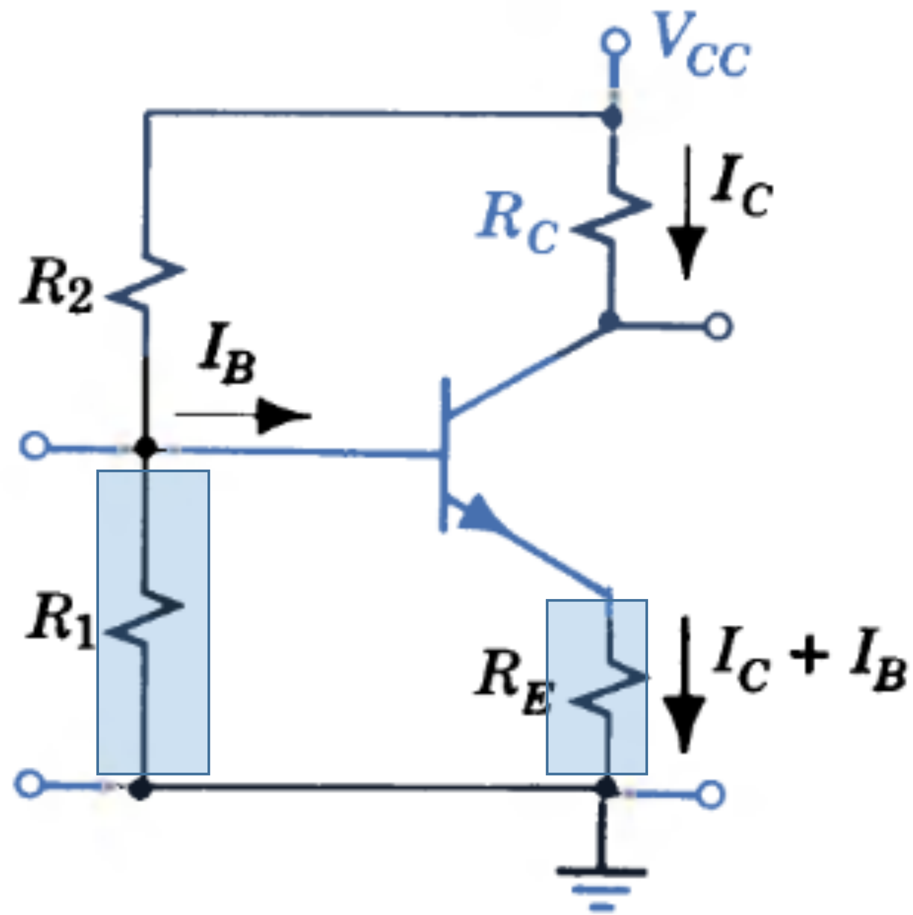
- Due to process variations, β may not be constant for a 'batch' of transistors.
- This means even when we know I_B from V_{CC}, I_C can vary widely.
- Say I_B = 0.3 mA, but β varies.
- The Q-point/Operating point

of BJT can now be in linear (β=50) OR saturation region (β=120).



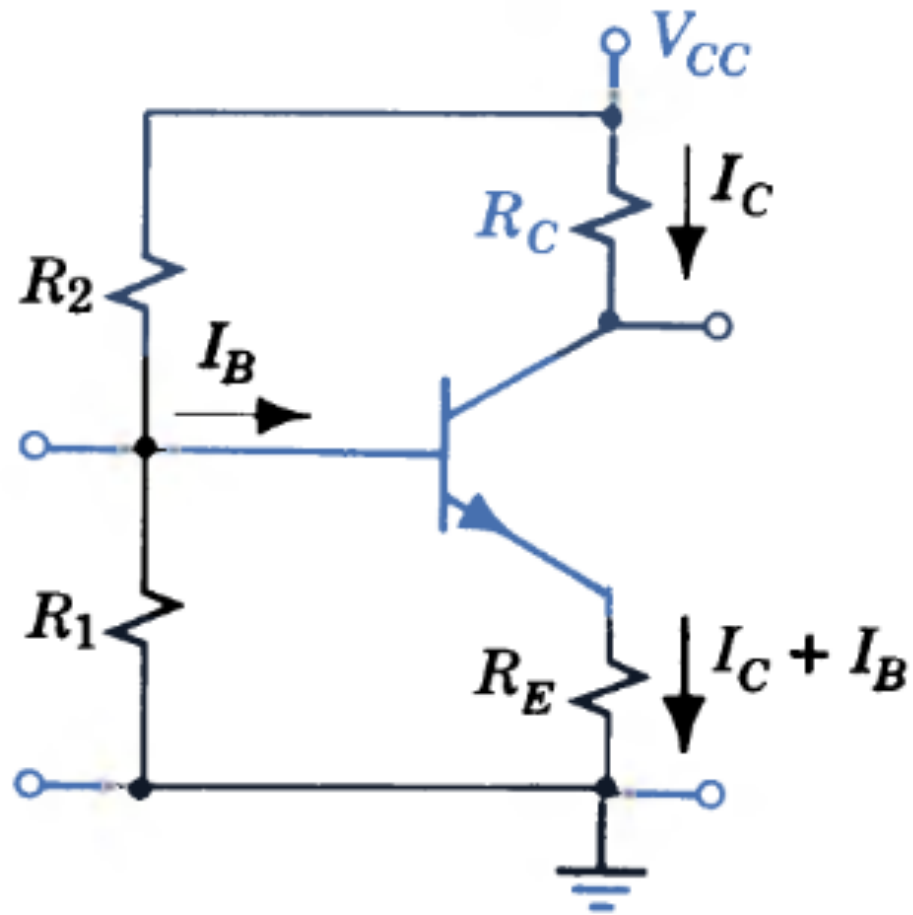
Self Bias

- Variable to be stabilized is I_C. Not I_B.
- Need a circuit whose dependence on V_{CC} varies less with change in β.

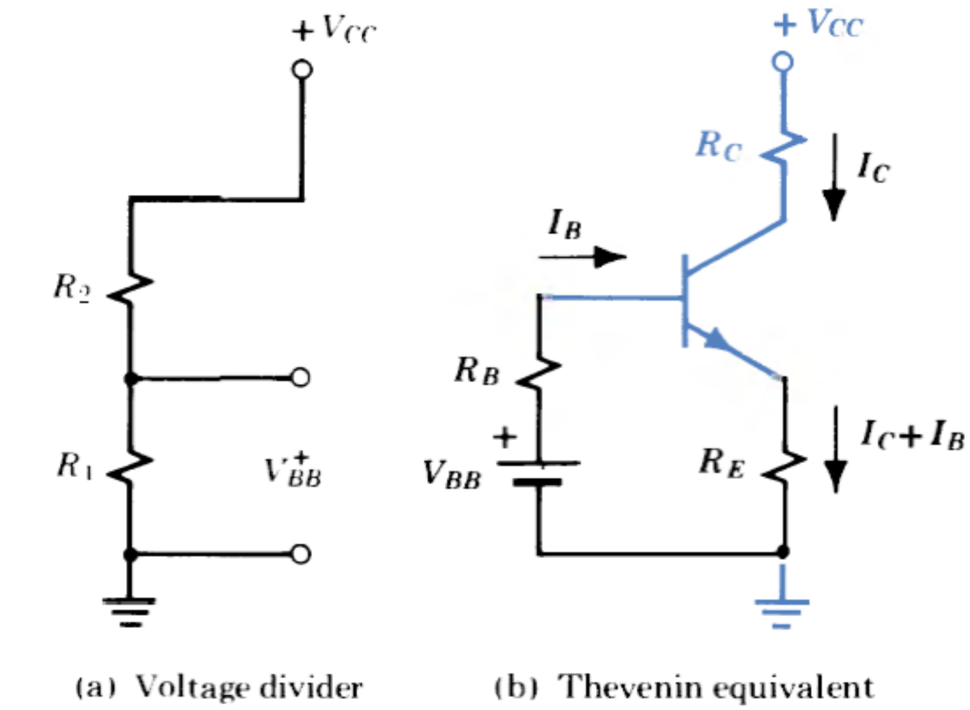


Self Bias

- R_1 and R_2 form a voltage divider. Bringing base to proper potential to Forward bias emitter junction.
- If I_C increases due to β, $I_E=I_B+I_C$ also increases.
- Raising V_E→ reducing V_{BE}→ reducing I_B→reducing I_C.
- Increase in I_C is fed back to modify the bias to oppose further increase.



Self Bias: Quantitative Analysis



- R_1 and R_2 form a voltage divider. Bringing base to proper potential to Forward bias emitter junction.
- Replacing it with its Thevenin equivalent yields

$$V_{BB} = \frac{R_1}{R_1+R_2} V_{CC}$$

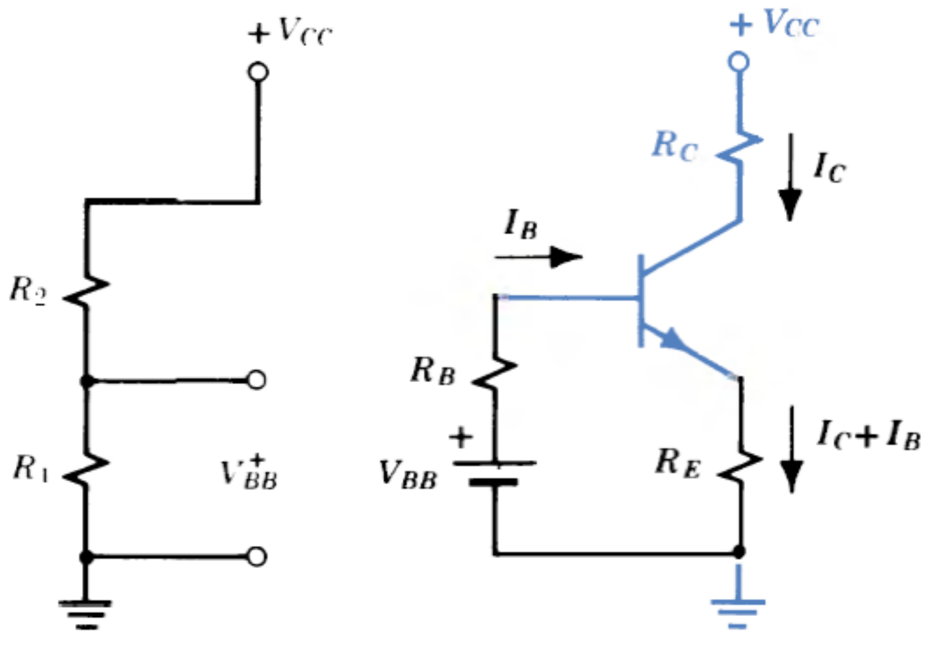
$$R_B = \frac{R_1 R_2}{R_1+R_2}$$

- Further

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

$$I_B = \frac{I_C}{\beta} - \frac{\beta+1}{\beta} I_{CBO}$$

Self Bias: Quantitative Analysis



(a) Voltage divider (b) Thevenin equivalent

$$V_{BB} = \frac{R_1}{R_1+R_2} V_{CC}$$
$$R_B = \frac{R_1 R_2}{R_1+R_2}$$

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$
$$I_B = \frac{I_C}{\beta} - \frac{\beta+1}{\beta} I_{CBO}$$

- Applying KVL in the base loop

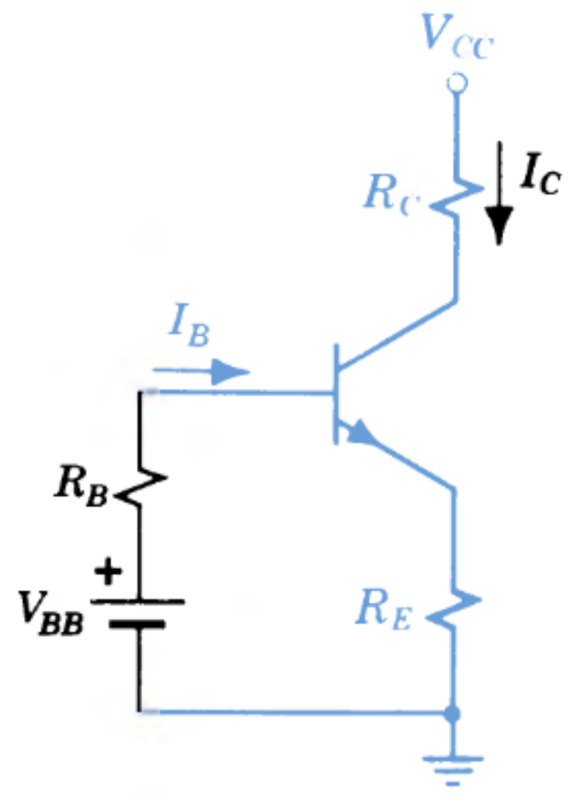
$$V_{BB} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$$

- Substituting for I_B gives:

$$I_C = \frac{V_{BB} - V_{BE} + \frac{\beta+1}{\beta} I_{CBO} (R_B + R_E)}{R_E + \frac{R_B + R_E}{\beta}}$$

BJT Self Bias Example

The β of individual specimens of a silicon transistor varies from 30 to 180. If V_{BE} may vary from 0.5 to 0.9 V and I_{CBO} may vary from 1 to 10 nA, predict the extreme variation in I_C in a self-biasing circuit where R_1 = 10 KΩ, R_2 = 90 KΩ, R_C = 15 KΩ, R_E = 2 KΩ and V_{CC} = 28 V.



Stabilizing effect of a self-biasing circuit.

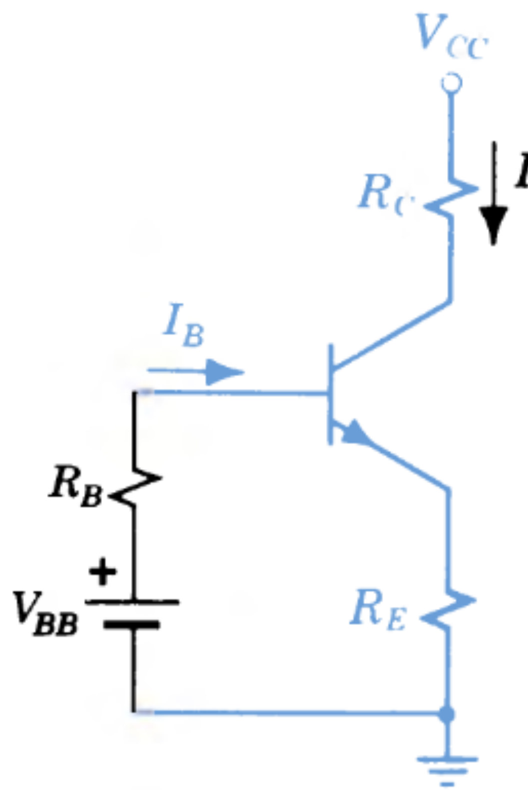
BJT Self Bias Example

The β of individual specimens of a silicon transistor varies from 30 to 180. If V_{BE} may vary from 0.5 to 0.9 V and I_{CBO} may vary from 1 to 10 nA, predict the extreme variation in I_C in a self-biasing circuit where R_1 = 10 KΩ, R_2 = 90 KΩ, R_C = 15 KΩ, R_E = 2 KΩ and

the Thévenin equivalents are

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 90}{10 + 90} = 9\ \text{k}\Omega$$

$$V_{BB} = \frac{V_{CC} R_1}{R_1 + R_2} = \frac{28 \times 10}{10 + 90} = 2.8\ \text{V}$$



Stabilizing effect of a self-biasing circuit.

BJT Self Bias Example

The ß of individual specimens of a silicon transistor varies from 30 to 180. If V_{BE} may vary from 0.5 to 0.9 V and I_{CBO} may vary from 1 to 10 nA, predict the extreme variation in I_C in a self-biasing circuit where R_1 = 10 KΩ, R_2 = 90 KΩ, R_C = 15 KΩ, R_E = 2 KΩ and

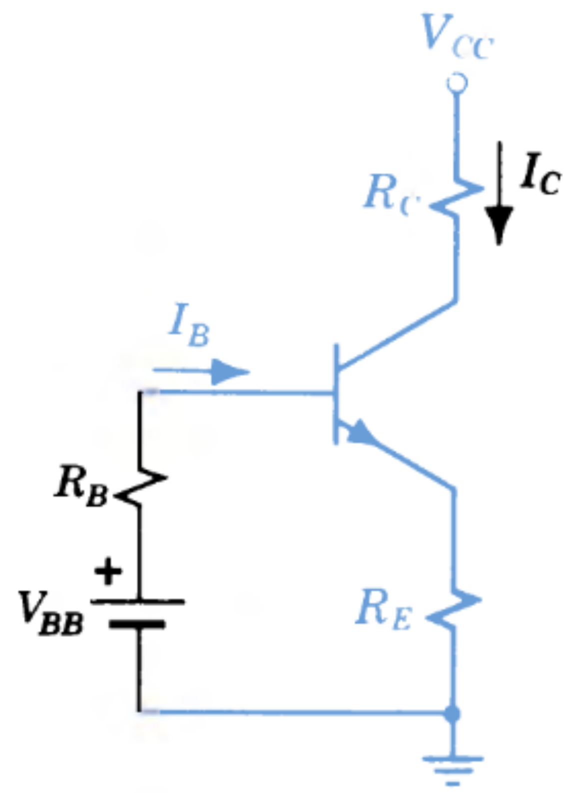
the Thévenin equivalents are

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 90}{10 + 90} = 9\ \text{k}\Omega$$

$$V_{BB} = \frac{V_{CC} R_1}{R_1 + R_2} = \frac{28 \times 10}{10 + 90} = 2.8\ \text{V}$$

the collector current

$$I_C = \frac{V_{BB} - V_{BE} + \left(\frac{\beta + 1}{\beta}\right) I_{CBO}(R_B + R_E)}{R_E + \frac{R_B + R_E}{\beta}}$$



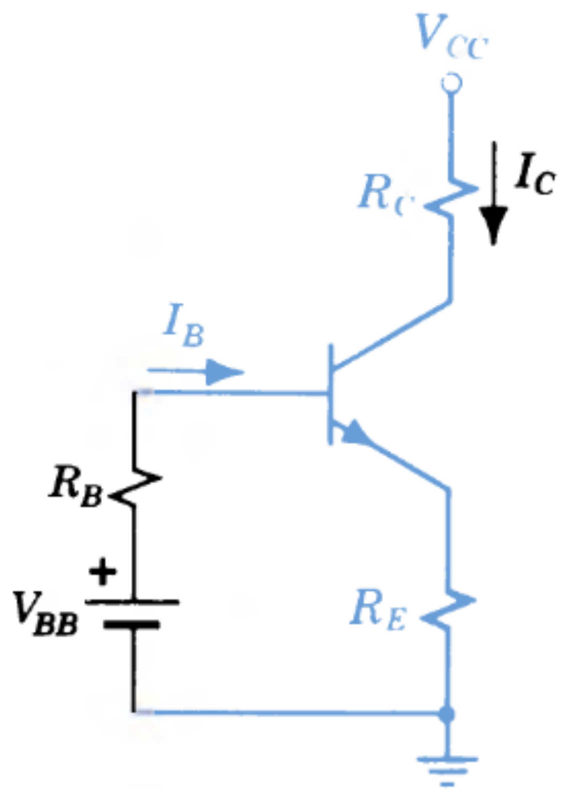
Stabilizing effect of a self-biasing circuit.

BJT Self Bias Example

The ß of individual specimens of a silicon transistor varies from 30 to 180. If V_{BE} may vary from 0.5 to 0.9 V and I_{CBO} may vary from 1 to 10 nA, predict the extreme variation in I_C in a self-biasing circuit where R_1 = 10 KΩ, R_2 = 90 KΩ, R_C = 15 KΩ, R_E = 2 KΩ and V_C For $\beta = 30$, $V_{BE} = 0.9$ V, and $I_{CBO} = 1$ nA, a "worst case"

$$I_C = \frac{2.8 - 0.9 + \left(\frac{31}{30}\right) 10^{-9}\,(11{,}000)}{2000 + 11{,}000/30}$$

$$= \frac{1.9 + 0.00001}{2367} = 0.8 \text{ mA}$$



Stabilizing effect of a self-biasing circuit.

BJT Self Bias Example

The ß of individual specimens of a silicon transistor varies from 30 to 180. If V_{BE} may vary from 0.5 to 0.9 V and I_{CBO} may vary from 1 to 10 nA, predict the extreme variation in I_C in a self-biasing circuit where R_1 = 10 KΩ, R_2 = 90 KΩ, R_C = 15 KΩ, R_E = 2 KΩ and V

For $\beta = 30$, $V_{BE} = 0.9$ V, and $I_{CBO} = 1$ nA, a "worst case"

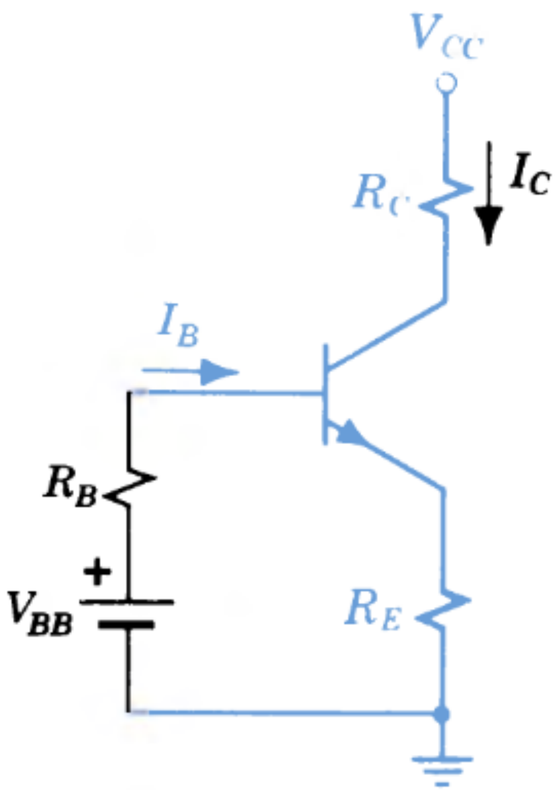
$$I_C = \frac{2.8 - 0.9 + \left(\frac{31}{30}\right) 10^{-9}\,(11{,}000)}{2000 + 11{,}000/30}$$

$$= \frac{1.9 + 0.00001}{2367} = 0.8 \text{ mA}$$

For $\beta = 180$, $V_{BE} = 0.5$ V, and $I_{CBO} = 10$ nA,

$$I_C = \frac{2.8 - 0.5 + \left(\frac{181}{180}\right) 10^{-8}\,(11{,}000)}{2000 + 11{,}000/180}$$

$$= \frac{2.3 + 0.0001}{2061} = 1.1 \text{ mA}$$

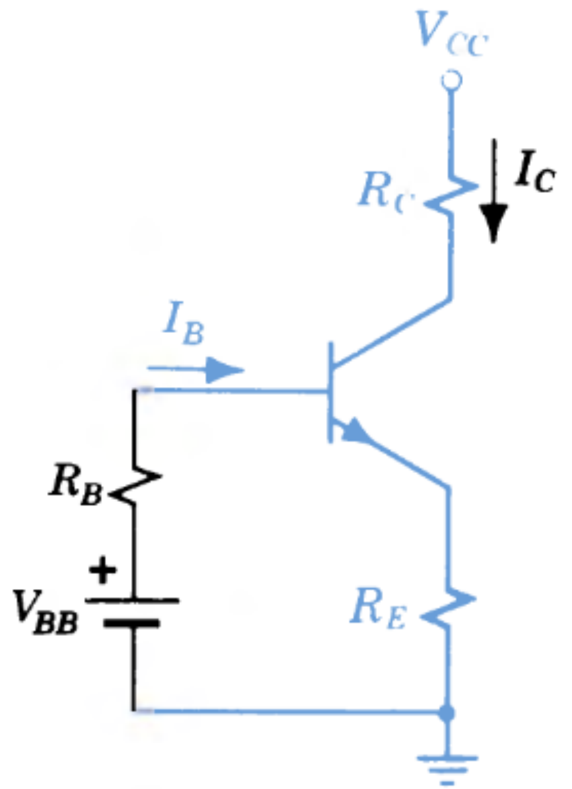


Stabilizing effect of a self-biasing circuit.

BJT Self Bias Example

The ß of individual specimens of a silicon transistor varies from 30 to 180. If V_{BE} may vary from 0.5 to 0.9 V and I_{CBO} may vary from 1 to 10 nA, predict the extreme variation in I_C in a self-biasing circuit where R_1 = 10 KΩ, R_2 = 90 KΩ, R_C = 15 KΩ, R_E = 2 KΩ and V_{CC} = 28 V.

For these extreme variations, I_C shifts only 0.3 mA. Note that for a typical silicon transistor, $(1 + \beta) I_{CBO} = I_{CEO}$ is negligible in bias calculations.



Stabilizing effect of a self-biasing circuit.

Stability Analysis of Self Biasing Circuit:

V_{CC} is used as the single bias source. A dc bias voltage at the base of the transistor can be developed by a resistive voltage divider consisting of R_1 and R_2.

$$I_C = \frac{V_{BB} - V_{BE} + \frac{\beta+1}{\beta} I_{CBO}(R_B + R_E)}{R_E + \frac{R_B + R_E}{\beta}}$$

If $\beta \gg 1, V_{BB} - V_{BE} \gg I_{CBO}(R_B + R_E)$

$$I_C = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B + R_E}{\beta}}$$

In addition if $R_B \ll \beta R_E$

$$I_C = \frac{V_{BB} - V_{BE}}{R_E} = \frac{R_1 V_{CC} - (R_1 + R_2) V_{BE}}{(R_1 + R_2) R_E}$$

Minimal dependence on the EXACT value of β. Only β>>1 will suffice.