

COL216

Computer Architecture

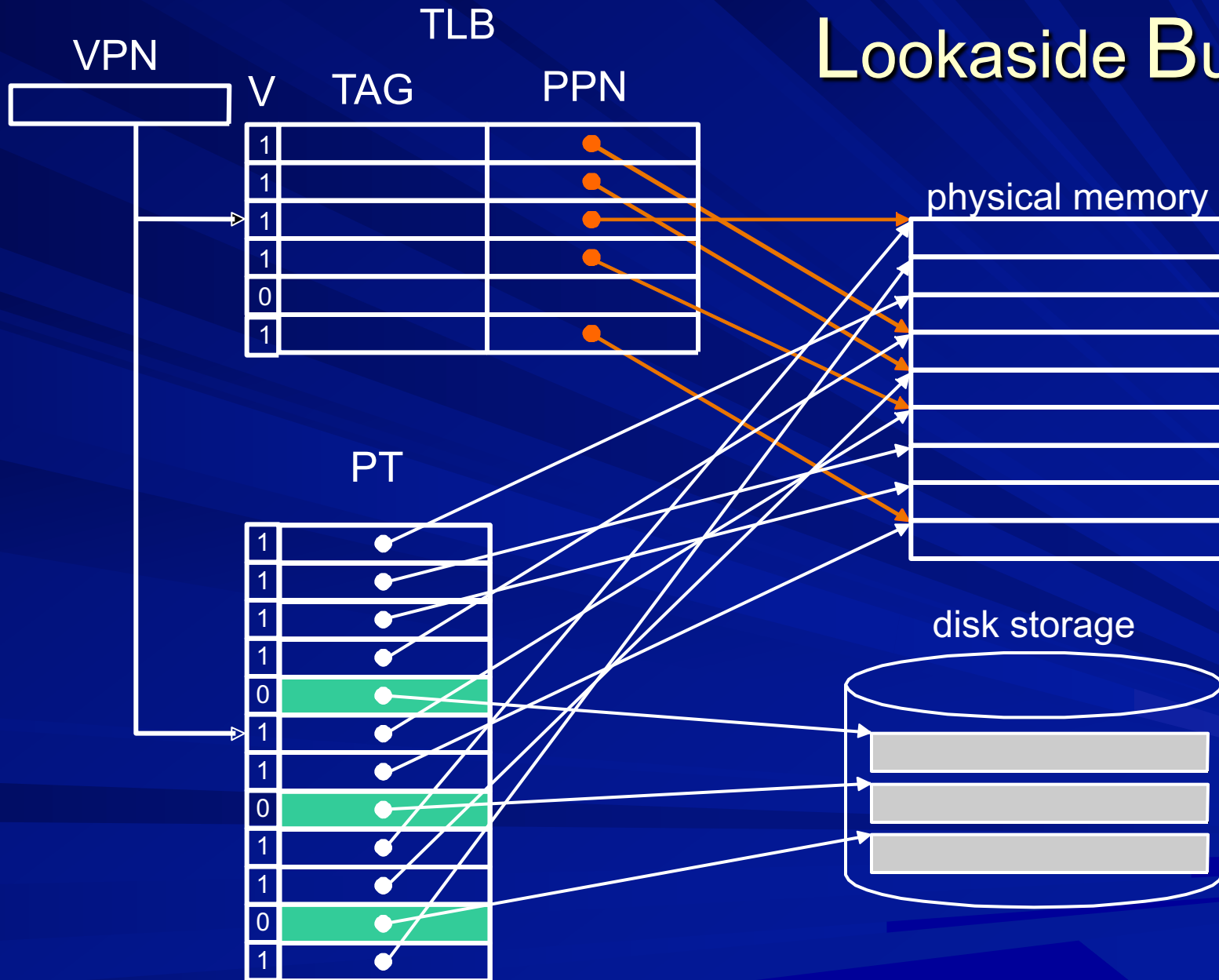
Virtual Memory
TLB illustration
14th March 2022

Virtual memory hit time

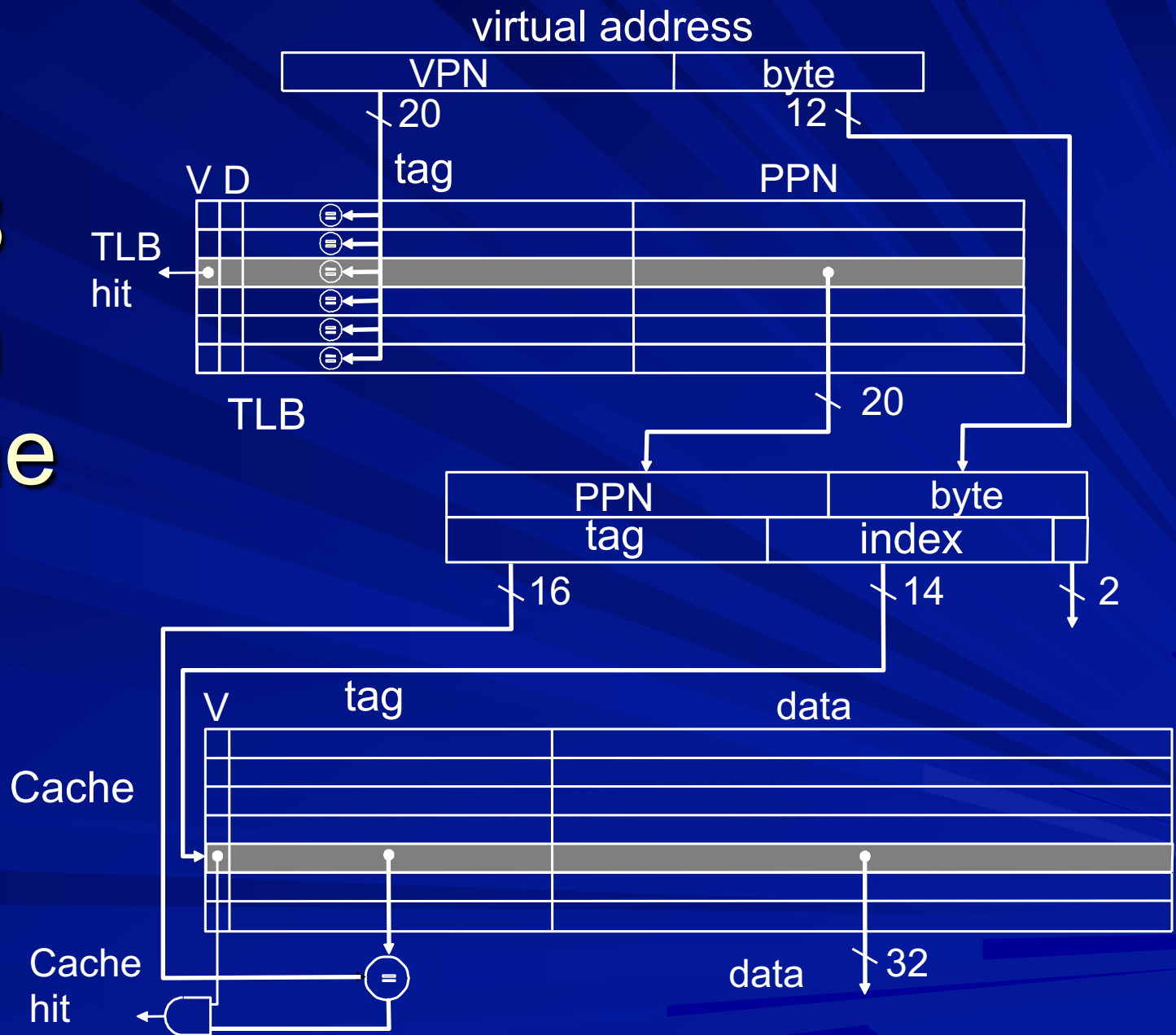
- simple page table :
2 x physical memory access time
- 2 level page table :
3 x physical memory access time
- paged page table :
3 x physical memory access time

Can this be better??

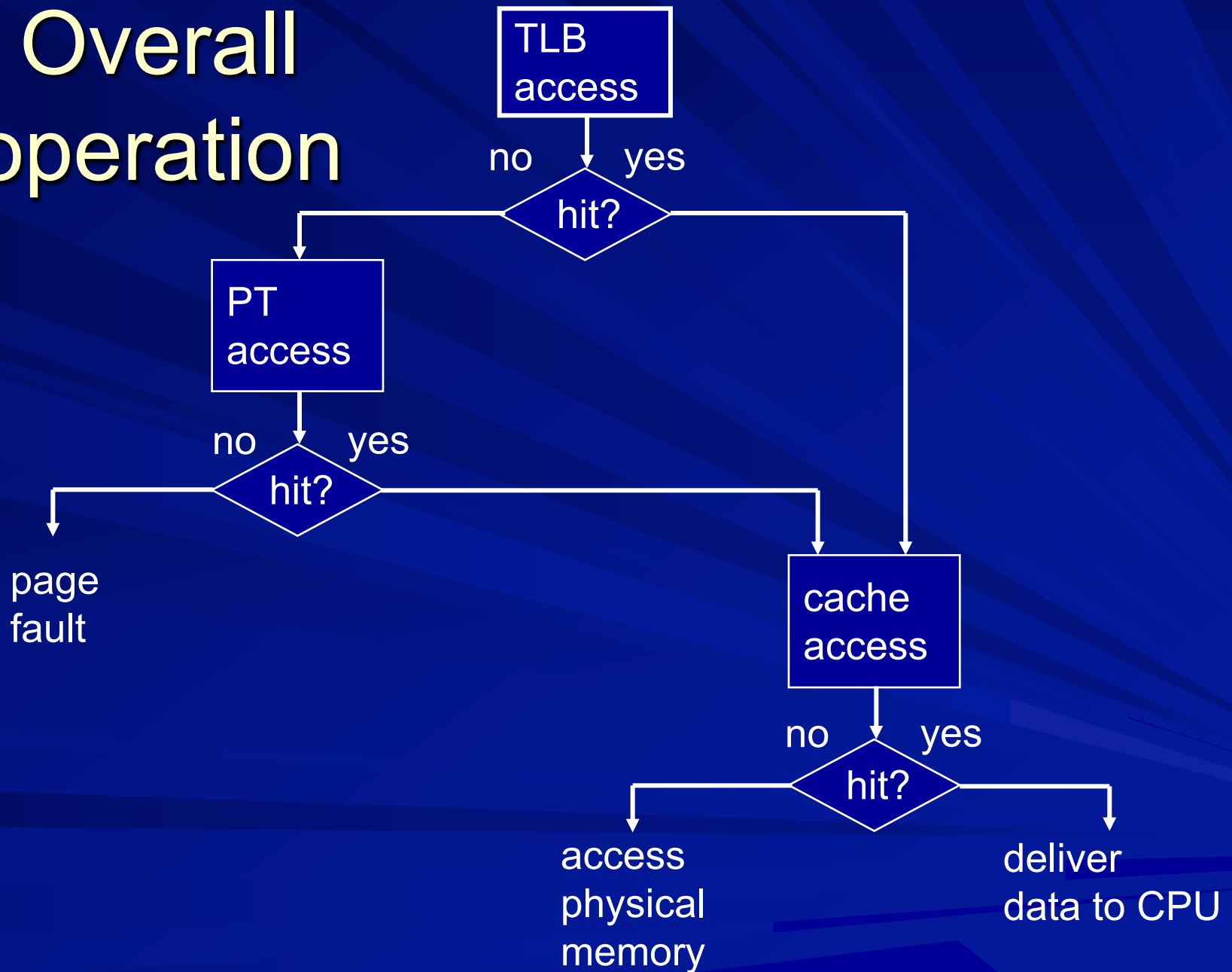
Translation Lookaside Buffer



TLB with Cache



Overall operation



Virtually addressed cache

- Tags in the cache are from virtual addresses
- Cache access is made first
- TLB accessed only after cache miss
- Problem of aliasing - two copies of a shared object in physical memory
- Physically tagged and virtually indexed cache may be used

Indexing before address translation

- Virtually indexed, physically tagged cache
 - simple and effective approach
 - indexing overlaps with address translation, tag matching after address translation
 - valid only if index field does not change during address translation (possible for caches that are not too large)

Virtual Page No.		Offset in page	
Tag		Index	

Example: TLB & PT operation (Ex 5.10)

PT	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

TLB	V	Tag(VPN)	PPN
	1	11	12
	1	7	4
	1	3	6
	0	4	9

fully associative

Page size = 4 KB

Example: TLB & PT operation (Ex 5.10)

PT	V	PPN
0	1	5
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Virtual address stream:

4095, 31272, 15789, 15000, 7193, 4096, 8912

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VPN:

0, 7, 3, 3, 1, 1, 2

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TLB hit/miss:

M

Page fault:

No

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	1	1	13
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