Synthesis of Digital Systems

COL 719

Part 7: Field Programmable Gate Arrays

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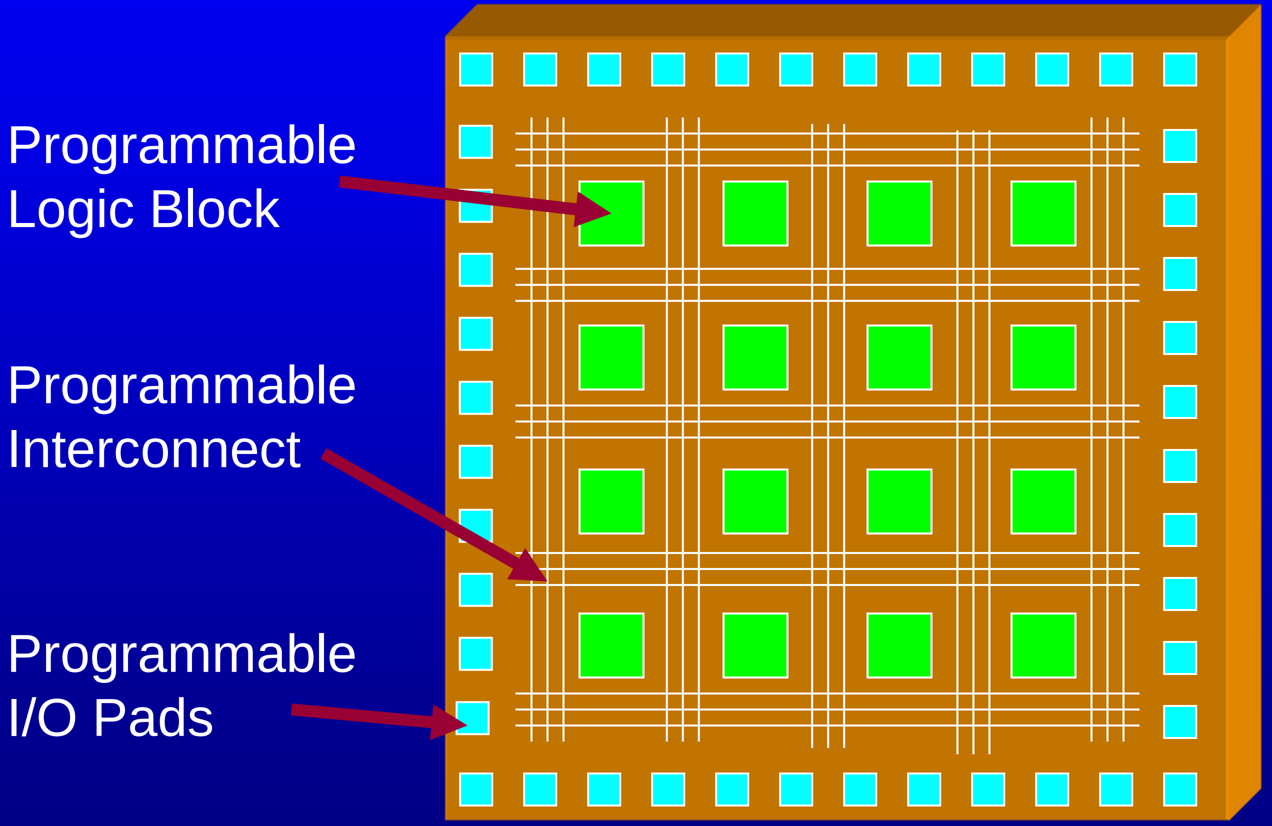
Field Programmable Gate Array

- “Field Programmable”
  - Customised by designer
  - vs. “Mask Programmable”: customised by foundry
- Customisation process simple/cheap
- FPGA chips produced in bulk
  - independent of functionality

FPGA architecture

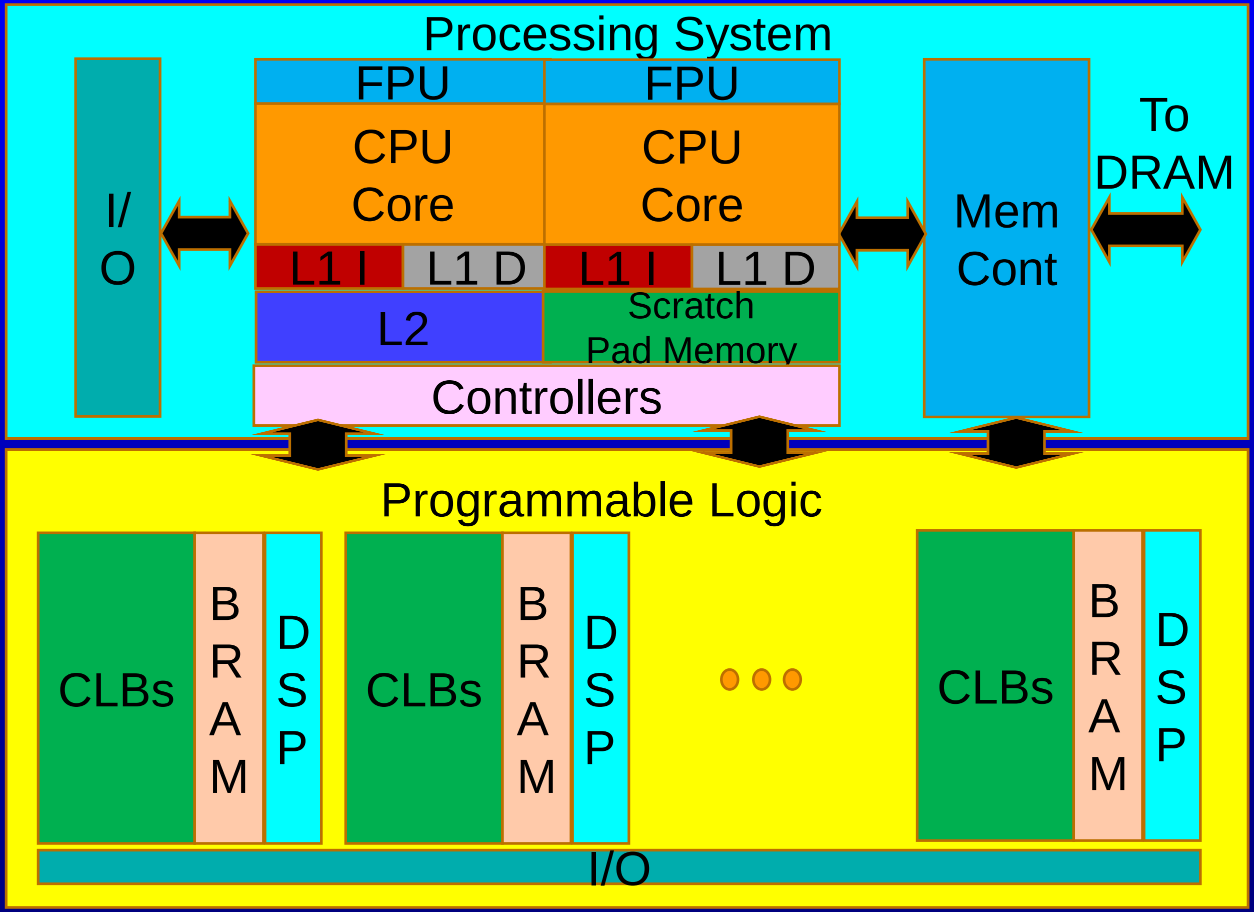


No mask layer is customized

Design turnaround time: few hours

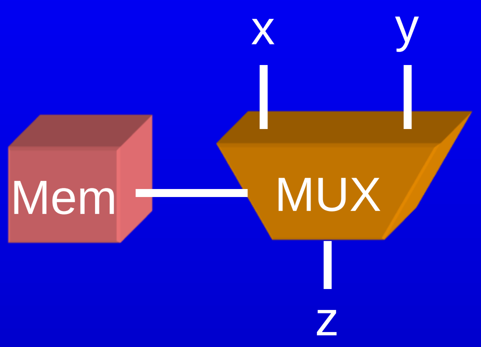
Modern FPGA Architecture

Xilinx
Zynq 7000
Series

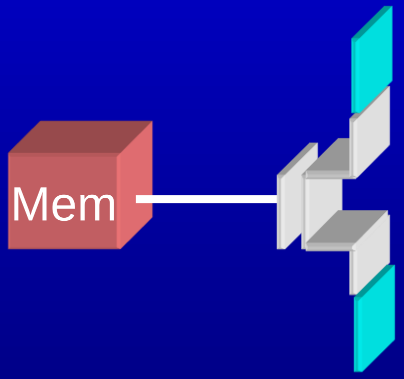


FPGA Programming: SRAM

- Normal SRAM cell
- Programming: writing 0 or 1 into SRAM cell
  - this, in turn, causes selections, connections, etc.



Programming the logic

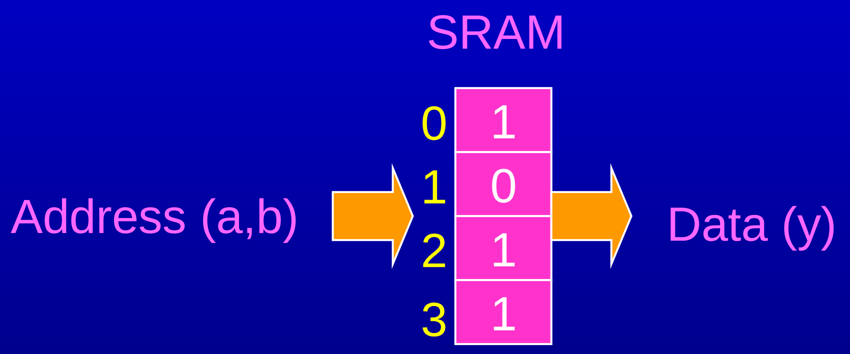


Programming the interconnection

SRAM-based FPGA

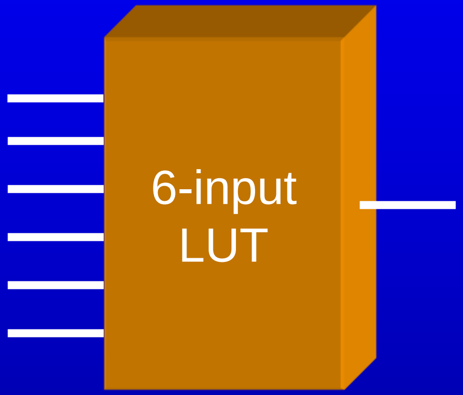
- Each logic block consists of an SRAM
- An SRAM with 2^n bits can implement ANY function of n inputs
  - Use inputs as address
  - Store value in locations

a b	y
0 0	1
0 1	0
1 0	1
1 1	1



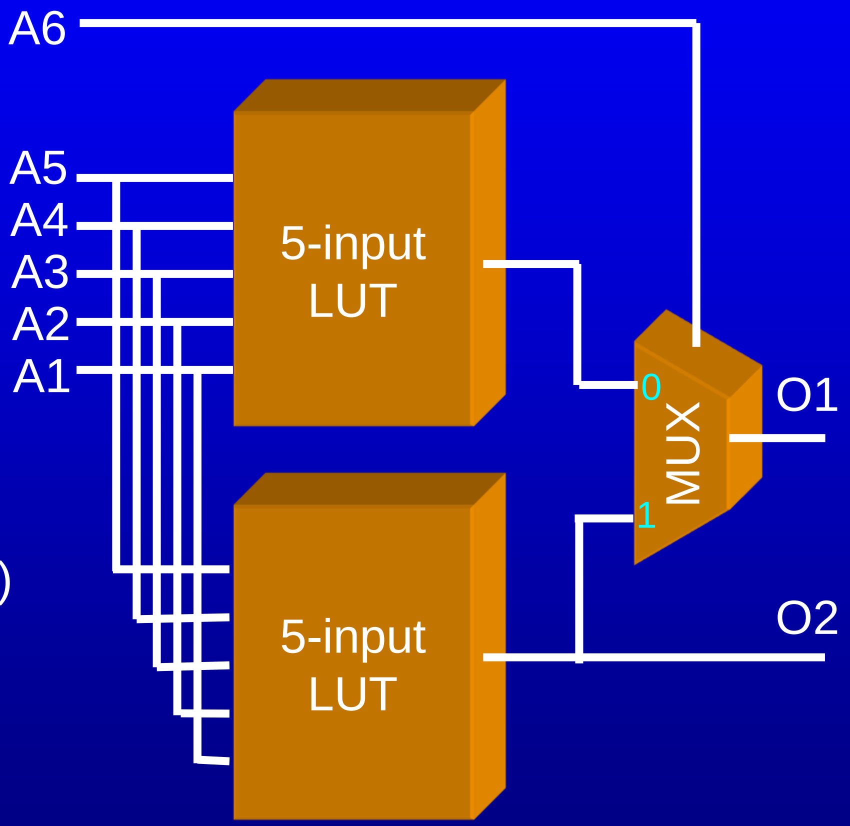
Xilinx 7-Series Architecture

- 64-bit Look-up Tables (LUT)
  - All functions of 6 inputs
- What if we wanted 2 functions of 5 inputs instead?



Xilinx 7-Series Architecture

- 2 Functions of 5 inputs
  - Split into 2 banks
    - 2 functions of 5 inputs



A6 = 0: 2 functions **O1** and **O2** of 5 variables (A1-A5)
A6 = input variable: 1 function **O1** of 6 variables (A1-A6)

Technology Mapping in FPGAs

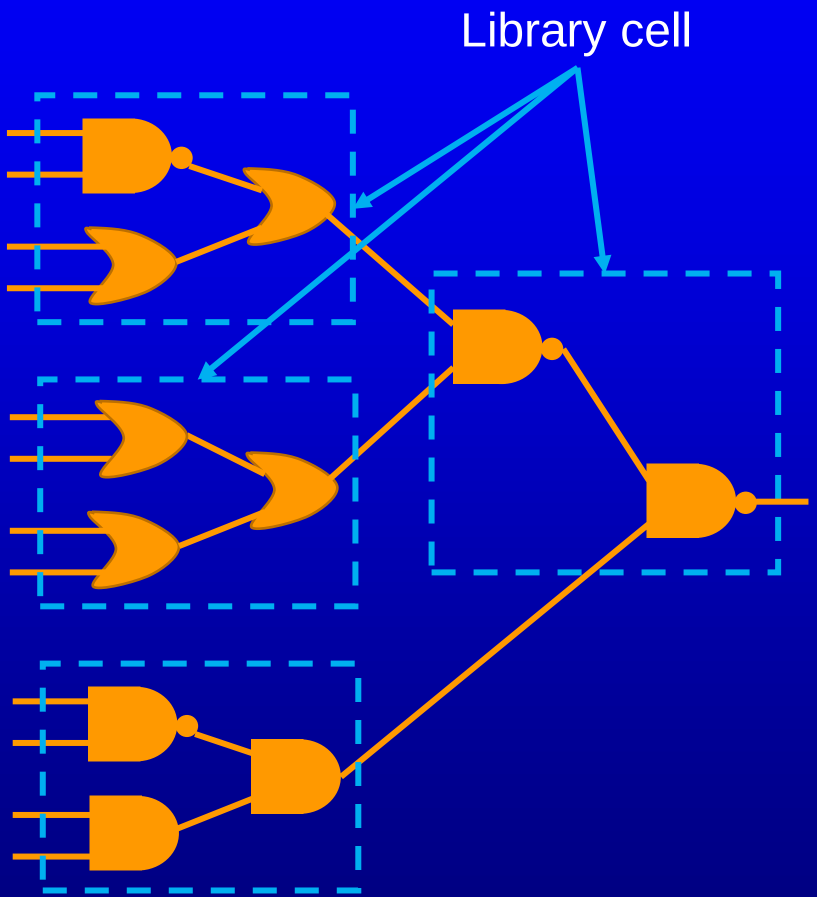
- More complex “library cells”
- Library cells can be customised
  - cannot enumerate fully

Matching

- Matching is trivial
  - ANY function can be implemented
  - make sure number of inputs match

Covering for 4 i/p block

- Treat library cell as
  - Black Box with 4 inputs, 1 output
    - no need to decompose into NAND/INV
- Technology Mapping
  - Cover the network by sub-graphs of 4 inputs, 1 output


Library cell