Synthesis of Digital Systems
COL719
Course Outline

II Semester 2023-24
Classroom: LH620
Schedule: J Slot
Class timings: Mon/Tue/Fri 12:00-13:00
(tentative)

Preeti Ranjan Panda
Dept. of CSE, IIT Delhi

Synthesis of Digital Systems

- Digital Hardware Synthesis
  - Automatic translation from “abstract high-level specification” to “detailed implementation”
- How do we design/implement a 100-million gate chip?
  - Start with specification language (looks like programming language)
  - Automatically convert to hardware
  - How to do this efficiently?

Synthesis Challenges

- Same input can have many equivalent implementations
  - similar to compiler
- Metrics of efficiency
  - area of system
  - performance
  - power and energy

Necessary Background

- Digital design
  - Combinational and sequential logic
    - gates, MUX, Adder/ALU,...
  - Finite State Machines (FSM)
    - specification and realisation using flip flops and gates
  - Logic Minimisation
- Data Structures and Algorithms
  - Arrays, Linked lists
- Programming experience

Emphasis on Assignments

- System Design/Optimisation problems
  - Metrics: Performance, Power/Energy, Temperature
  - Applications: General purpose, Application-specific Workloads
- Evaluation
  - 60% exams
  - 40% assignments

Reference Material

- Slides
- Lecture videos on YouTube (“Synthesis of Digital Systems”)
- Book on Synthesis
  - Giovanni de Micheli, **Synthesis and Optimization of Digital Circuits**, McGraw Hill, 1994
- HDL Background
  - Internet sources