Lecture 23
Multiple State Machine Implementation & Clock Period

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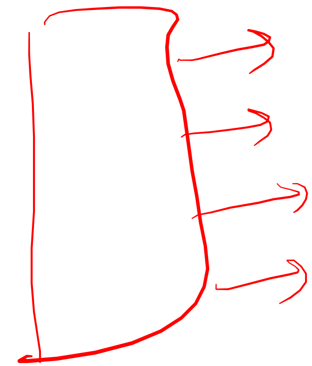
Steps in State Machine Synthesis using Counters

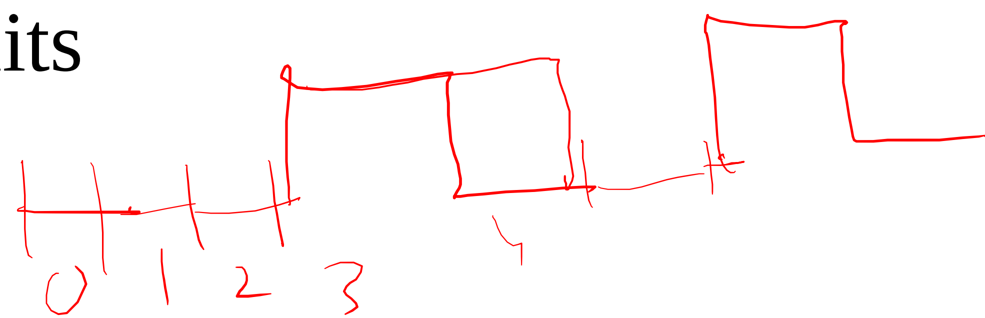
- Encode the states
- Choose a counter with appropriate control inputs to implement the state register
- Use the counter functionality table to arrive at the spec. of the combinational logic
- Synthesize the combinational logic

Applications of Sequential Machines

0, 1, - - - 15

- Pattern matching
  - Overlapped or non-overlapped
  - Blocked or non-blocked
- Sequential decoding
- Controllers
- Memory based circuits





Interacting State Machines : Example

- Search for a pattern P = ‘1101’ within blocks of 256 bits. The pattern should not cross block boundaries.
- Design two state machines M1 and M2
  – M1 is a modulo 256 counter
  – M2 is the pattern recognizer
- The 256th transition of M1 should initialize M2

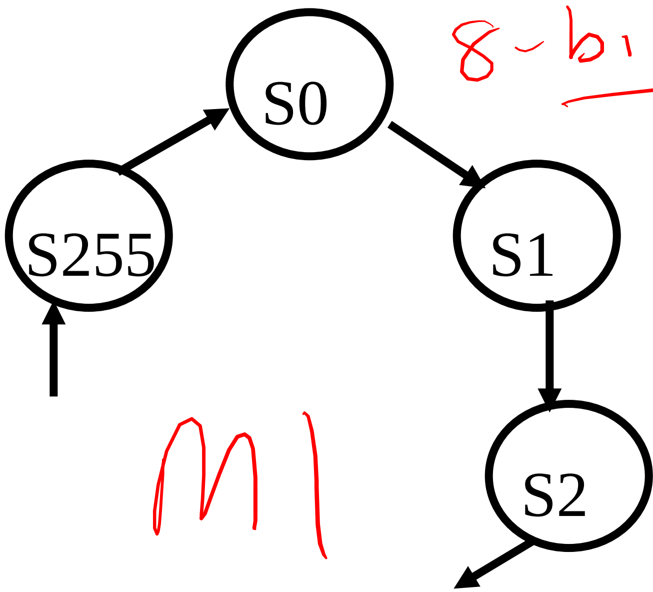
Example (Contd.)

Blocked Overlapping

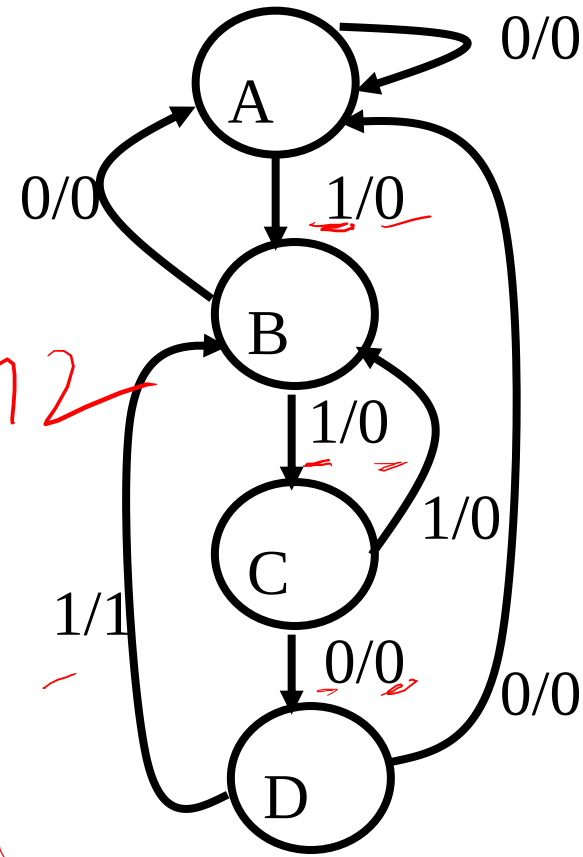
1101

mod256

8-bit Counter

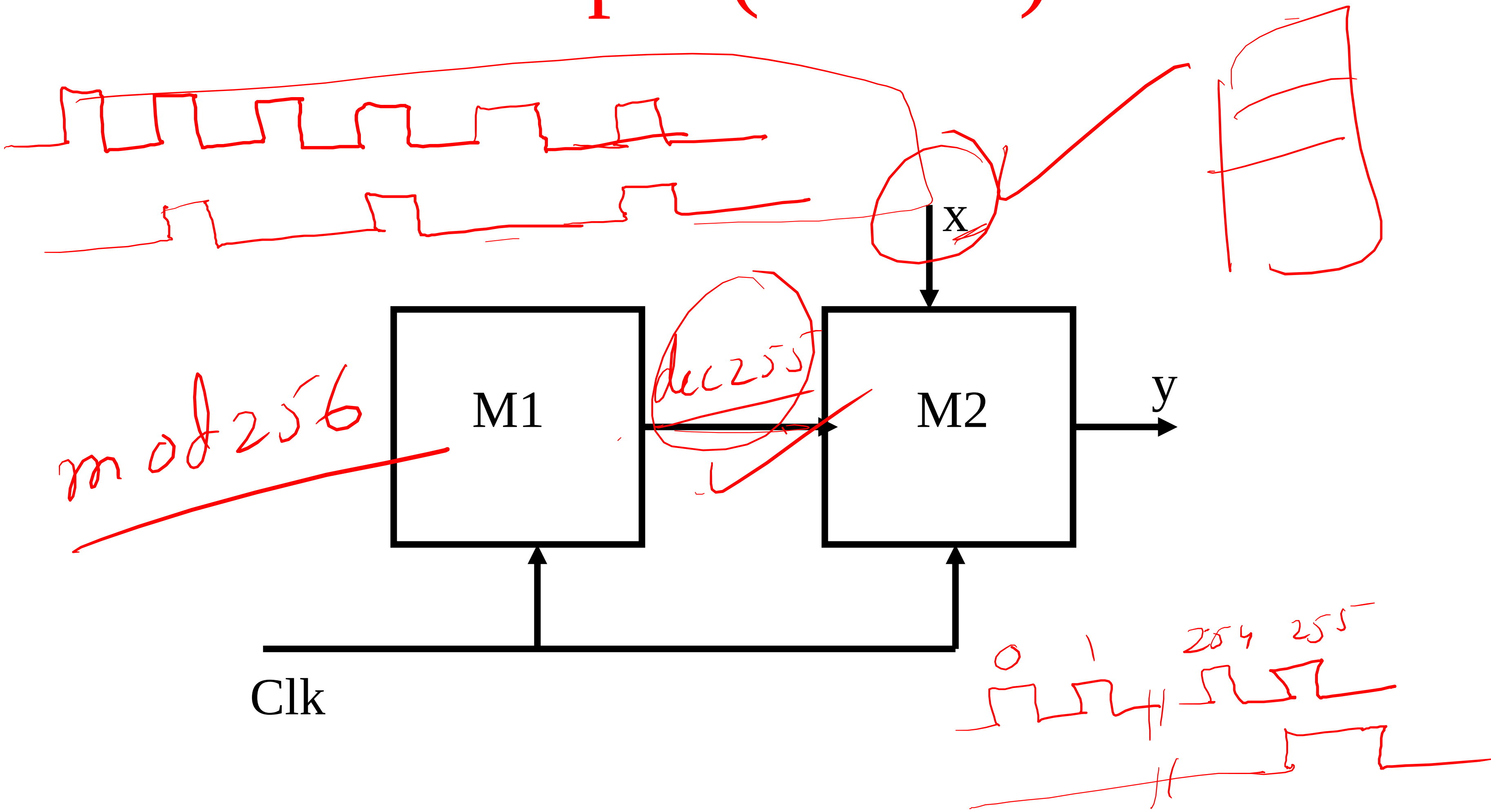


M1



M2

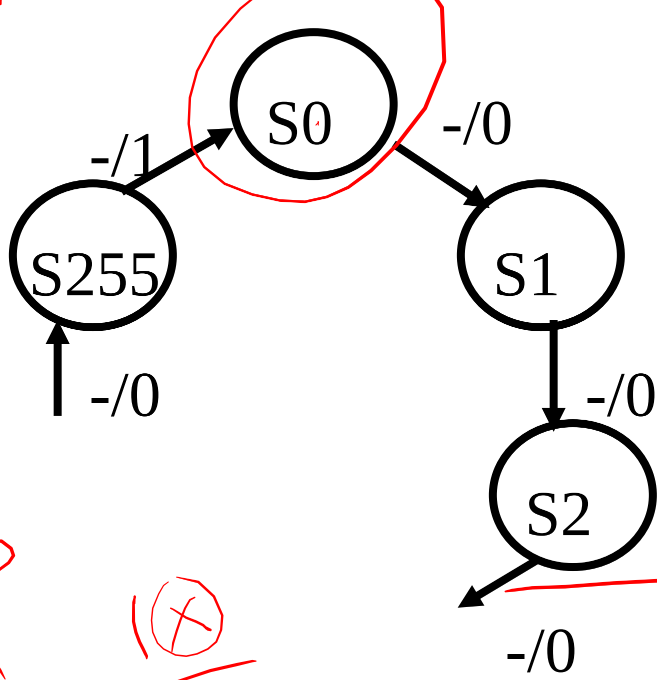
Example (Contd.)

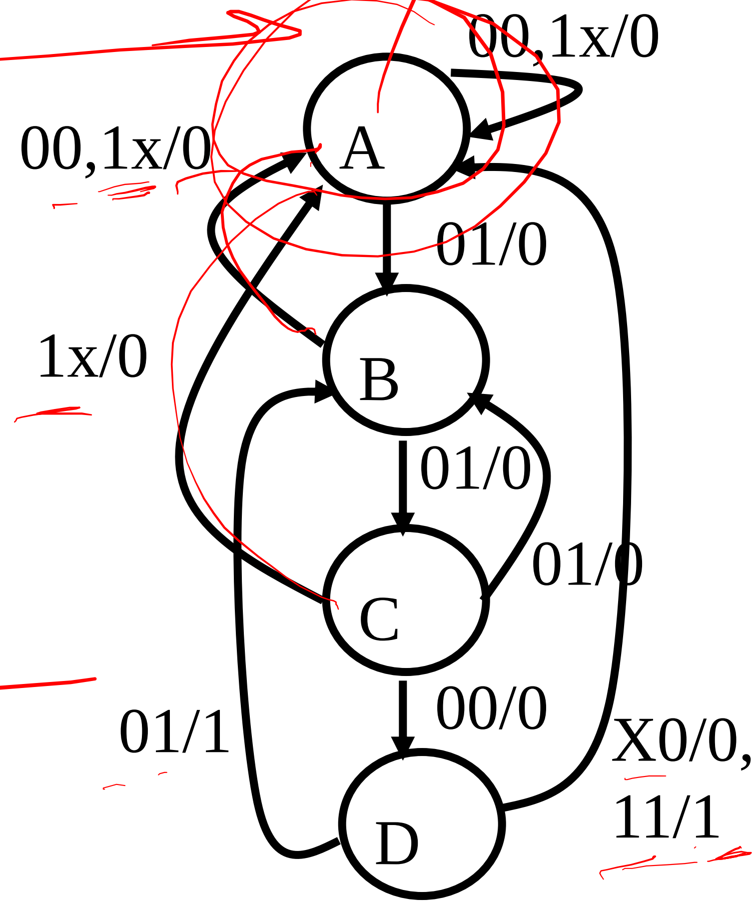


Example (Contd.)

00 01
10 11
Dec255

00



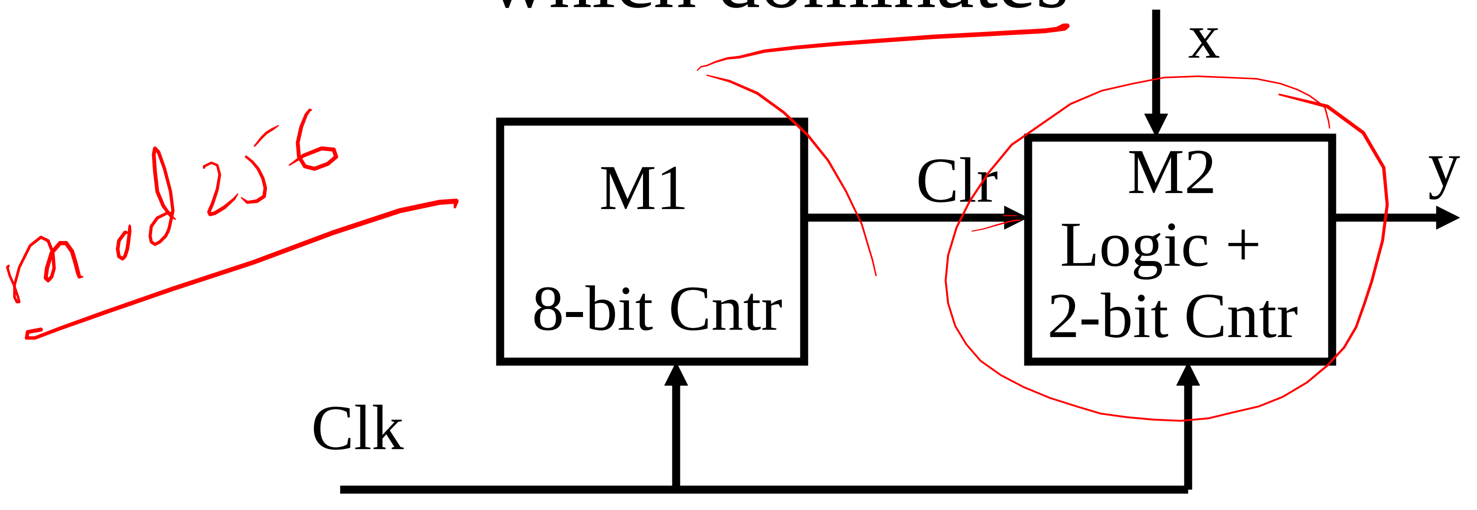


10
11

Design Summary: Example

- M1 : 8-bit free running counter
- M2 : Counter with synchronous clear which dominates

1101



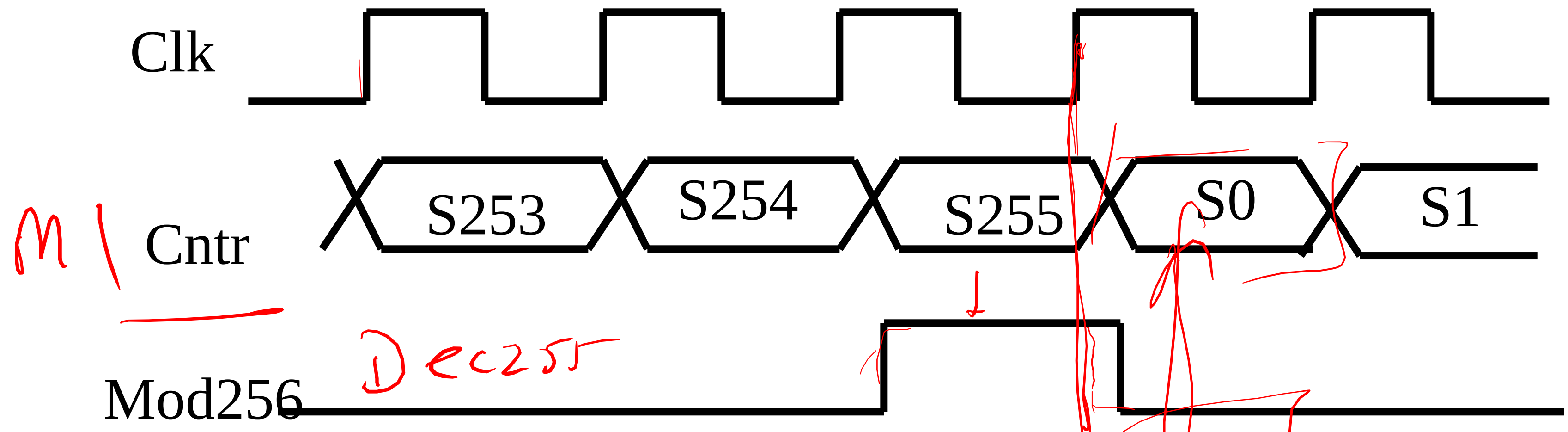
$O = f(PI, PS)$

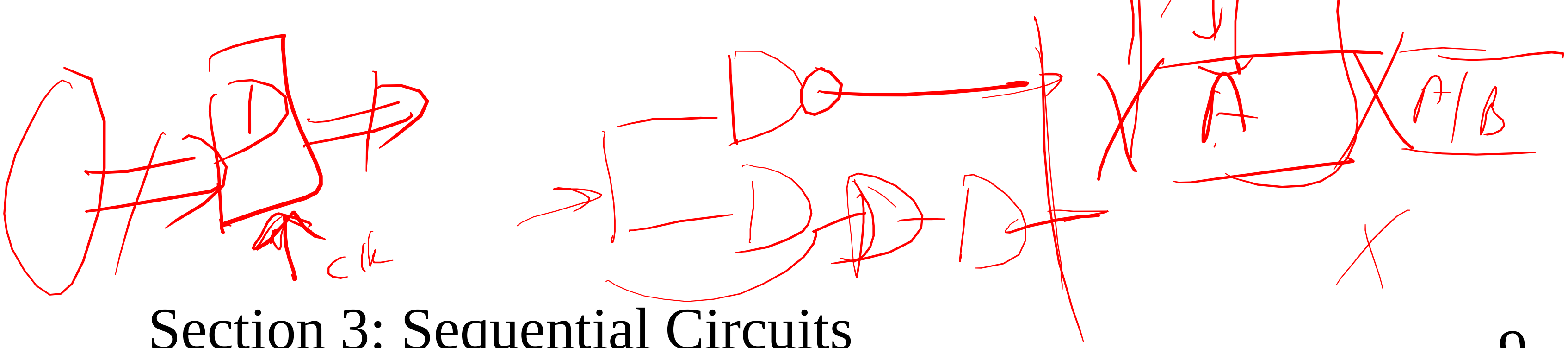
$O = f(PS)$ | moore

Register & Latch Waveforms

$NS = g(PI, PS)$

$NS = g(PS, PI)$





Multiple State Machines: Another Example

email @ 8-bit

- In a bit stream, count the number of "@" (ASCII Code) characters in blocks of 256 8-bit characters
- Three state machines: M1, M2 and M3
  - M1: Pattern recognizer for "@" character
  - M2: 8-bit counter for counting 256 characters
  - M3: 8-bit Counter for counting no. of "@"

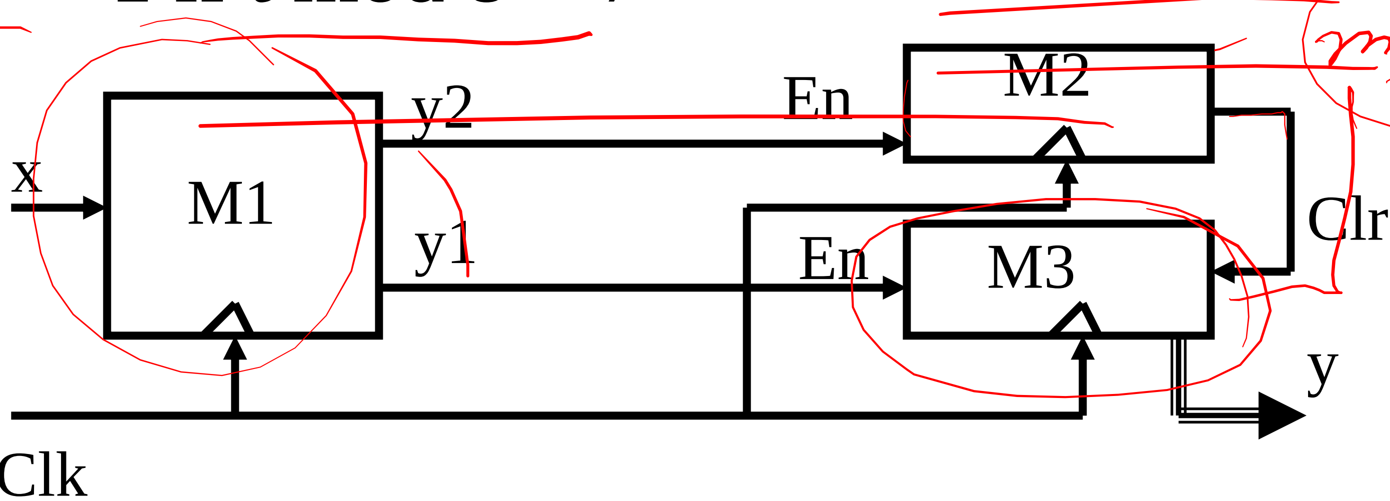
Second Example (Contd.)

@ 10110110 @

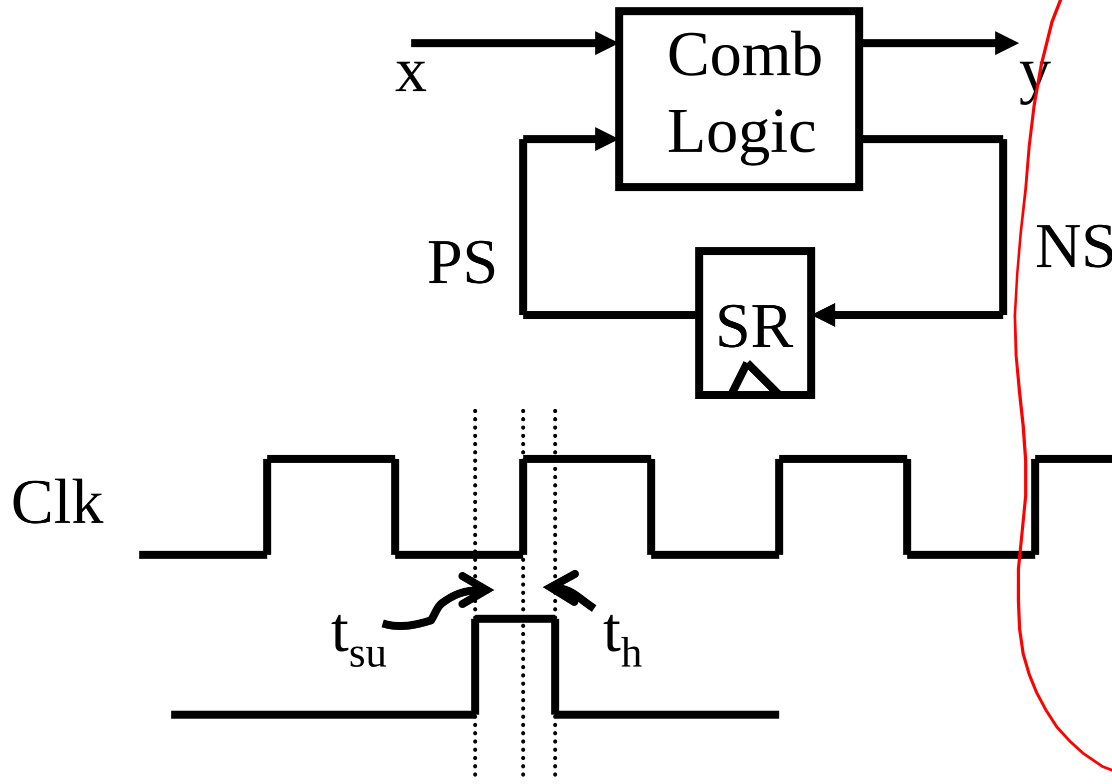
Specification of M1

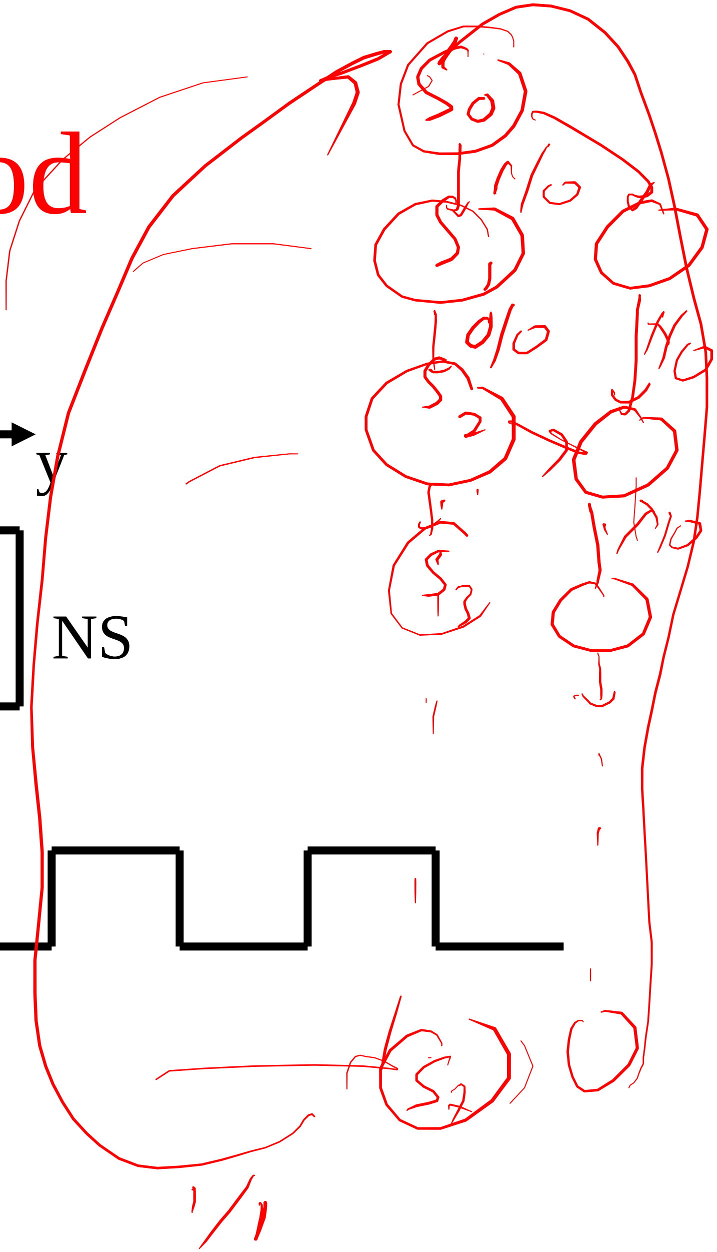
y1 = 1 if <x(t-7)..x(t)> = “@” and t mod 8 = 7

y2 = 1 if t mod 8 = 7



Clock Period





Clock Period Computation

t_o: Critical path delay (x,PS) to y

t_{ns}: Critical path delay (x,PS) to NS

t_d: SR delay

t_{su}: Setup time of the SR

t_h: Hold time of the SR

$$t_{clk} \geq \max\{ t_d + t_o, t_d + t_{ns} + t_{su} \}$$