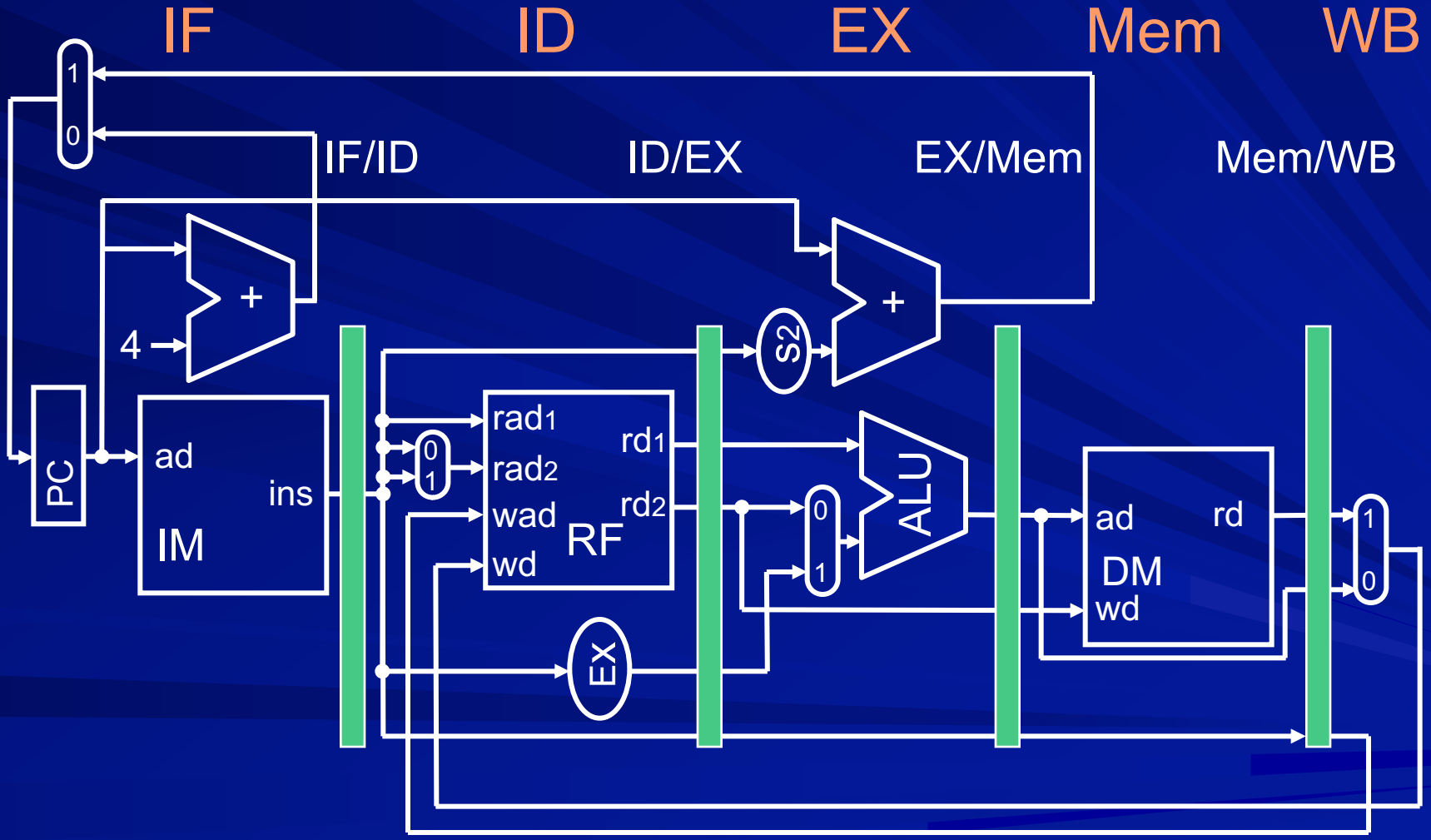
COL216
Computer Architecture

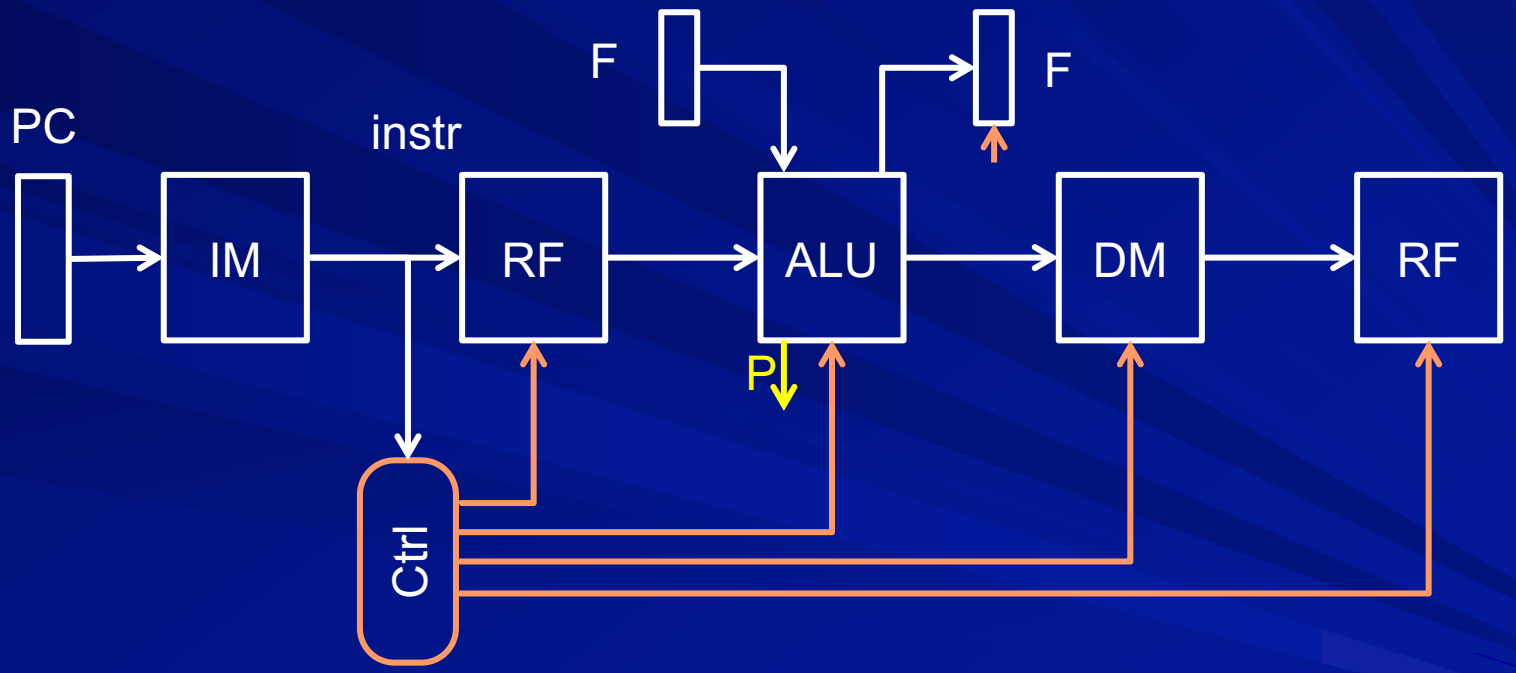
Pipelined Processor design –
Controller, Data forwarding
21st February 2022

5 Stage Pipeline

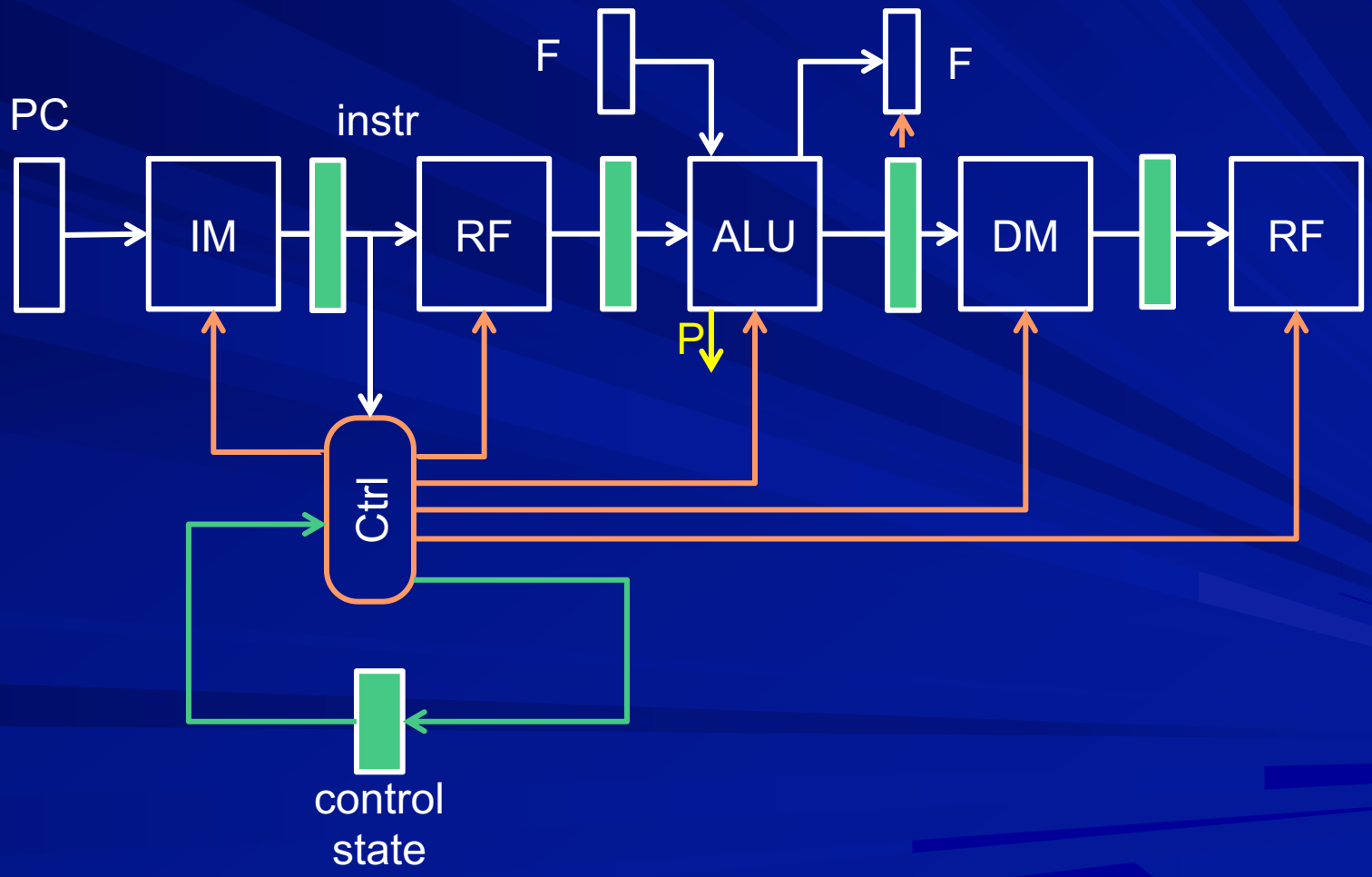


Controllers for different design styles

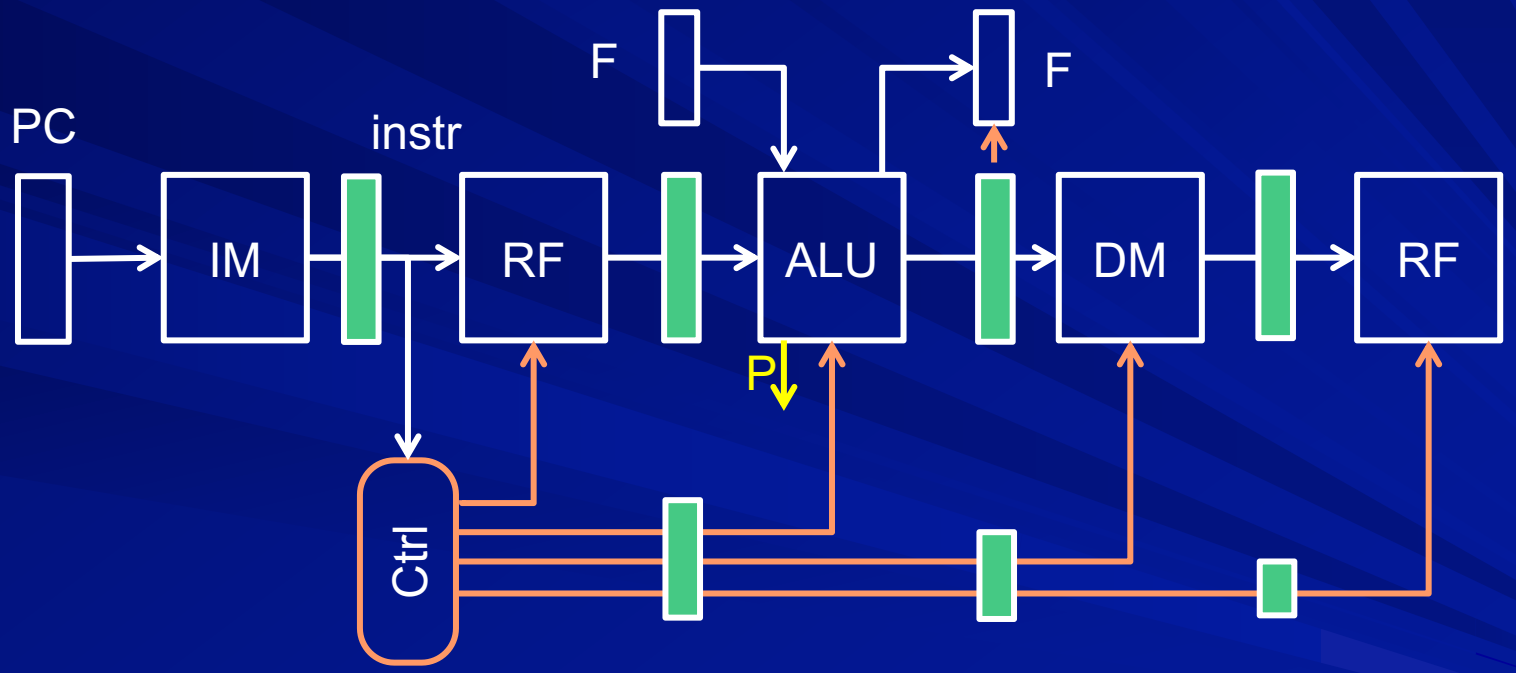
Controller for single cycle DP



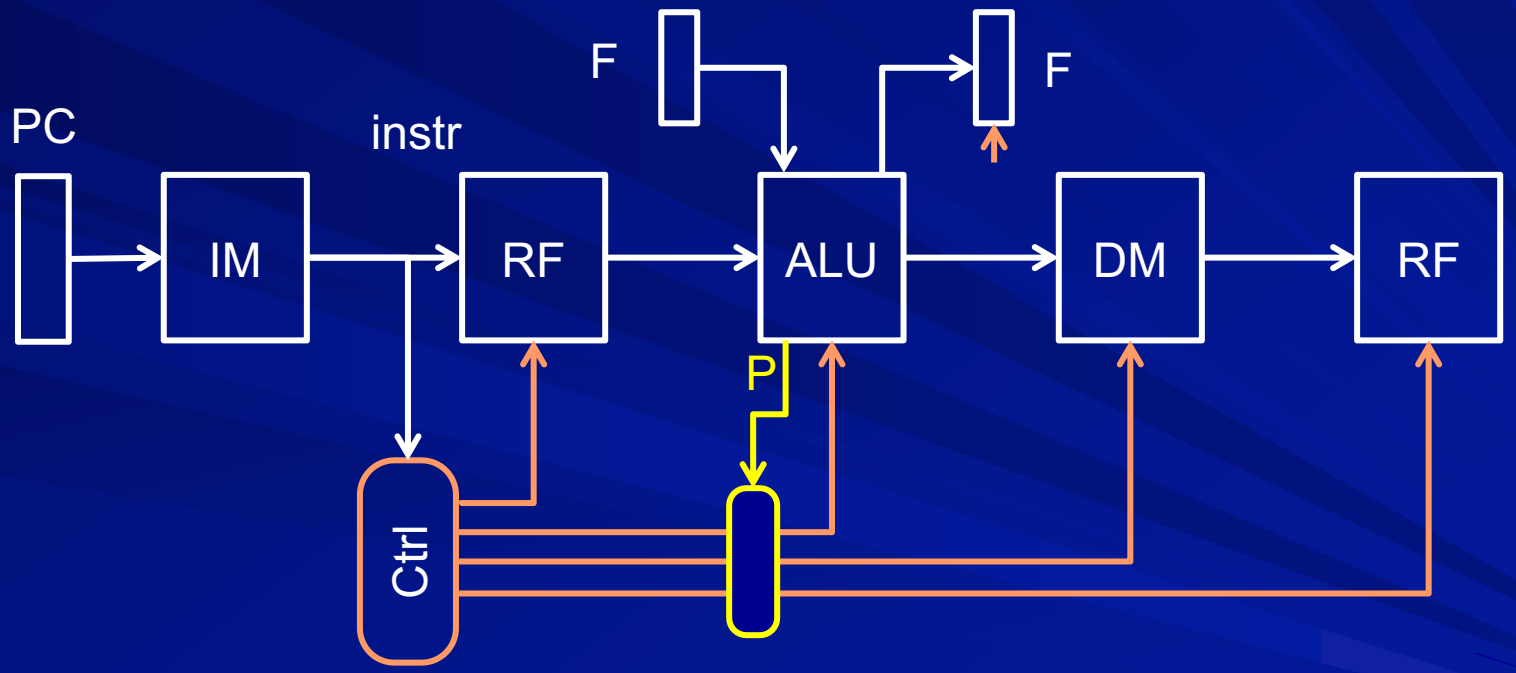
Controller for multi-cycle DP



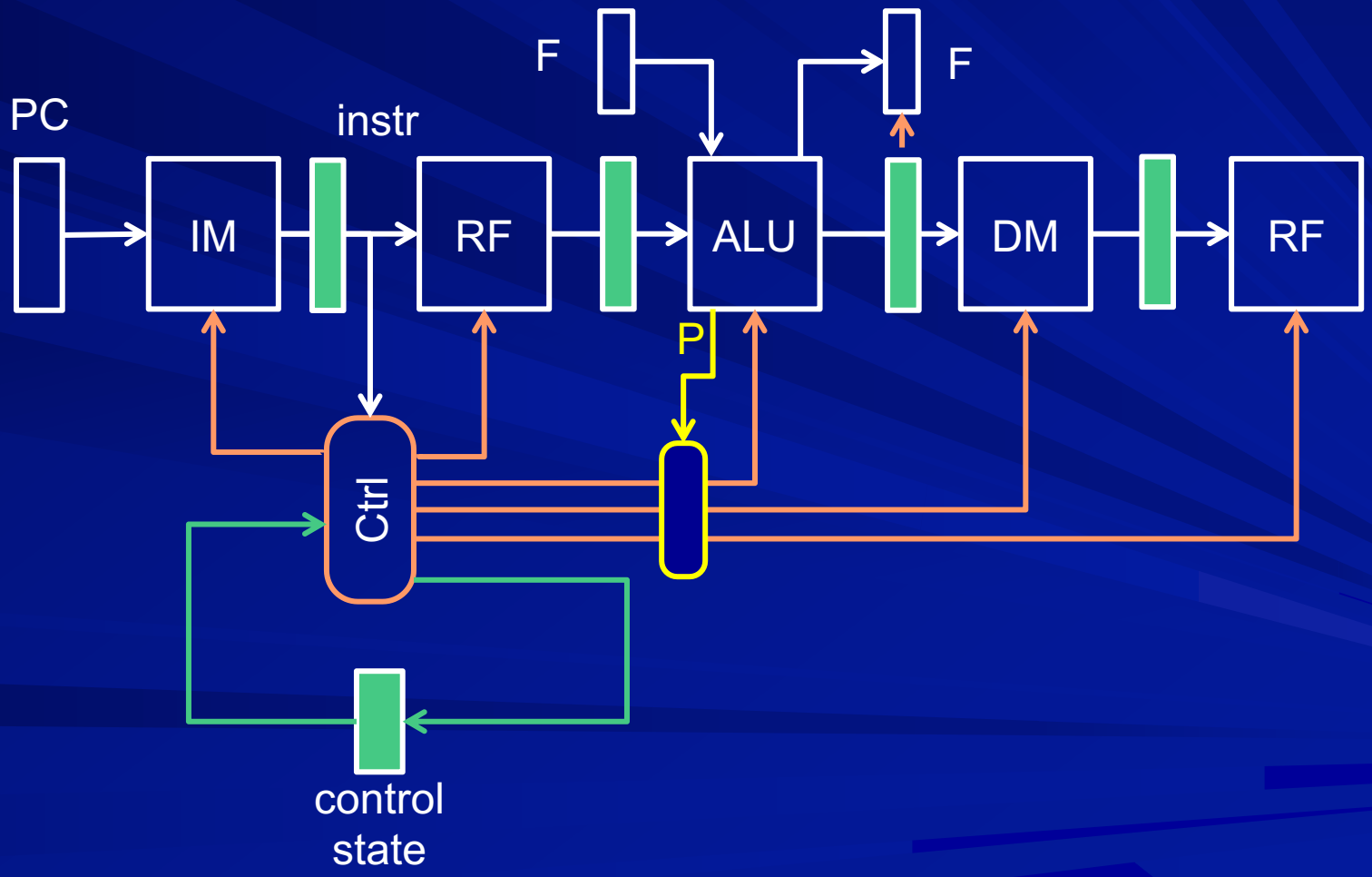
Controller for pipelined DP



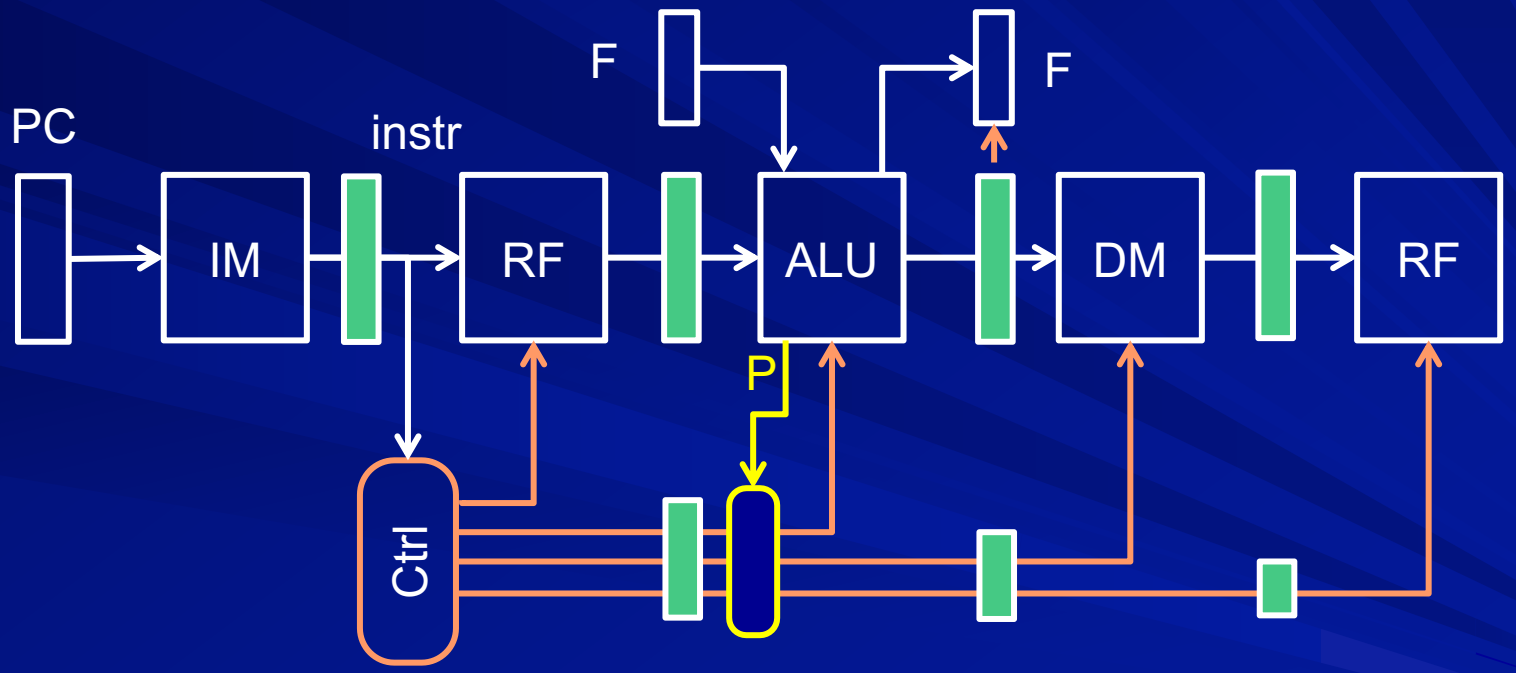
Controller for single cycle DP



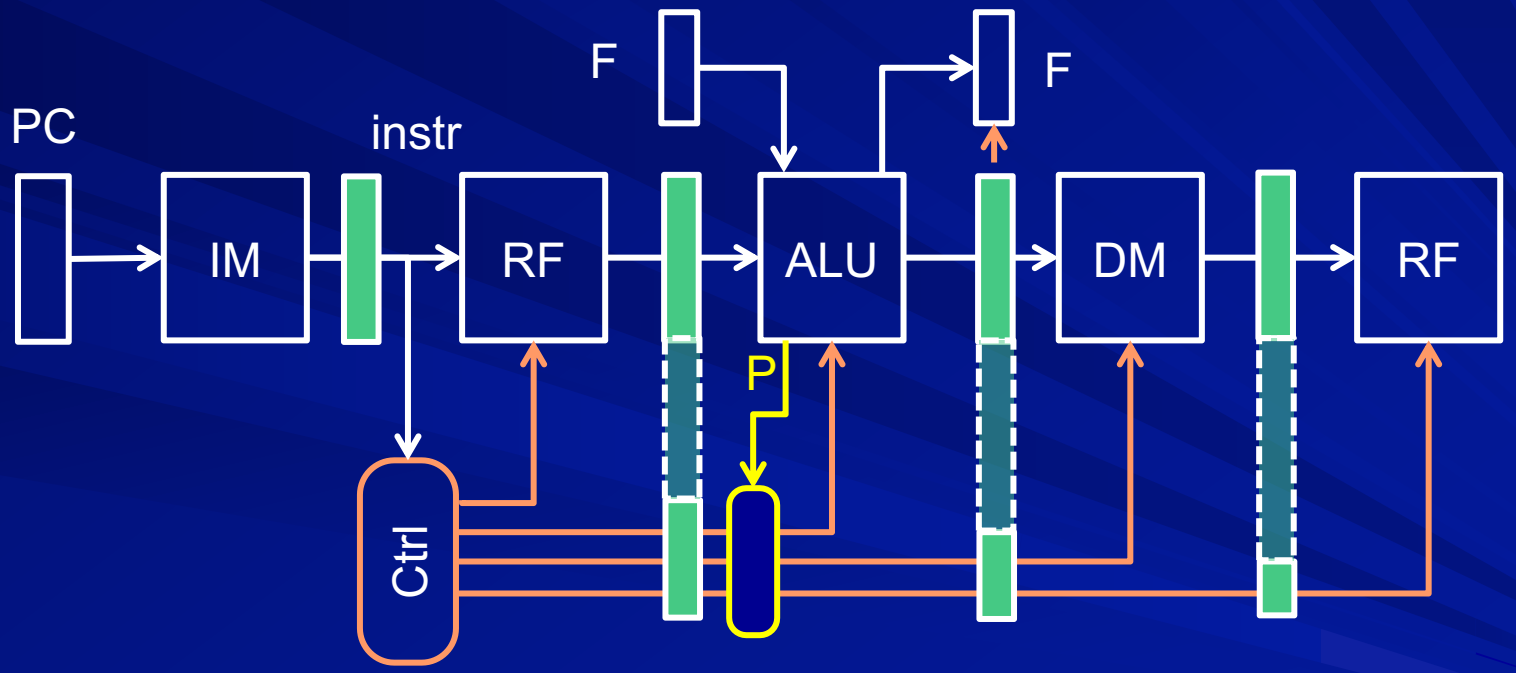
Controller for multi-cycle DP



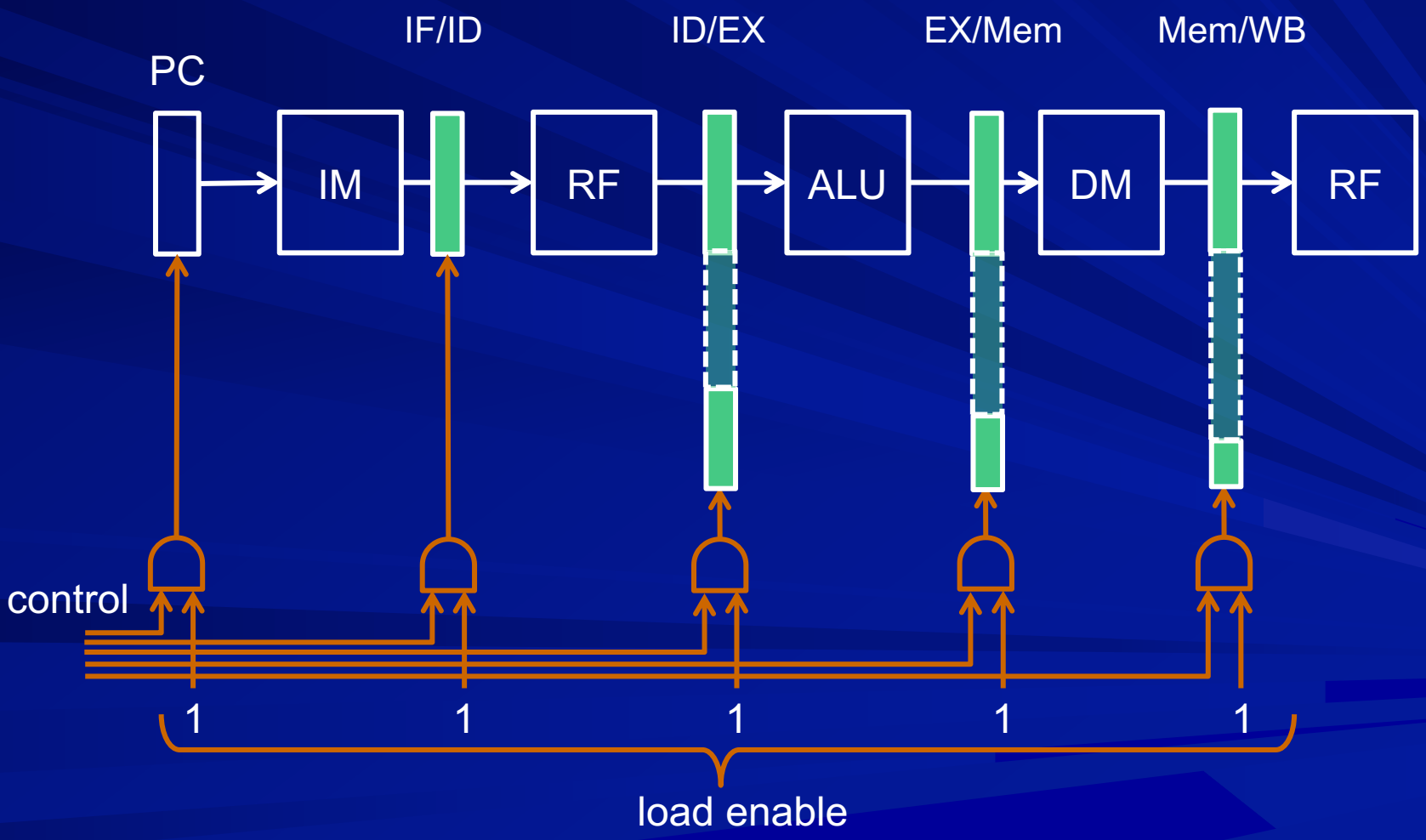
Controller for pipelined DP



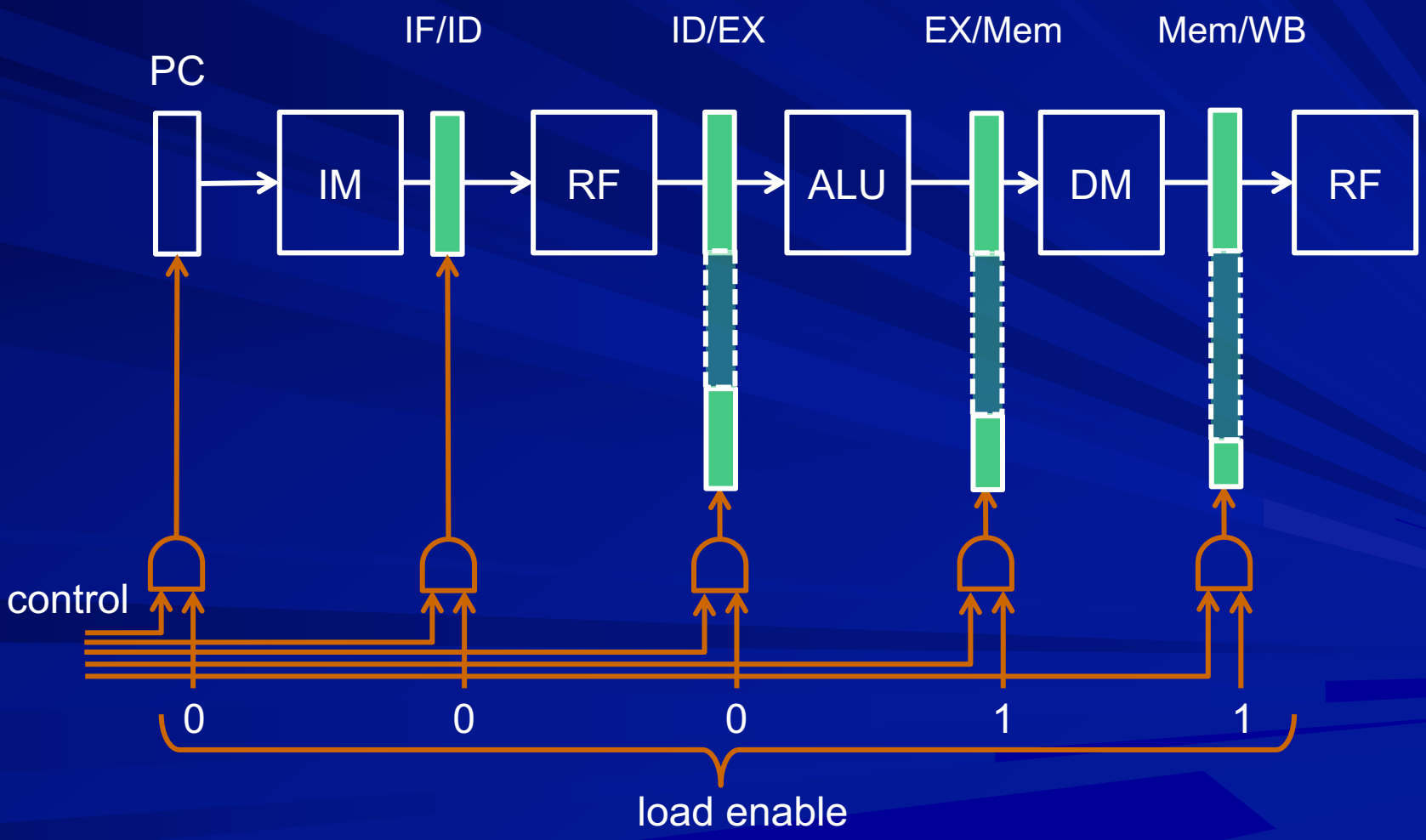
Extending inter-stage registers



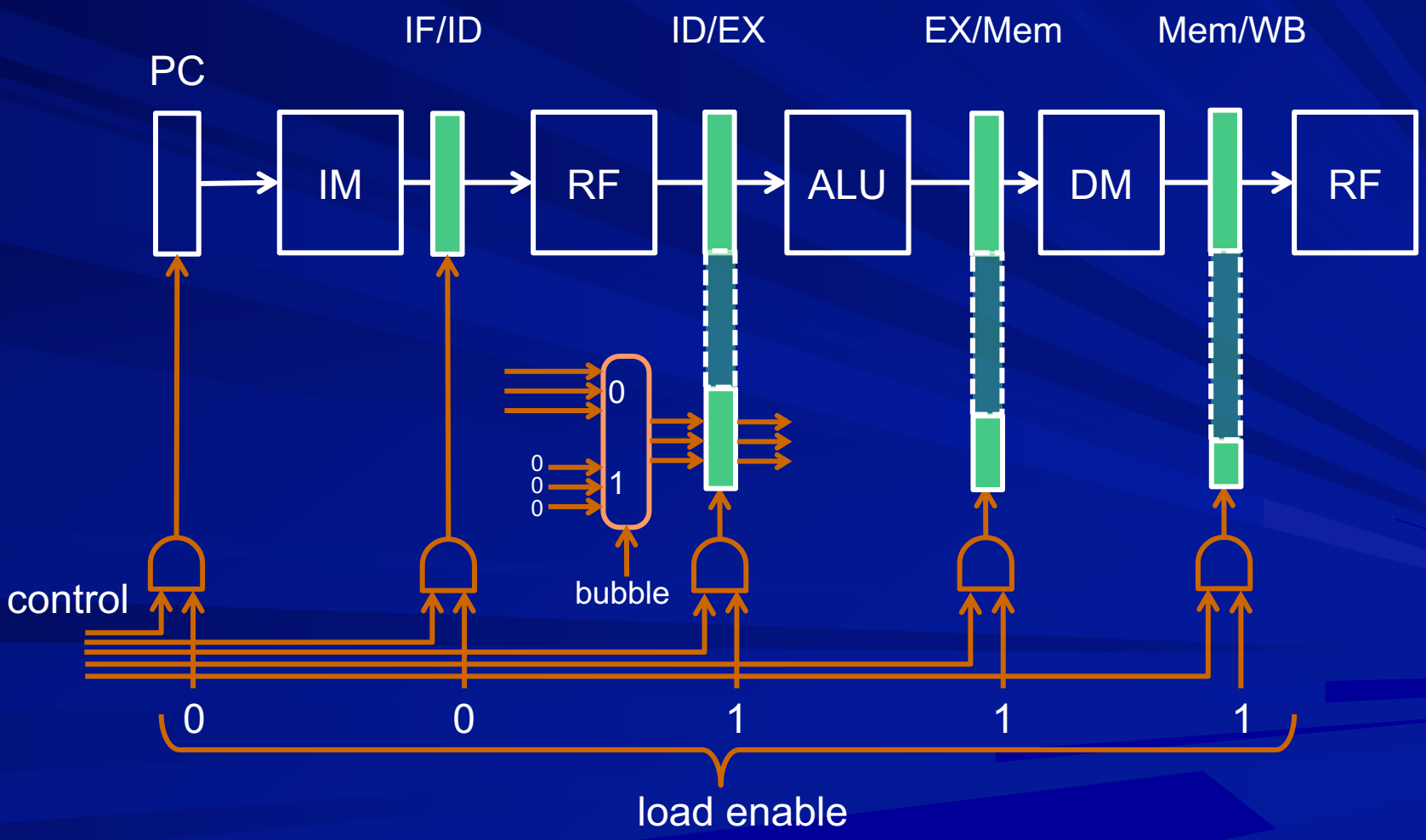
Controlling inter-stage registers



Stalling instructions



Inserting bubbles



Dependence check logic

Condition to be checked:

Operand of instruction in RF stage is a register in which instruction in ALU stage or DM stage is going to write

ID/EX.RW = 1 and

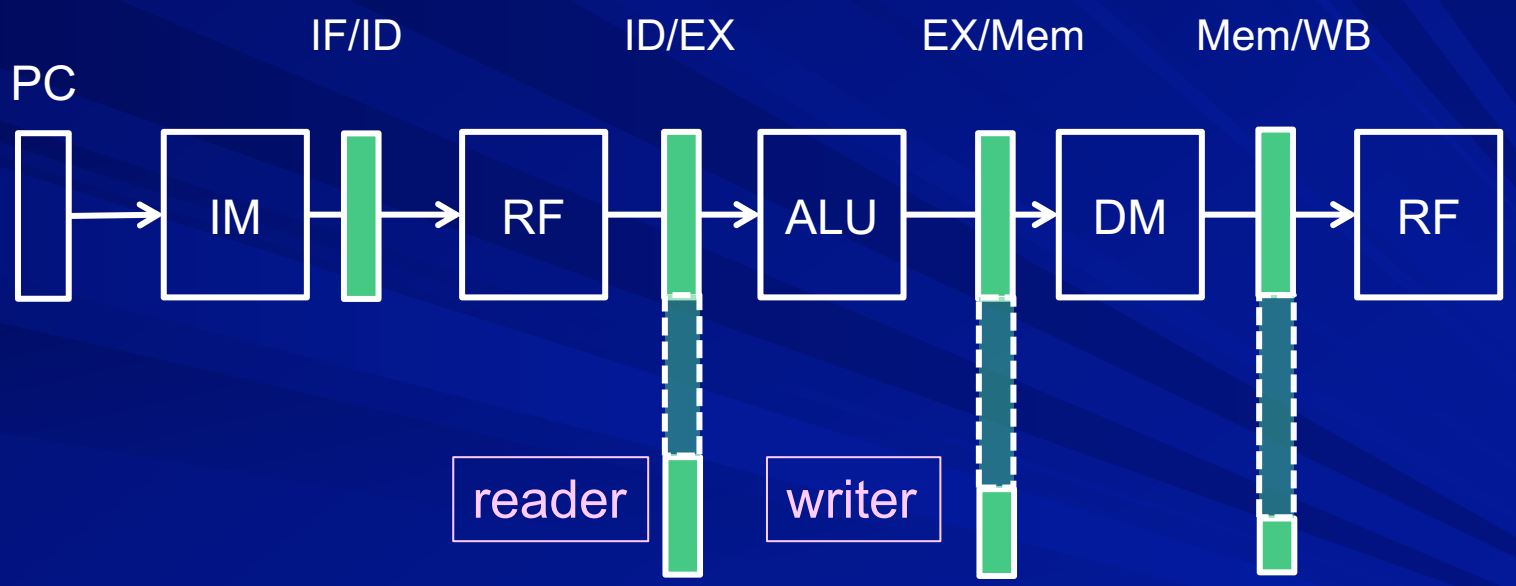
(IF/ID.Rn=ID/EX.Rd or IF/ID.Rm=ID/EX.Rd)

EX/Mem.RW = 1 and

(IF/ID.Rn=EX/Mem.Rd or IF/ID.Rm=EX/Mem.Rd)

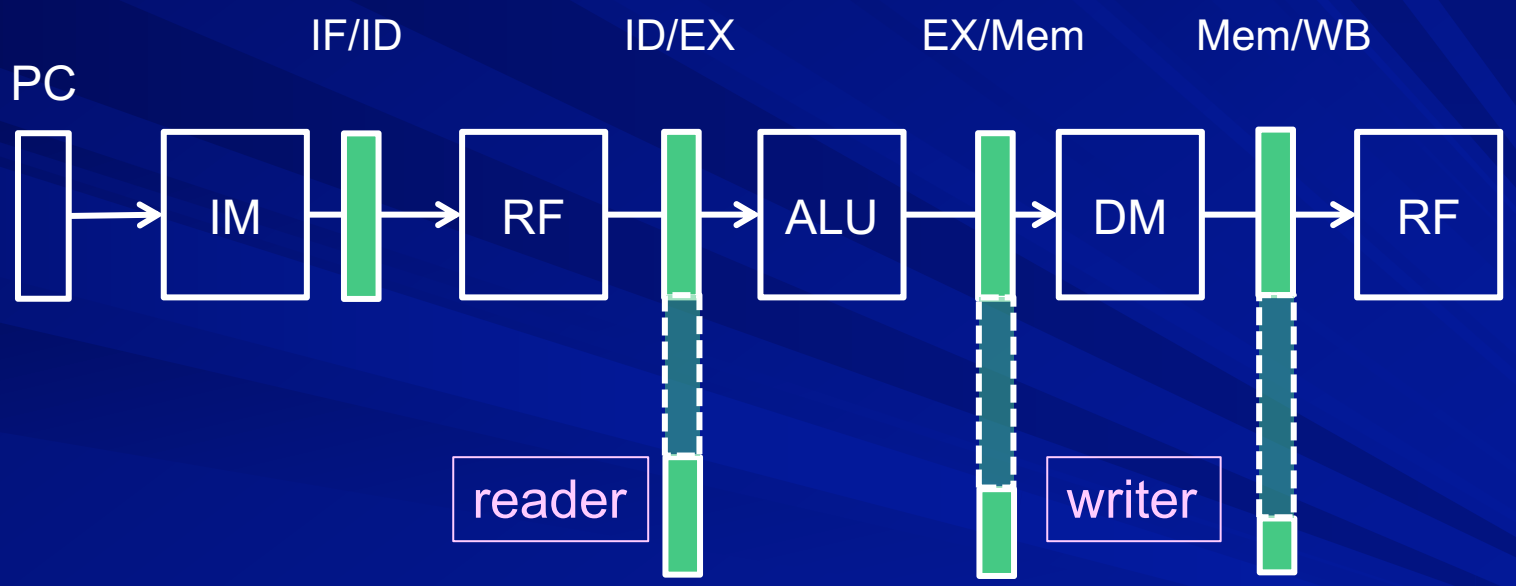
We need to ensure that instruction in RF stage actually reads Rn and/or Rm (not taken care here)

Dependence check



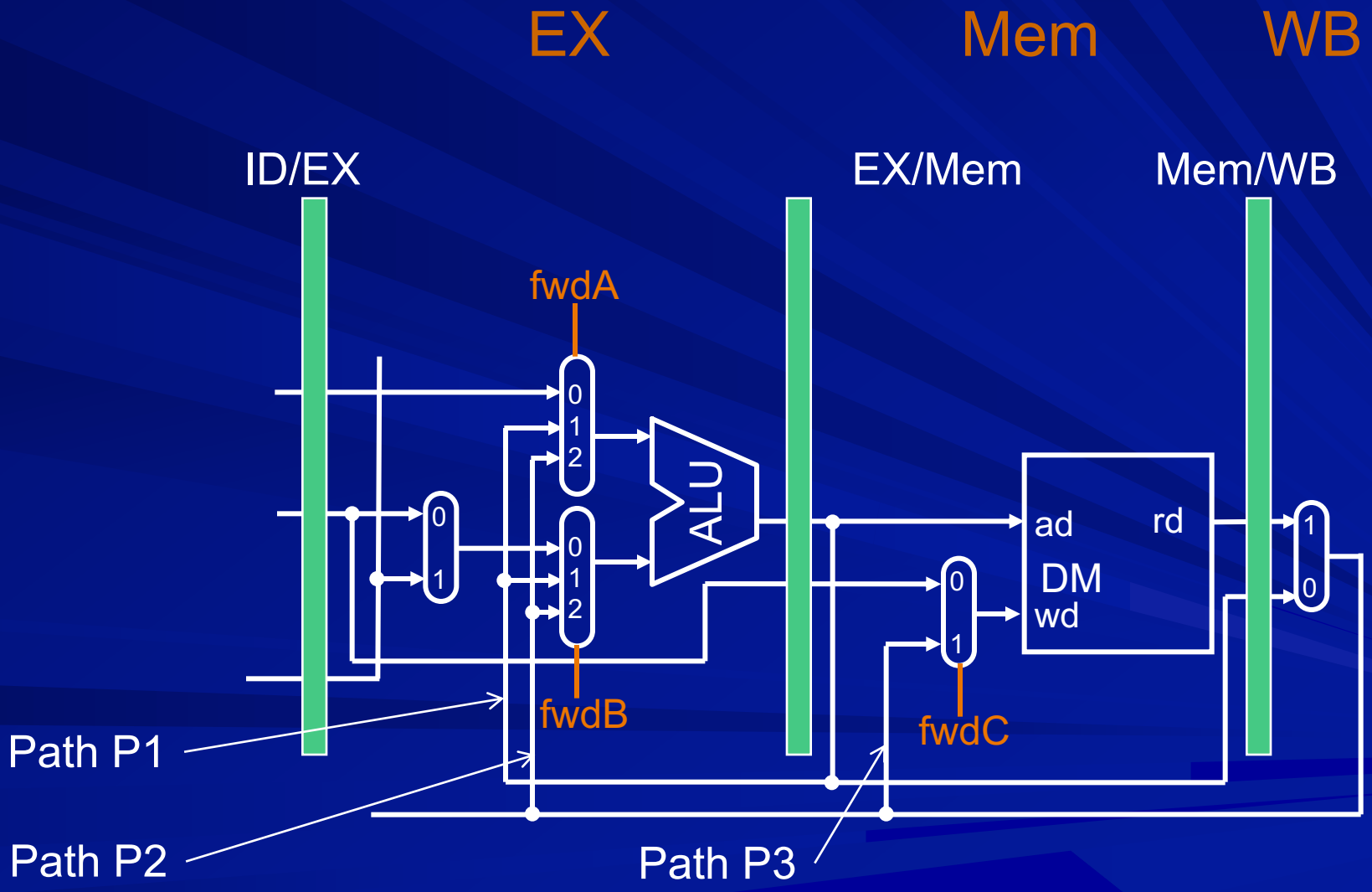
ID/EX.RW = 1 and
(IF/ID.Rn = ID/EX.Rd or
IF/ID.Rm = ID/EX.Rd)

Dependence check



EX/Mem.RW = 1 and
(IF/ID.Rn = EX/Mem.Rd or
IF/ID.Rm = EX/Mem.Rd)

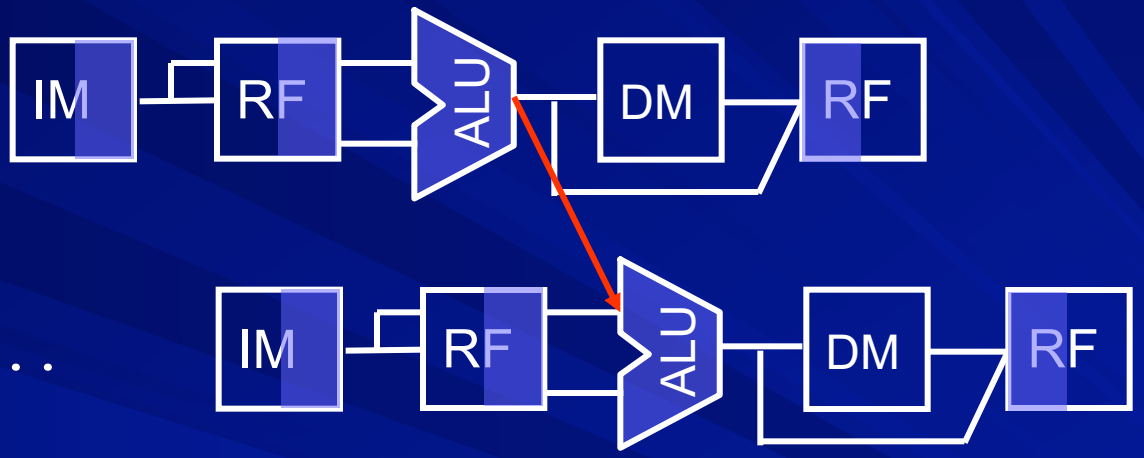
Data forwarding paths



Data forwarding path P1

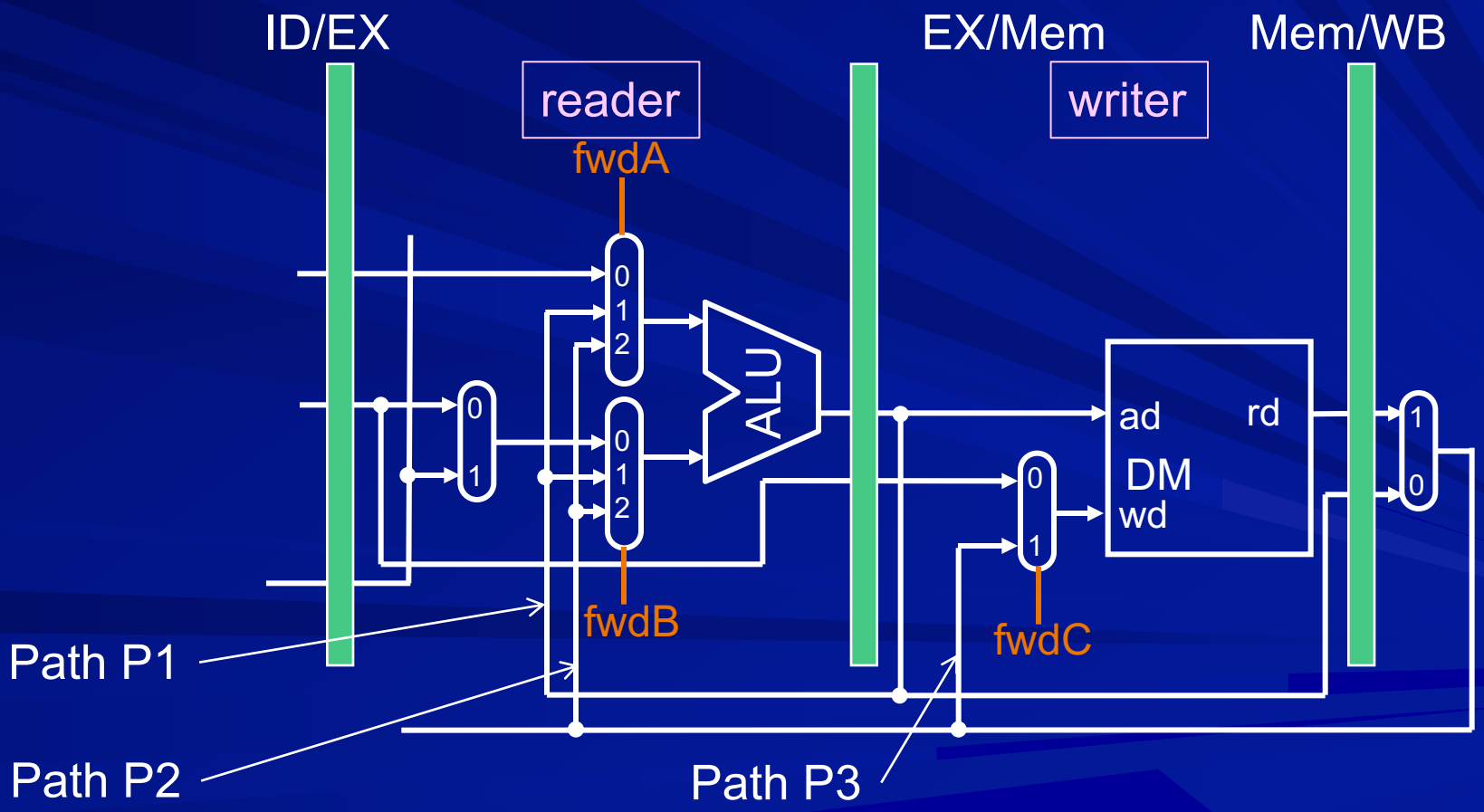
I:add r6,..

I+1:add r4,r6,..

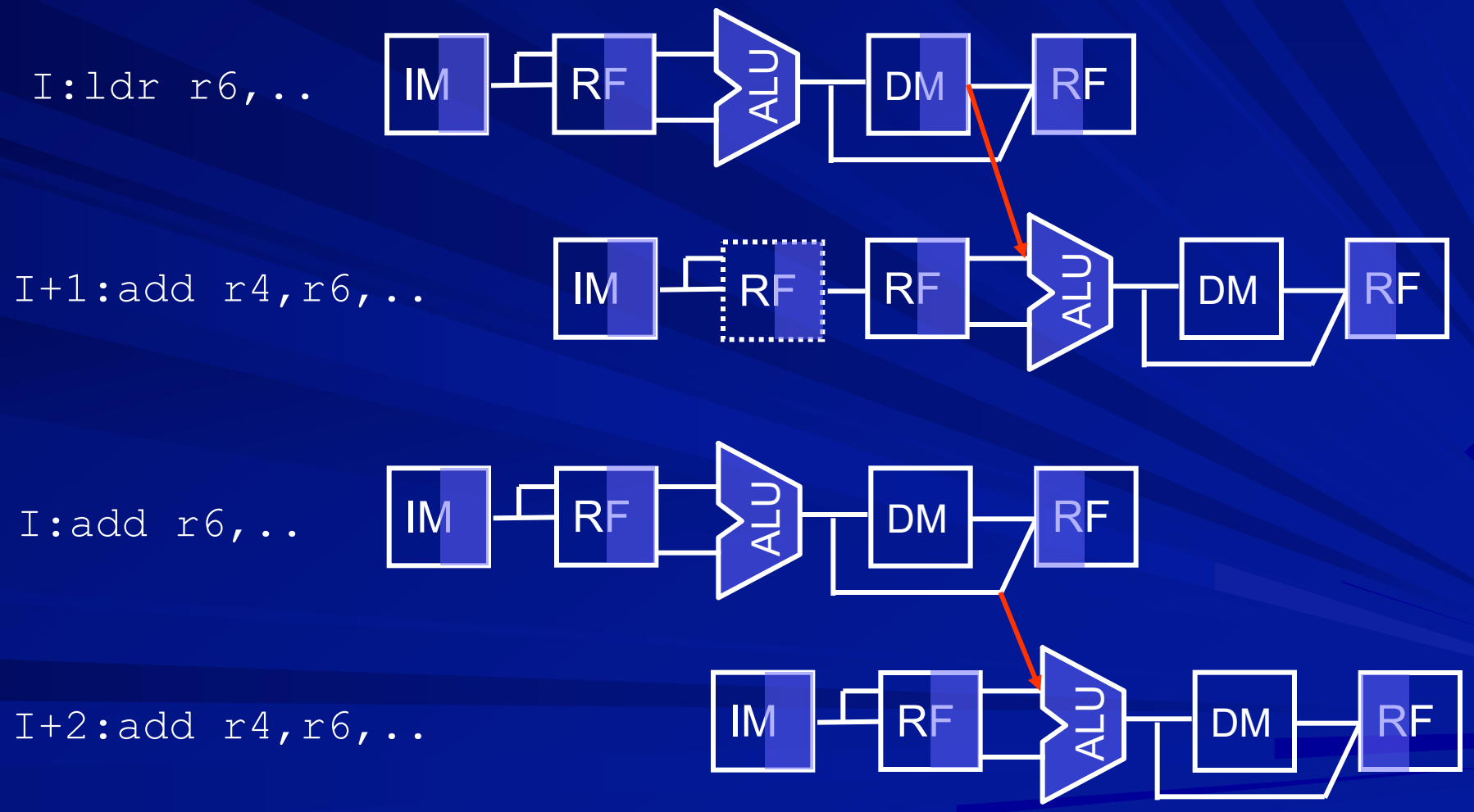


Control for forwarding path P1

fwdA = 1 if
EX/Mem.RW = 1 and
EX/Mem.Rd = ID/EX.Rn

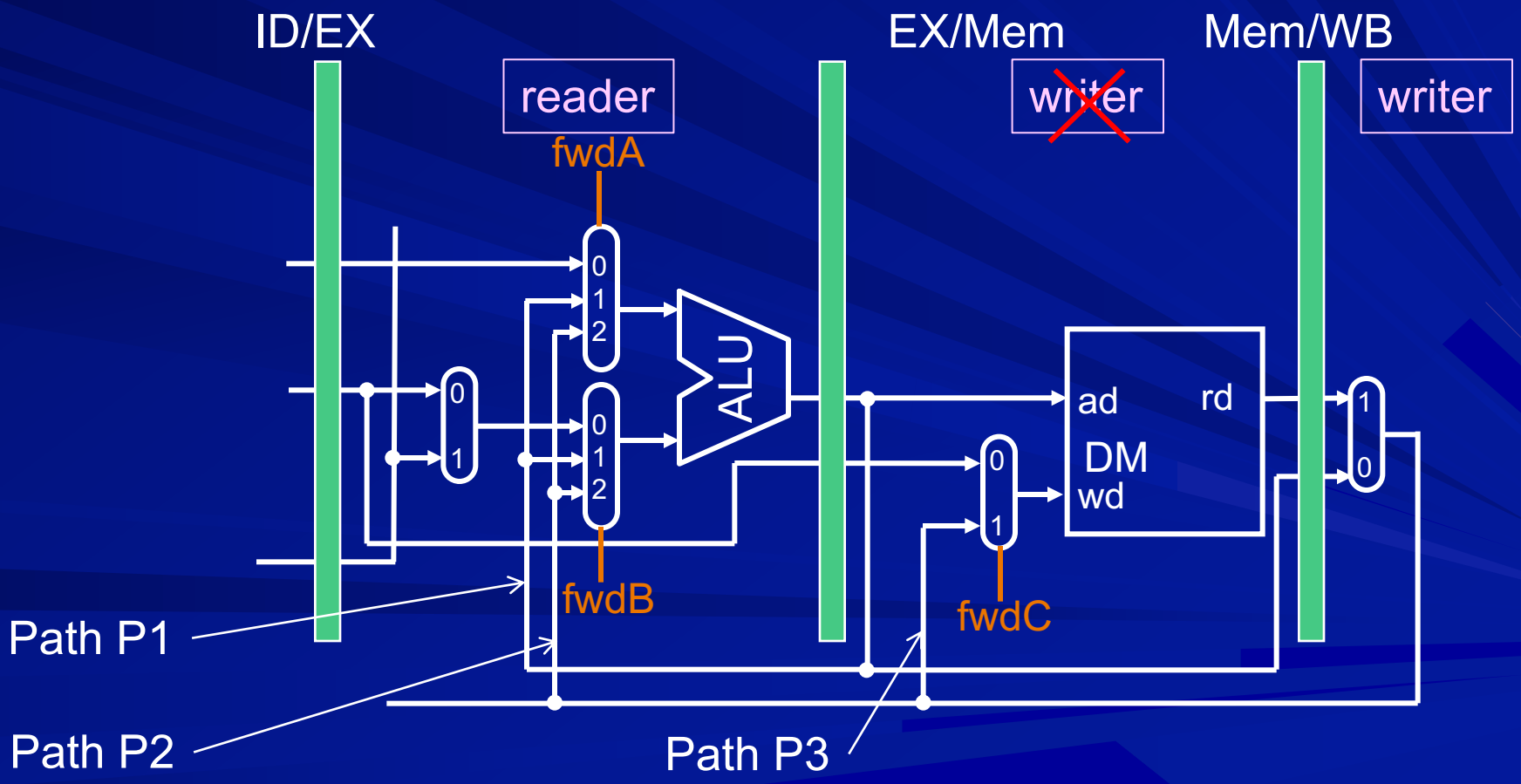


Data forwarding path P2

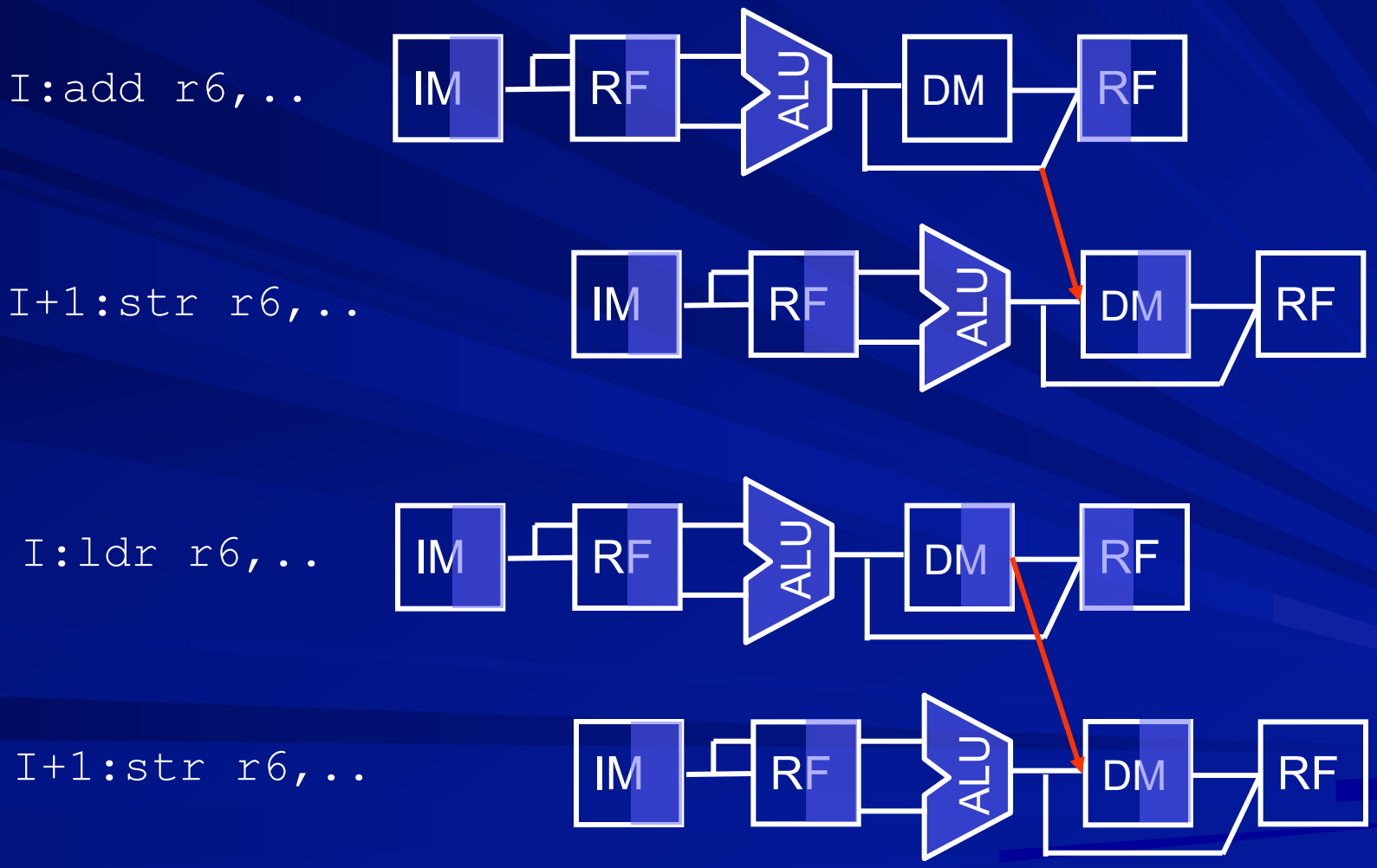


Control for forwarding path P2

fwdA = 2 if
Mem/WB.RW = 1 and
EX/Mem.Rd ≠ ID/EX.Rn and
Mem/WB.Rd = ID/EX.Rn

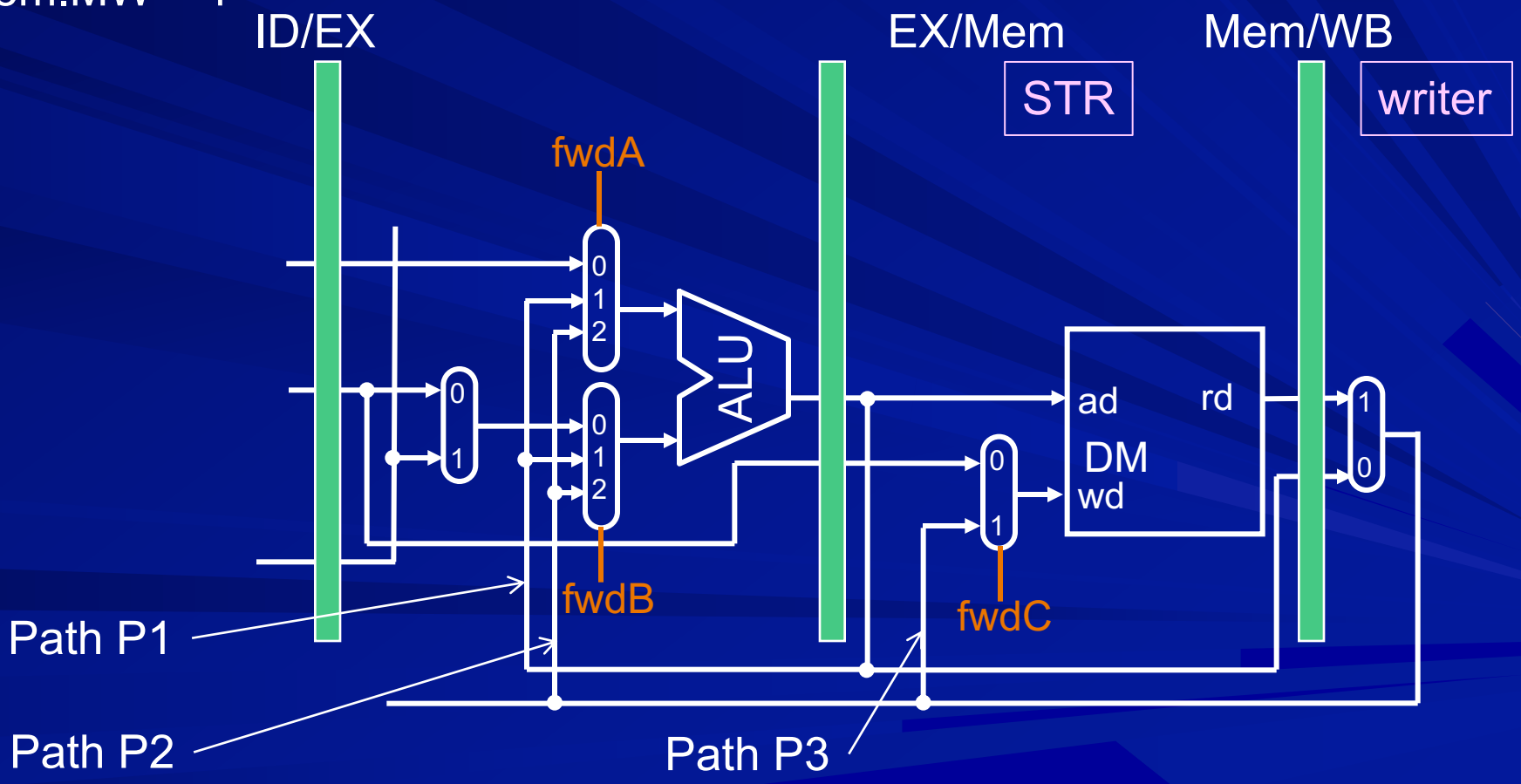


Data forwarding path P3



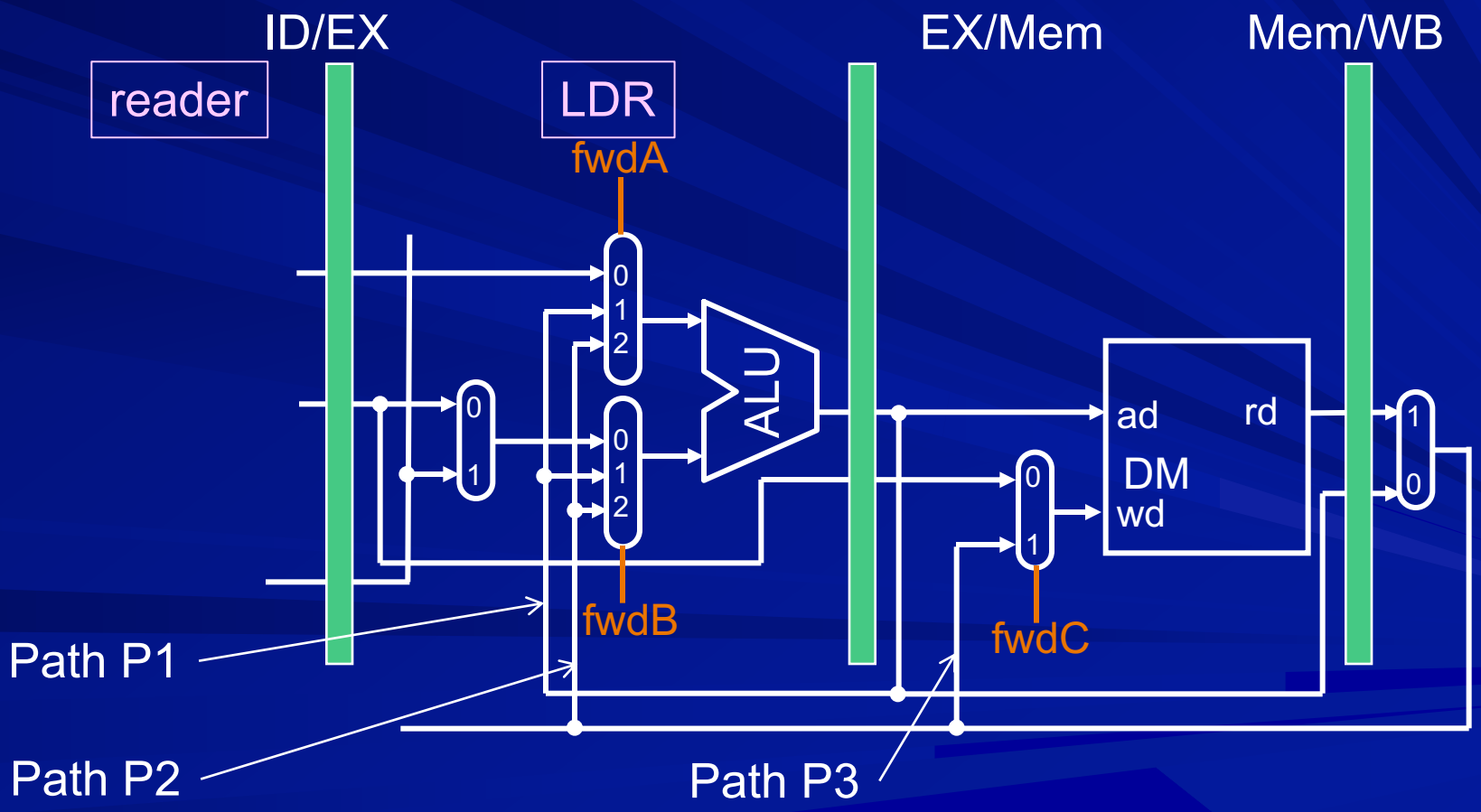
Control for forwarding path P3

fwdC = 1 if
Mem/WB.RW = 1 and
Mem/WB.Rd = EX/Mem.Rd and
EX/Mem.MW = 1



Stalling with data forwarding

ID/EX.MR and
(IF/ID.Rn=ID/EX.Rd or
IF/ID.Rm=ID/EX.Rd)



Thanks