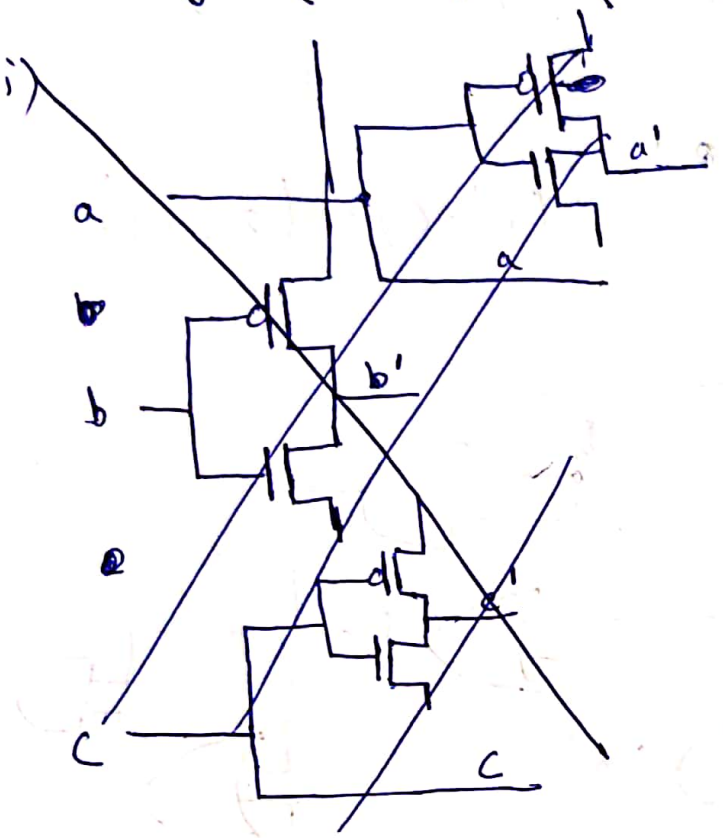
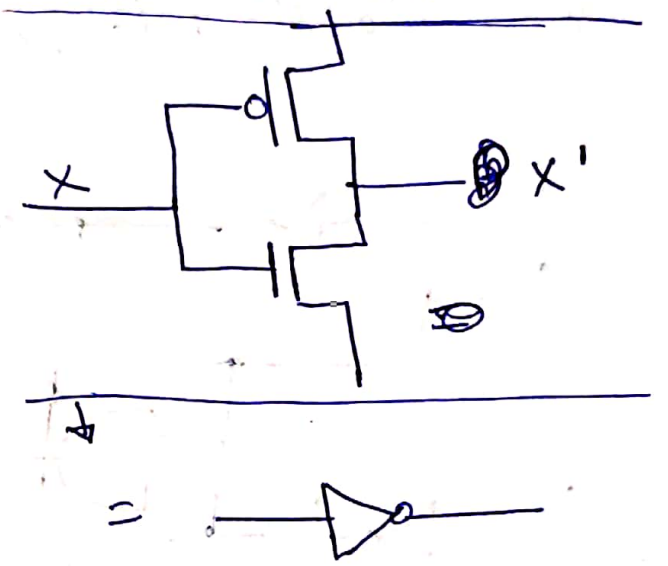
Harshit Mewandia 2020CS10348

Q2) $y = ((a.b') + (a'.c'))'.((b'.c) + (a.c))$

i)

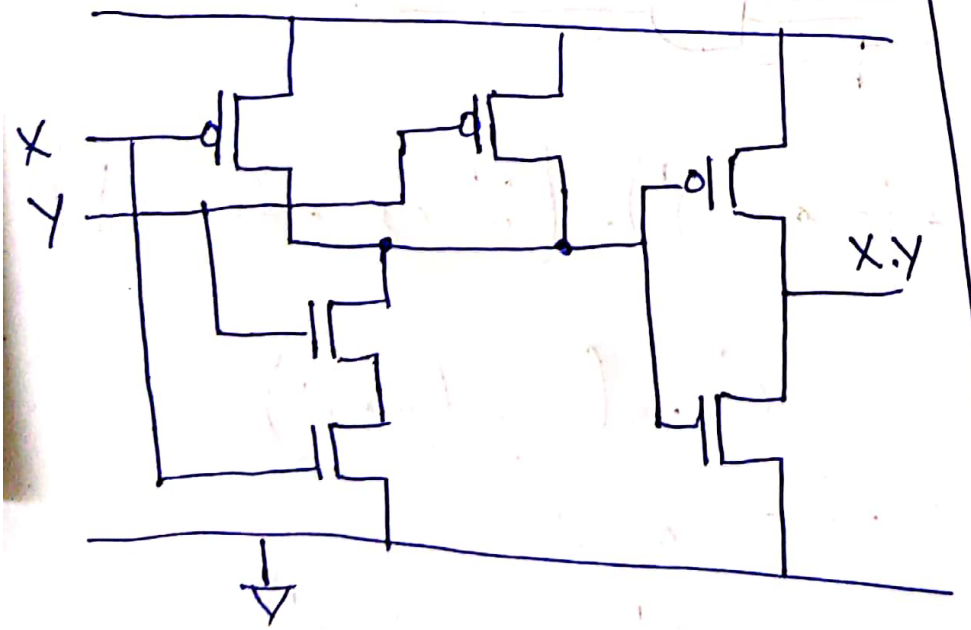


CMOS NOT

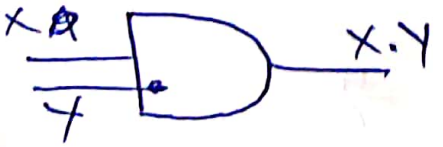


=

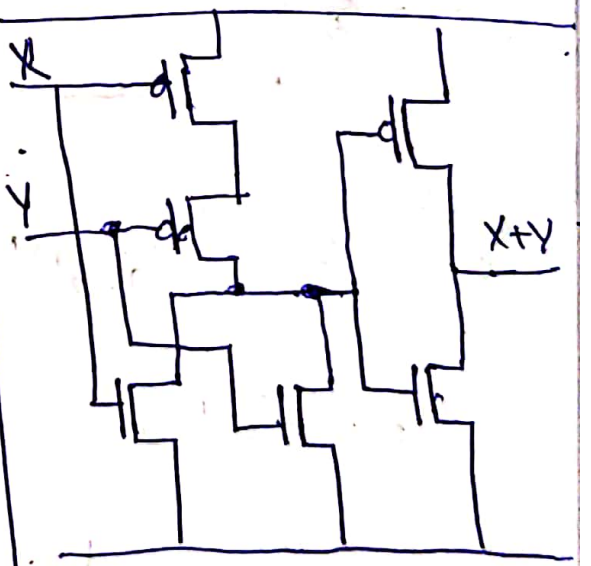
CMOS AND



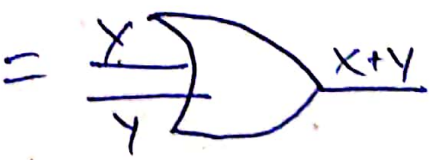
=



CMOS OR



=



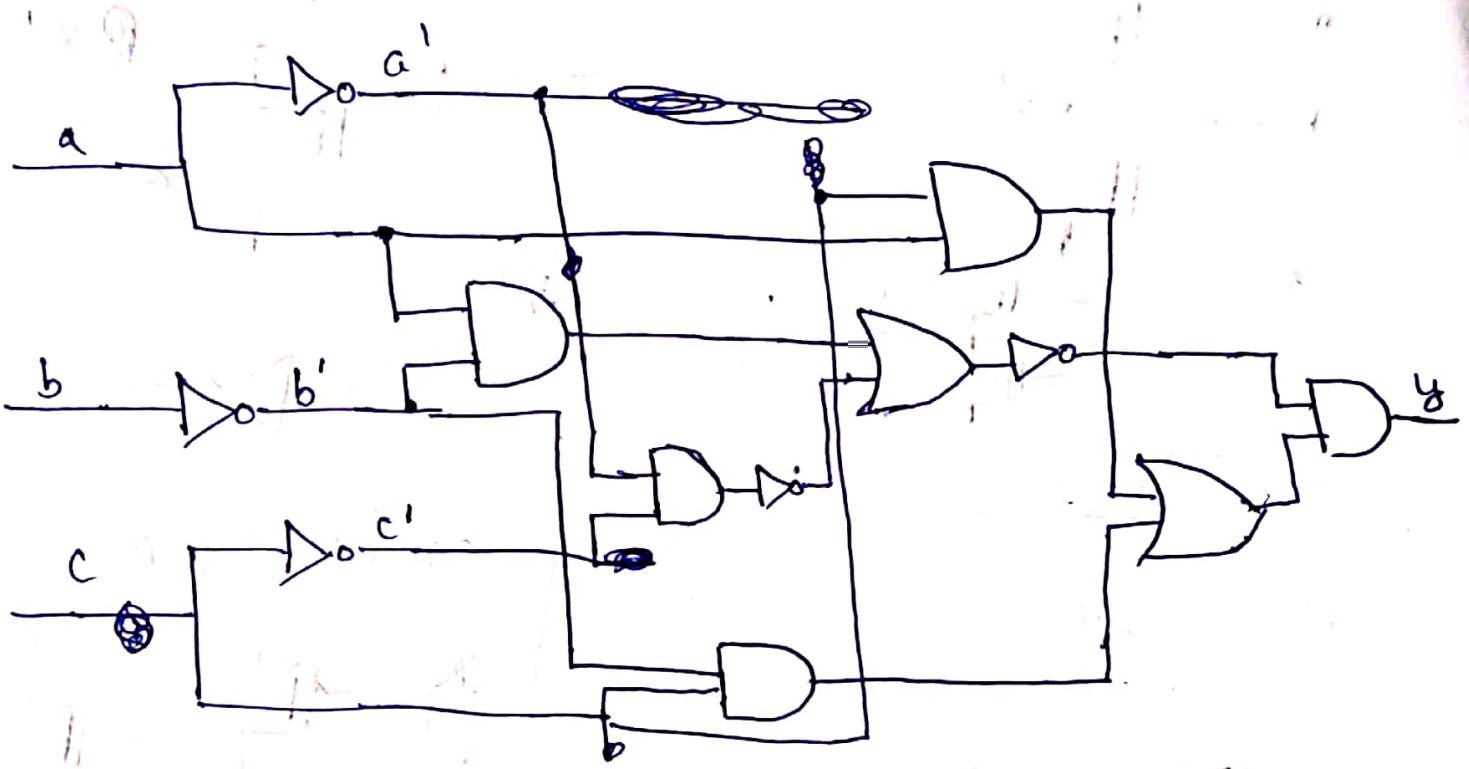
Harshit Mansukhia 2020CS10348 (2)

2)

Now using the given representation for the

a) circuits

$$y = \left((a \cdot b') + (a' \cdot c')\right)' \cdot \left((b' \cdot c) + (a \cdot c)\right)$$

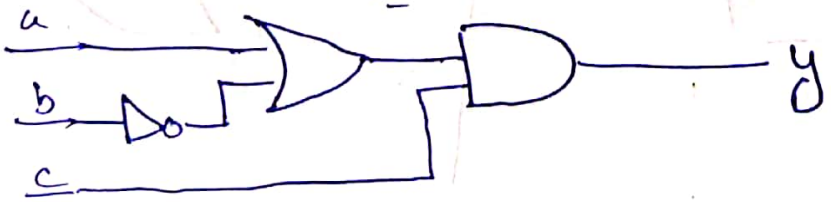


b) $y = \left((a \cdot b')' + (a' + c')'\right) \cdot \left((b' \cdot c) + (a \cdot c)\right)$

$= (a' + b + a + c) \cdot (c \cdot (a + b'))$

$= (1 + b + c) \cdot (c \cdot (a + b'))$

$= c \cdot (a + b')$



Harshit Mawandia 2020CS10348

Q3) $f(a,b,c,d) = \sum m(0,1,3,9) + \sum d(2,11,15)$

ab \ cd	00	01	11	10
00	1	1	1	X
01	0	0	0	0
11	0	0	X	0
10	0	1	X	0

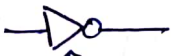
$= a'b' + b'd$

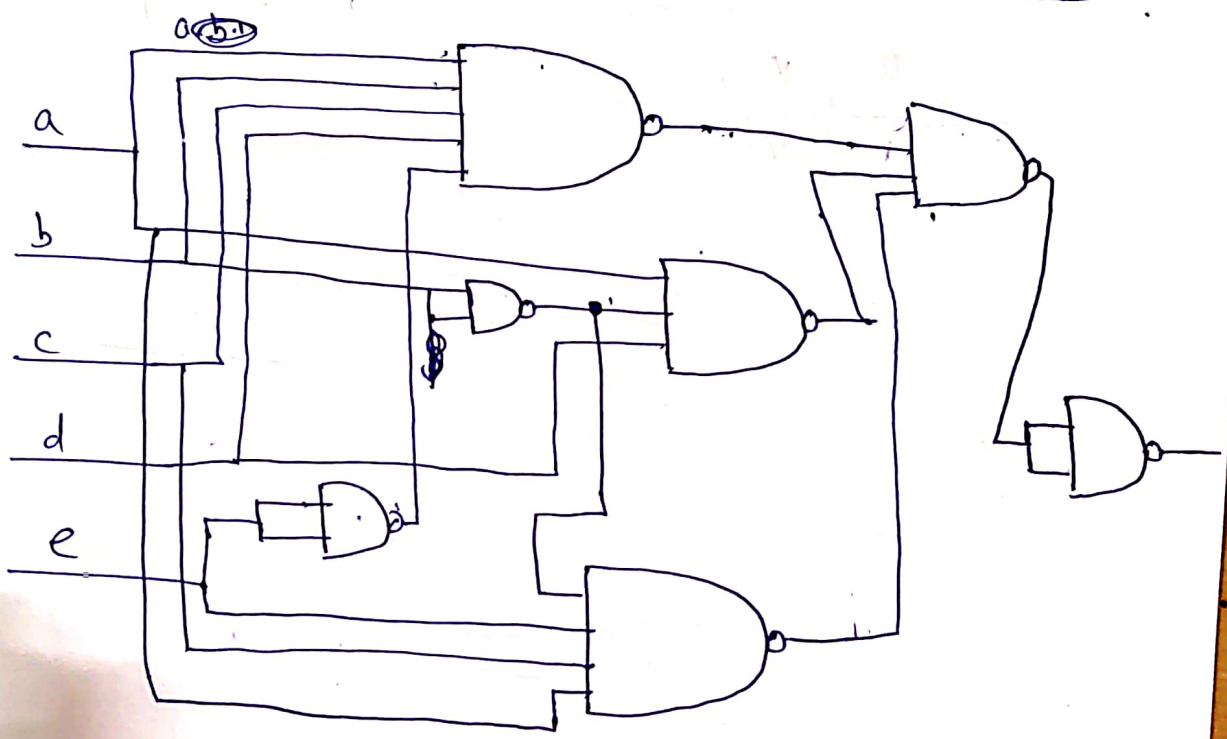
$= b'.(a' + d)$

Harshit Mewandia 2020CS10348 (4)

Q4)

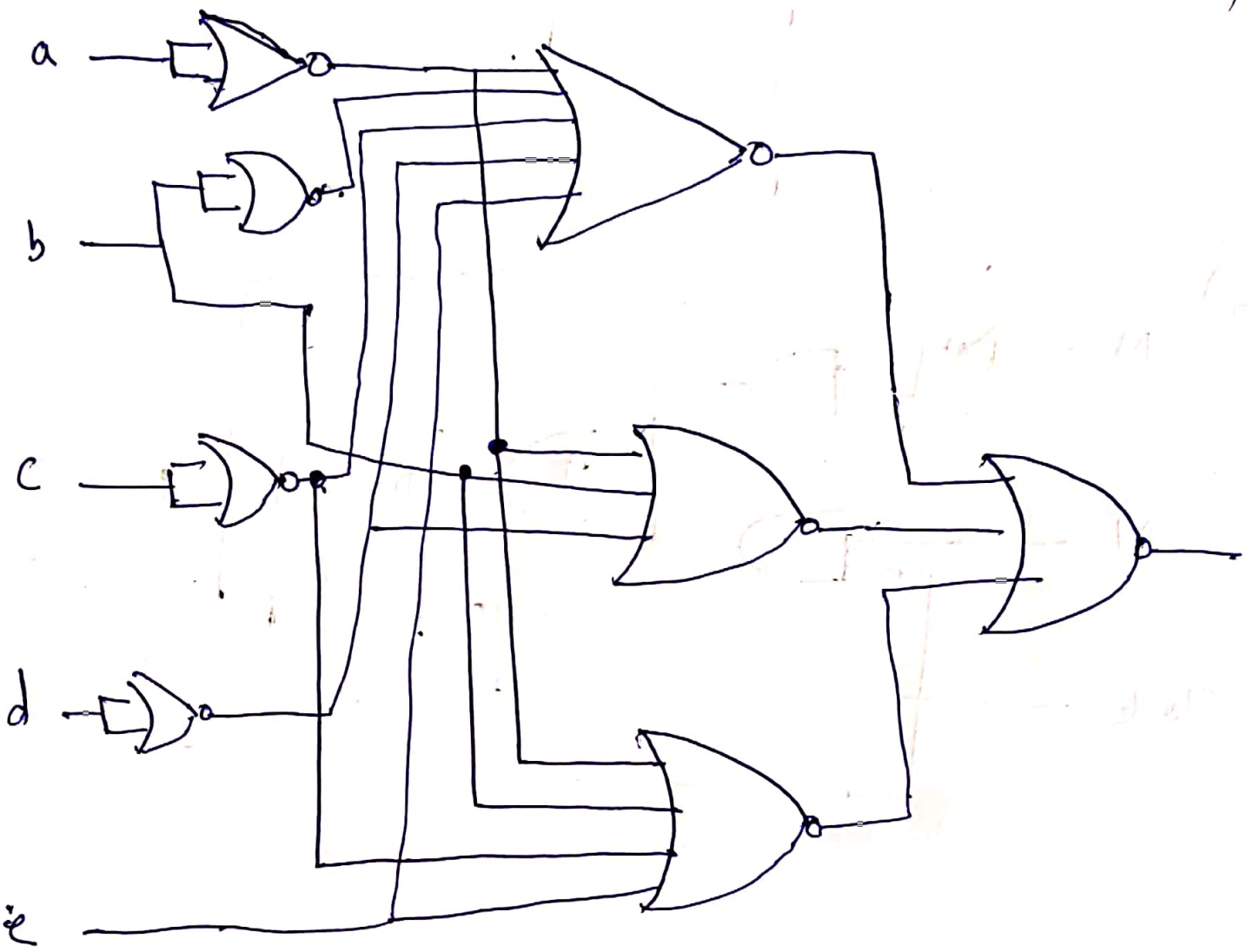
a) $(a' + b' + c' + d' + e) \cdot (a' + b + d') \cdot (a' + b + c' + e)$

b) Let NOT gate be 



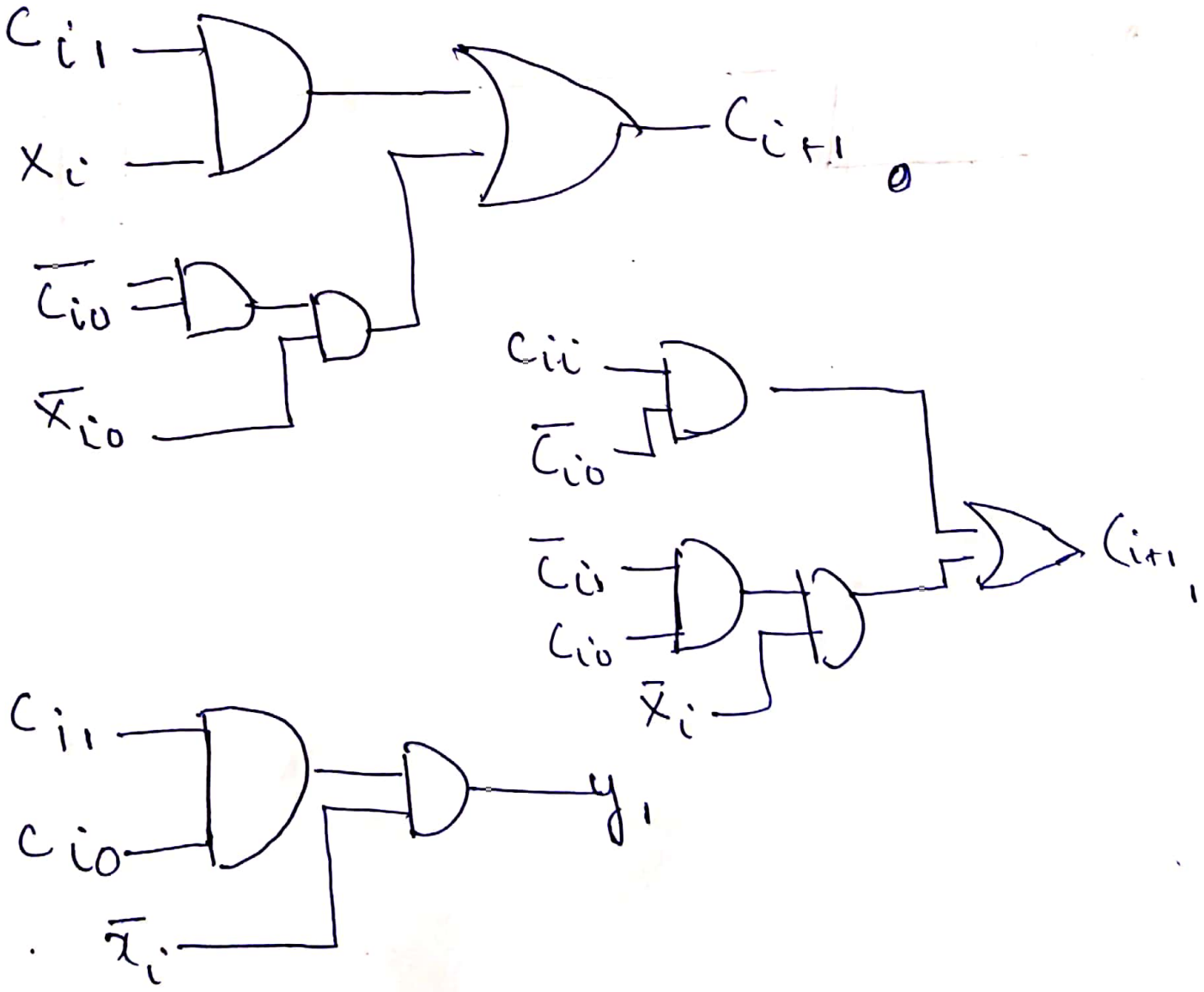
Q4)

c) (a)' + ( )' + ( )')'



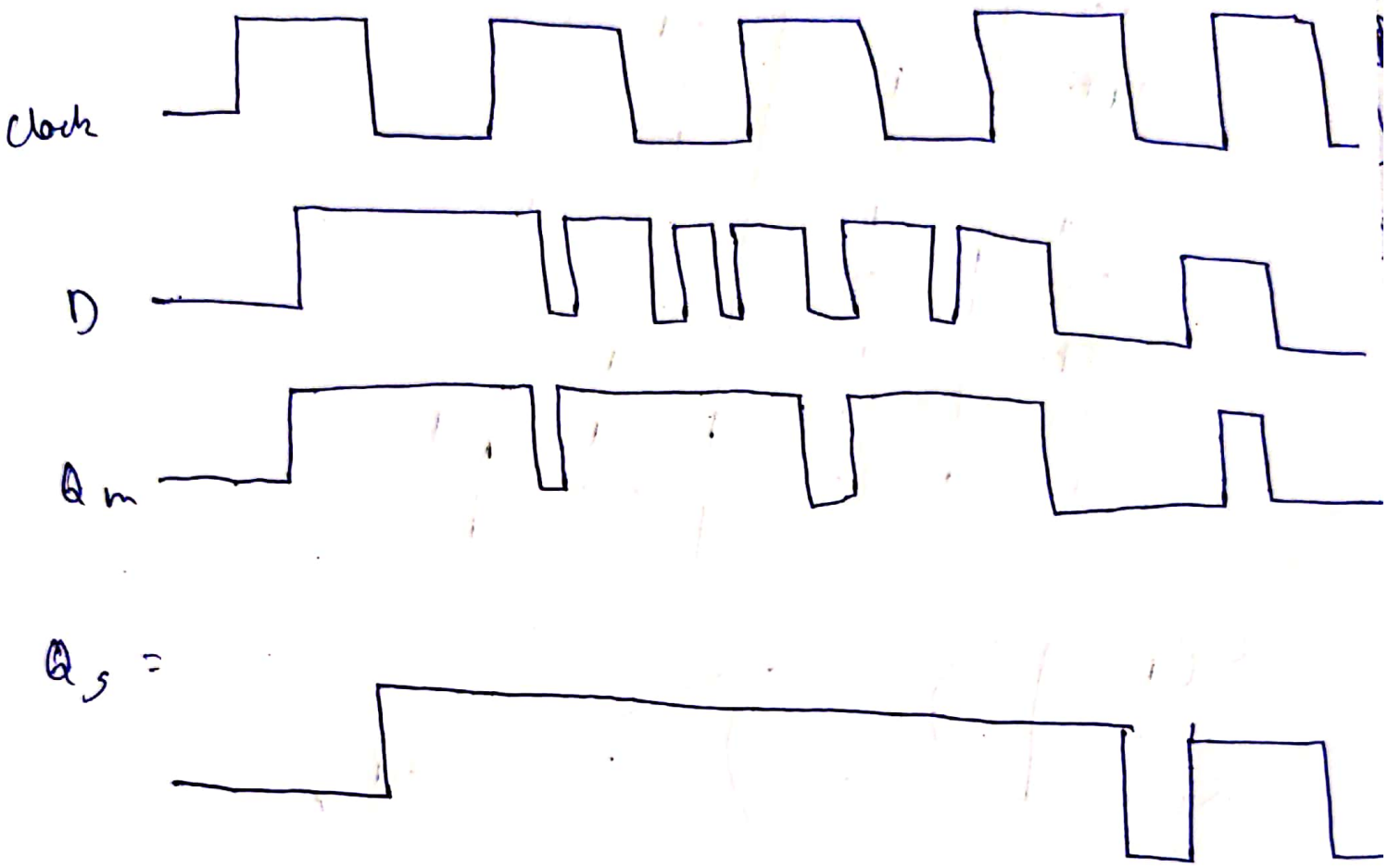
Q6

c_i	x_i	c_{i+1}	y
00	0	01	0
00	1	00	0
01	0	10	0
01	1	00	0
10	0	10	0
10	1	11	0
11	0	01	1
11	1	00	0



Harshit Nawandar 2020CS10345

Q7)



Harshit Mawandia 2020CS10348

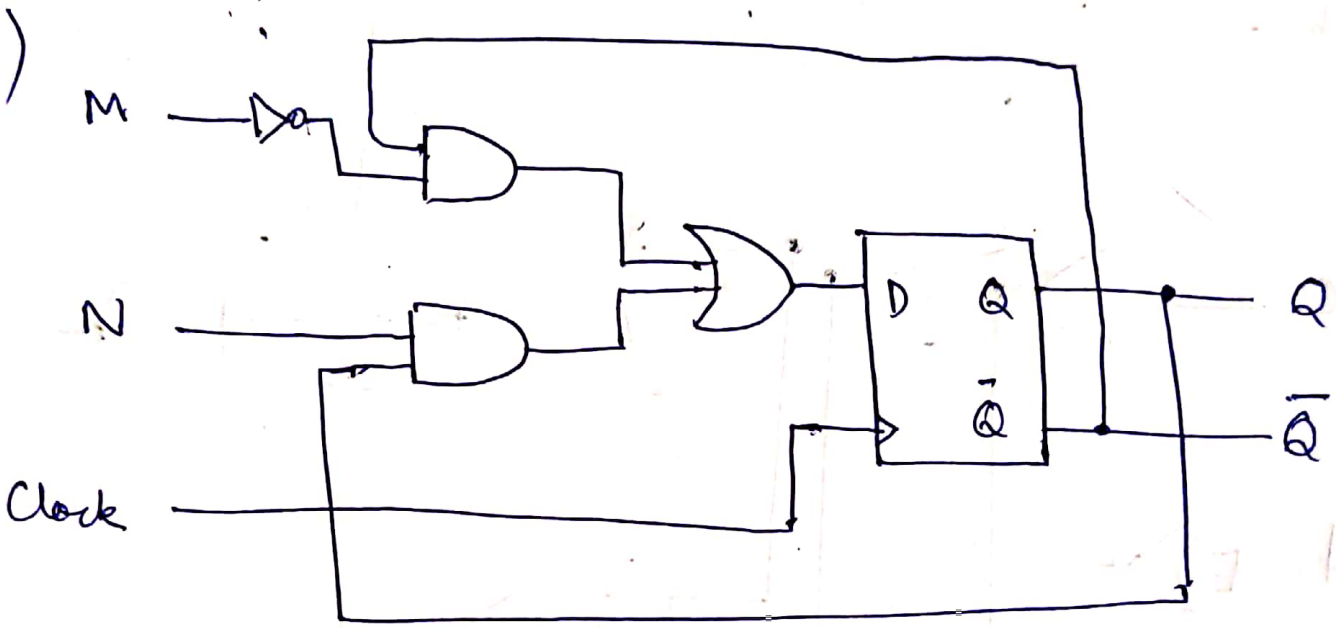
(8)

Q8)

a)

M	N	Q(t+1)
0	0	Q(t)'
0	1	1
1	0	0
1	1	Qt

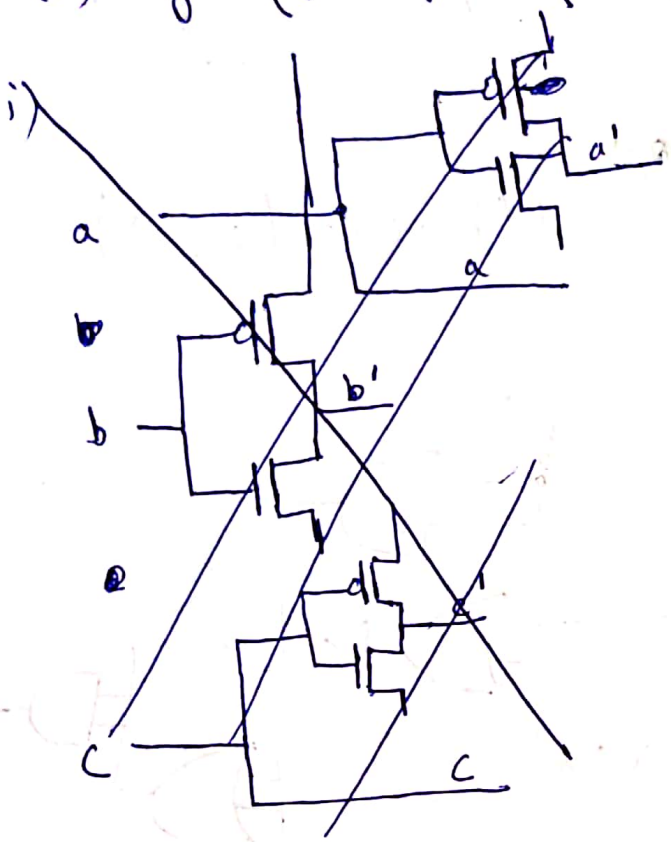
b)



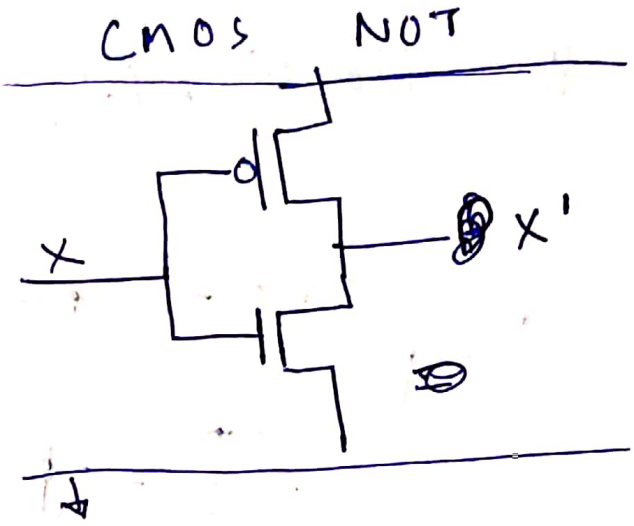
Harshit Mewandia 2020CS10348

Q2) $y = ((a.b') + (a'.c'))'.((b'.c) + (a.c))$

i)

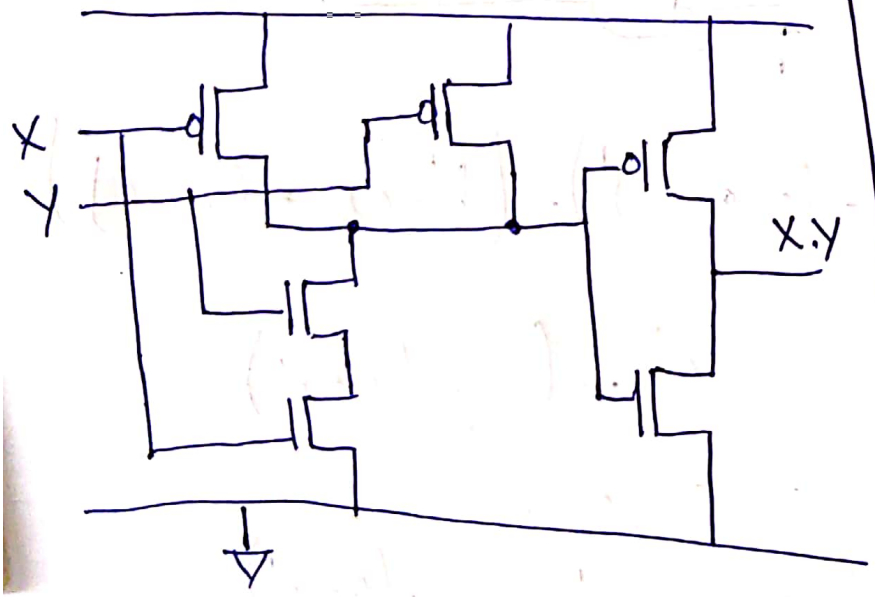


CMOS NOT

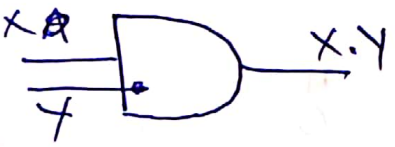


=

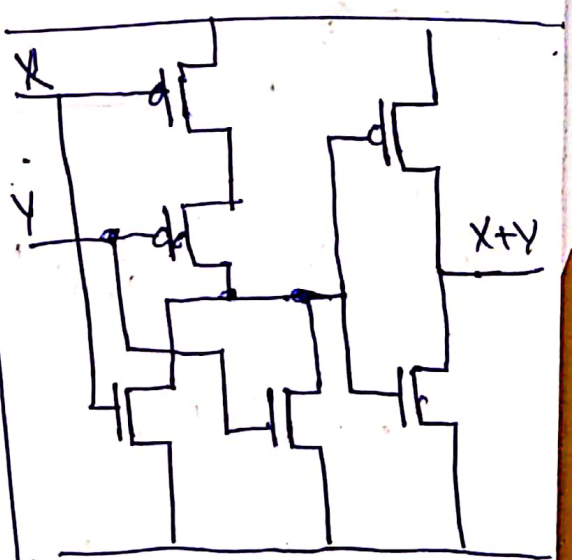
CMOS AND



=



CMOS OR



=