Lecture 25
System Design Case Studies

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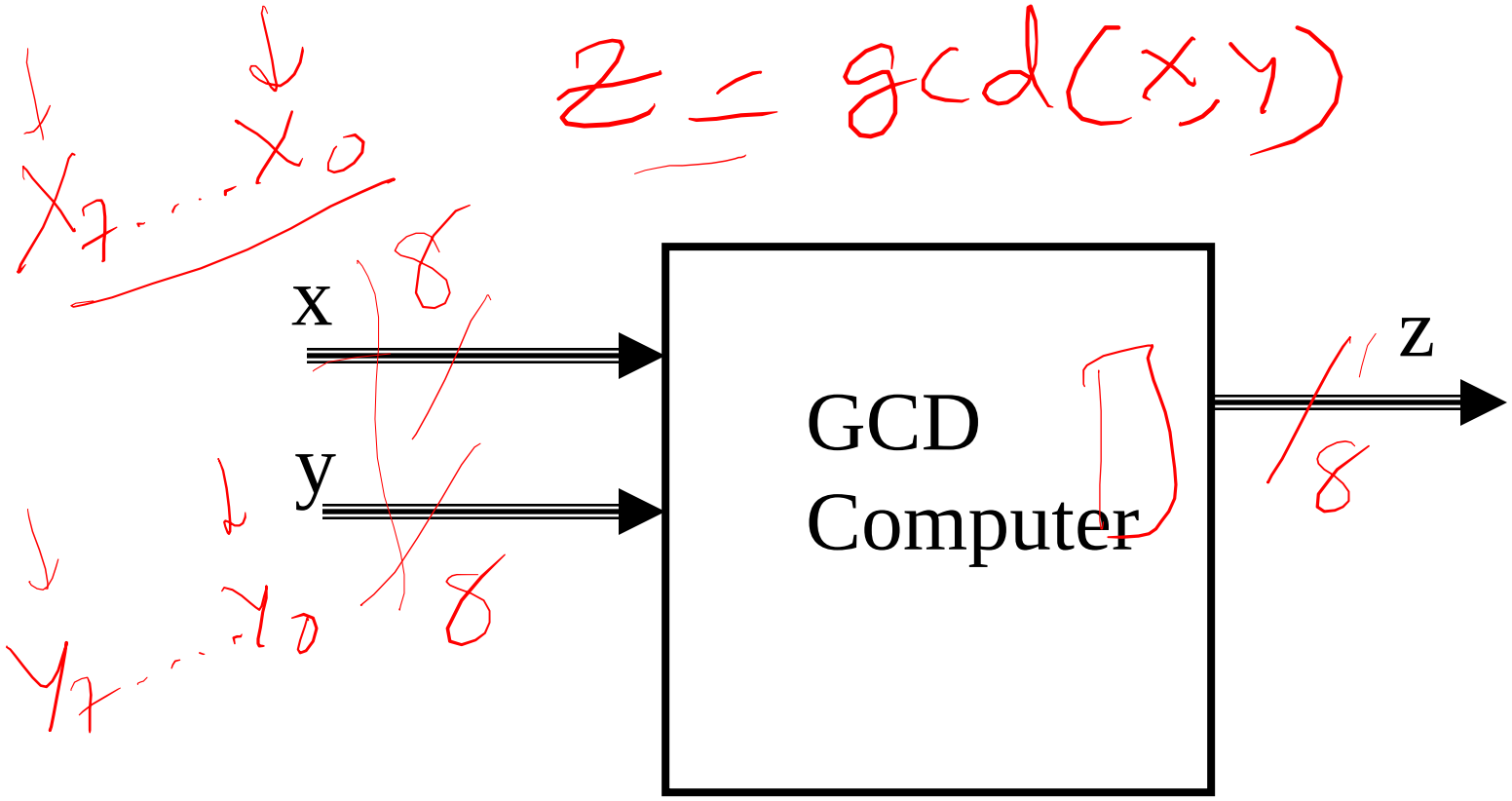
Case Study1: GCD Computer

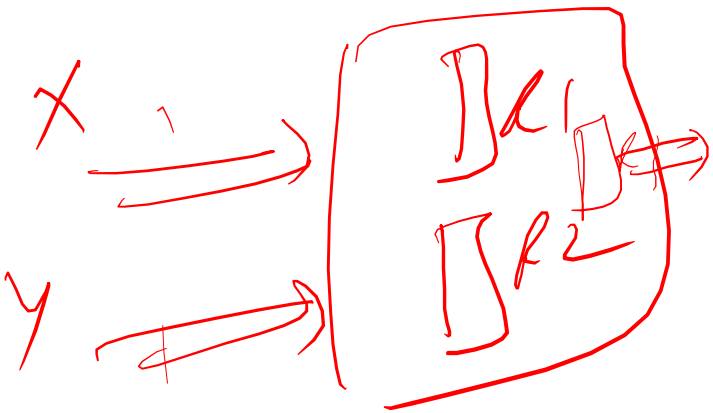


GCD Algorithm

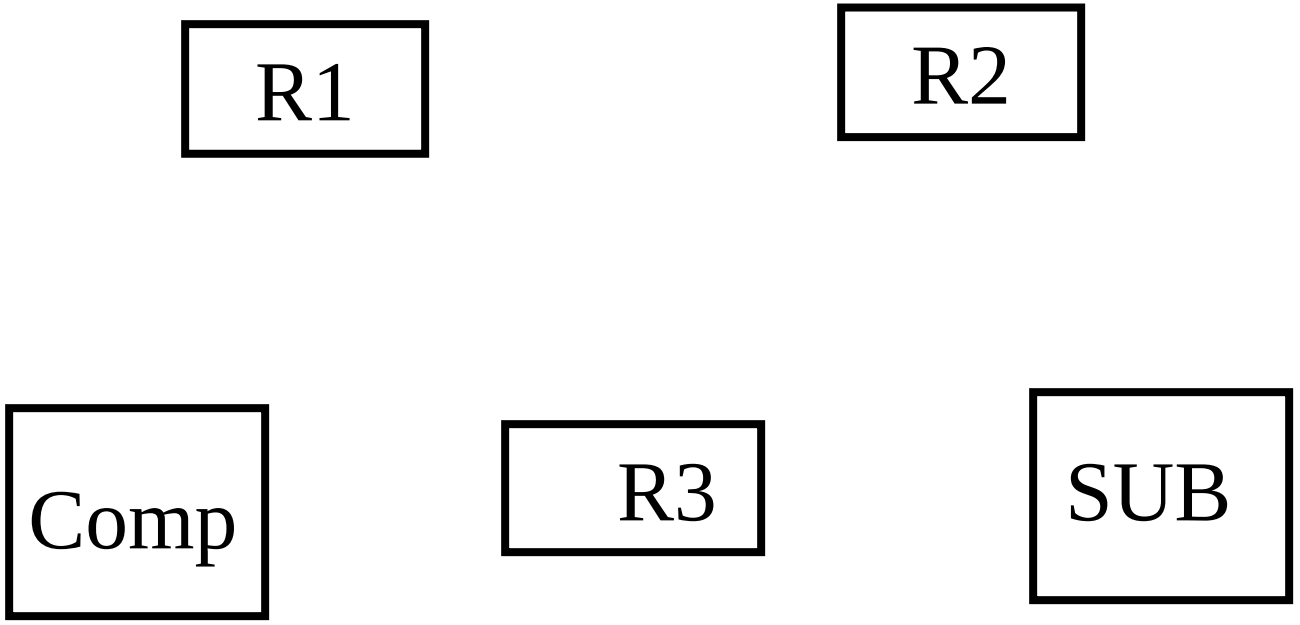
```
Input x, y;
while ( x ≠ y ) do
    if  ( x > y )     then  x := x - y
                      else  y := y - x
    endif;
endwhile;
z := x;
end.
```

Modified GCD Algorithm (RTL)

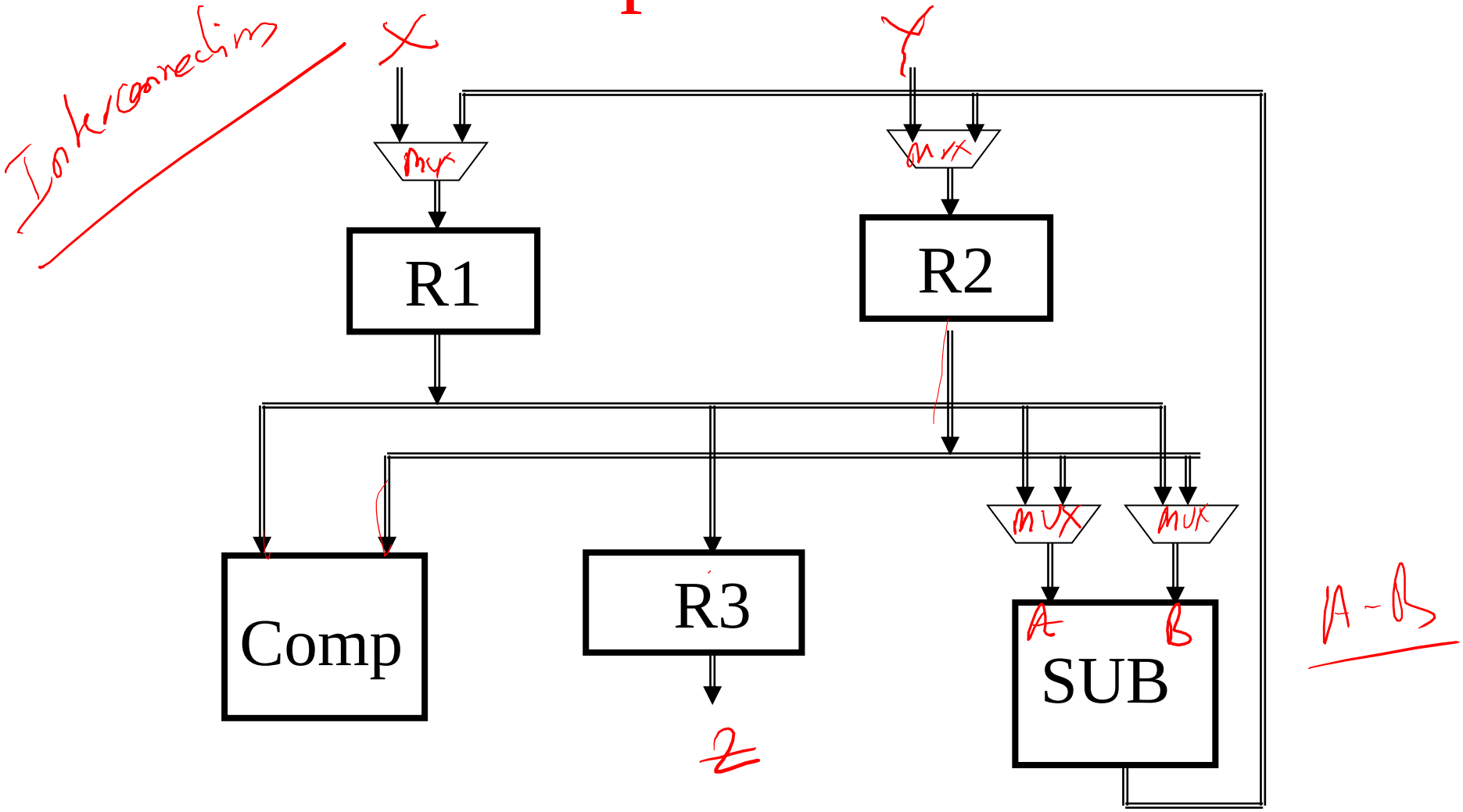
```
S0:R1:= x,  R2:= y;
S1:while ( R1 ≠ R2 ) do
   S2: if ( R1 > R2 )
   S3: then R1:= R1 - R2
   S4: else  R2:= R2 - R1
   endif;
endwhile;
S5: R3:= R1;
```



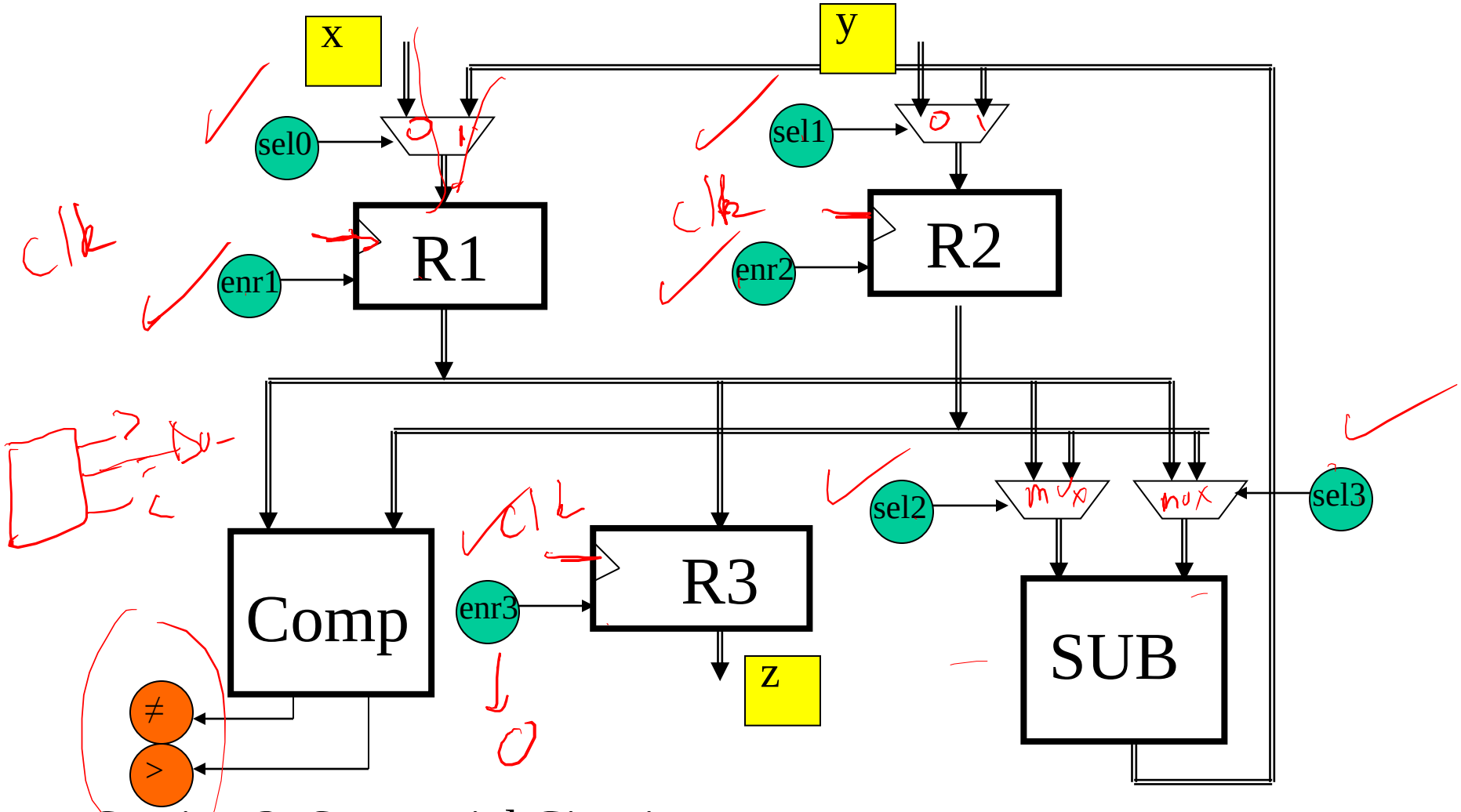
GCD Computer: Data Part



GCD Computer: Data Part



GCD Computer: Data Part



Control Part FSM

S0:R1:= x, R2:= y;

S1:while (R1 ≠ R2) do

S2: if (R1 > R2)

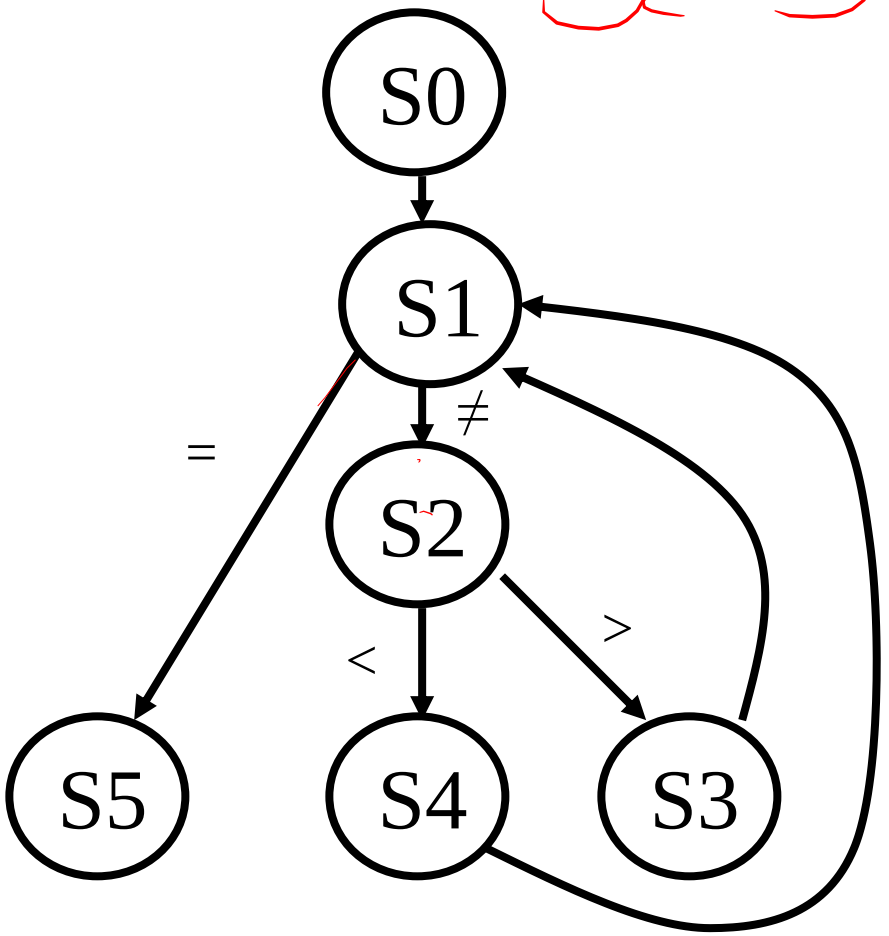
S3: then R1:= R1 - R2

S4: else R2:= R2 - R1

endif;

endwhile;

S5: R3:= R1;



FSM: Control Signals

S0:R1:= x, R2:= y;

S1:while (R1 ≠ R2) do

S2: if (R1 > R2)

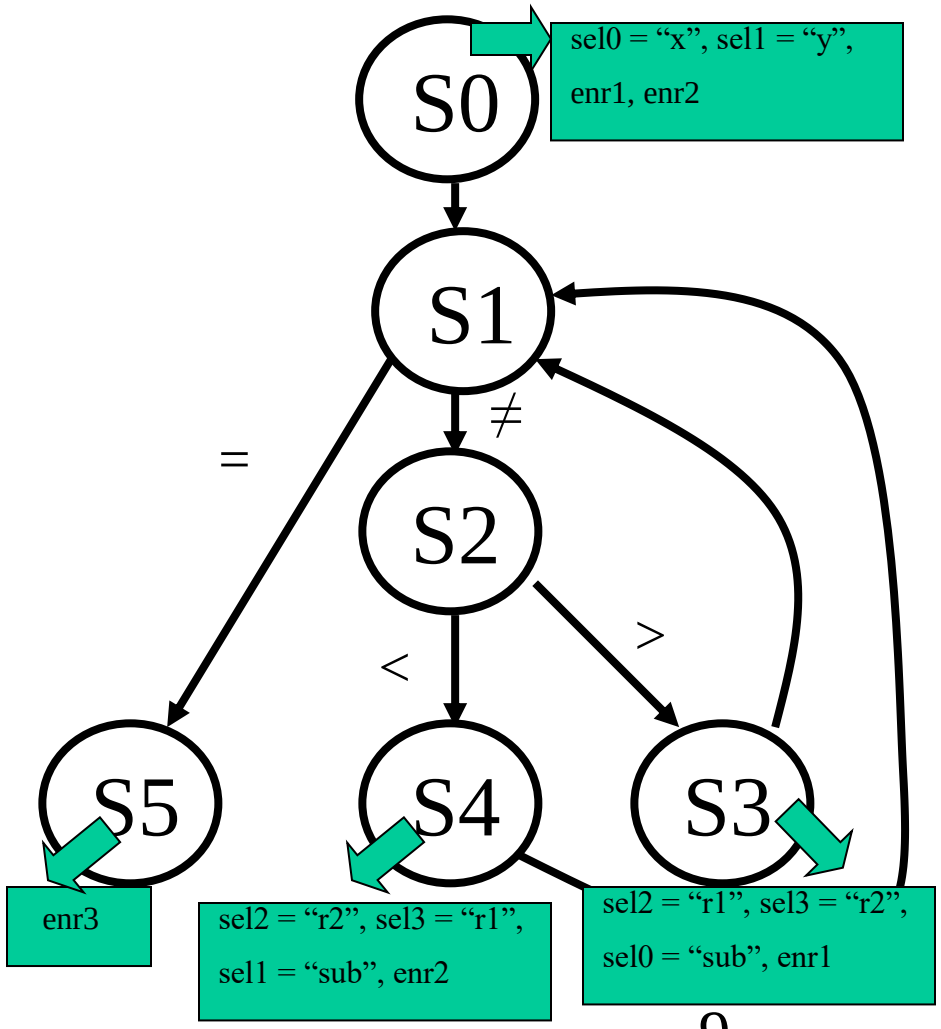
S3: then R1:= R1 - R2

S4: else R2:= R2 - R1

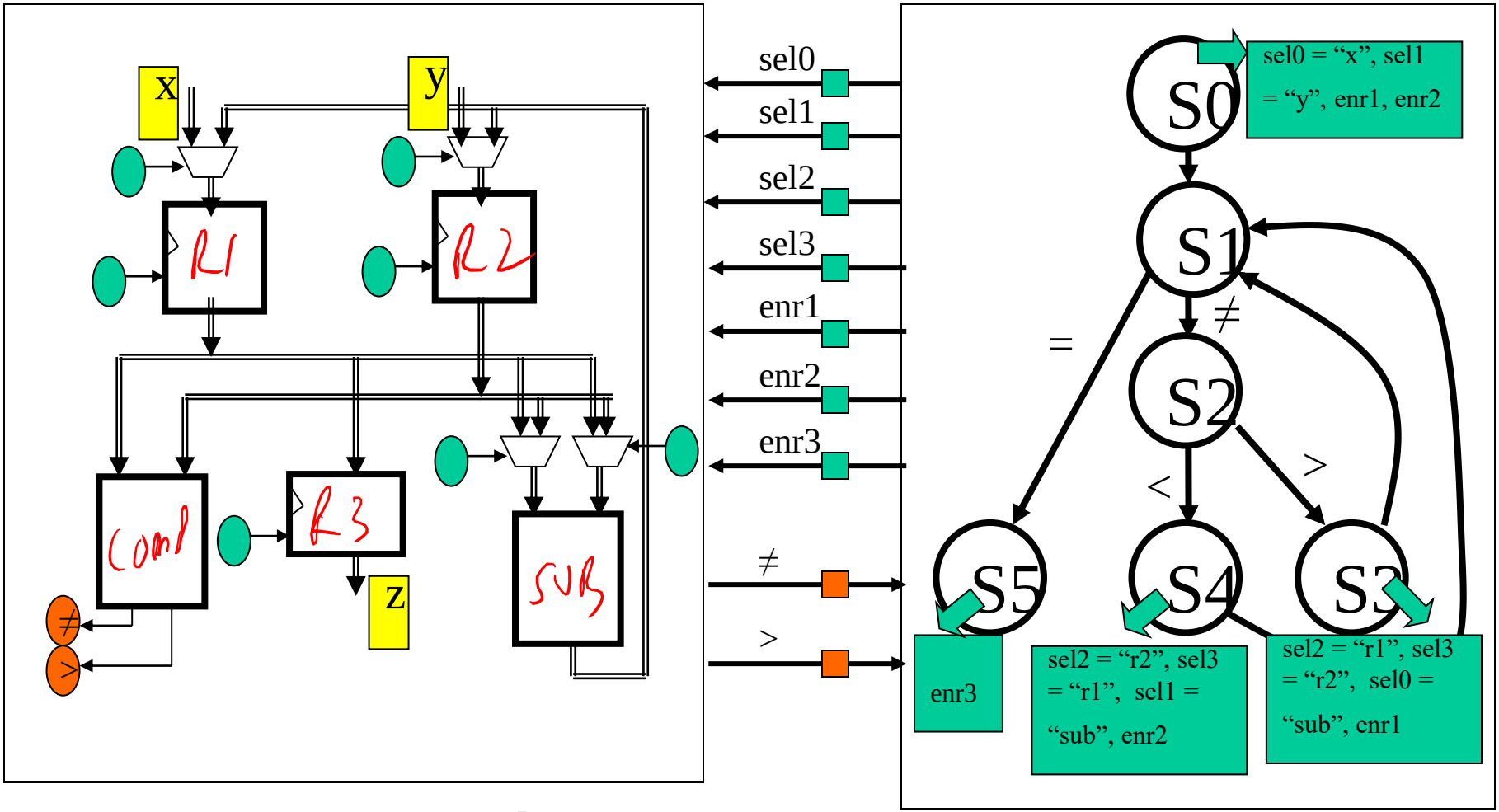
endif;

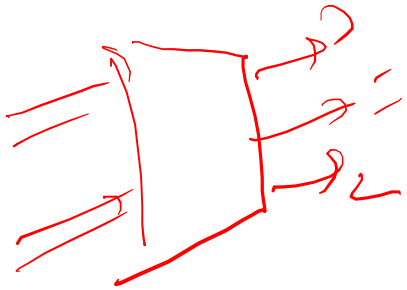
endwhile;

S5: R3:= R1;



Data-Control Interface





Modified RTL + FSM

S0:R1:= x, R2:= y;

S1: Case (R1 “Compare” R2)

S2: “>” R1:= R1 - R2,

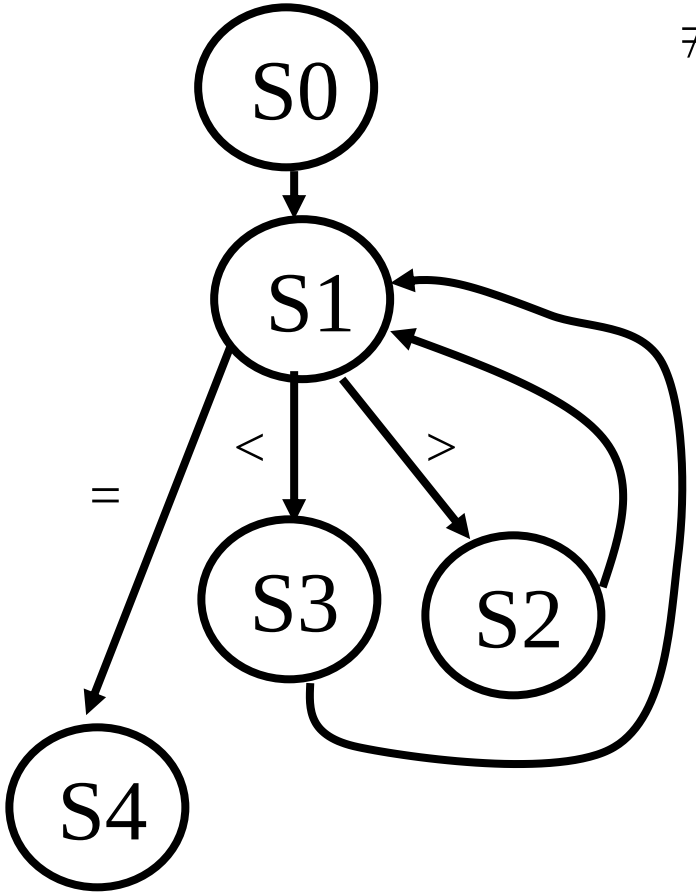
go to S1;

S3: “<“ R2:= R2 - R1,

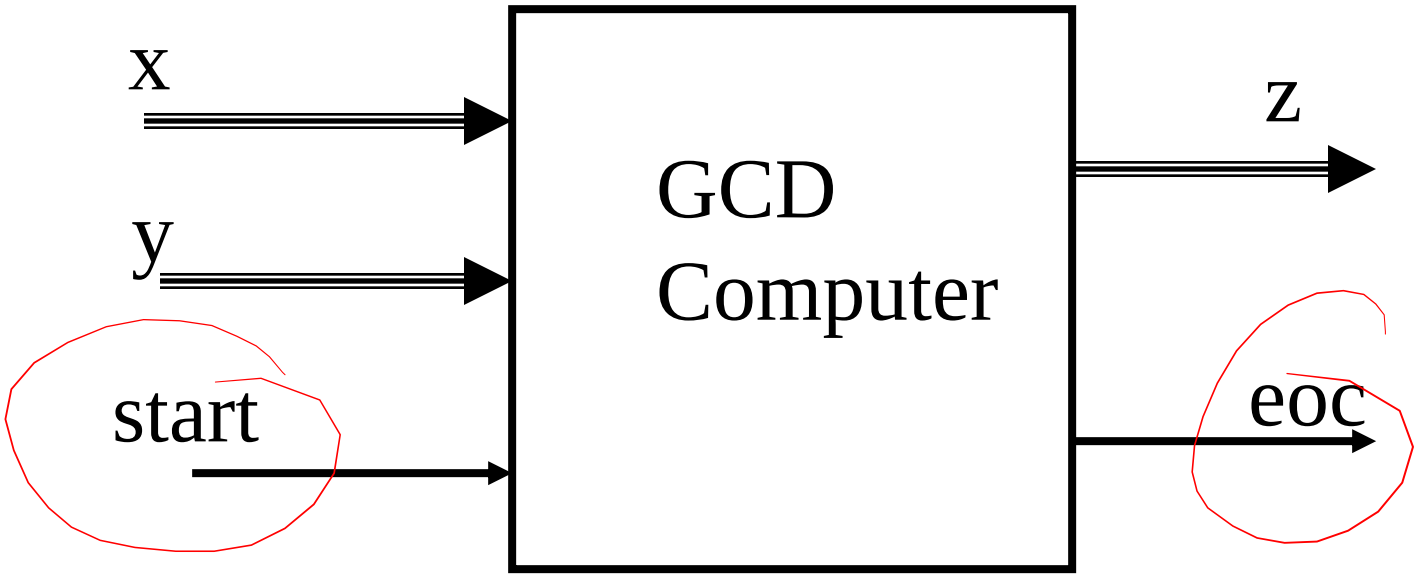
go to S1

S4: “=“ R3:= R1;

endcase;



GCD Computer: Interface



Modified FSM

Si: wait for “start”

S0: R1:= x, R2:= y, eoc := “0”;

S1:while (R1 ≠ R2) do

S2: if (R1 > R2)

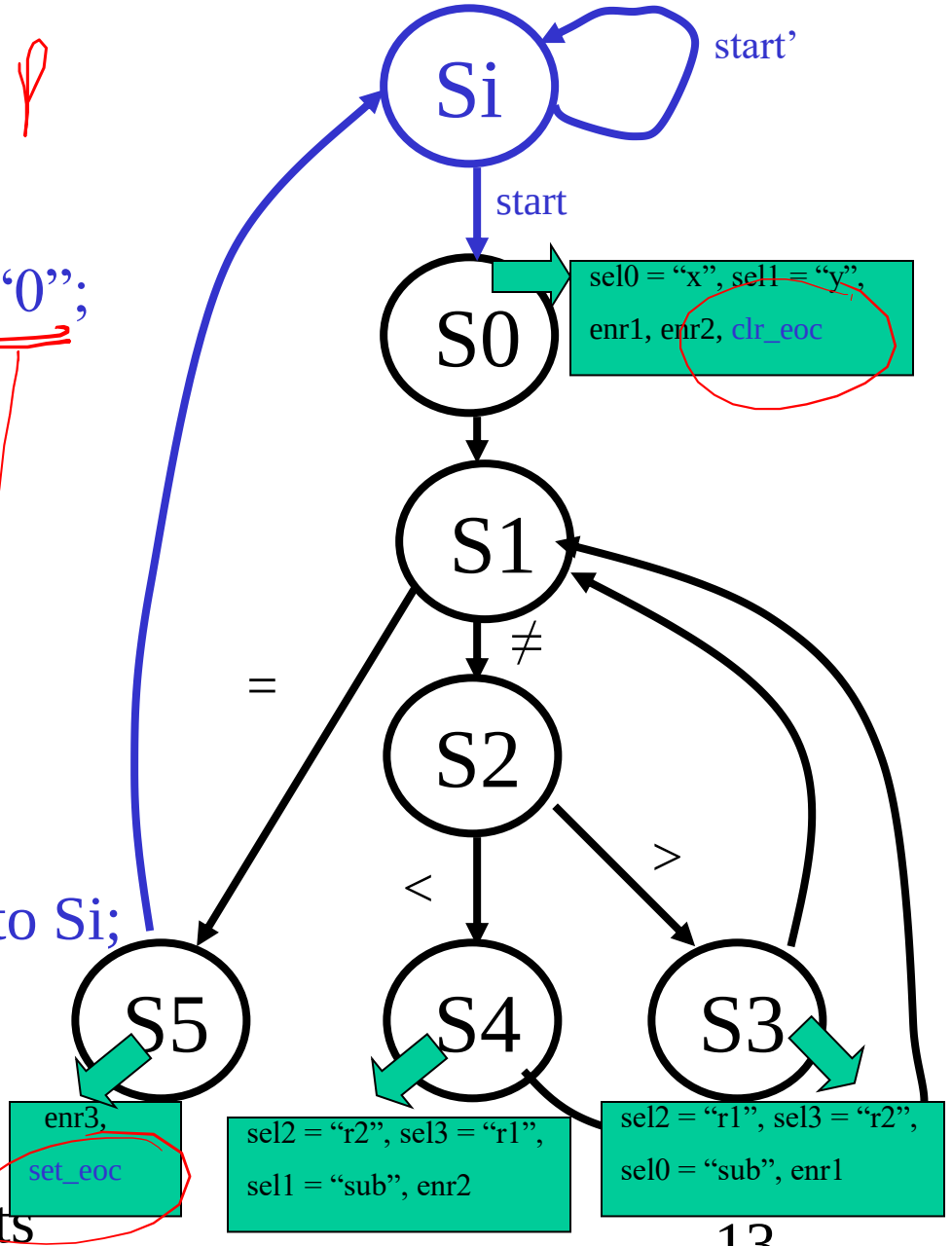
S3: then R1:= R1 - R2

S4: else R2:= R2 - R1

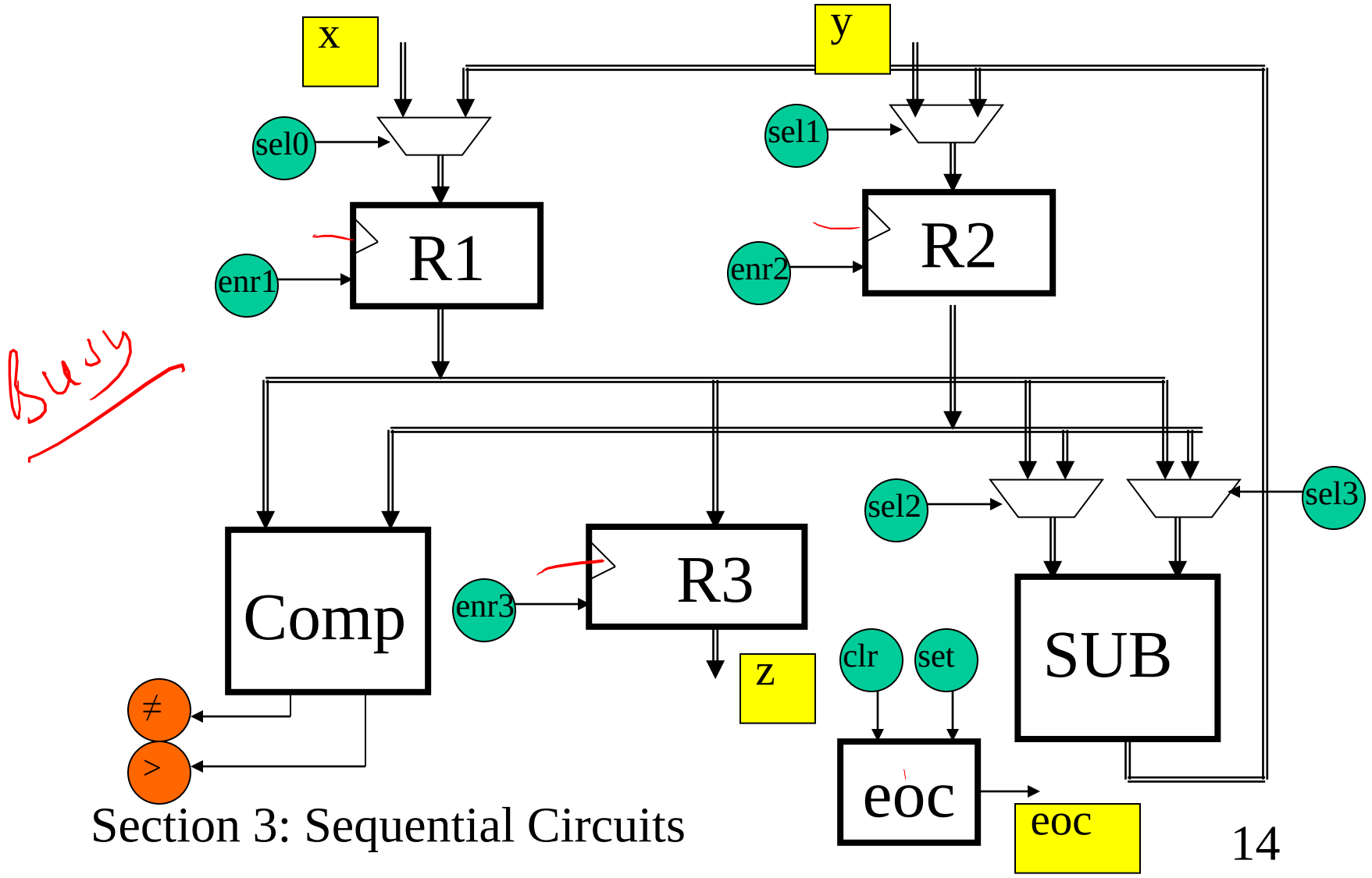
endif;

endwhile;

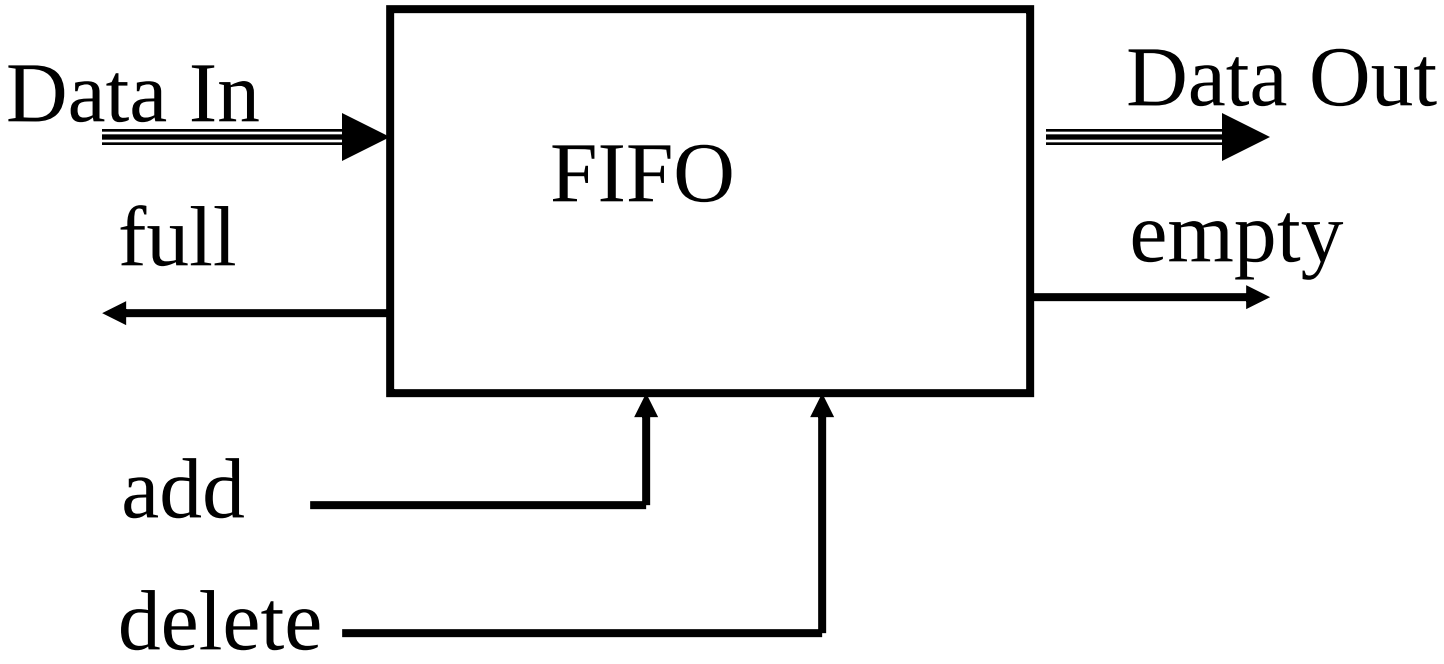
S5: R3:= R1, eoc := “1”, goto Si;



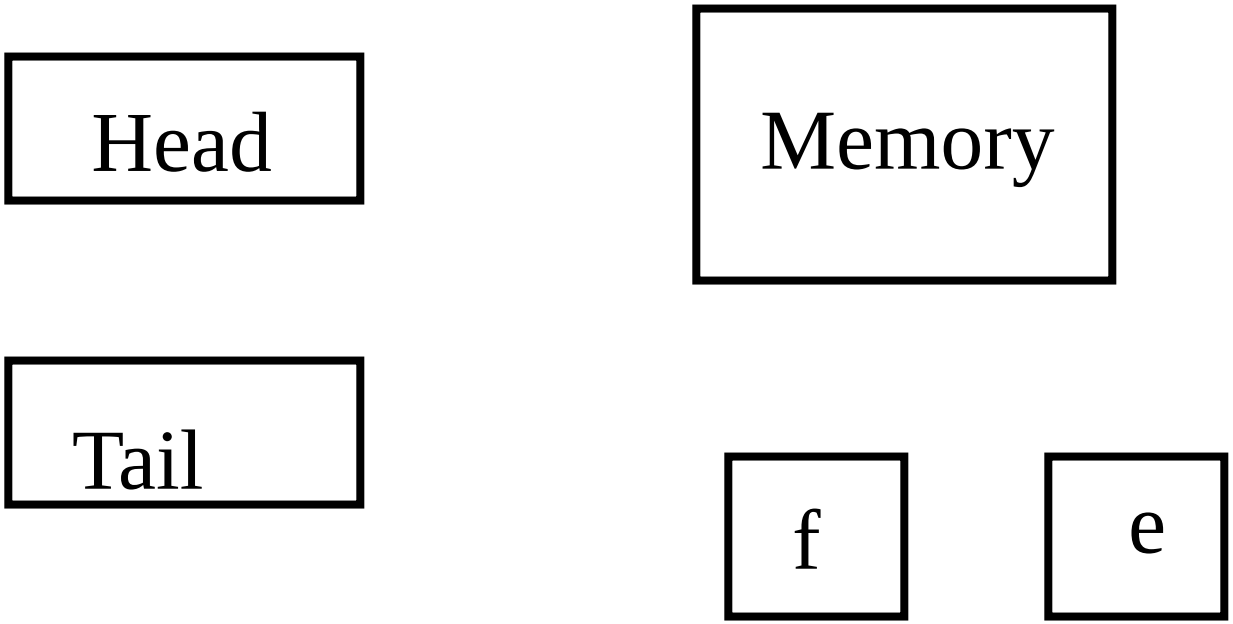
GCD Computer: Data Part



Case Study 2: FIFO



FIFO: Data Part



FIFO: RTL

Si: head := “0”, tail := “0”, full := “0”, empty := “1”;

S0: If (add and full’) then

S1: mem(head) := data_in;

S2: head := head +1;

S3:: full := (head = = tail); go to S0;

S4: else if (delete and empty’) then

S5: tail := tail + 1;

S6: data_out:= mem(tail);

S7: empty := (head = = tail); go to S0;

Design Problem

Design a system which uses GCD module and multiple FIFO modules. An array of numbers are stored in a memory and GCD of these numbers is to be computed and stored back into the memory. FIFO buffers are used to supply the inputs to the GCD module and take the outputs from the GCD module.