COL215L: Digital Logic & System Design

Lecture 21: Finite State Machines (Cont.)

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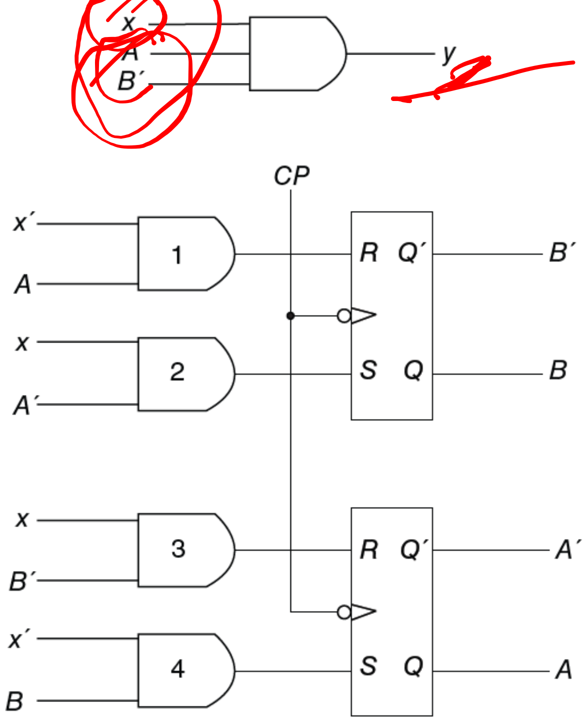
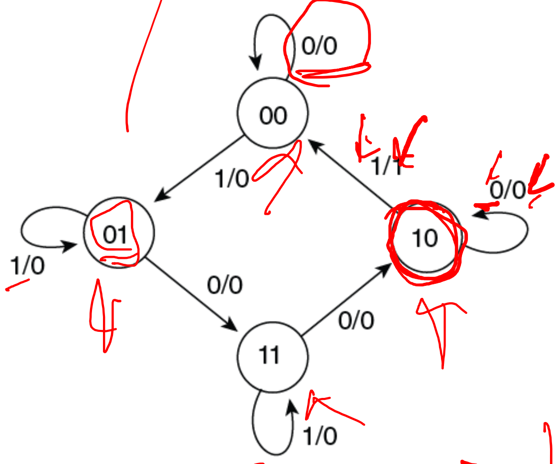
Circuit, State Table and State Diagram

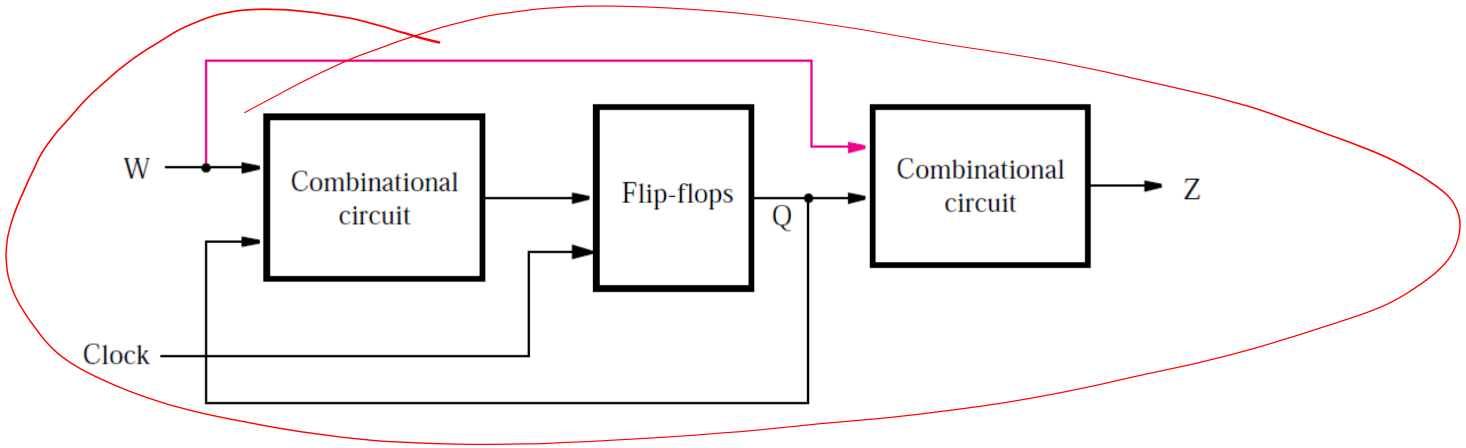


Present State	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	AB	AB	y	y
00	00	01	0	0
01	11	01	0	0
10	10	00	0	1
11	10	11	0	0



Finite State Machine

- Circuits that can be represented with finite number of states
  - Output – Present State with/without Input
- Output
  - Present State - Moore type
  - Present State & Inputs – Mealy type



Design Steps

1. Specification
2. State Diagram
3. State Table
4. State Assignment (Minimize States)
5. Select Flip-Flop and Implement Circuit

Inputs & output → condition

A, B, C, D, E

000

1011

000
001
010
110

8 state

0
1
2
3

2 bit

Step-1: Specification

Example

Mealy

Moo

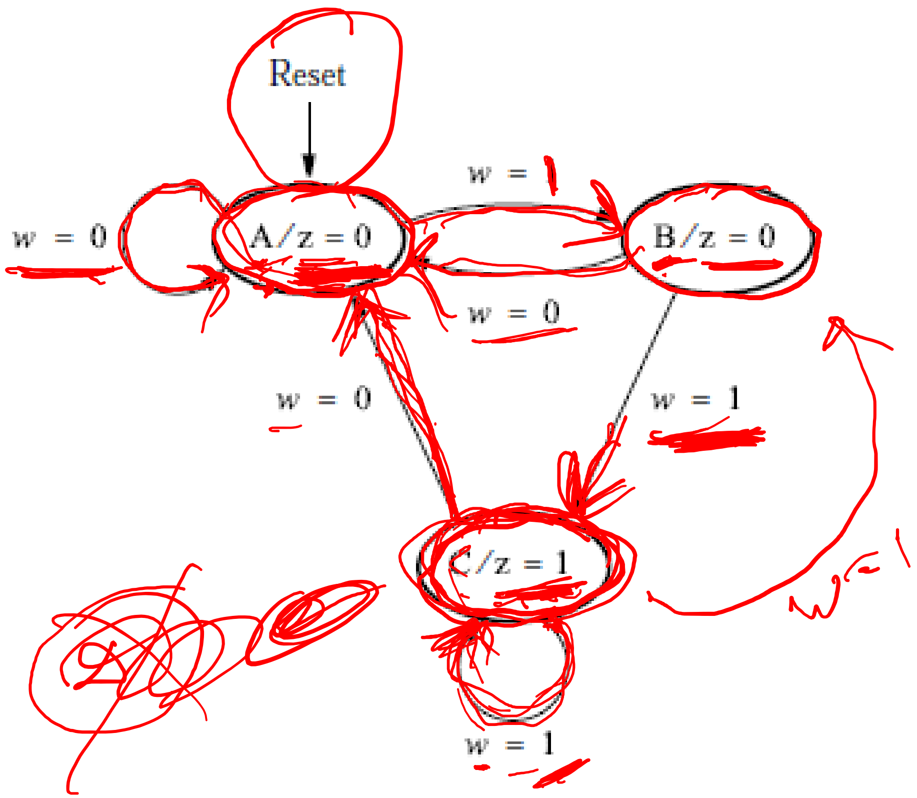
- one input, w
- one output, z
- Recognize the pattern 11
  - If $w_{i-1} = 1$ and $w_{i} = 1$, $z_{i+1} = 1$
  - Otherwise, $z_{i} = 0$

$\boxed{z_{i} = 1}$

Step-2: State Diagram

Reset

w → 0 0 0 0 0 0



Moore

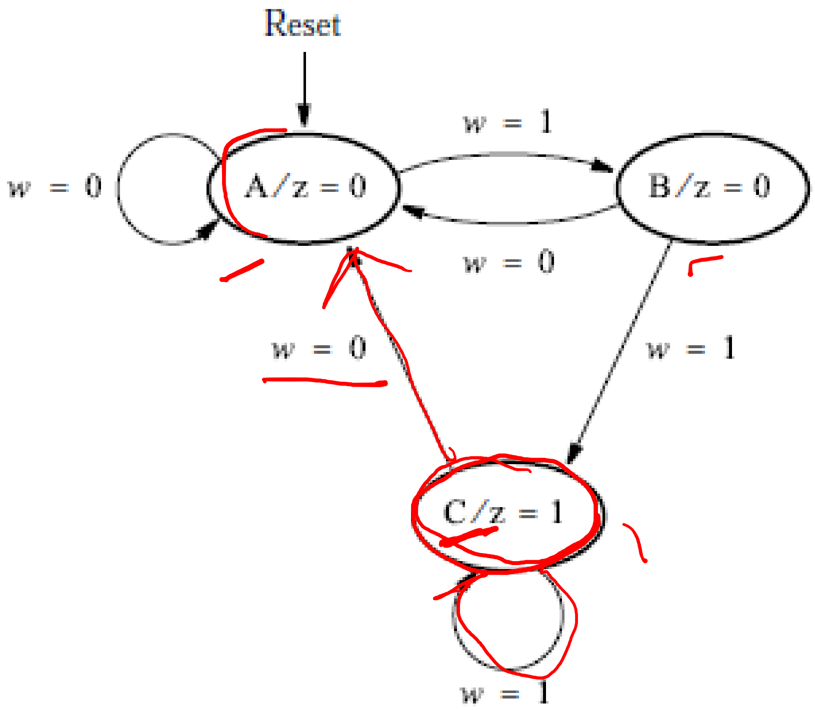
{ Output → Present state }

$w_{i-1}=1$

$w_i=1$

$\boxed{z_{i+1}=1}$

Step-3: State Table



Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	A	B	0
B	A	C	0
C	A	C	1

Step-4: State Assignment

Present state	Next state		Output
	$w = 0$	$w = 1$	z
$y_2 y_1$	$Y_2 Y_1$	$Y_2 Y_1$	
A 00	00	01	0
B 01	00	10	0
C 10	00	10	1
11	dd	dd	d

Step-5: Circuits

Flip

$Y_2 = w(y_1 + y_2)$

$Y_1 = w y_2' y_1'$

$z = y_2$

$y_2 y_1 w$

	Present state	Next state		Output
		$w = 0$	$w = 1$	
	$y_2 y_1$	$Y_2 Y_1$	$Y_2 Y_1$	z
A	00	00	01	0
B	01	00	10	0
C	10	00	10	1
	11	dd	dd	d

Y_1

$w \backslash y_2 y_1$	00	01	11	10
0	0	0	d	0
1	1	0	d	0

Y_2

$w \backslash y_2 y_1$	00	01	11	10
0	0	0	d	0
1	0	1	d	1

z

$y_2 \backslash y_1$	0	1
0	0	0
1	1	d

Step-5: Circuits (Cont.)