COL215L: Digital Logic & System Design

Lecture 18: Sequential Circuits (Cont.)

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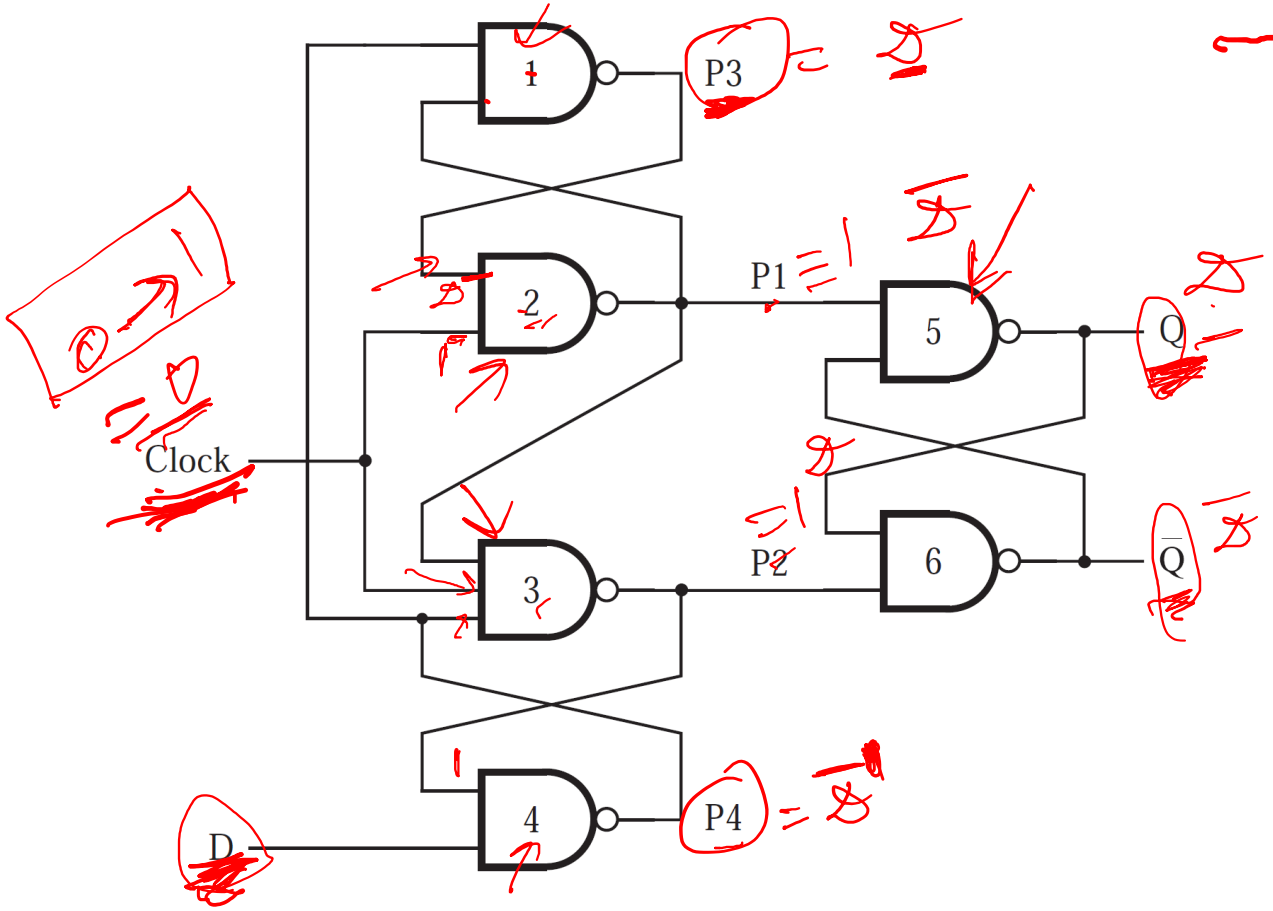
Sequential Circuits (Revision)

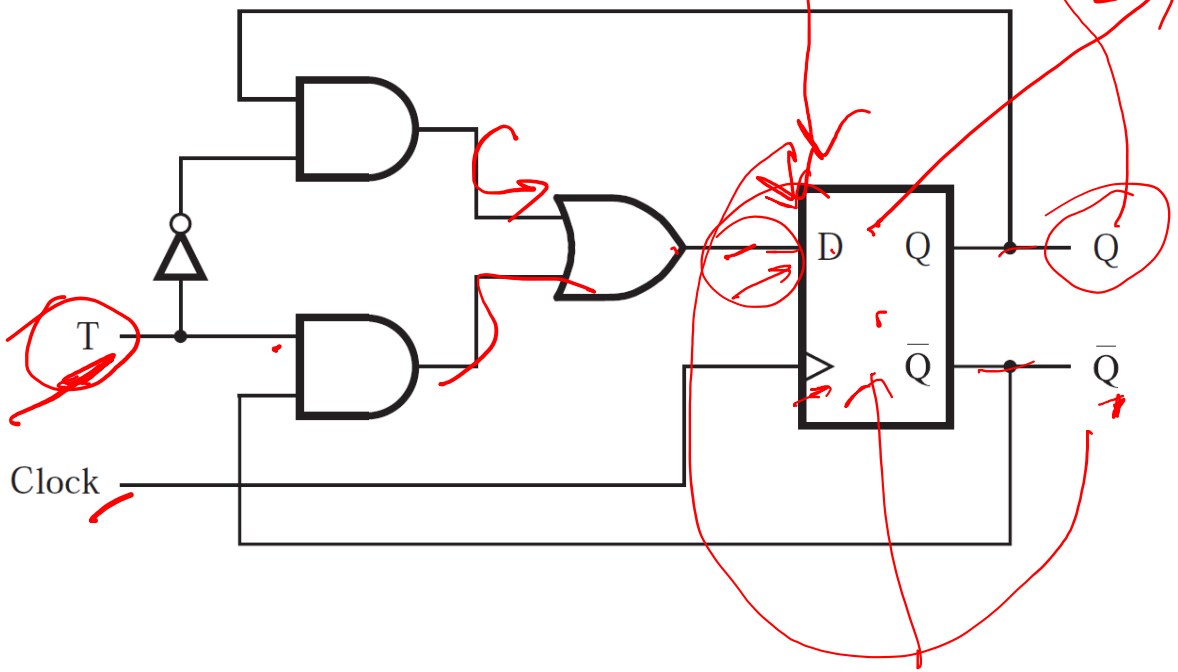
- Level Sensitive
  - SR Latch
  - Gated SR Latch
  - Gated D Flip-Flop

- Edge-Triggered
  - Master-Slave D Flip-Flop
    - Clock
    - Clock’

Edge-Triggered D Flip-Flop



T Flip-Flop

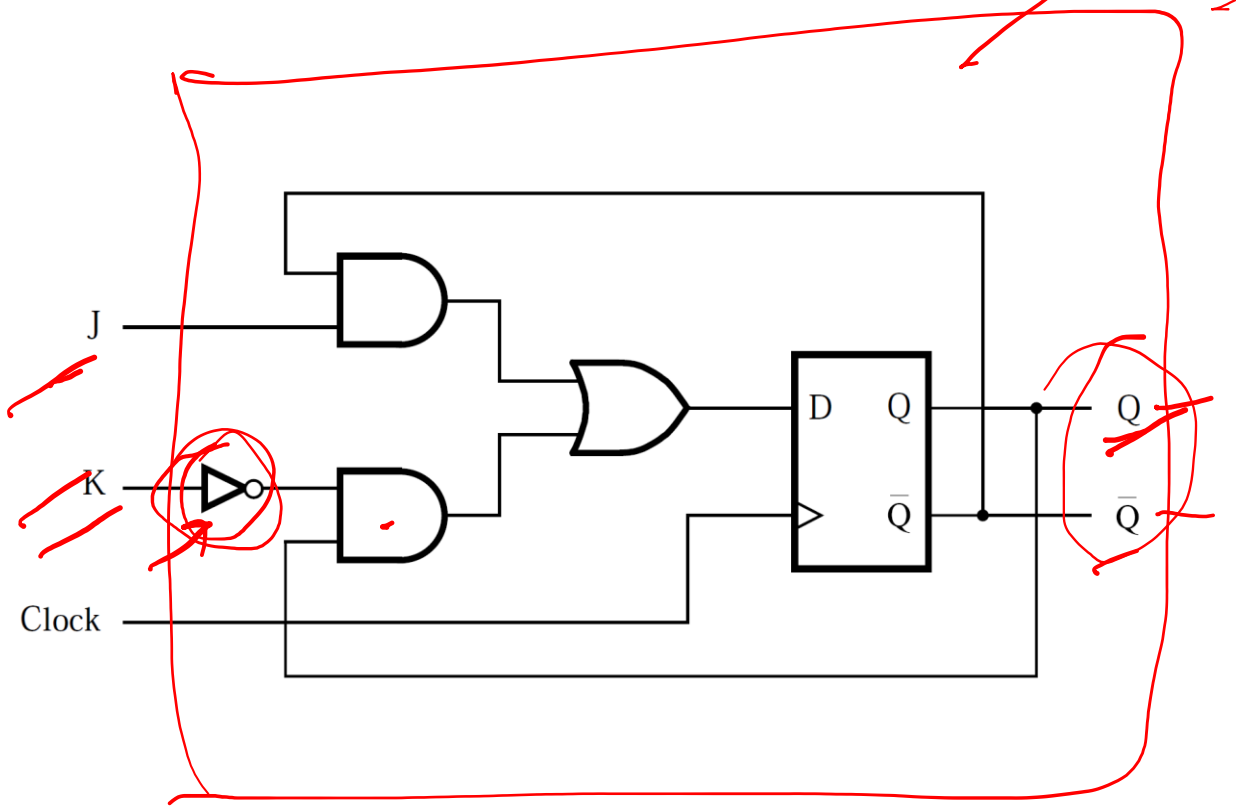


T	$Q(t+1)$
0	$Q(t)$
1	$\bar{Q}(t)$

$$Q(t+1) = T \cdot \bar{Q}(t) + \bar{T} \cdot Q(t)$$

$Q(t) = 0$ -(1)

JK Flip-Flop

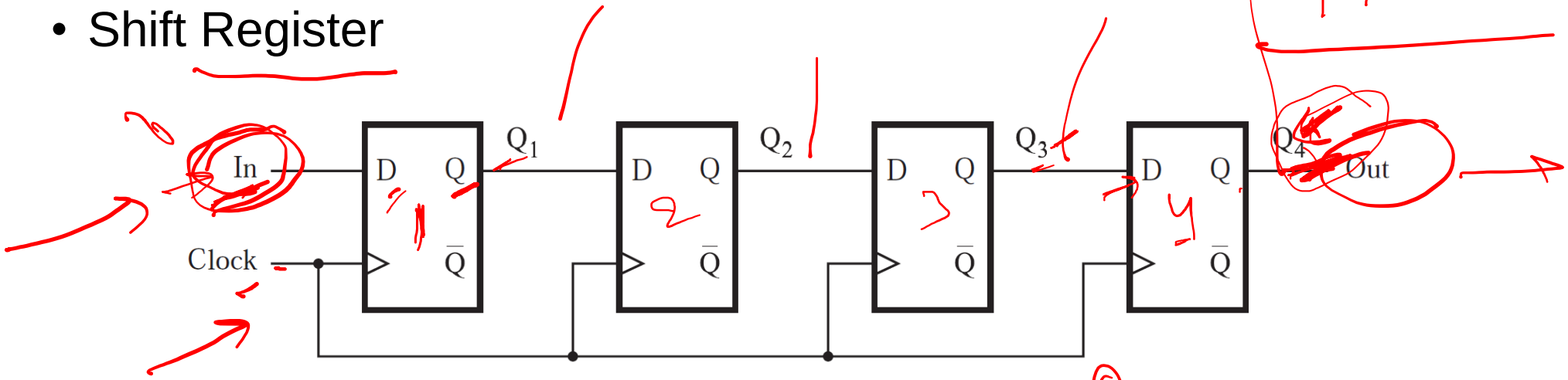


J	K	Q(t + 1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

$$Q_{t+1} = J\bar{Q}_t + \bar{K}Q_t$$

Register

- Shift Register



Parallel-Access Shift Register

- Serial-Serial
- Parallel-Parallel
- Serial-Parallel
- Parallel-Serial