# Synthesis of Digital Systems

COL 719

# Part 9: Physical Synthesis - Placement and Routing

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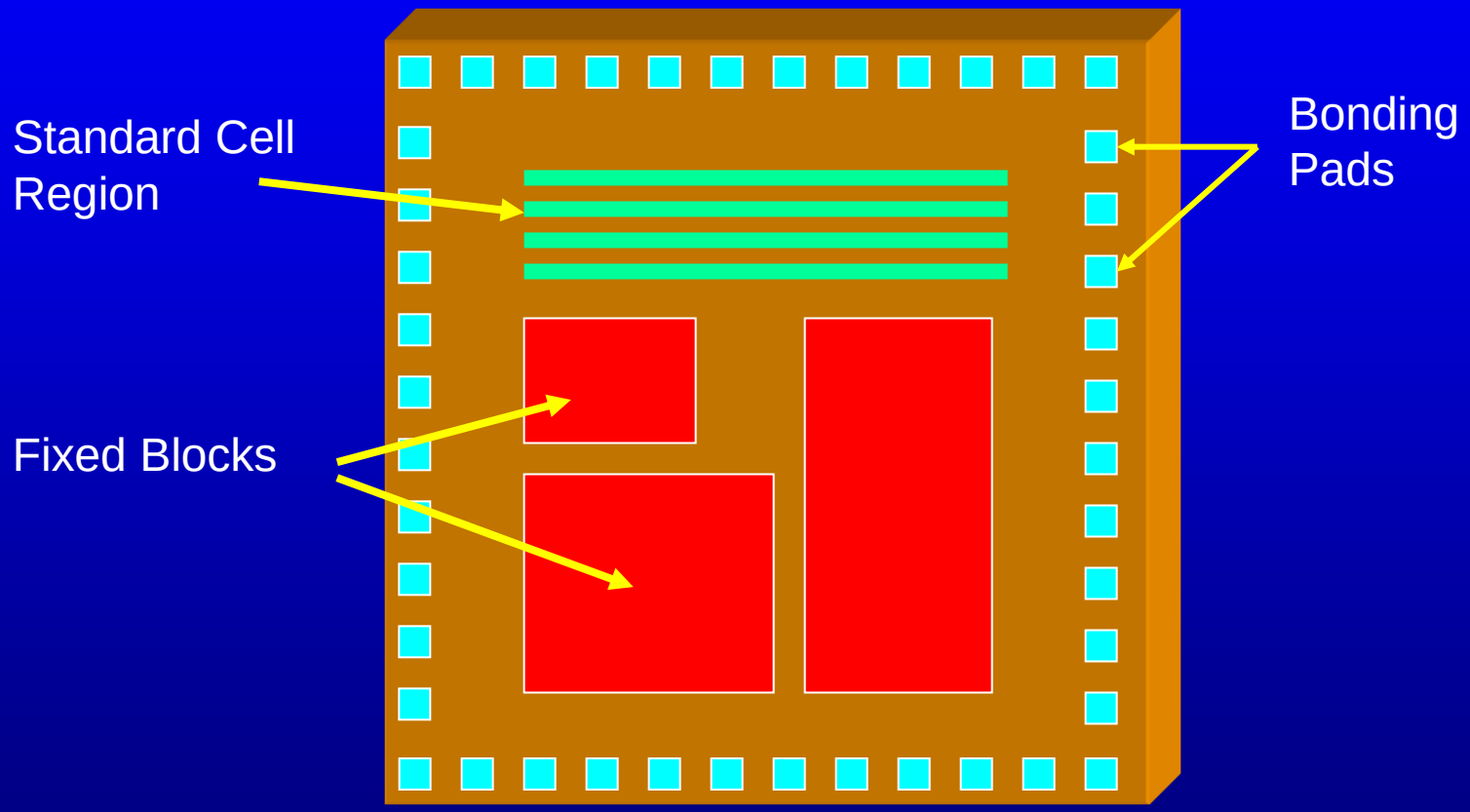
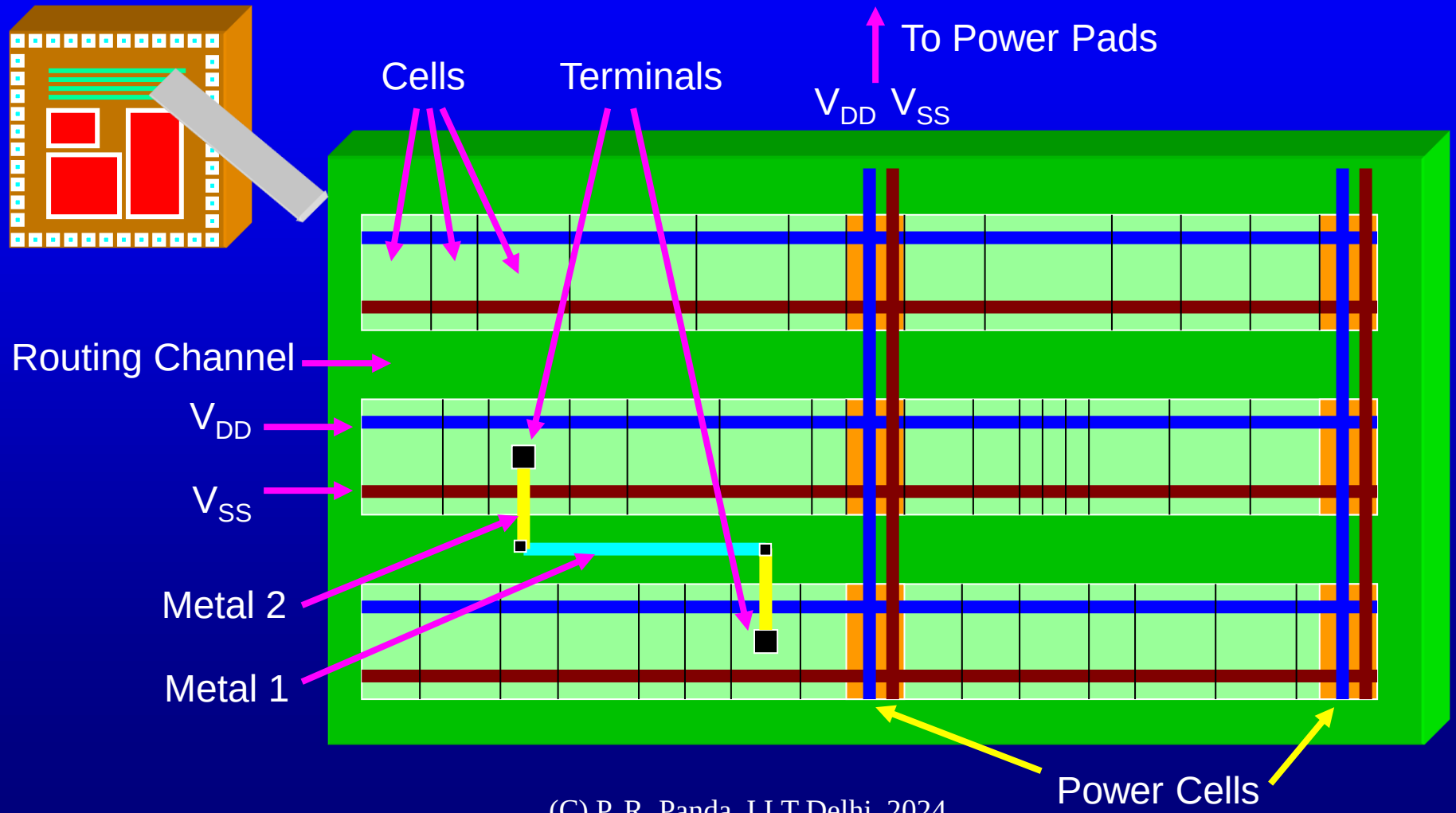
# Standard cell-based ASIC

- Rows of standard cells
  - pre-designed cell library
- Fixed blocks
  - embedded mega-cells (may be custom blocks)
- Placement and interconnect decided by ASIC designer
- Saves time: cells are hand-optimised and pre-tested
- All mask layers are customised for chip
  - design turnaround time: ~8 weeks

# Standard cell architecture



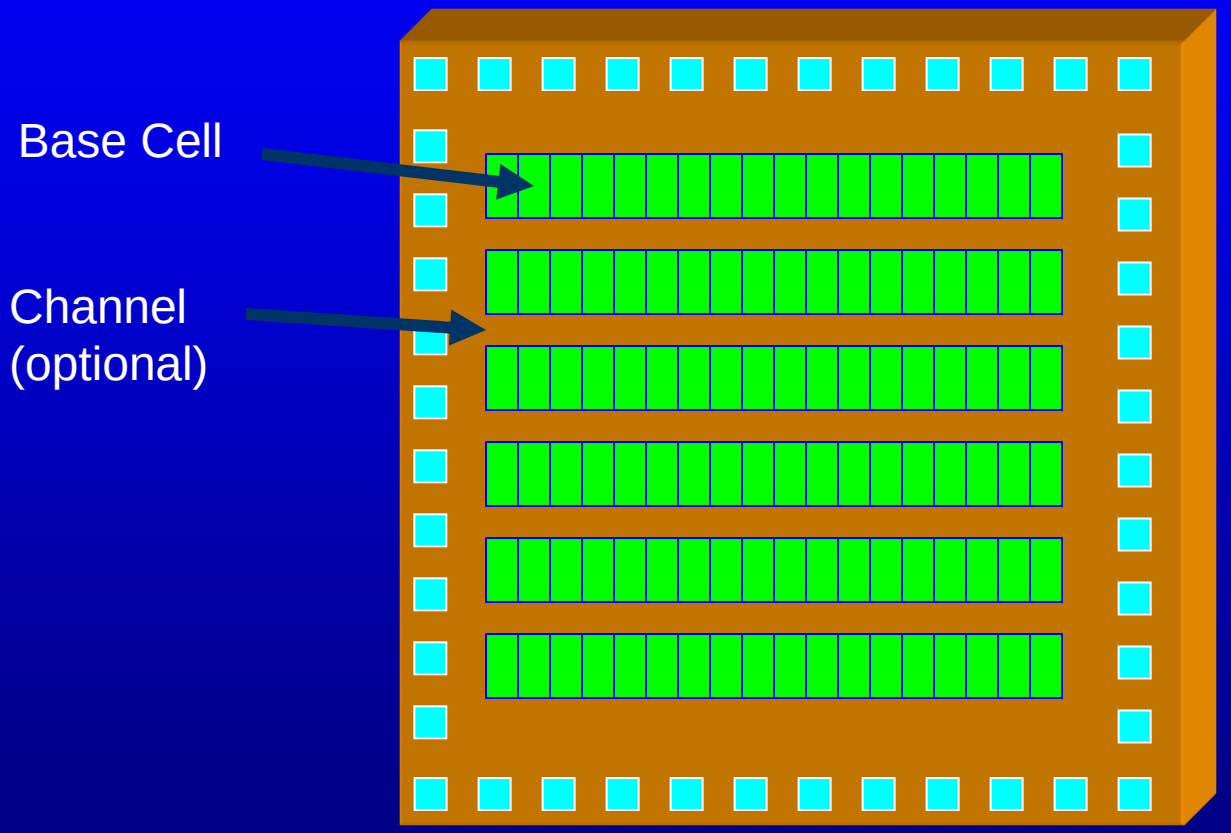
# Standard Cell Architecture: Details



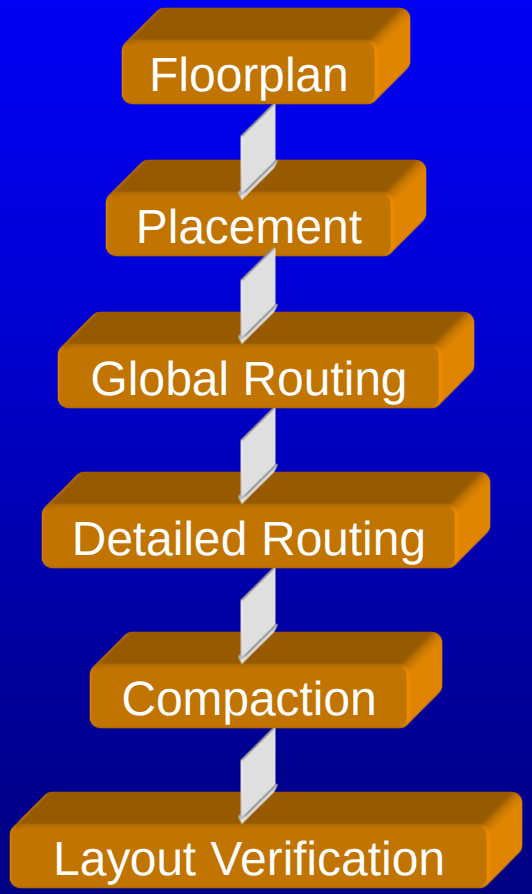
# Gate array-based ASIC

- Transistors pre-fabricated on wafer
- Interconnect decided by ASIC designer
- Small base cell replicated all over chip
- Only top metal layers are customised for chip
  - design turnaround time: ~2 weeks

# Gate array architecture

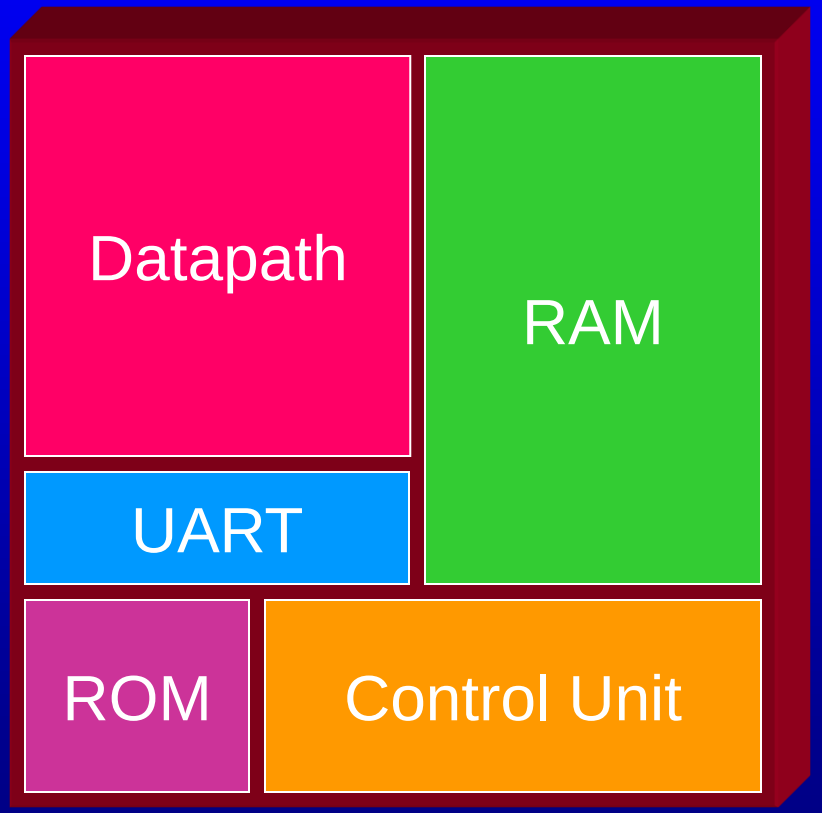


# Layout Methodology

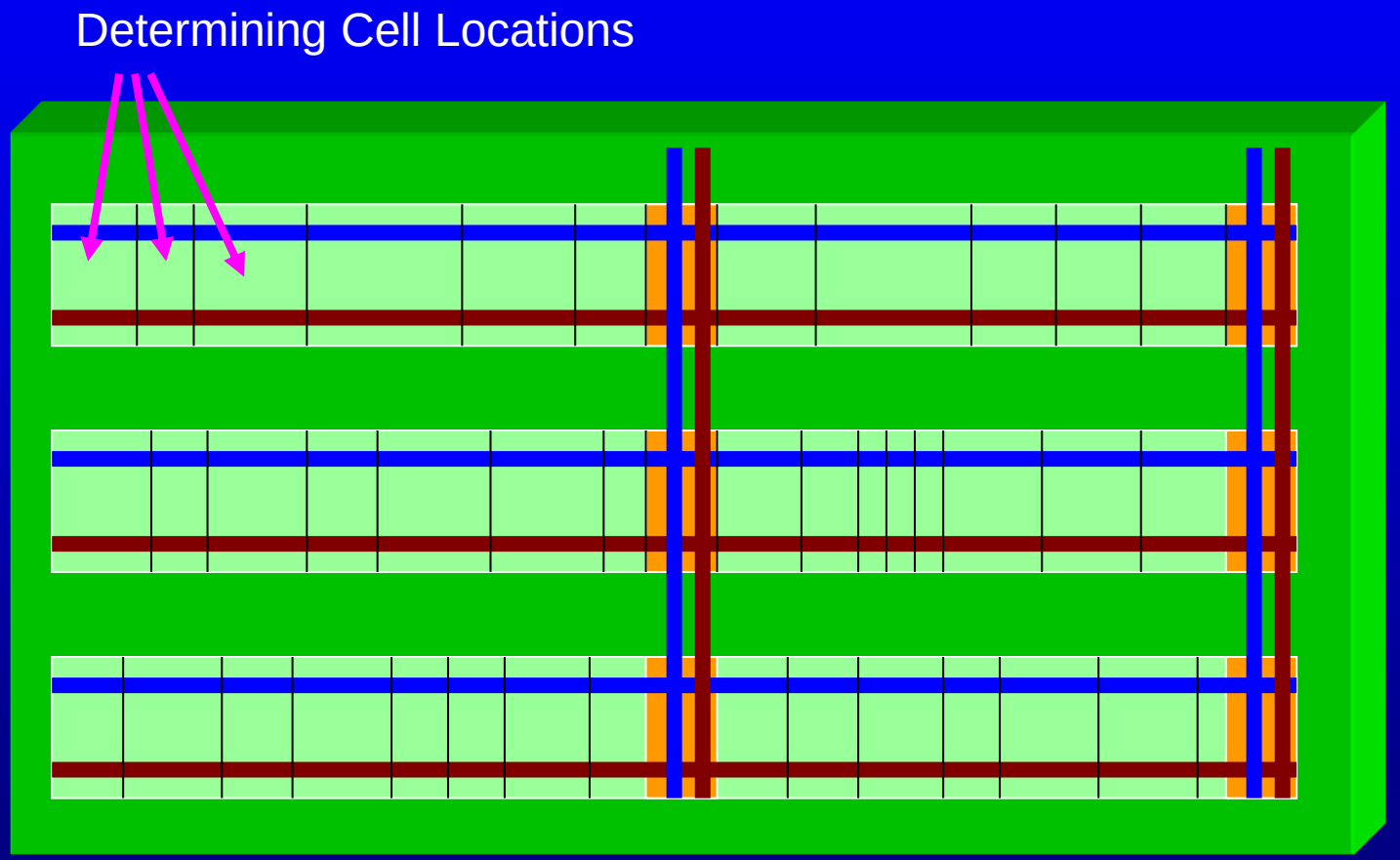


# Floorplan

- Determing location of blocks
  - memory, datapath, control unit
- Coarse grained

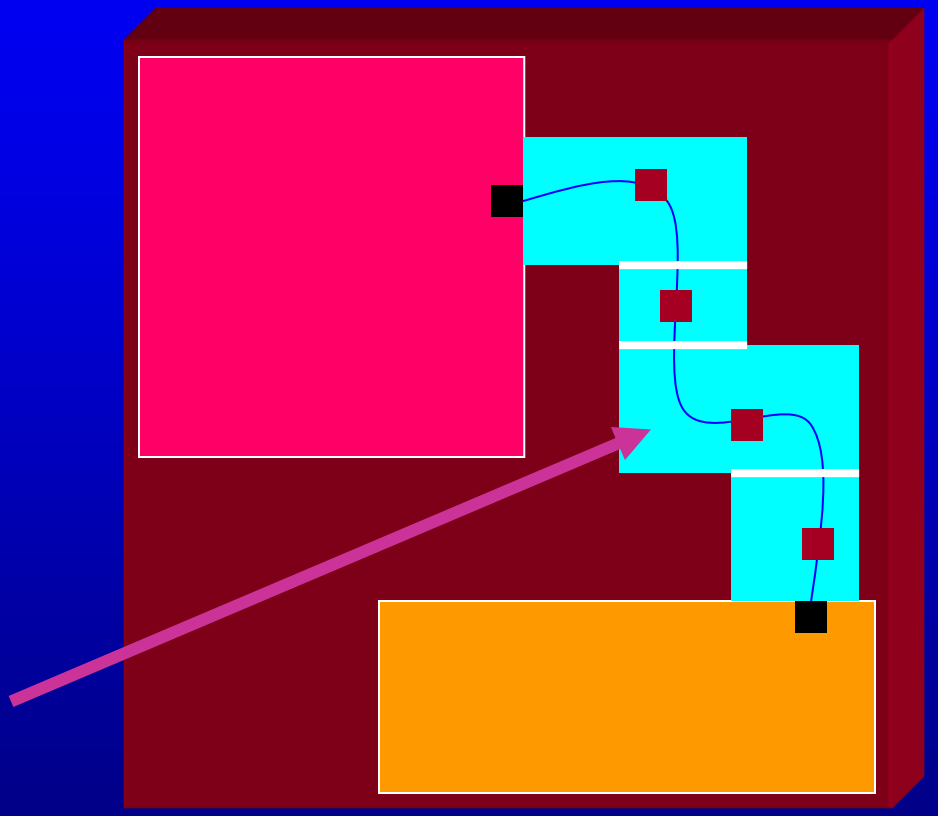


# Standard Cell Placement



# Global Routing

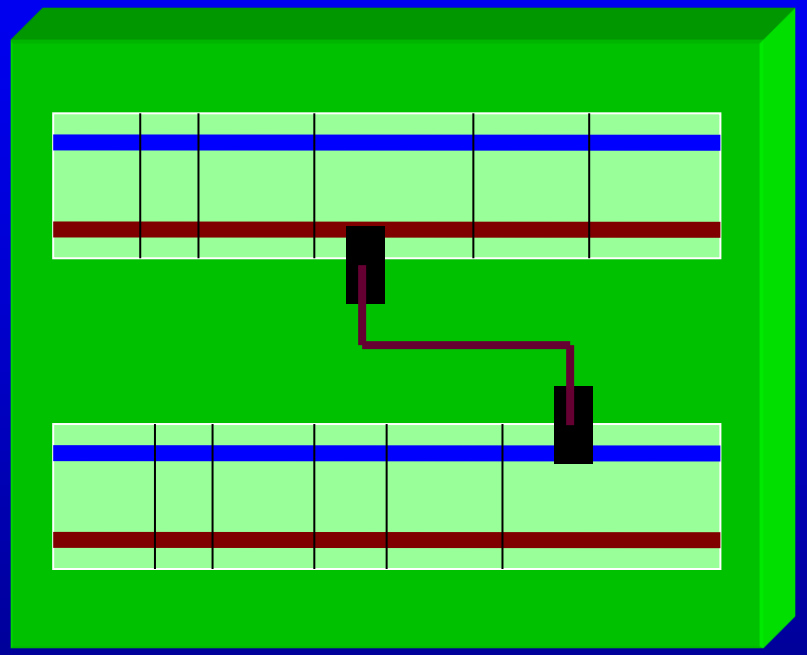
- Allocating regions routing of wires
- Coarse grained
- Exact co-ordinates determined later



Approximate region for routing of wire

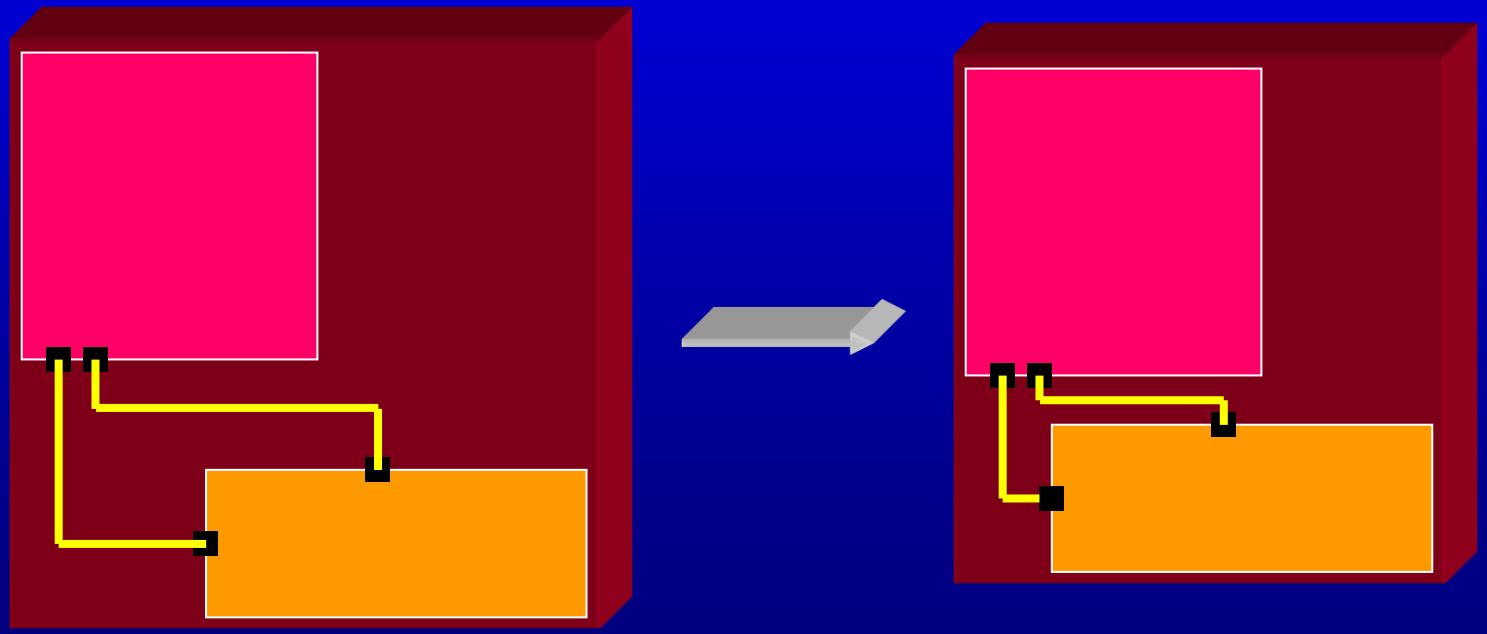
# Detailed Routing

- Determining exact co-ordinates of wires



# Compaction

- Removing unused space
  - keeping same connectivity
  - obeying design rules



# Layout Verification

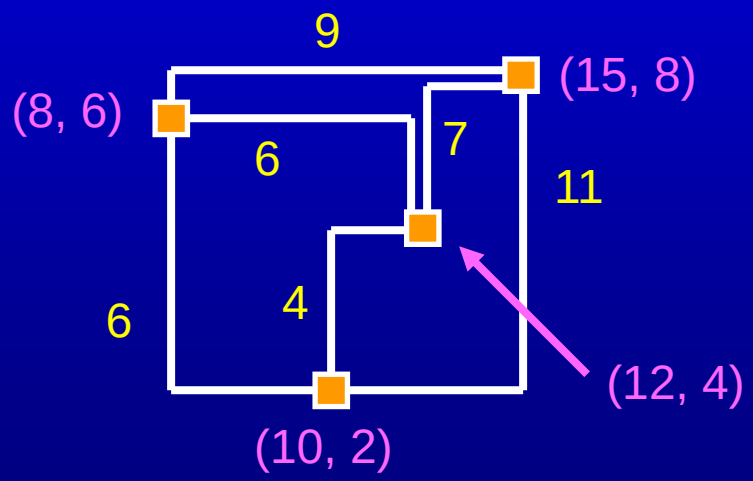
- Checking for design rule constraint violations

# Placement

- Exact solution time consuming
  - not practical for large circuits
- Use heuristics
- Ideal objectives
  - guarantee routable placement
  - minimise critical net delays
  - maximise density
- Realistic objectives
  - minimize total wirelength estimate
  - meet timing requirements for critical nets

# Wire Length Estimate: Complete-Graph Measure

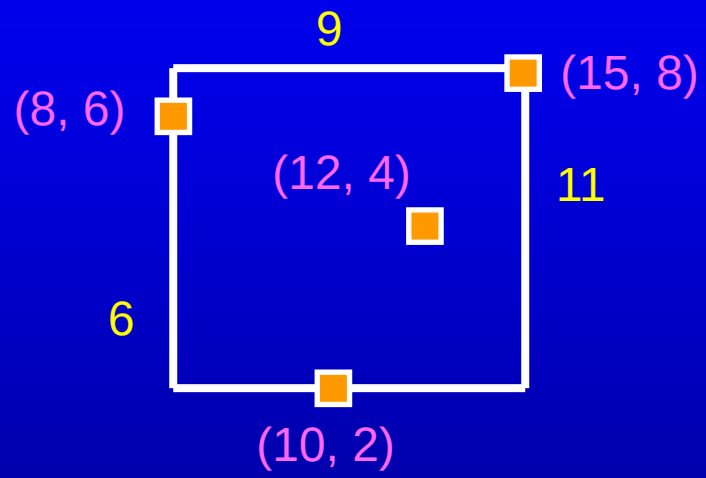
- (n-1) wires needed for connecting n terminals
- Estimate:
  - (average of all wire lengths between n terminals) x (n-1)




Estimate =
(9 + 6 + 7 + 6 + 4 + 11)/6 * 3

# Wire Length Estimate: Semi-Perimeter

- Find bounding box
  - smallest rectangle enclosing all the terminals
- Estimate:
  - 1/2 * (perimeter of rectangle)
- Exact (minimum) for up to 3 terminals




Estimate = (9 + 11 + 6) / 2

# Placement Algorithm: Simulated Annealing

- Start with existing solution
- Iteratively improve
  - make random moves
  - accept move based on energy function
  - may accept inferior move to move from local minima
- Analogous to annealing (metallurgical process)
  - start with high temperature
  - gradually cool the metal

# Simulated Annealing

```
Temperature T = 10000
Start with random placement
Evaluate objective function E
while (T > 0.001) {
  loop 100 times {
    Randomly interchange two cells
    if ΔE ≤ 0 accept move /* better solution */
    else accept with probability e^(-ΔE/T) /* worse solution */
  }
  T = 0.99 T
}
```

Constants
10000, 0.001, 0.99, 100
empirically determined for specific problem

Window shrinks with T

Moves with larger $\Delta E$ accepted early (when T is large) but not later

# Objective Function

- Wire length estimate ($C_1$)
- Overlapping area ($C_2$)
  - may result from swapping of cells of different area
- Excess row length ($C_3$)

$$\text{Energy } E = \alpha C_1 + \beta C_2 + \gamma C_3$$