

COL215L: Digital Logic & System Design

Lecture 22: Finite State Machines (Cont.)




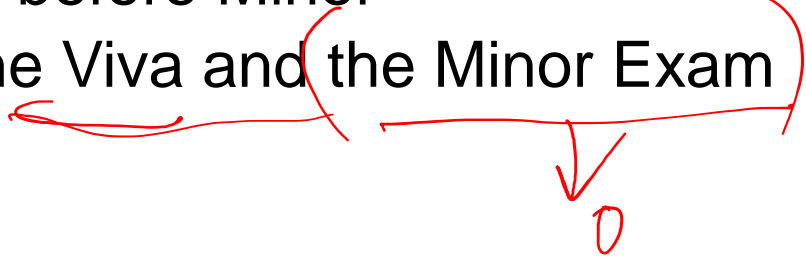


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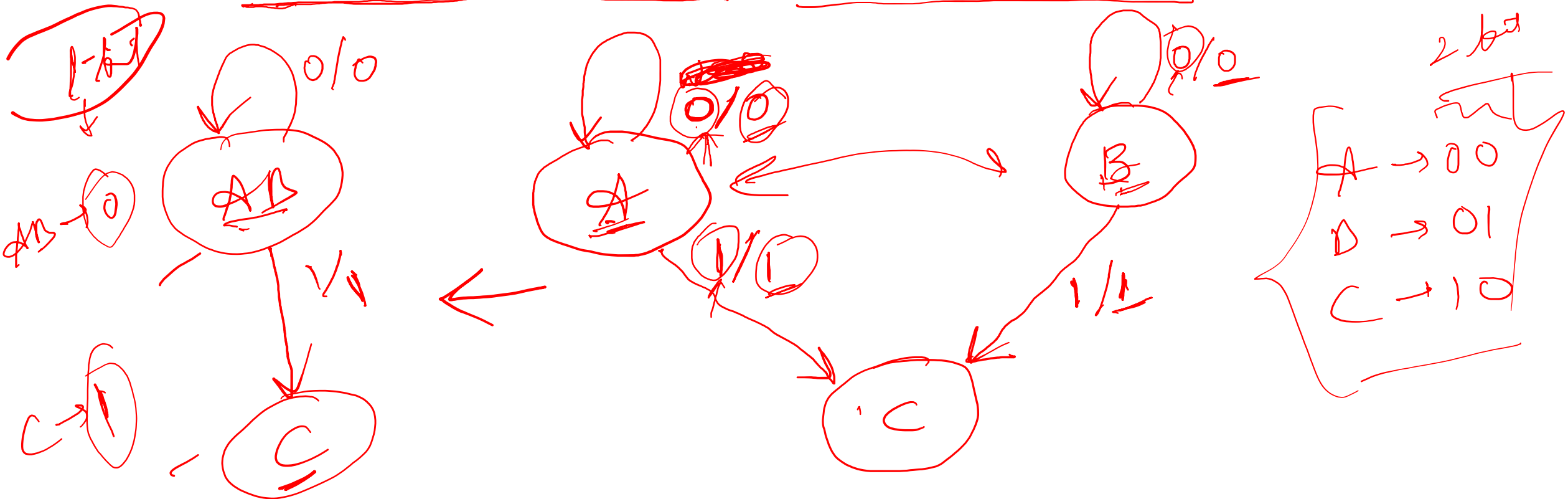
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Handling Suspicious Cases in Minor

- There is a direct correlation between those who are suspicious and those who used only one device  *everyone*
 - Penalty - TBD
- Suspicious cases 
 - Viva related to all topics discussed before Minor 
 - Disproportionate performance in the Viva and the Minor Exam 
 - Penalty – TBD

State Minimization

- State A – equivalent to – State B
 - Every possible input sequence – the same output sequence



Minimization Procedure - Example

• P1 = (ABCDEFGG) ←

• P2 = (ABD)(CEFG) ↓

• P3 = (ABD)(CEG)(F) ↓

• P4 = (AD)(B)(CEG)(F) ↓

• P5 = (AD)(B)(CEG)(F)

(A) (D) (C) (A) (E) (F) '
 { (A B) }
 A

Present state	Next state		Output z
	w = 0	w = 1	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

w=0 w=1
 A D C
 B C C
 C E F
 F
 (A B D)
 (C E F G)
 B B B
 F F E F
 (C F G)
 E C G

Minimized State

Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0



Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	B	C	1
B	A	F	1
C	F	C	0
F	C	A	0

. 1 1
1 1
1 1

1 1
1 1

Incompletely Specified FSM

• z=0

- P1 = (ABCDEFGG)
- P2 = (ABDG)(CEF)
- P3 = (AB)(D)(G)(CE)(F)
- P4 = (A)(B)(D)(G)(CE)(F)
- P5 = (A)(B)(D)(G)(CE)(F)

Present state	Next state		Output z	
	w = 0	w = 1	w = 0	w = 1
A	B	C	0	0
B	D	—	0	—
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	—	0	—

z=0
1 -

• z=1

- P1 = (ABCDEFGG)
- P2 = (AD)(BCEFG)
- P3 = (AD)(B)(CEFG)
- P4 = (AD)(B)(CEG)(F)
- P5 = (AD)(B)(CEG)(F)

w=1
B