COL215L: Digital Logic & System Design

Lecture 17: Sequential Circuits (Cont.)

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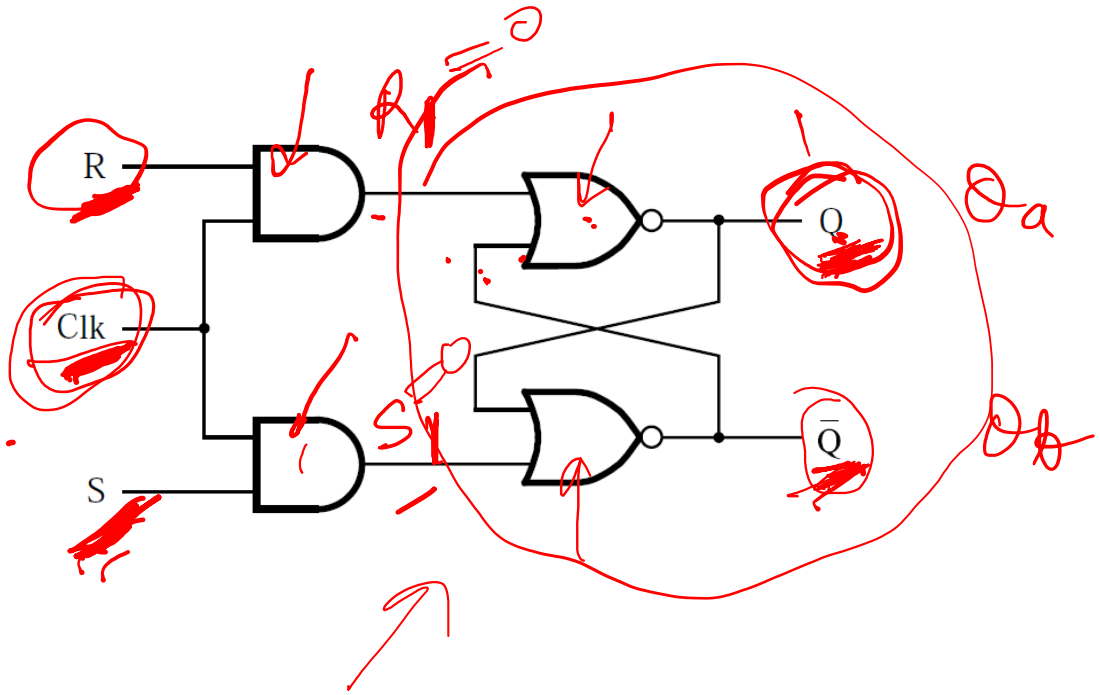
Gated SR Latch



Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

- Set (Q = 1) and reset (Q = 0)

$\bar{Q}$ complement

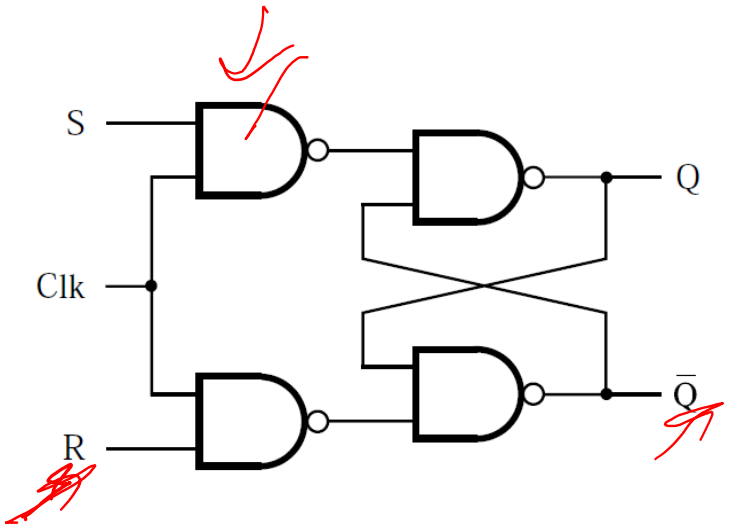
$$Q^{t+1} = \overline{(Clk \cdot R) + \bar{Q}^{t}}$$

$$= \overline{Clk \cdot R} \cdot Q^{t}$$

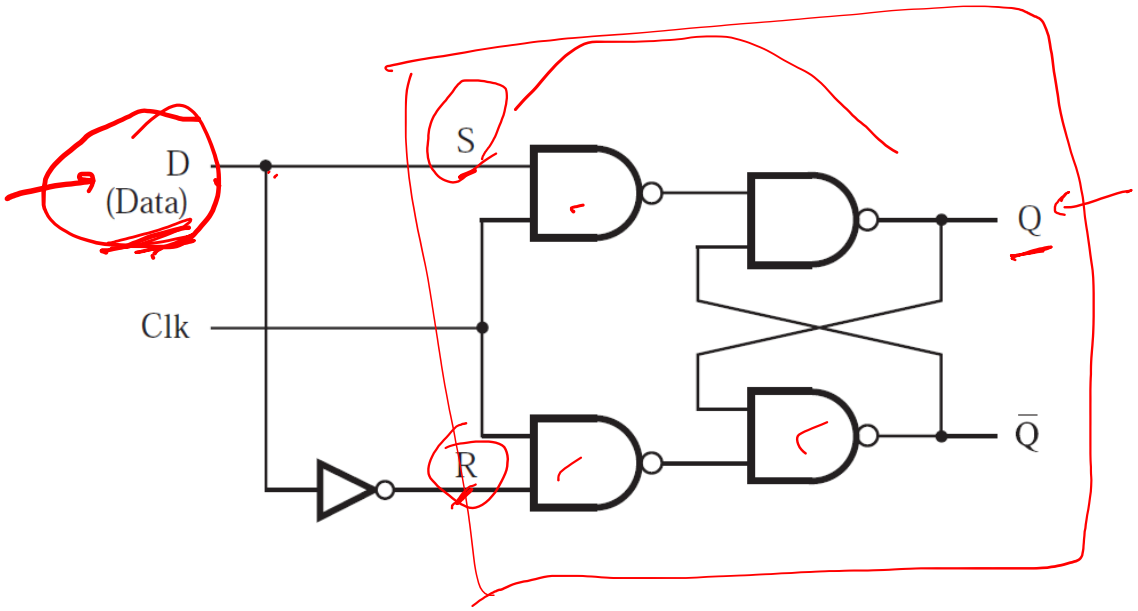
$$\Rightarrow \bar{Q}^{t+1} = \overline{(Clk \cdot R)} \cdot Q^{t}$$

Gated SR Latch with NAND

- Exercise
  - Write the characteristic table

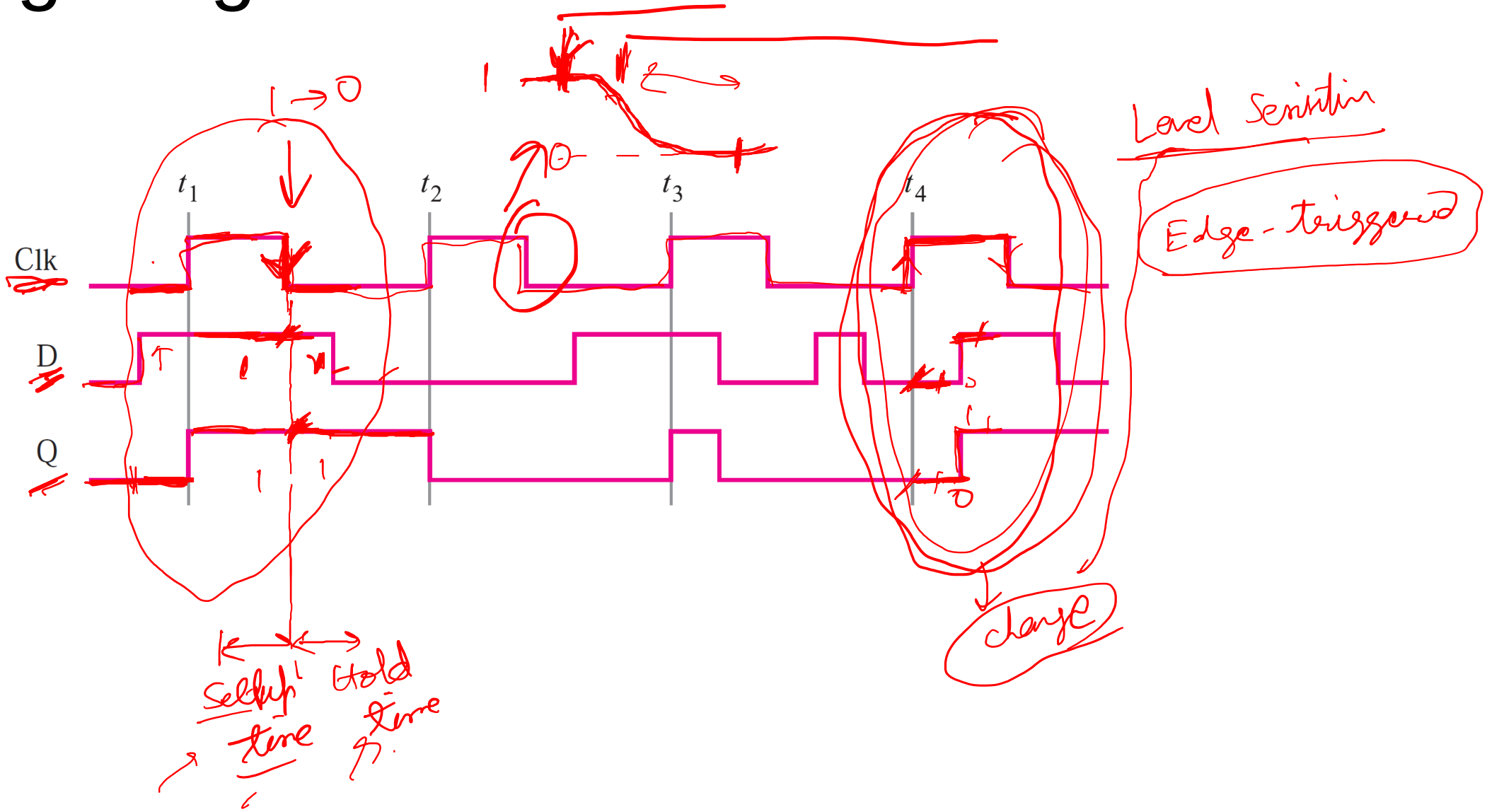


Gated D Latch

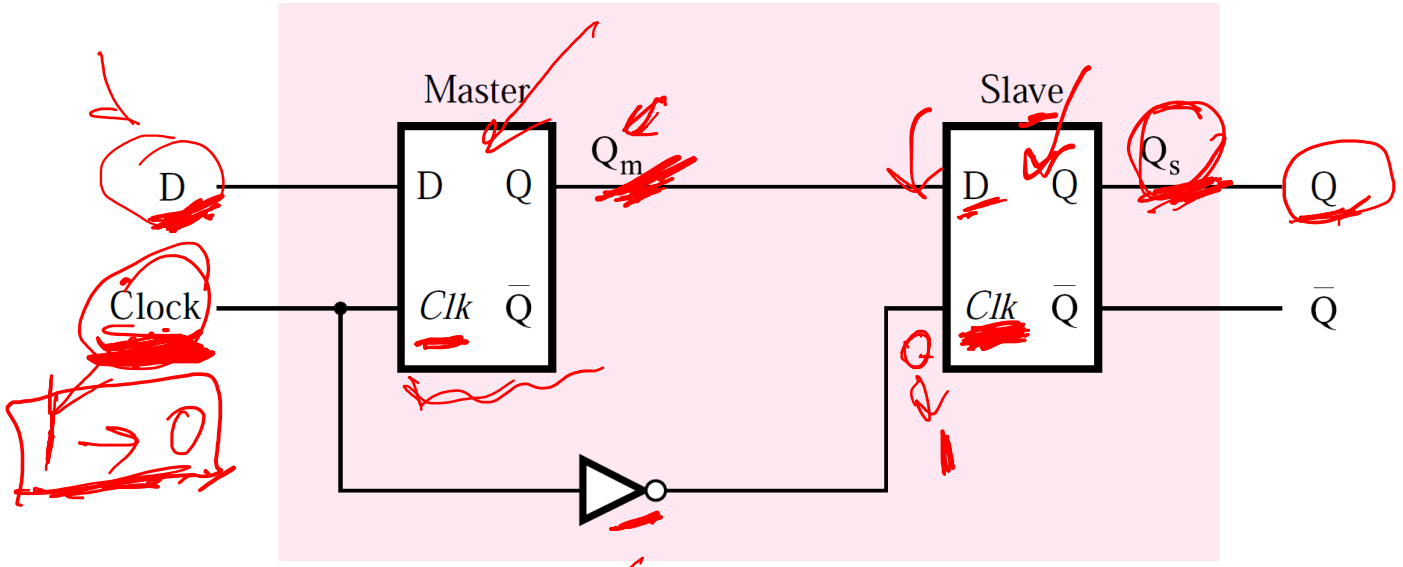


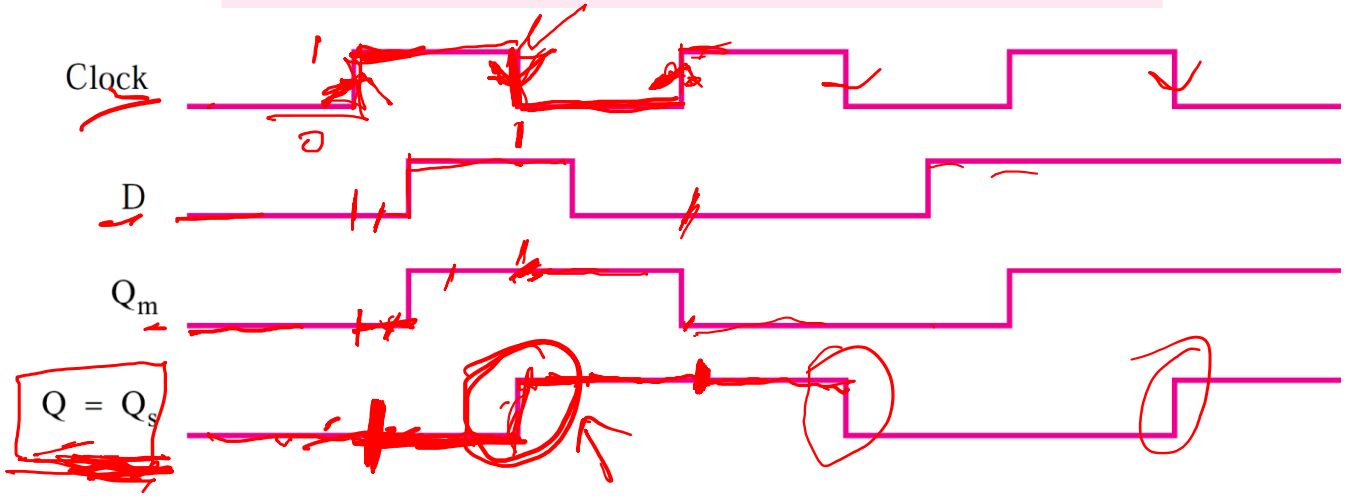
Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

Timing Diagram of Gated D Latch



Master-Slave D Flip-Flop





edge-trigger