## Synthesis of Digital Systems COL 719

**Part 4: Retiming** 

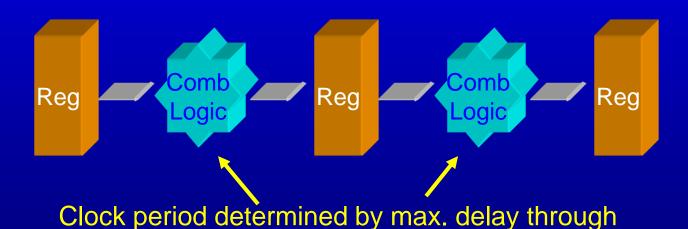
Instructor: Preeti Ranjan Panda

Department of Computer Science and Engineering

Indian Institute of Technology Delhi

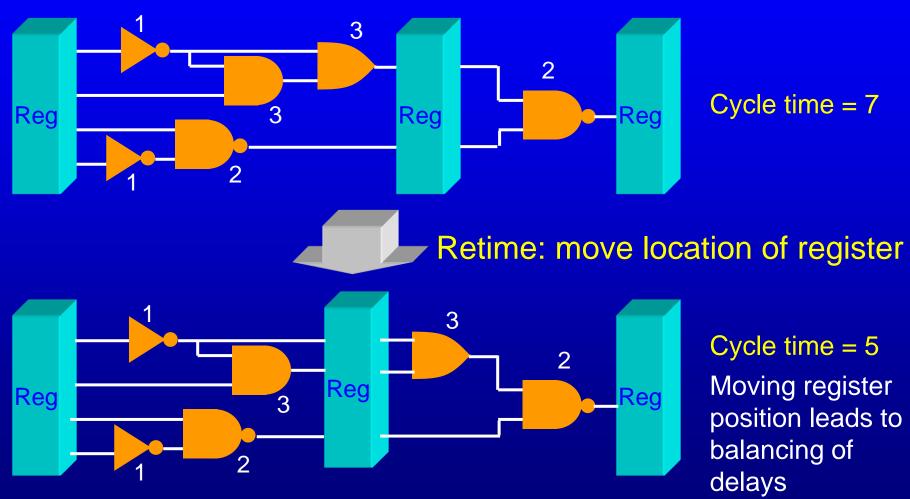
### **Optimising Sequential Circuits**

- Minimise area and cycle time
  - Optimise combinational parts independently
  - Retiming by moving registers

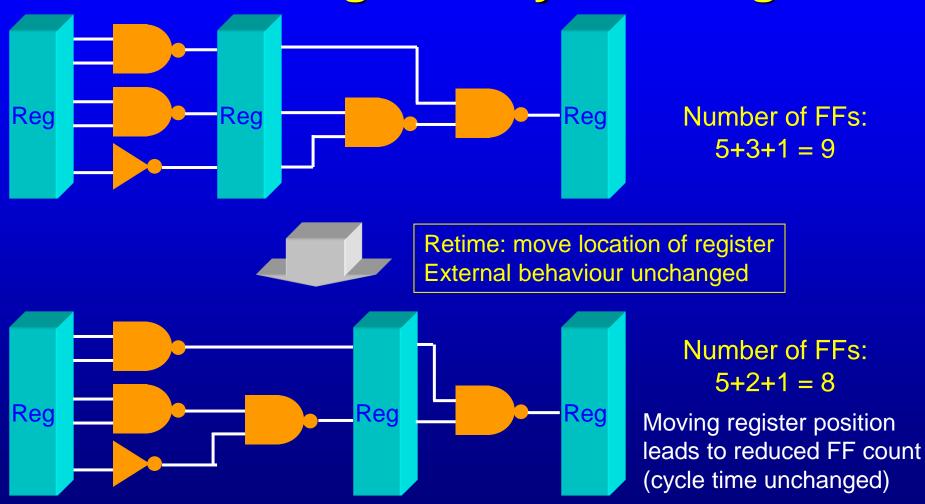


combinational logic stages

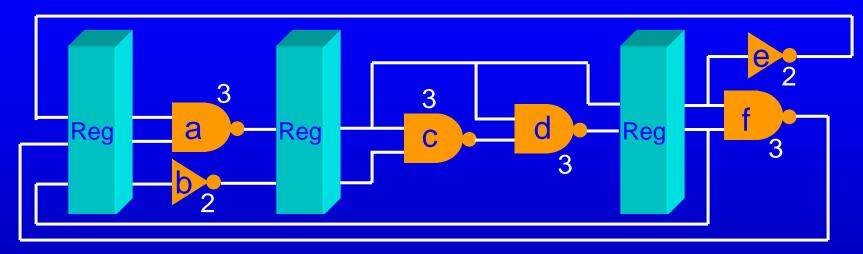
### Reducing Cycle Time by Retiming



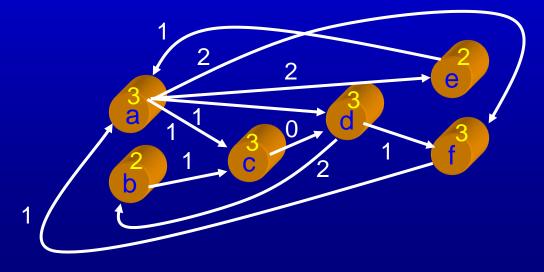
#### **Reducing Area by Retiming**



# Graph Representation of Sequential Circuits for Retiming



- Nodes = Gates
  - weight = gate delay
- Edges = Registers
  - weight = #Registers between gates



#### Path Delay between Nodes

- Sum of propagation delays of nodes along path (including end-points)
- Let d<sub>k</sub> be path delay of node v<sub>k</sub>
- For path (v<sub>i</sub>,...,v<sub>i</sub>), path delay:

$$d(v_i,...,v_j) = \sum_{vk \in (vi,...,vj)} d_k$$

$$\begin{pmatrix} 2 \\ x \end{pmatrix} \begin{pmatrix} 3 \\ 1 \end{pmatrix} \begin{pmatrix} 3 \\ y \end{pmatrix} \begin{pmatrix} 4 \\ z \end{pmatrix} \begin{pmatrix} 3 \\ 2 \end{pmatrix} \begin{pmatrix} 3 \\ w \end{pmatrix}$$

d (x,...,w) = 2+3+4+3 = 12

Path delay is
independent of registers

#### Path Weight between Nodes

- Register count along path (including end-points)
- Let  $w_{kl}$  be weight of edge  $v_k \rightarrow v_l$
- For path (v<sub>i</sub>,...,v<sub>i</sub>), path weight:

$$w(v_i,...,v_j) = \Sigma_{vk \rightarrow vl \in (vi,...,vj)} w_{kl}$$

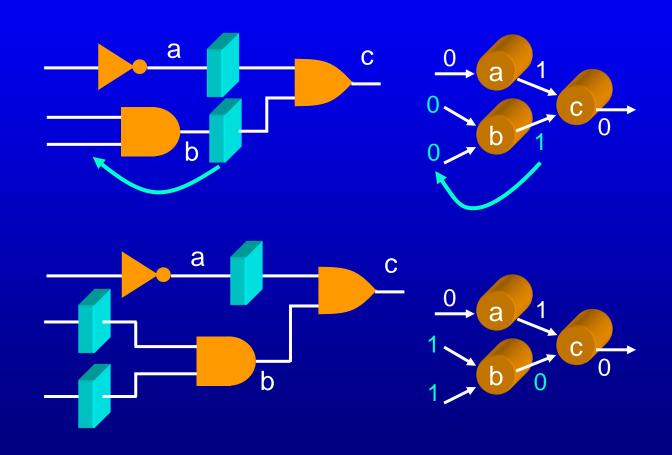
$$a \xrightarrow{1} b \xrightarrow{0} c \xrightarrow{2} d$$

$$w(a,...,d) = 1+0+2 = 3$$

Path weight is independent of node delays

### Retiming a Node

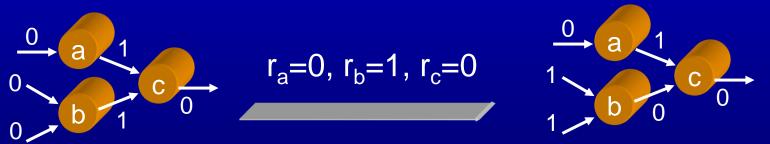
- Moving registers from outputs to inputs
  - or vice versa
  - amount of synchronous delay moved past node
  - "register" = "flip flop"
- Positive or negative value



#### **Retiming the Graph**

- Graph transformation: G(V,E,W) to G'(V,E,W')
- Integer vector r:V→Z
- For all edges v<sub>i</sub>→v<sub>j</sub>

$$w'_{ij} = w_{ij} + r_j - r_i$$
 $r_j$  registers added to edge
 $r_i$  registers removed from edge



#### Path Weights after Retiming

· Path weight depends on retiming of extreme nodes only

$$w'(v_{i},...,v_{j}) = w(v_{i},...,v_{j}) + r_{j} - r_{i}$$

Weight of cycle is invariant on retiming

#### **Definitions**

 $W_{ij} = min w(v_i,...,v_j)$  for all paths  $(v_i,...,v_j)$ 

$$W_{ae} = w(a,b,e) = w(a,c,e) = 4$$

 $D_{ij} = \max d(v_i,...,v_j)$  for all paths  $(v_i,...,v_j)$  with weight  $W_{ij}$ 

$$d(a,b,e) = 1+3+2=6$$
  
 $d(a,c,e) = 1+2+2=5$   $D_{ae} = d(a,b,e) = 6$ 

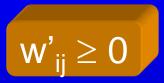
#### **Legality and Timing Feasibility**

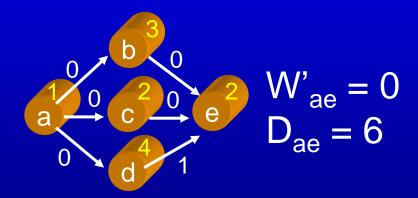
#### Legality

No negative edge weights (number of registers ≥ 0)

#### Timing Feasibility

- given clock period ∮
- Path delay larger than φ should be broken by at least one register





$$W'_{ij} \ge 1 \text{ if } D_{ij} > \phi$$

Infeasible for  $\phi = 5$ Feasible for  $\phi = 6$ 

#### Feasibility of Retiming

- Retiming is feasible if
  - legal
  - retimed graph is timing feasible
- Retiming r is feasible if

$$\forall \ (v_i, v_j) \in E$$
 Legality Check 
$$w'_{ij} \ge 0 \Rightarrow w_{ij} + r_j - r_i \ge 0 \Rightarrow r_i - r_j \le w_{ij}$$
 
$$\forall \ v_i, v_j : D(v_i, v_j) > \varphi$$
 Timing Check 
$$w'_{ij} \ge 1 \Rightarrow W_{ij} + r_j - r_i \ge 1 \Rightarrow r_i - r_j \le W_{ij} - 1$$

#### System of Linear Inequalities

- Compute W and D matrices
- Build set of linear inequalities
  - Upto 2 inequalities for every pair of nodes
- Solve for vector r

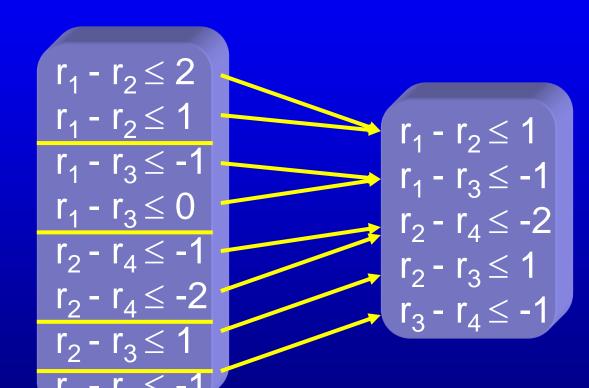
$$\forall (v_i, v_j) \in E$$

$$r_i - r_j \le w_{ij}$$

$$\forall v_i, v_j : D(v_i, v_j) > \phi$$

$$r_i - r_j \le W_{ij} - 1$$

#### Remove Redundant Inequations and Solve



Retain one equation per  $(r_{i,}r_{j})$  pair Solve for  $r_{1,}r_{2,}r_{3,}r_{4}$ 

# How do we Solve System of Inequalities?

- General problem: Linear Programming (LP)
  - Maximise  $\Sigma c_i x_i$  given  $Ax \leq b$
  - Simplex method (Exponential time)
  - Ellipsoid/Karmakar (Polynomial time)
- Restricted version: Integer Linear Programming (ILP)
  - Variables restricted to be integers
  - NP-Complete!

$$r_1 - r_2 \le 1$$
  
 $r_1 - r_3 \le -1$   
 $r_2 - r_4 \le -2$   
 $r_2 - r_3 \le 1$   
 $r_3 - r_4 \le -1$ 

```
\begin{aligned} &A_{11}x_1 + A_{12} x_2 \le b_1 \\ &A_{21}x_1 + A_{22} x_2 \le b_2 \\ &A_{31}x_1 + A_{32} x_2 \le b_3 \\ &A_{41}x_1 + A_{42} x_2 \le b_4 \\ &A_{51}x_1 + A_{52} x_2 \le b_5 \end{aligned}
```

#### Inequalities in Retiming Problem

- Restricted system of inequalities
  - Exactly 2 variables in each inequality
  - Coefficients are 1, -1
- Can be solved in Polynomial time!

```
r_1 - r_2 \le 1

r_1 - r_3 \le -1

r_2 - r_4 \le -2

r_2 - r_3 \le 1

r_3 - r_4 \le -1
```

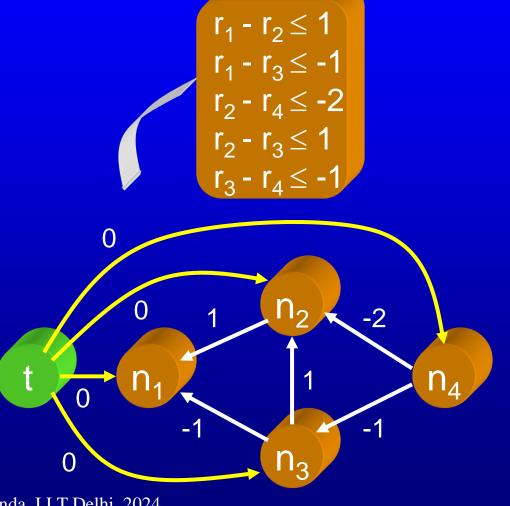
#### Solution to System of Inequalities

- No solution
- System has infinite solutions.
  - if r is a solution, r+c is also a solution
- Let  $r_1 = 0$ 
  - Can set arbitrary r<sub>i</sub> to 0
  - For example:
    - if (2,3,-1,0) is one solution,
       (0,1,-3,-2) is also a solution

$$r_1 - r_2 \le 1$$
  
 $r_1 - r_3 \le -1$   
 $r_2 - r_4 \le -2$   
 $r_2 - r_3 \le 1$   
 $r_3 - r_4 \le -1$ 

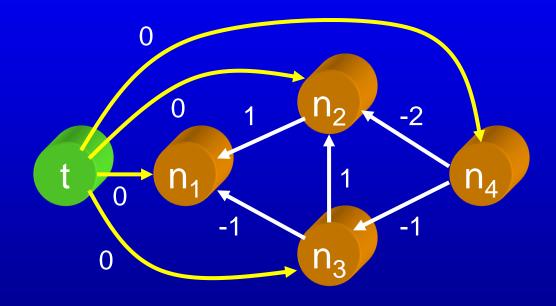
#### **Build Constraint Graph**

- One node n<sub>i</sub> for each r<sub>i</sub>
- Constraint  $r_a r_b \le k$  implies Edge Weight  $wt(n_b \rightarrow n_a) = k$
- Add auxiliary node t
  - zero-weight edges to all other nodes from t



#### Solution using Shortest Path Algorithm

- Find shortest path in graph from t to all other nodes
  - Polynomial time
  - Bellman-Ford algorithm
- This gives r<sub>i</sub> values for other nodes!



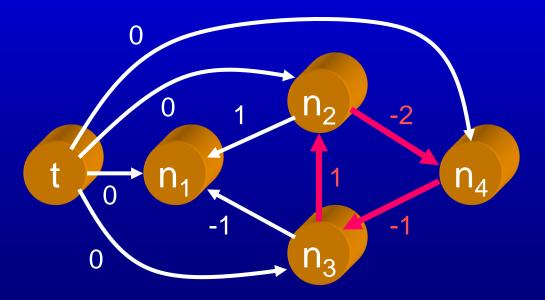
Solution: 
$$r_1 = -2$$
,  $r_2 = -2$ ,  $r_3 = -1$ ,  $r_4 = 0$ 

#### Why does Shortest Path work?

Consider edge n<sub>b</sub>→n<sub>a</sub> sp  $(t\rightarrow n_a) \le sp (t\rightarrow n_b) + wt (n_b\rightarrow n_a) -- by define of shortest path$  $sp(t\rightarrow n_a) - sp(t\rightarrow n_b) \leq wt(n_b\rightarrow n_a)$ Letting  $r_a = sp (t \rightarrow n_a)$  $r_b = sp (t \rightarrow n_b)$  $r_a - r_b \le wt (n_b \rightarrow n_a)$  $r_a - r_b \le k$ Thus, choice of sp for r<sub>i</sub> satisfies constraint represented by edge wt

#### What if Graph has Negative Cycle?

- Sum of edge wts in cycle is negative
- Bellman-Ford algorithm returns error
  - shortest path not defined



# Negative Cycle Leads to Infeasible Constraints

```
r_2 - r_1 \le wt (n_1 \rightarrow n_2)

r_3 - r_2 \le wt (n_2 - n_3)

r_4 - r_3 \le wt (n_3 - n_4)

...

r_k - r_{k-1} \le wt (n_{k-1} - n_k)

r_1 - r_k \le wt (n_k - n_1)
```

Ref: Cormen, Leiserson, and Rivest, "Introduction to Algorithms"

Adding both sides:

 $0 \le wt (n_1 \rightarrow n_2) + wt (n_2 - n_3) + ... + wt (n_{k-1} - n_k) + wt (n_k - n_1)$ Impossible because RHS is negative i.e., Bellman-Ford algorithm can be used directly for our problem Now, we have Retiming values for all nodes (gates)

#### **Retiming Strategy**

- Compute D and W of original circuit

$$\forall (v_i, v_j) \in E \qquad r_i - r_j \le w_{ij}$$

$$\forall v_i, v_j : D(v_i, v_j) > \phi \qquad r_i - r_j \le W_{ij} - 1$$

- If solution exists reduce φ and solve again
- Until no more solution

#### 

- Optimal clock period has to be one of the D<sub>ii</sub> values
  - otherwise, we could reduce φ to the nearest D<sub>ij</sub> value without violating clock period
- First enumerate and sort all D<sub>ij</sub> values in decreasing order
  - E.g.: 20, 16.5, 15, 13.2, 10, 8, 7, 5
- Use binary search