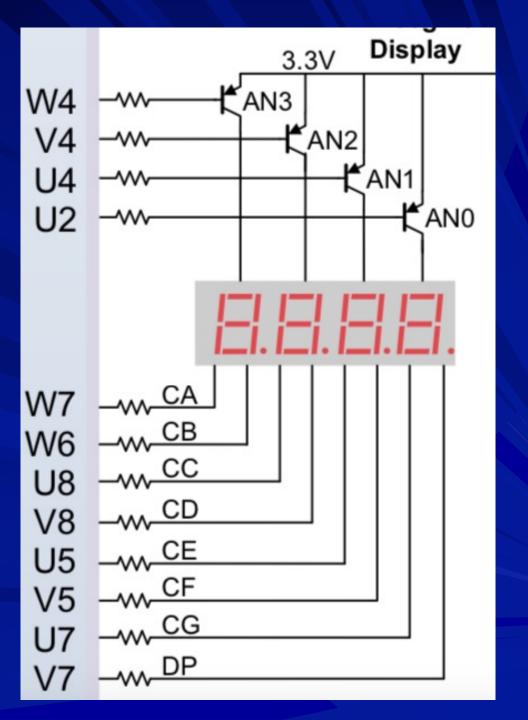
COL216 Computer Architecture

Input/Output – 2 17th March 2022

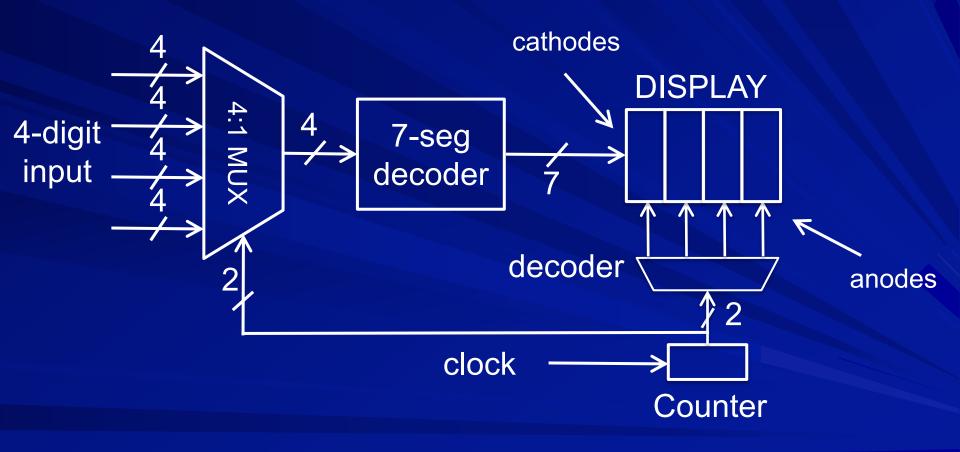
4-digit Display on BASYS 3 Board



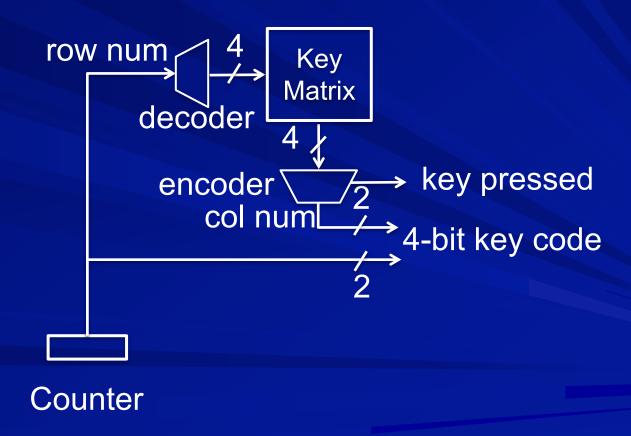
16 Button Key-pad



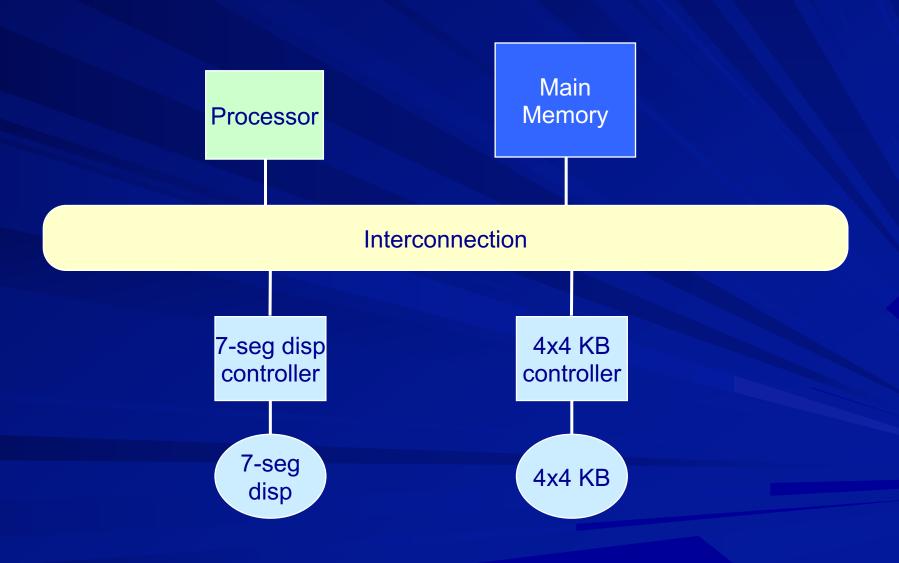
7-segment Display Controller



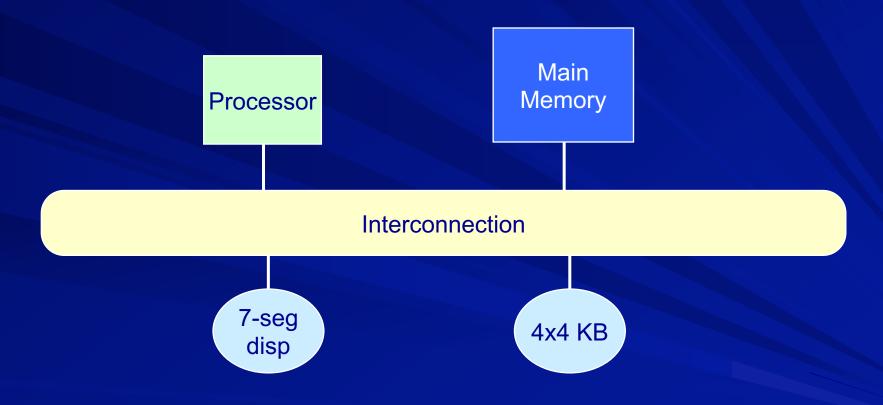
4 x 4 Keyboard Encoder



Block diagram

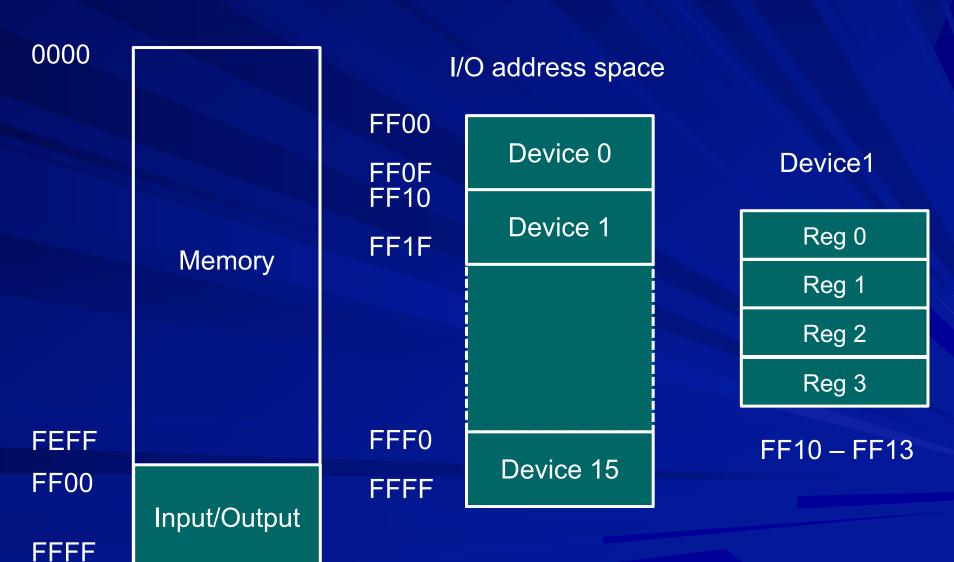


Block diagram

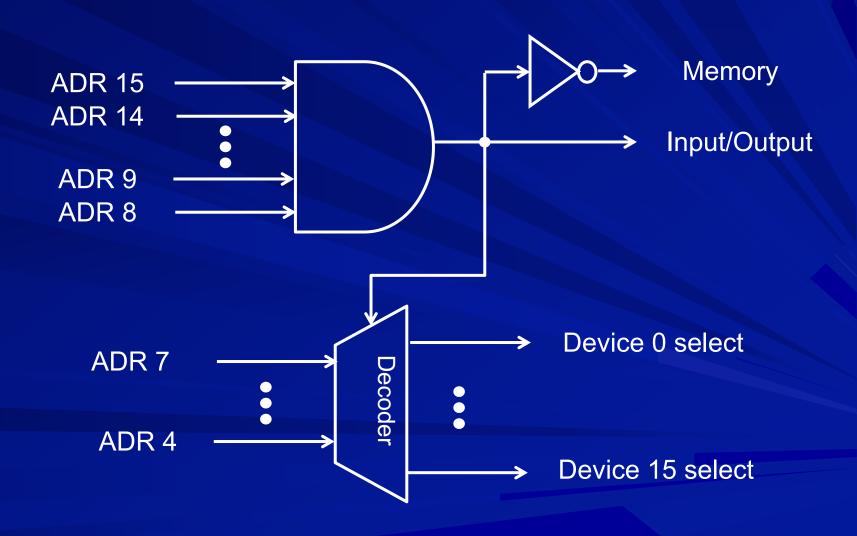


Low level control by software

Address Map Example

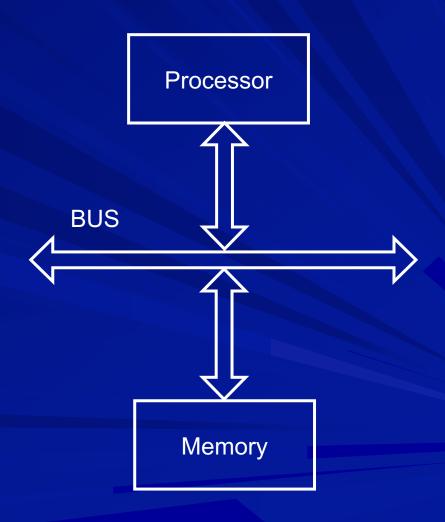


Decoding Address

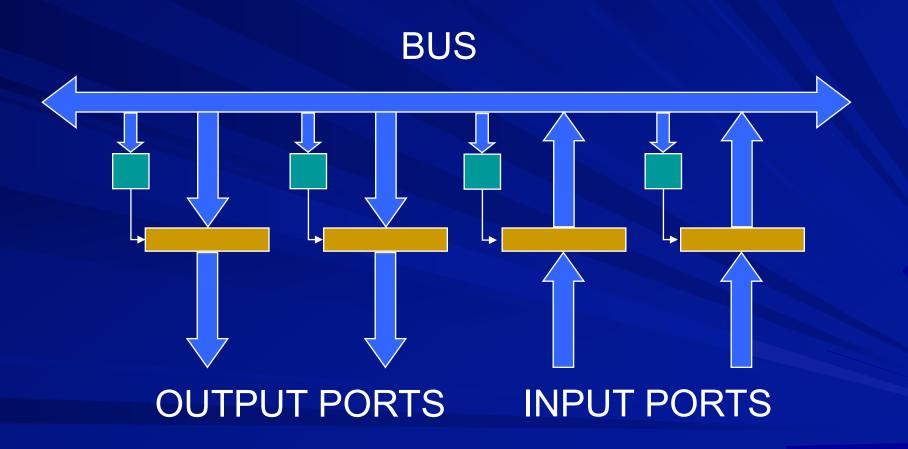


Interconnection using a bus





INPUT / OUTPUT PORTS



Ports for Disp, KB controllers

Display
out
Digit 0
out
Digit 1
out
Digit 2
out
Digit 3

in status
in key code

Ports for raw Disp, KB

DisplayKey Boardoutanode patternoutrow patternoutcathode patternincolumn pattern

refresh required

repeated scan required

Taking care of device timings

Devices may have latency of hundreds or thousands of cycles.

Can the instruction execution be stretched for so long?

How CPU checks the device status

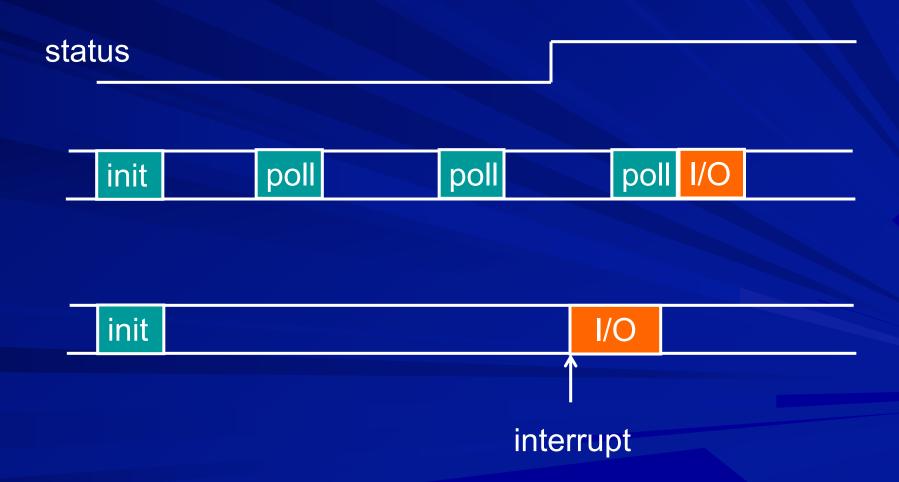
Polling

- periodically read the status register and figure out whether the device is ready or not
- should be frequent enough so that no events are missed out

Interrupt

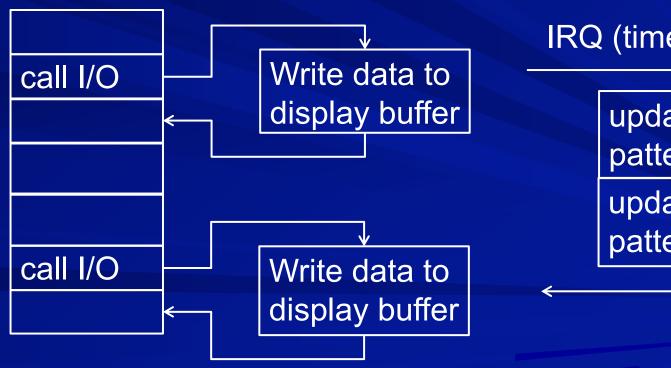
 keep busy with some other task and allow the device to intimate its readiness by sending a signal

Polling vs interrupt



Reset
initialize display
buffer
initialize anode,
cathode pattern

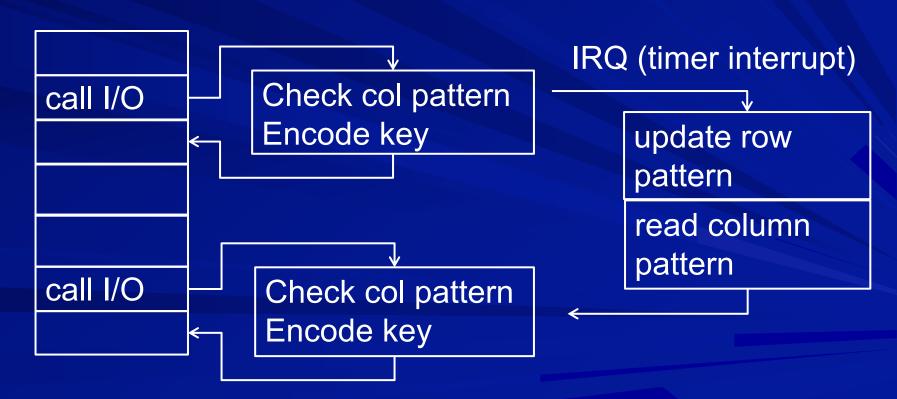
Display refresh using interrupt



update cathode pattern
update anode pattern

Reset
initialize KB
status
initialize row
pattern

Keyboard scan using interrupt

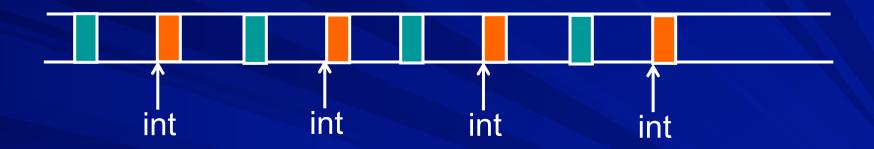


Direct memory access

- Allow direct data transfer between the device and the memory
- The process is initiated by the processor
- When the entire job is done, the device informs the processor by an interrupt
- A specialized controller called DMA controller is used

Benefit of DMA

Without DMA



With DMA



Direct memory access

