Synthesis of Digital Systems

COL 719

Part 8: Static Timing Analysis

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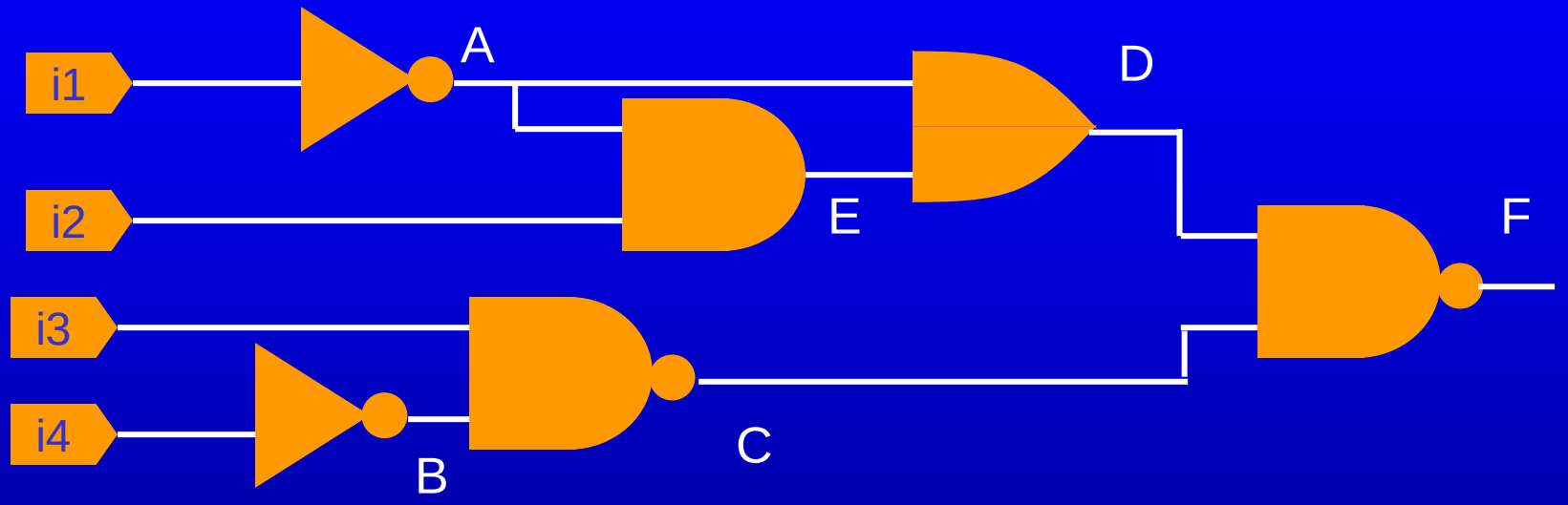
What is Timing Analysis?

- Compute the delay of a combinational circuit
  - Worst case
- Why?
  - So we can decide clock rate
- Why not just simulate?

Timing Analysis

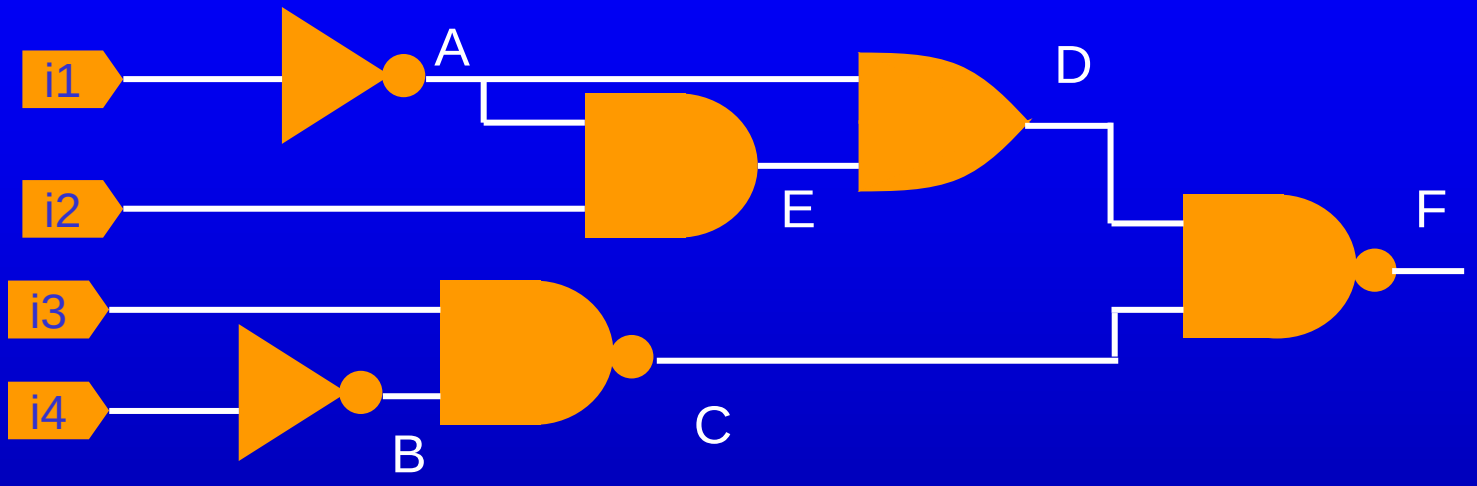
- Simulation
  - High Accuracy
  - Functional Verification
  - Limited Coverage
  - Slow
  - Limited Capacity
  - Needs Test Patterns
- Timing Analysis
  - Reasonable Accuracy
  - No Functional Verification
  - High Coverage
  - Fast
  - High Capacity
  - No Test Pattern

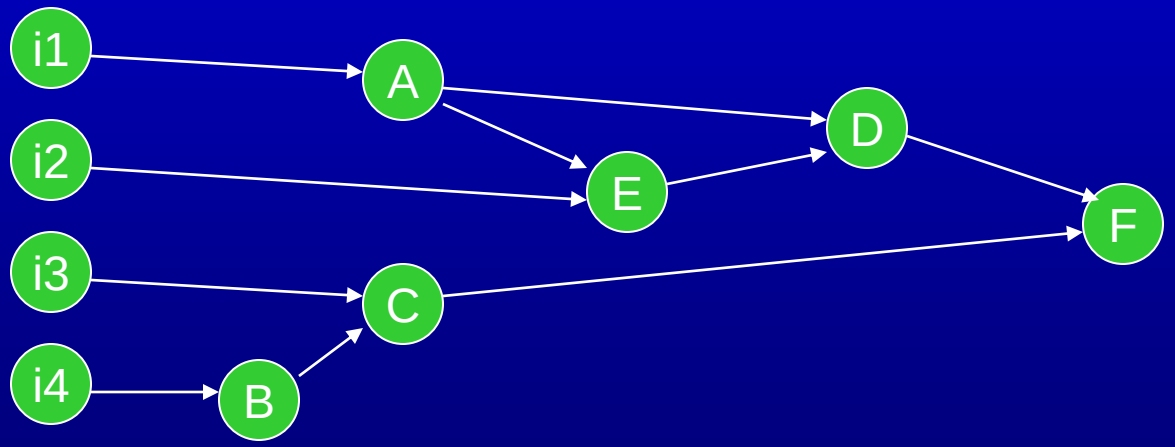
Simple Timing Model: Unit Delay



- Gate delay = 1 unit
- Same gate delay from all input pins
- Same delay for up and down transitions
- Same delay for all loads
- No wire delay
- All inputs ready at t=0

Delay Graph



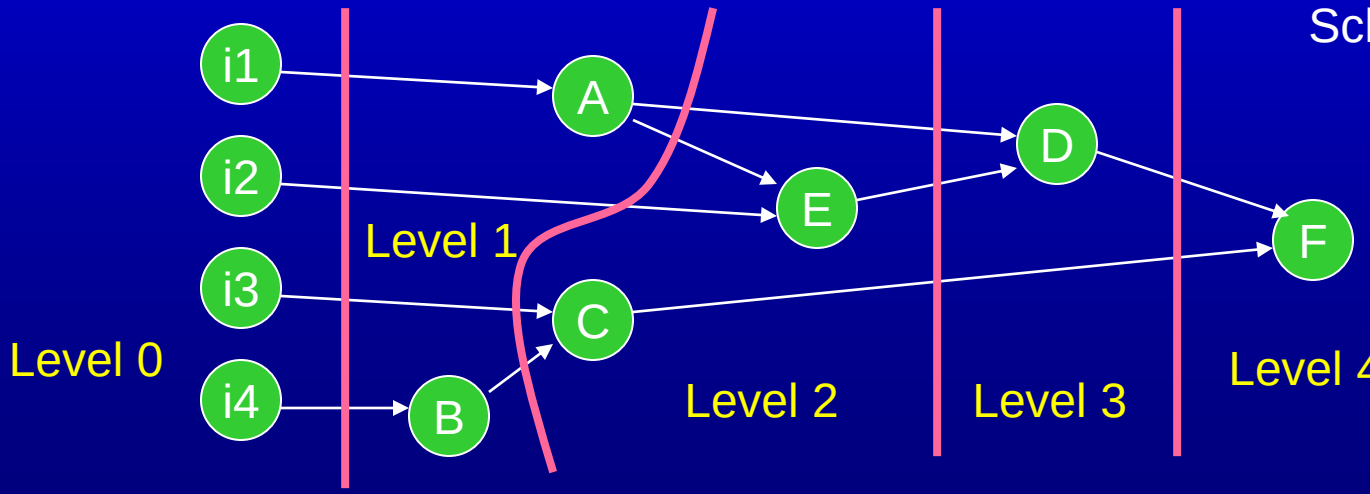


- Nodes = Nets
- Edges = Gates

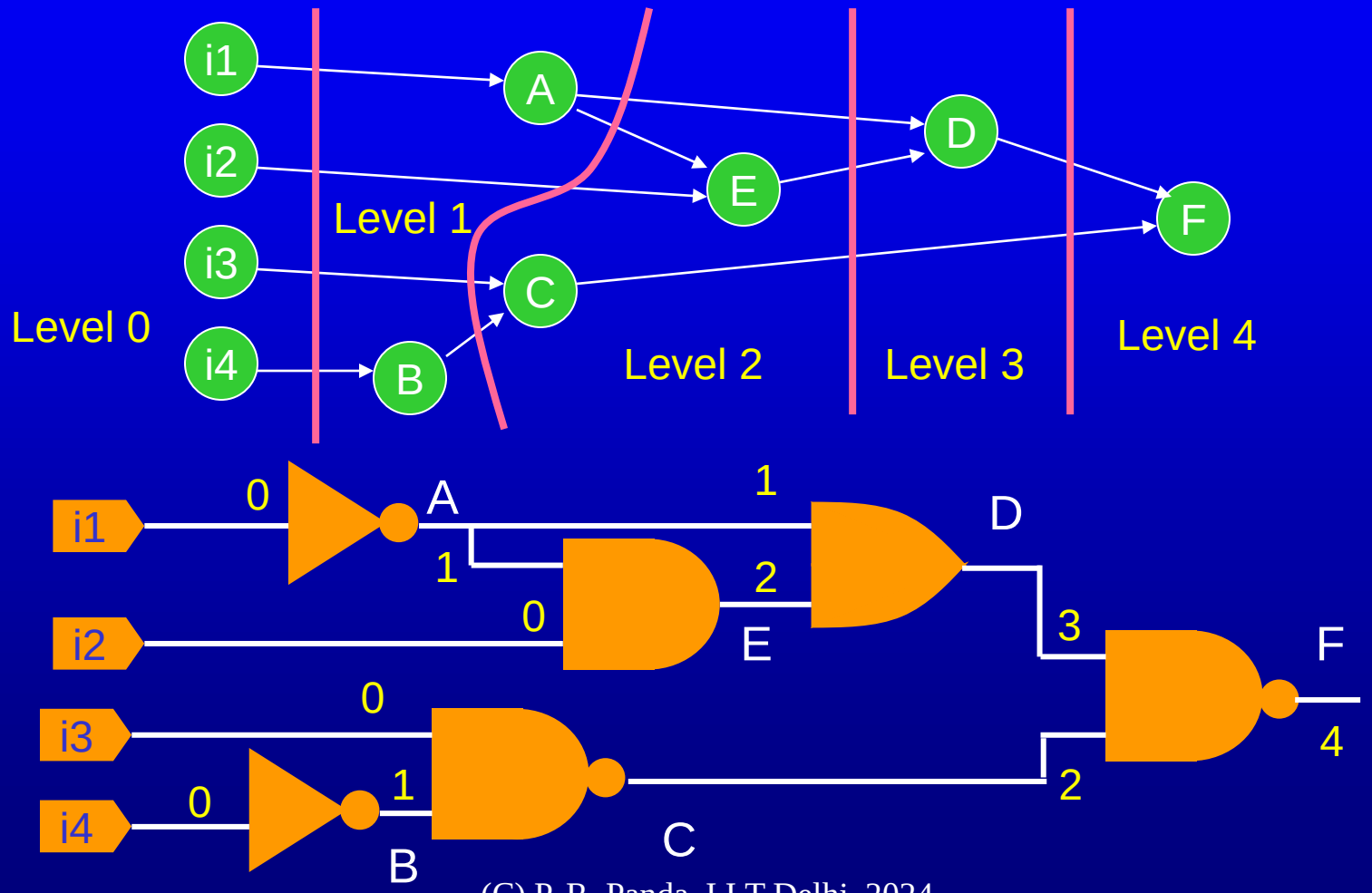
Levelising Algorithm

```
while all nodes not yet labelled
    for all nodes v
        If PRED(v) are assigned level < L
            Level (v) = L
    L = L + 1
```

Similar to ASAP Scheduling



Level is Estimate of Signal Arrival Time



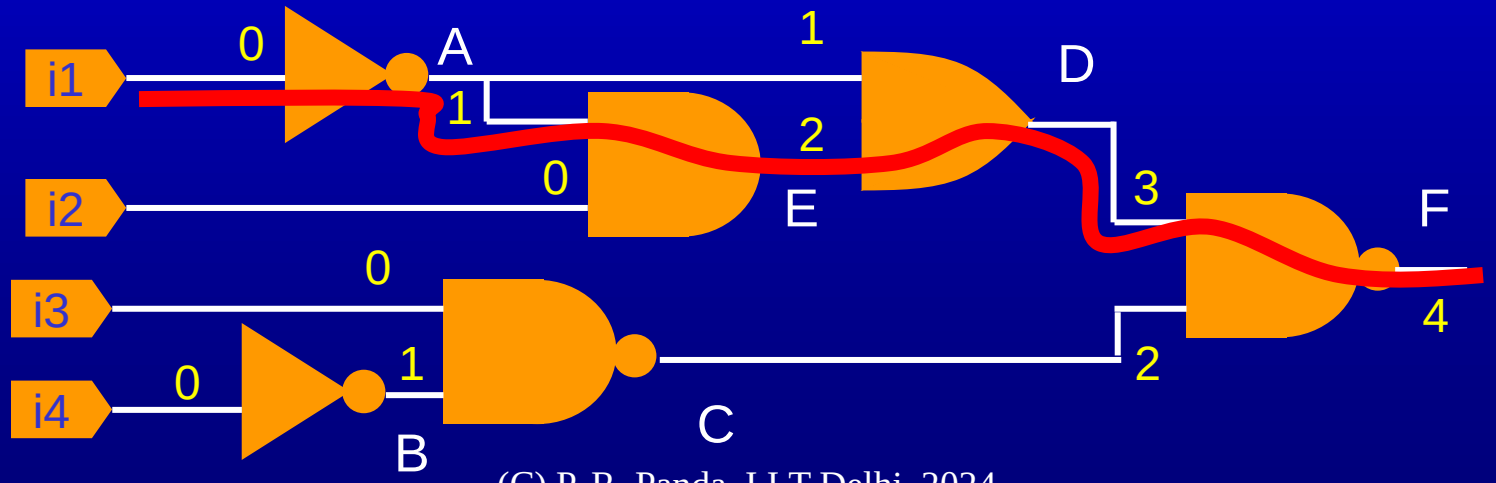
Critical Path found by Backtracking

Longest delay from any input to any output (on a sensitisable path)

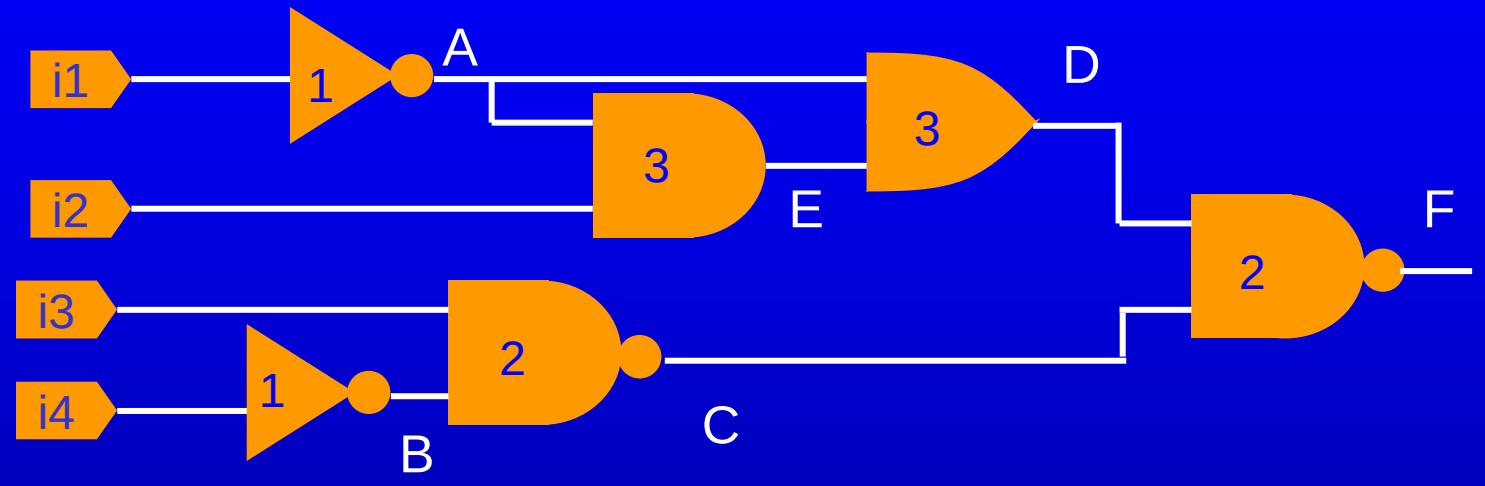
Longest delay from primary inputs to each node is known

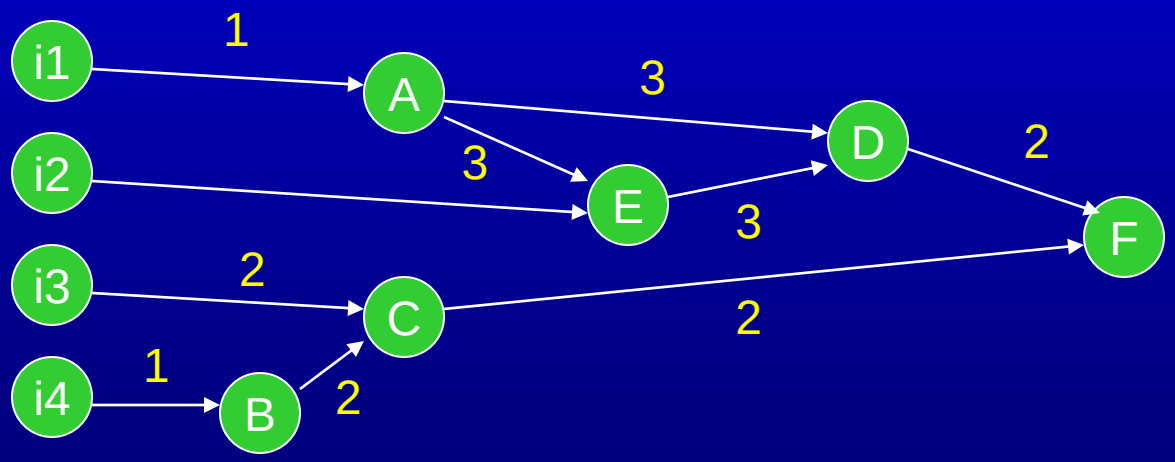
Find critical path by tracing back

- Start at output
- Recursively visit predecessor with highest level



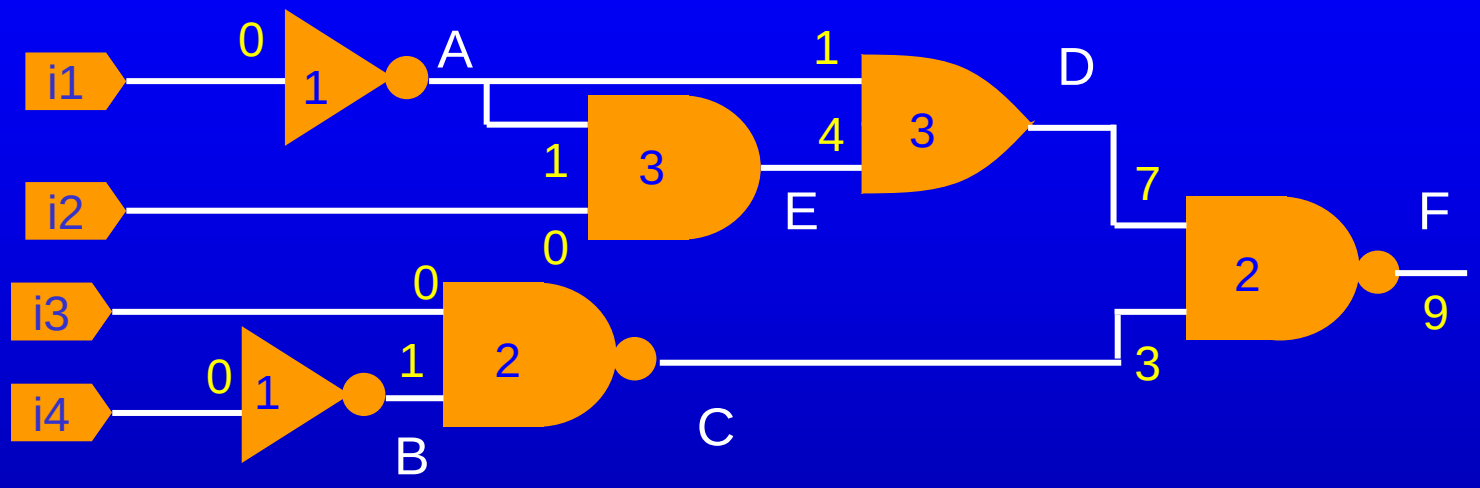
Relaxing Assumptions: Fixed Delay for Gates





- Nodes = Nets
- Edges = Gates
- Edge Weight = Gate delay

Signal Arrival Times



Use same algorithm

add delay (edge-wt) instead of incrementing level

Use latest input transition

Other Extensions

- Different pin-to-pin delays within a gate
  - use same graph, but different edges representing same gate have different delays
- Finding earliest arrival times
  - same algorithm, use MIN instead of MAX
- Finding shortest path
  - backtrace on delay graph using min. arrival times
- Non-zero arrival times at primary inputs
  - initialise appropriately

Required Arrival Times

- Also relevant to discuss required arrival times
  - Earliest time when a signal is required to arrive at a node
- Algorithm
  - start at output node
  - traverse delay graph backwards

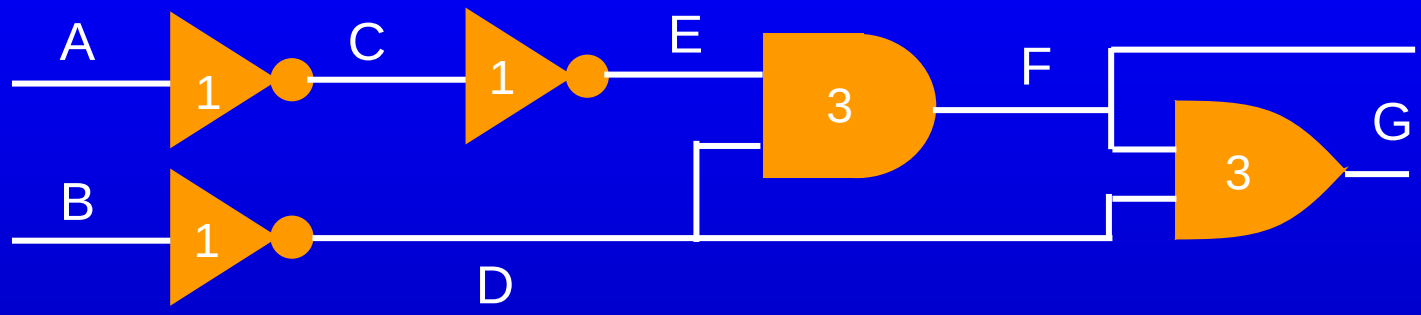
Slack

Slack = (Earliest Required Arrival Time) - (Latest Arrival Time)

Slack indicates Sensitivity of Circuit to Signal

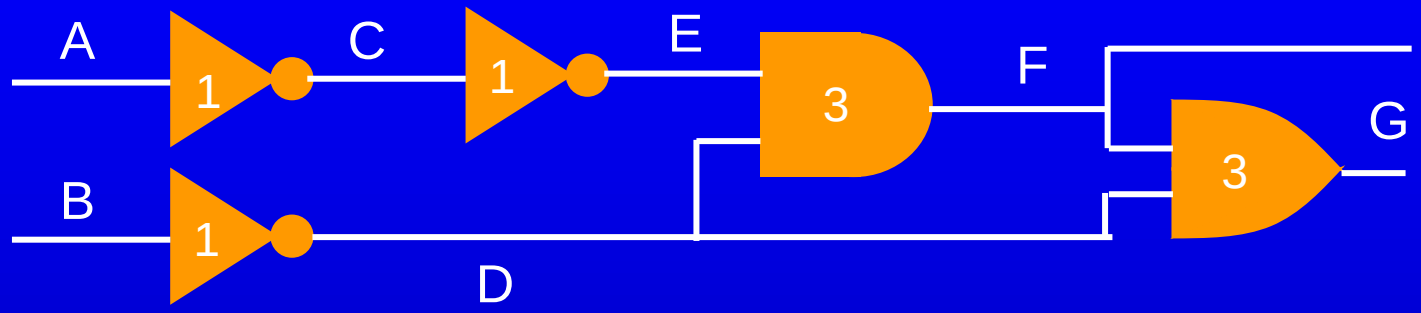
- If positive Slack T at node V
  - Signal at V can be delayed by T without affecting critical path of circuit
- If Slack = 0, V is on critical path
- If negative Slack at V
  - Signal will not meet requirement: will arrive too late
  - Indicates desired speed-up

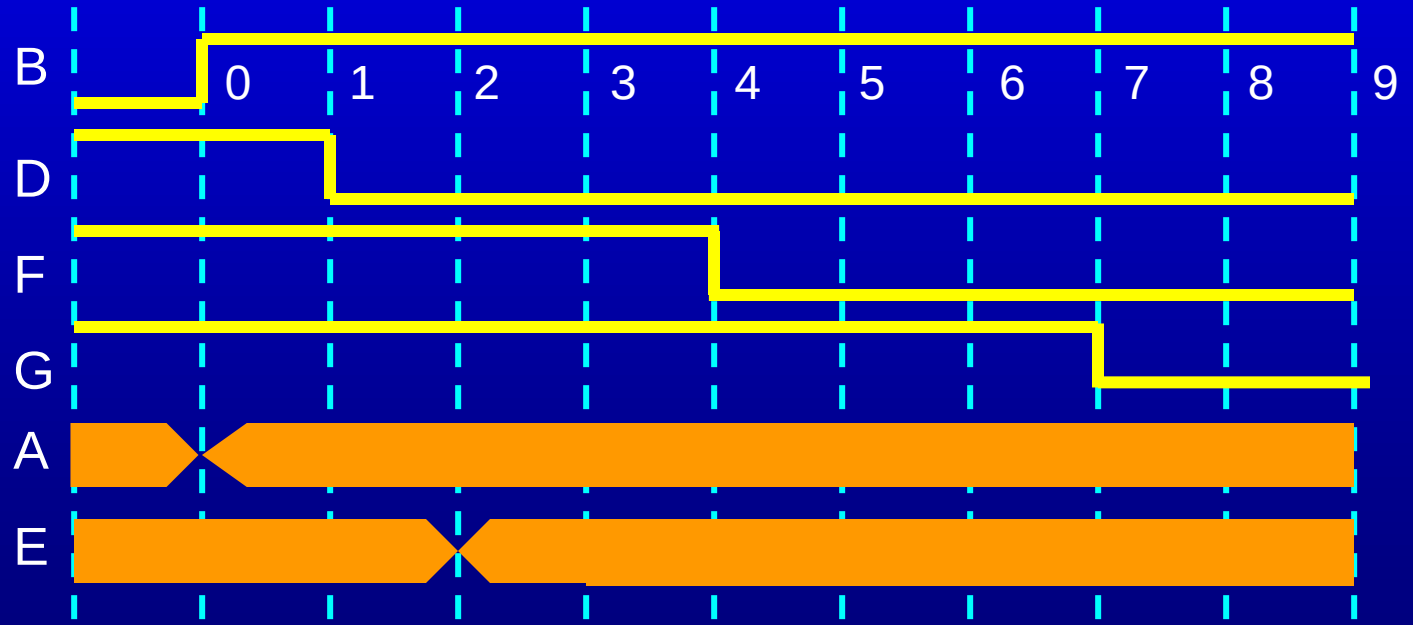
False Paths



- Longest path is A-C-E-F-G
  - delay = 1+1+3+3 = 8
- Can this path be sensitised?
  - keep other inputs constant
  - change in A should cause change in G

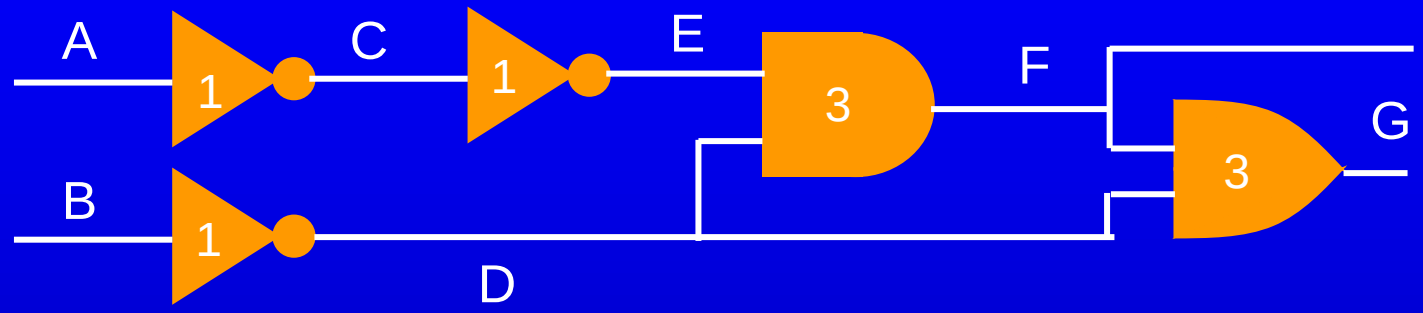
Path Sensitisation

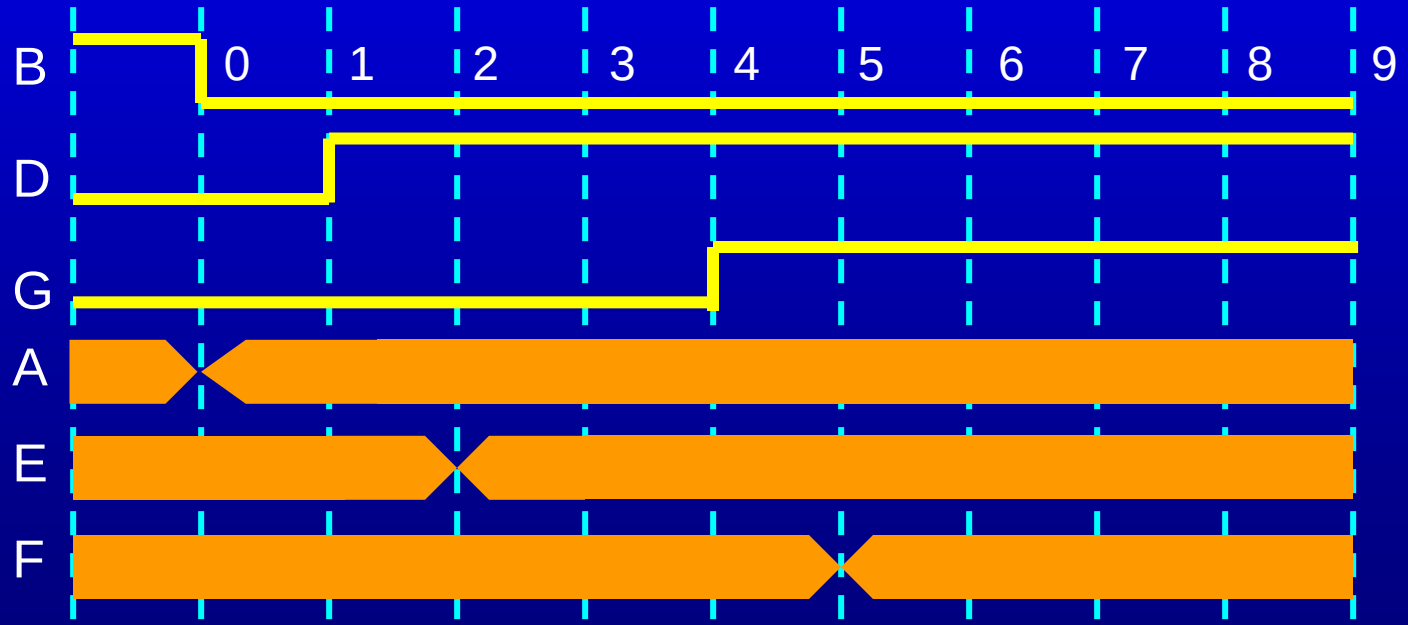




Input transition at A has no impact on G

Path Sensitisation





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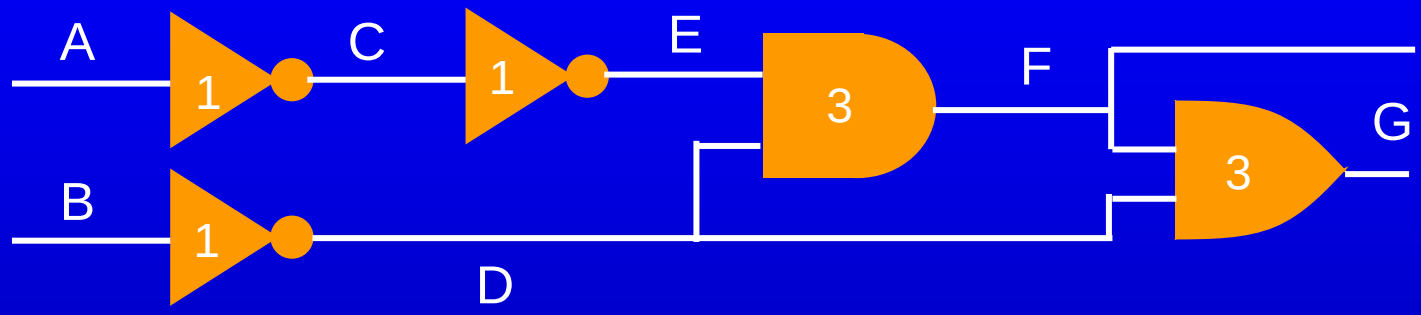
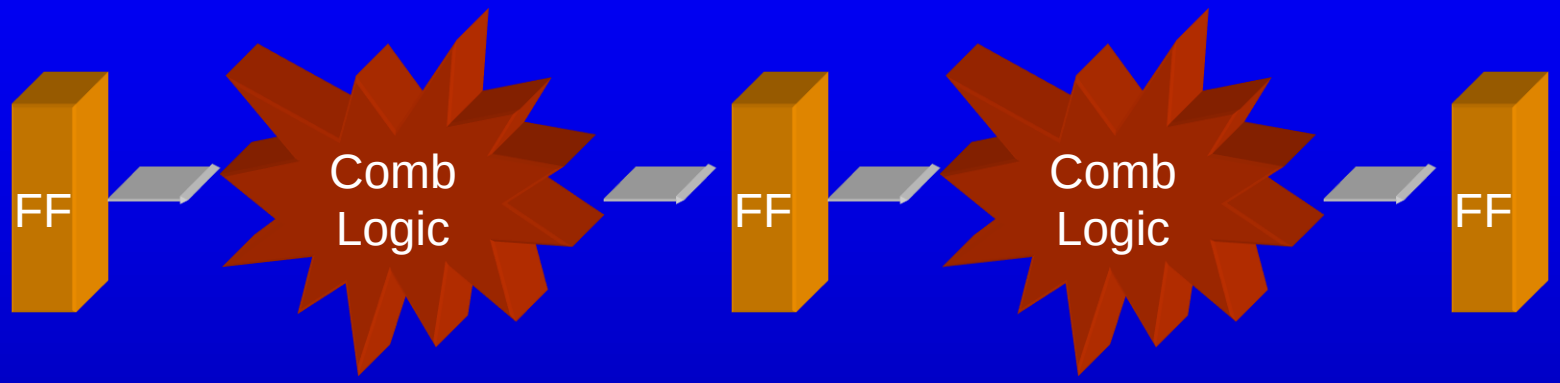
False Paths



- Longest path A-C-E-F-G is a FALSE PATH
  - It can never be sensitised
- Critical Path is B-D-F-G
  - delay = 1 + 3 + 3 = 7
- Necessary to examine the logic!
  - cannot treat the gates as black boxes

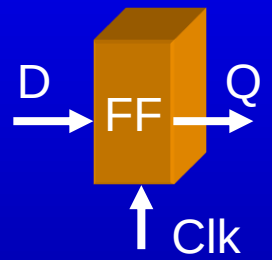
Sequential Circuit Timing

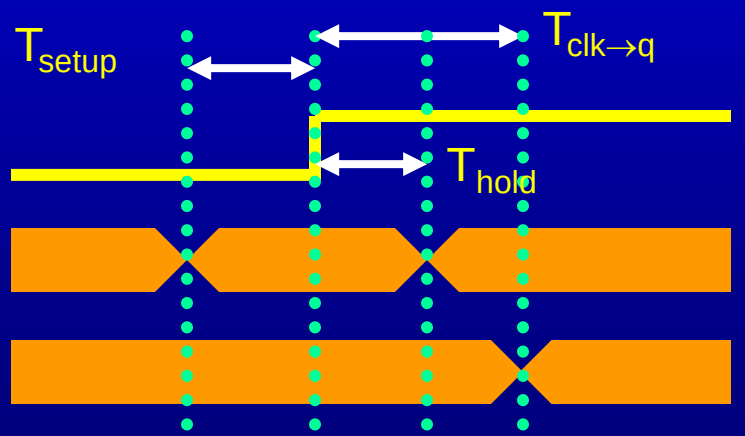


- Earlier analysis valid for combinational logic part
- Flip-flop timing has to be considered

Flip-flop Timing

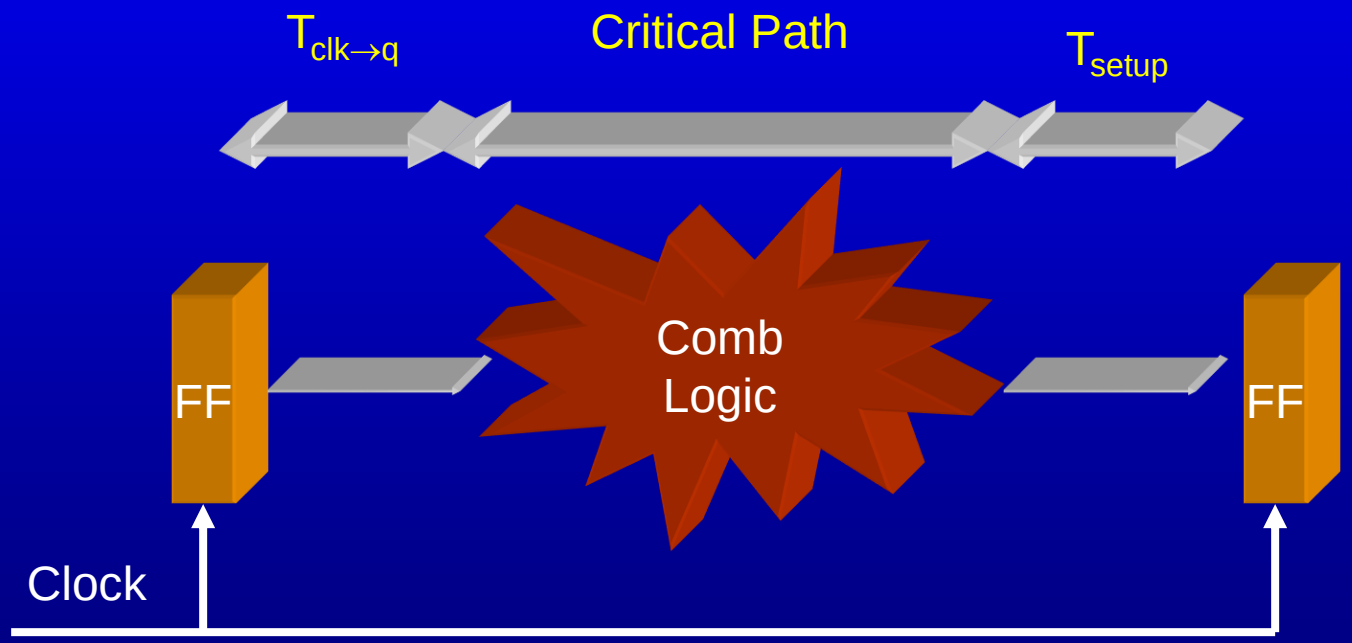
- D-Flip-flop operation
  - On rising edge of clock, D propagates to Q after a delay $T_{clk \rightarrow q}$
- Timing constraints
  - D must stabilise T_{setup} before clock edge
  - D must remain stable for T_{hold} after clock edge





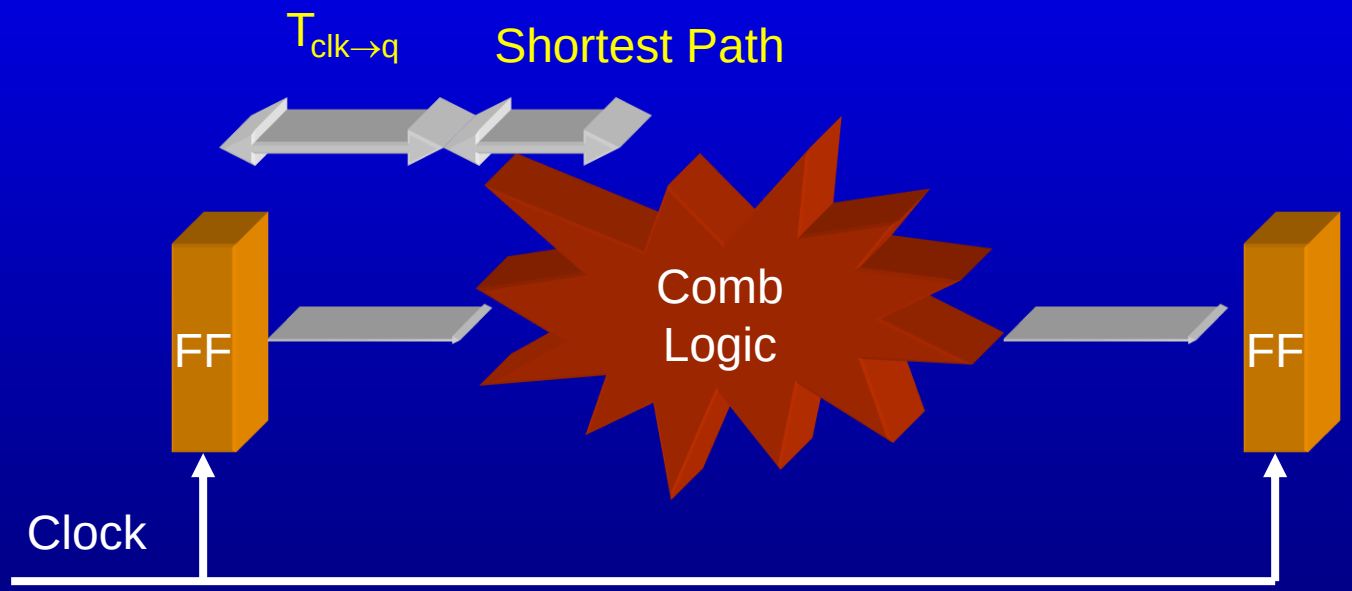
Sequential Circuit Timing: Max. Delay Constraint

$T_{clk \rightarrow q}$ + Critical Path + T_{setup} < Clock Period



Sequential Circuit Timing: Min. Delay Constraint

$T_{clk \rightarrow q}$ + Shortest Path Delay > T_{hold}



Delay Modeling: Extensions

- Variable gate delays
  - depends on output load
  - depends on input slew
- Unequal rising and falling transitions
  - depends on transistor types
- Significant wire delays
  - wire capacitance needs to be modelled