

# COL215L: Digital Logic & System Design

## Lecture 5: CMOS Circuits (Cont.)



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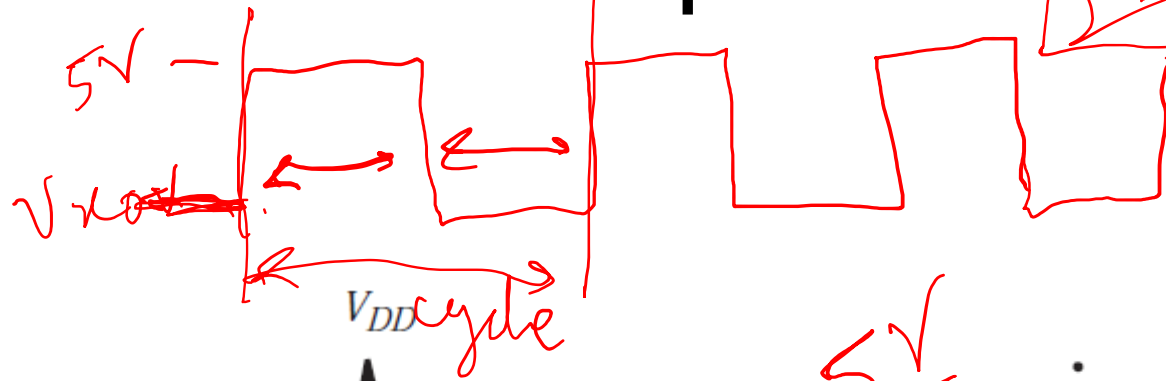
August 18, 2021

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# Agenda

- Previously
  - Dynamic behavior
  - Propagation delay
- Today
  - Power dissipation
  - Fan-in and fan-out limitations

# Power Dissipation



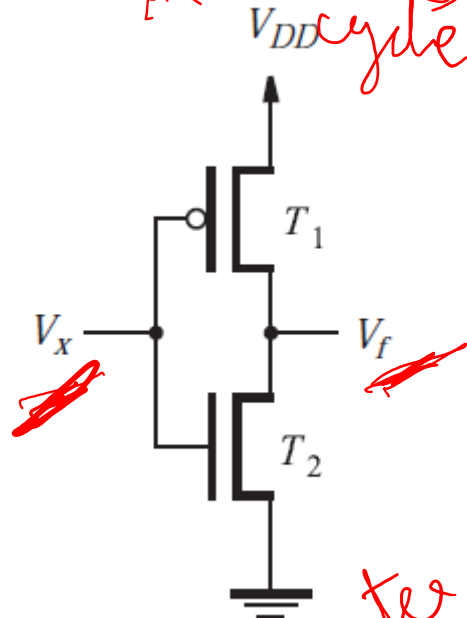
Handwritten notes and equations:

$$E_{total} = C V_{DD}^2$$

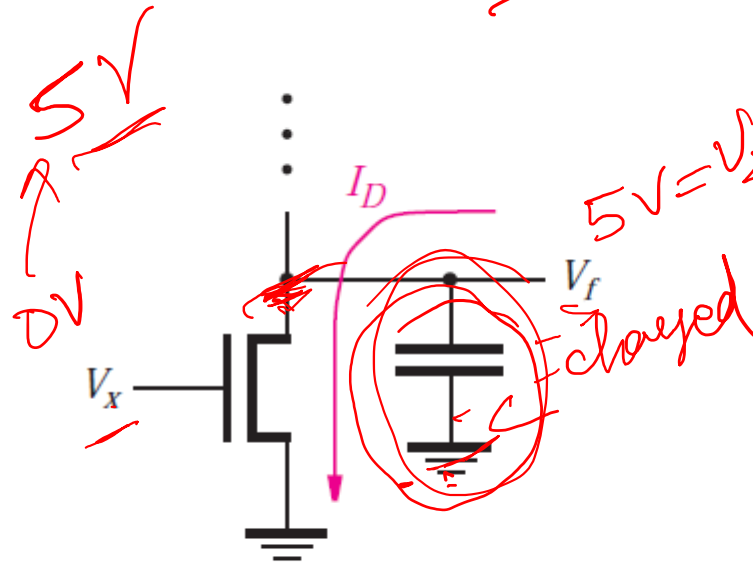
$$P = \frac{1}{2} C V_{DD}^2 f$$

Handwritten equation:

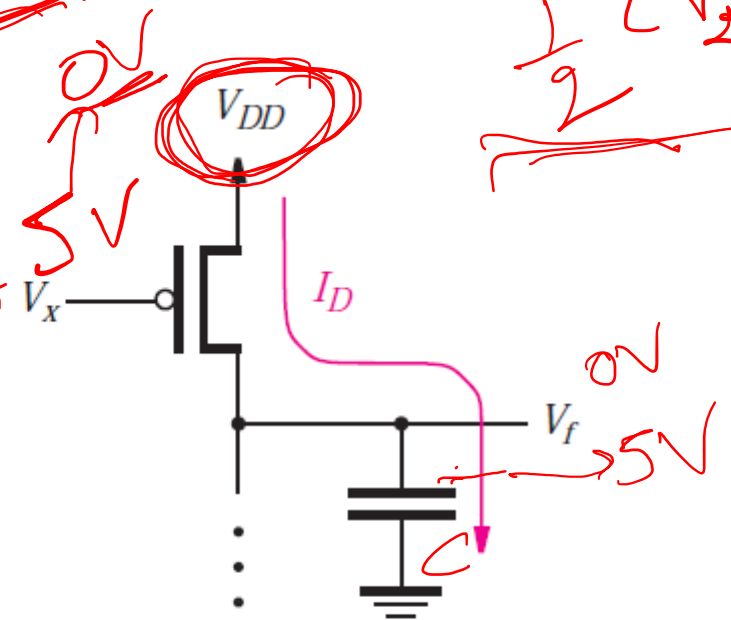
$$\frac{1}{2} C V_{DD}^2$$



Inverter



(a) Current flow when input  $V_x$  changes from 0 V to 5 V



(b) Current flow when input  $V_x$  changes from 5 V to 0 V

$f \rightarrow$  frequency

Handwritten equation:

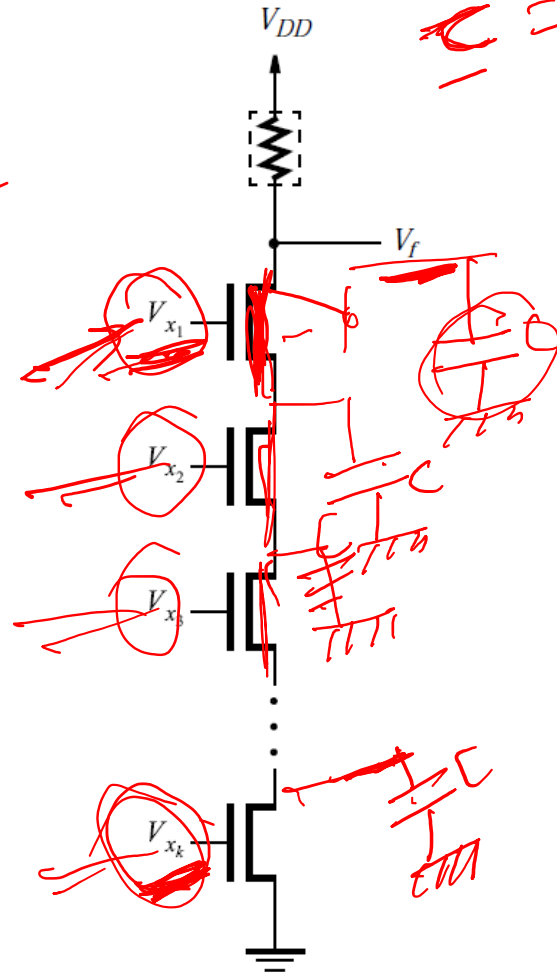
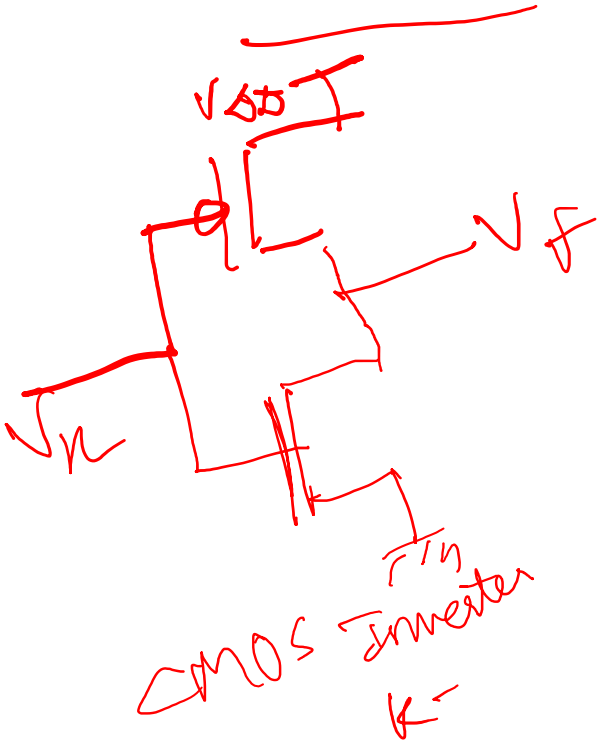
$$P_d = f \cdot C V_{DD}^2$$

# Impact of High Fan-in

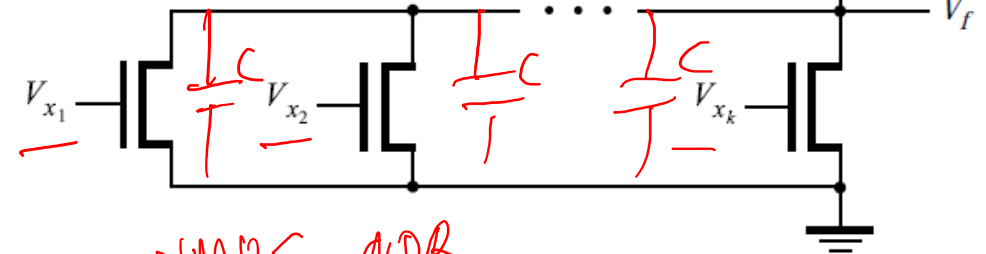
propagation delay  
Y inputs

$\tau = R_{eq} \cdot C_{eq}$

$kC$



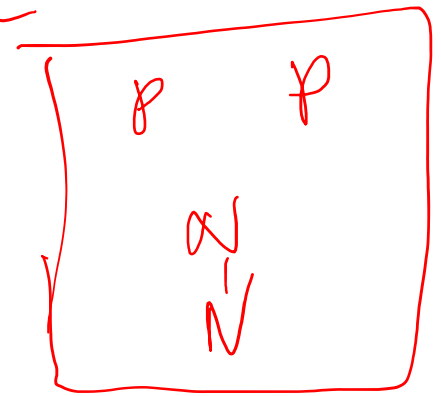
CMOS NAND



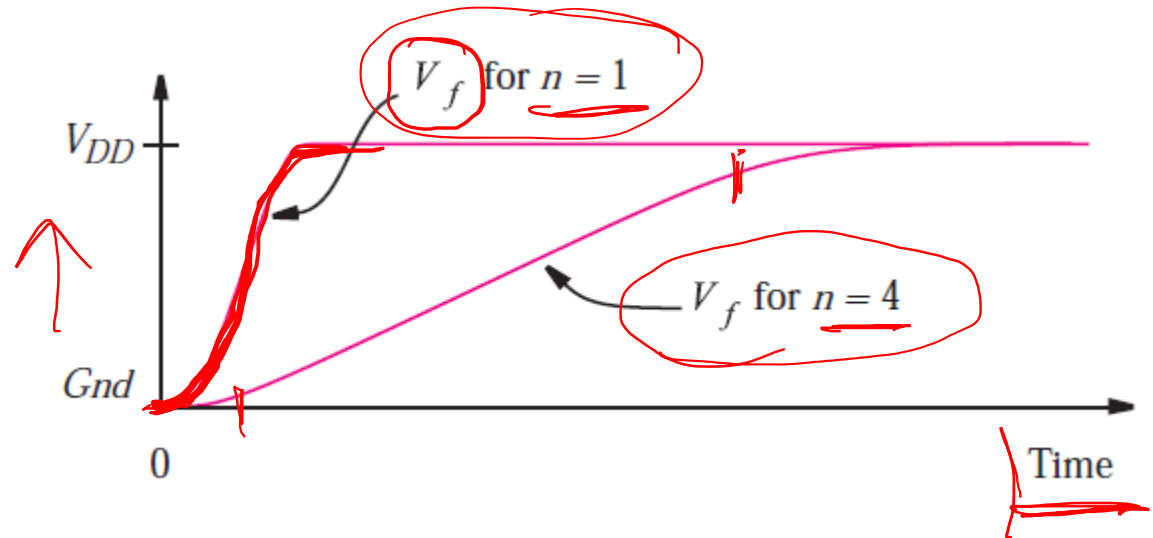
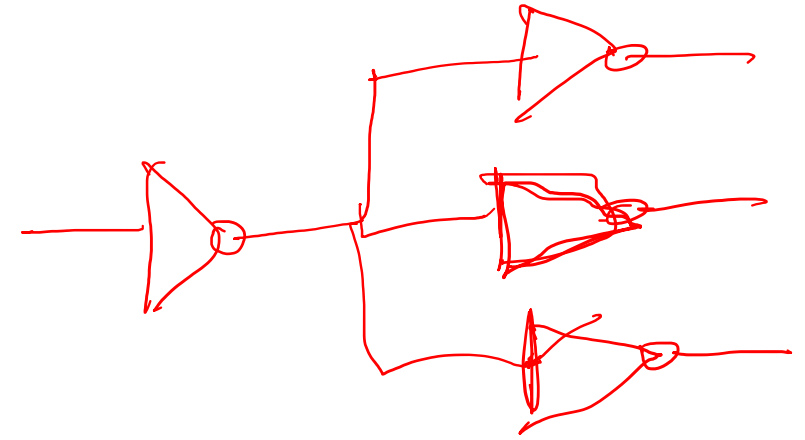
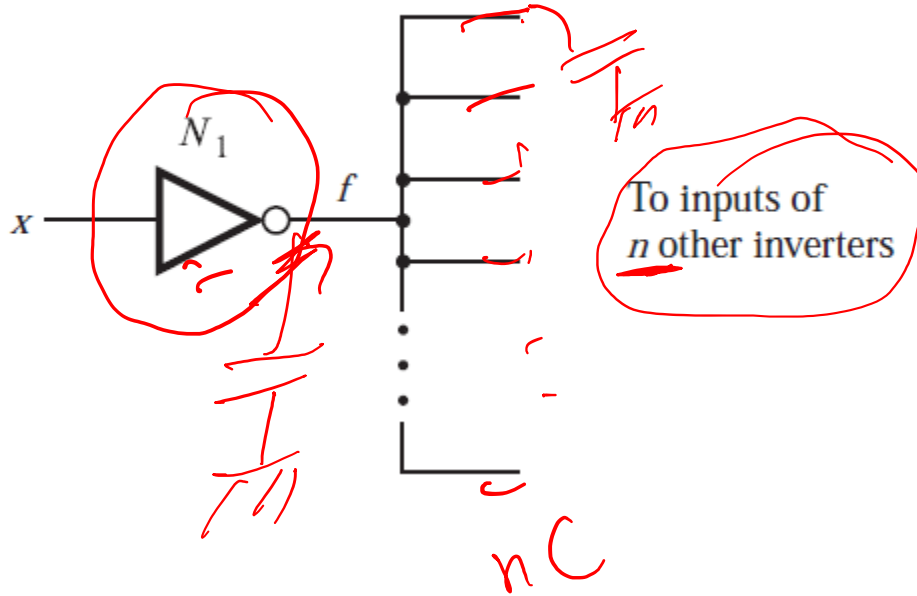
NMOS NOR

$kC$

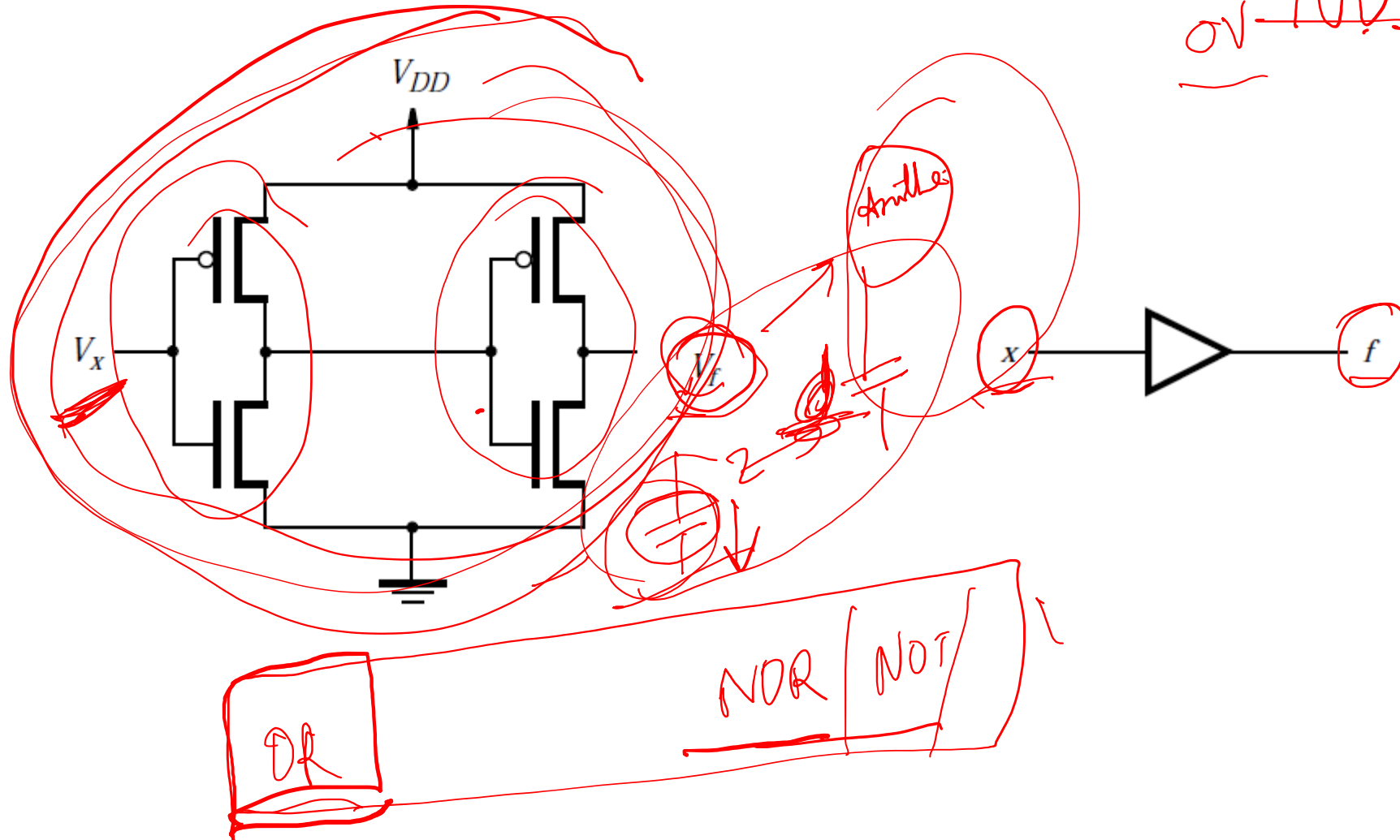
CMOS



# Impact of High Fan-out

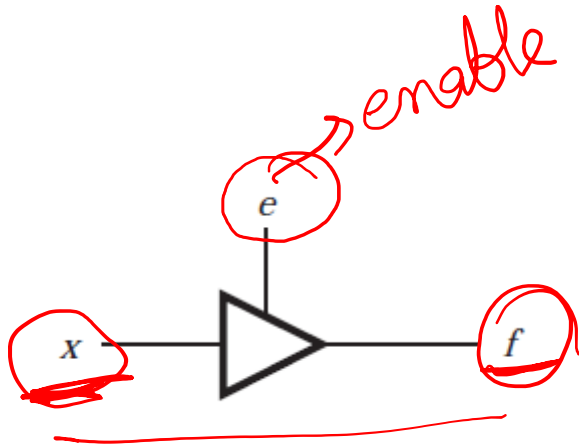


# Buffers



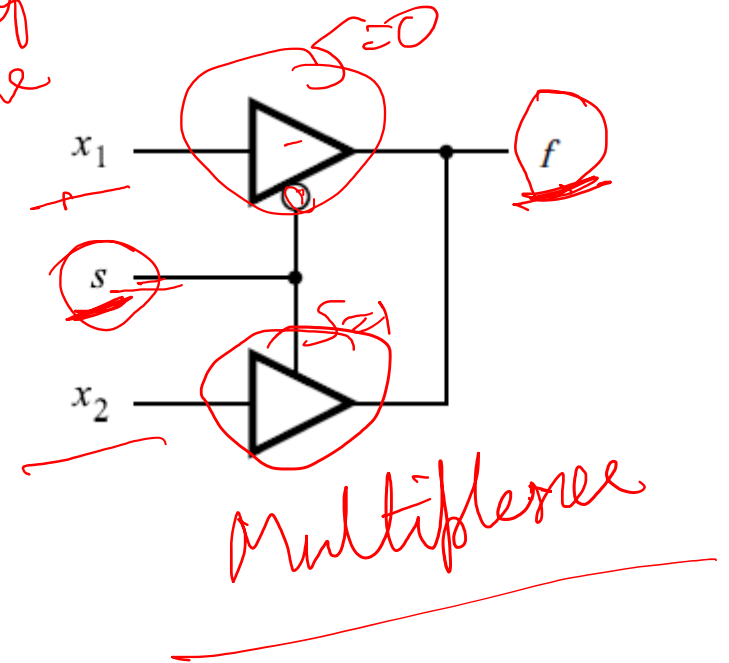
5V ~~~~~~~~~ ↑  
→  
~~~~~~~~~  
0V ~~~~~~~~~  
↓

# Tri-state Buffer

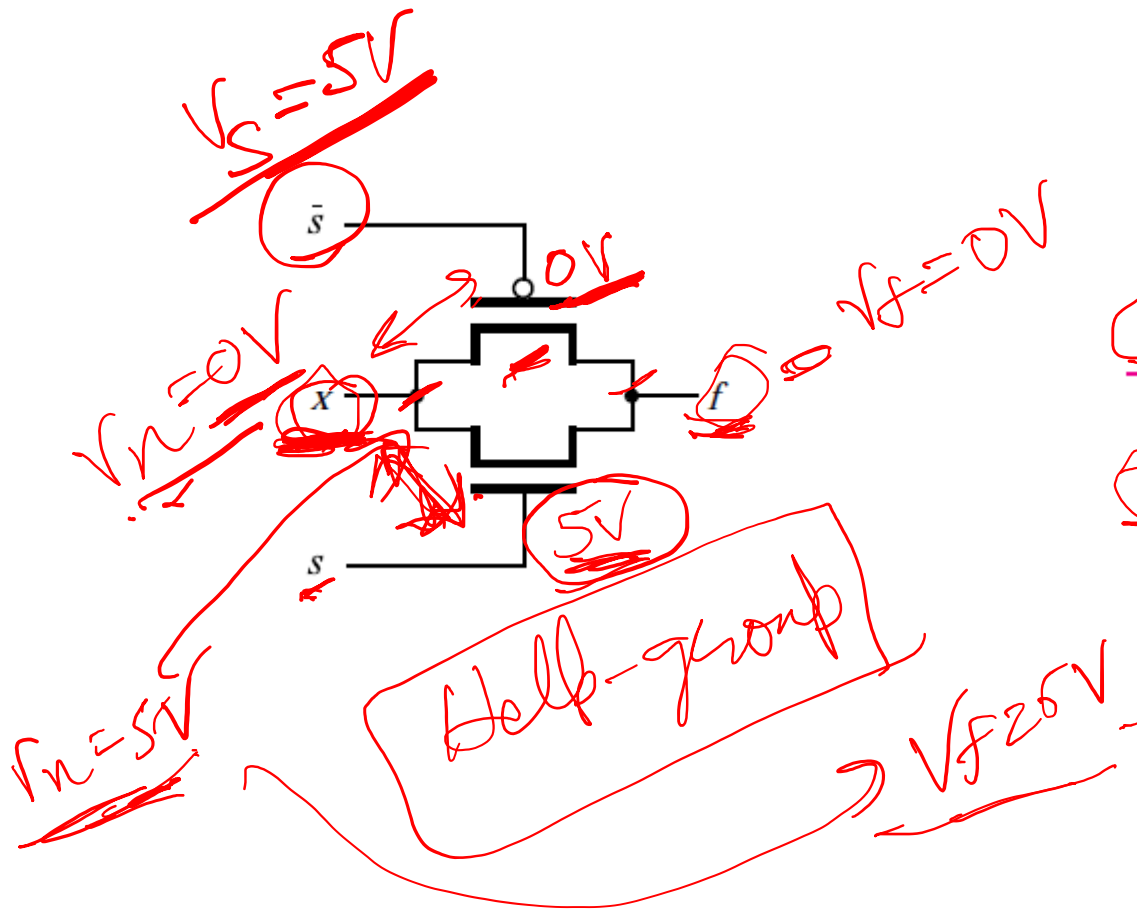


| $e$ | $x$ | $f$ |
|-----|-----|-----|
| 0   | 0   | Z   |
| 0   | 1   | Z   |
| 1   | 0   | 0   |
| 1   | 1   | 1   |

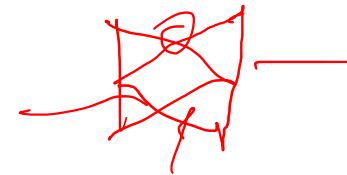
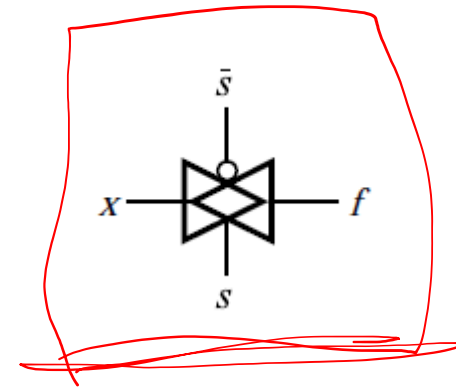
Handwritten red notes: "floating state" with arrows pointing to the 'Z' (high impedance) outputs in the first two rows of the truth table.



# Transmission Gate



| $s$ | $f$ |
|-----|-----|
| 0   | Z   |
| 1   | x   |





# XOR Gate

