

COL216

Computer Architecture

Input/Output – 3

21st March 2022

Interrupts/Exceptions

What are exceptions

- Unusual events/conditions
 - Source: internal or external
 - Synchronous or asynchronous
 - Intentional or unintentional
- Require change in flow of control
 - Mechanism to alter the control flow
 - Event identification and response to it
 - Halt or resume original control flow

Hardware and Software Interrupts

■ Software interrupts

- caused by specific instructions to get some system service
- alternative terms : system calls, traps, exceptions

■ Hardware interrupts are caused by events/conditions detected by hardware

- intentional : e.g., I/O event
- unintentional : e.g., hardware fault, power outage, arithmetic overflow

Terminology

Exceptions vs. Interrupts

- Use both the terms interchangeably
- MIPS, ARM: exception - internal as well as external, interrupt - external
- Intel 80x86: interrupt - internal as well as external
- PowerPC: exception - unusual event, interrupt - change in flow of control

Examples of exceptions

◆ synchronous

◆ asynchronous

	Intentional	Unintentional
Internal	Invoke OS function, Trace/debug	Access to privileged inst, Overflow/underflow, Undefined instruction, Hardware malfunction
External	I/O device request	Mem access exception, Alignment error, Timeouts, Power down, Hardware malfunction

Interrupt identification and response

- S/w interrupt identified during instruction decoding
- H/w interrupt identified by checking specific signals
- Response mechanism in both cases (h/w and s/w interrupts) is same
 - execution of some code : interrupt handler or interrupt service routine (**ISR**)
 - after serving interrupt, terminate or resume

Checking for exceptions



undefined instruction
checked here

overflow
checked here



hardware interrupts can be checked any time

ISR vs normal subroutine

- Processors have two or more modes
 - normal mode / user mode
 - privileged mode / kernel mode / supervisor mode
- Application program executes in user mode
- To do certain privileged tasks, execution of some code in OS kernel is required
- ISR executes in privileged mode, provides controlled access to kernel functions

How exceptions are handled

uninterrupted execution



interrupt and halt



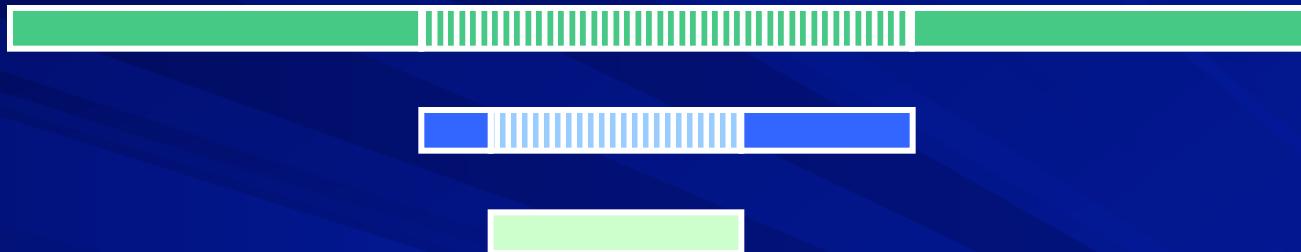
interrupt and resume
(vectored interrupt)



interrupt and resume
(non-vectored)



Nested interrupts



Exceptions in ARM

Exception type	Mode	Address
Reset	Supervisor	0x00000000
Undef instr	Undefined	0x00000004
S/W interrupt	Supervisor	0x00000008
Prefetch Abort	Abort	0x0000000C
Data Abort	Abort	0x00000010
Interrupt	IRQ	0x00000018
Fast interrupt	FIQ	0x0000001C

SWI software interrupt

cond	1111	comment
4	4	24

- Control transferred to address 0x00000008
- Mode changes to ‘supervisor’ mode
- CPSR (Current Processor Status Register) is saved in SPSR_{svc} (Saved Processor Status Register)
- PC is saved in R14_{svc}
- Comment field may specify a particular service/function

Processor status register



ARM register set

Mode	Registers			SP	LR	PC
	R0-R7	R8-R12	R13			
User:			R14	R15	CPSR	
System:						
Supervisor:			R13	R14		SPSR
Abort:			R13	R14		SPSR
Undefined:			R13	R14		SPSR
Interrupt:			R13	R14		SPSR
Fast int:	R8-R12	R13	R14			SPSR

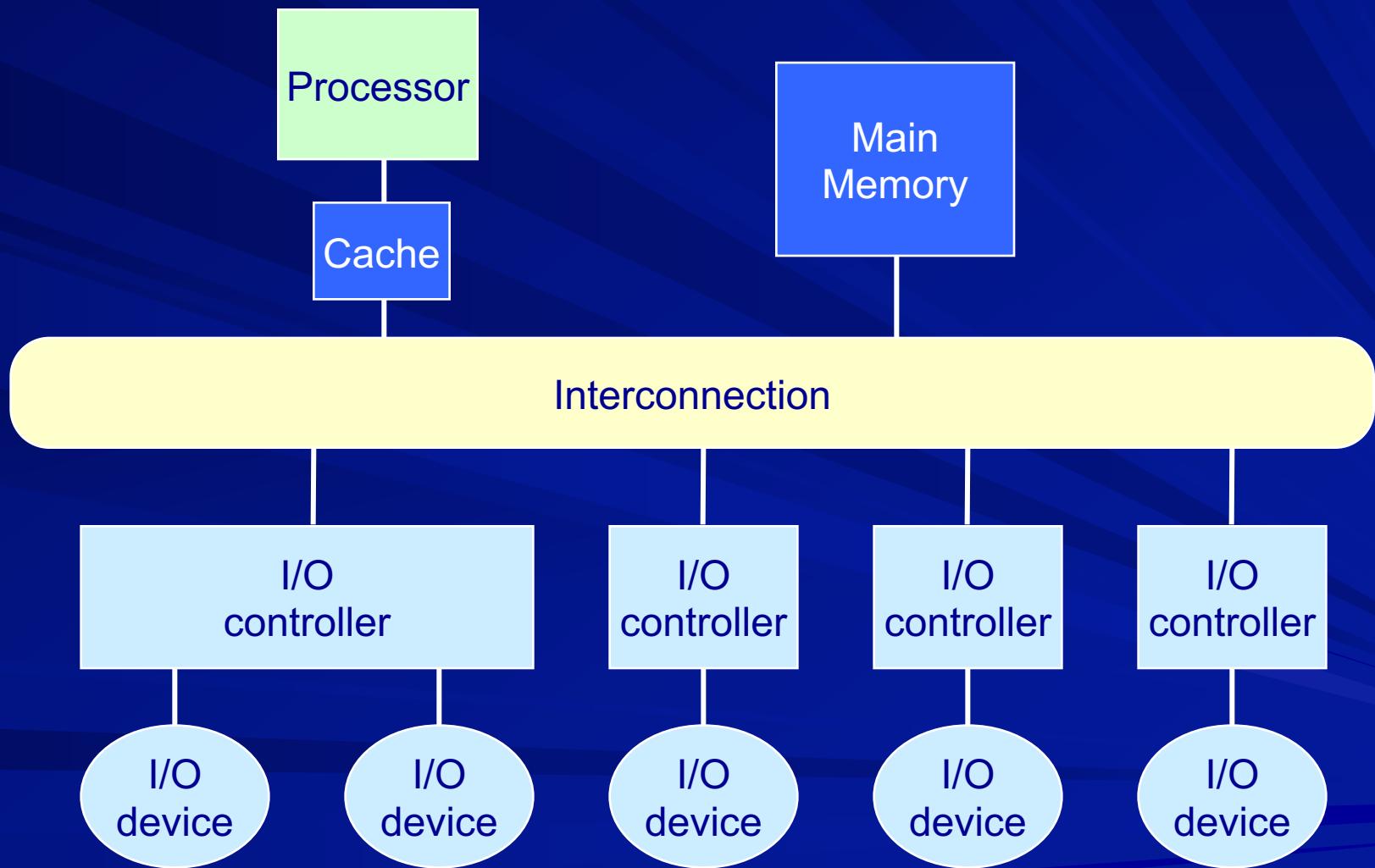
Total 37

Exception handling in pipelined design

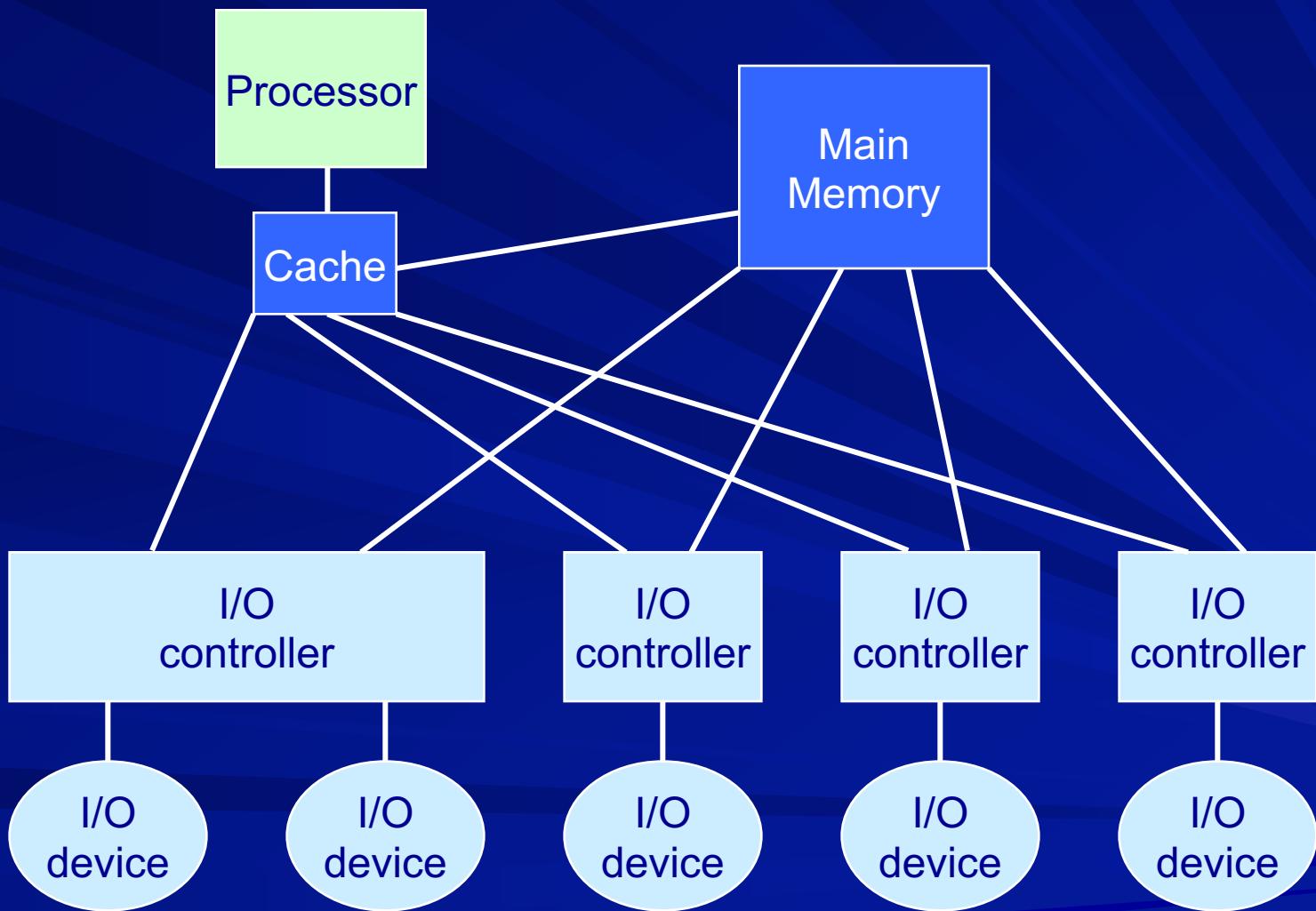
- Difficulty in status saving
 - multiple instructions under execution
- Possibility of
 - multiple exceptions in same cycle
 - change in order of exceptions
- Handling approaches
 - precise
 - imprecise

Interconnecting Subsystems

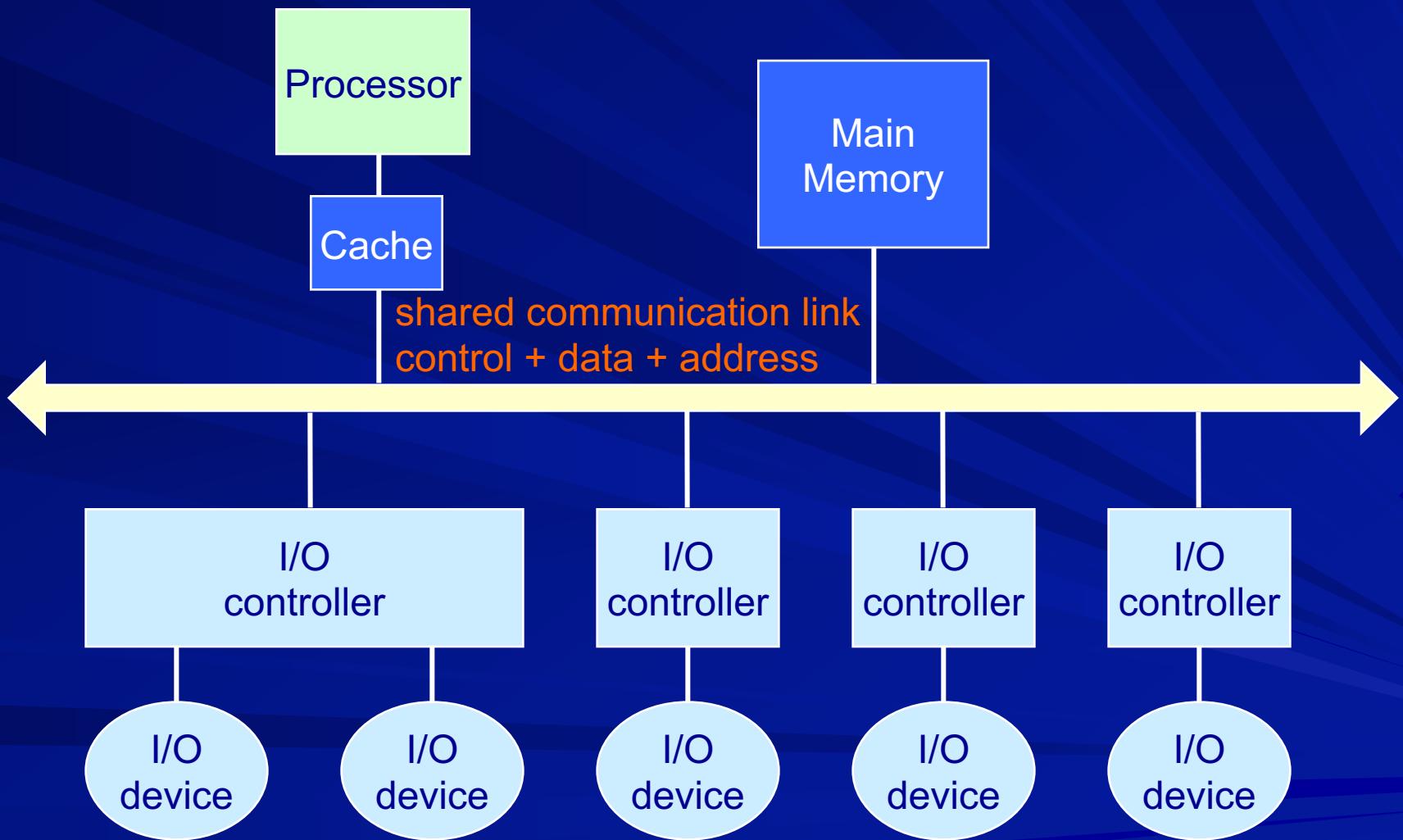
Interconnecting Subsystems



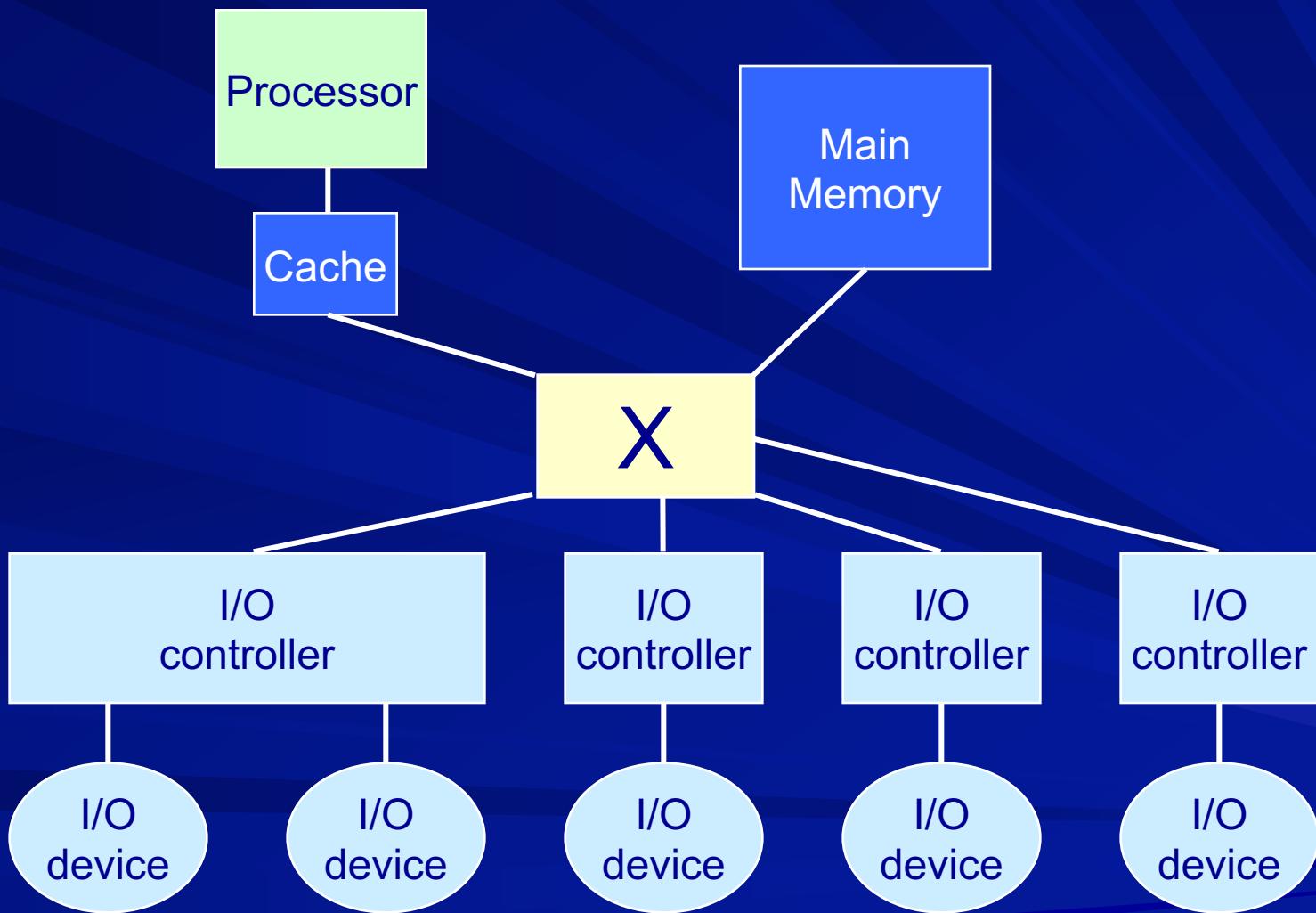
Point to point connections



Single bus connecting all



Cross bar switch



Comparison

	<u>P to P</u>	<u>Bus</u>	<u>X-bar</u>
Cost	high	low	high
Throughput	high	low	high
Ports	multi	single	single
Expansion	difficult	easy	difficult

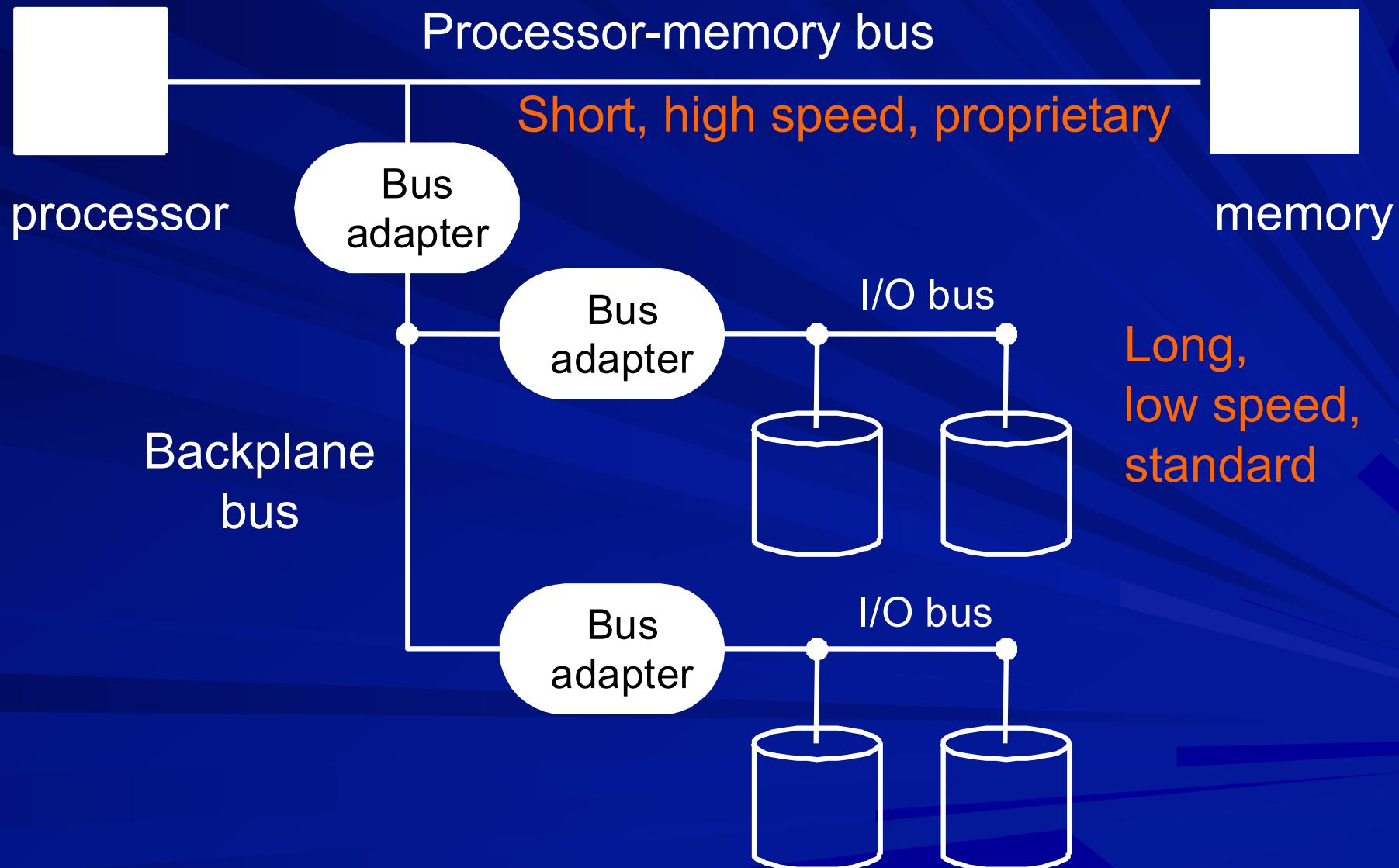
Multi-buses: More performance, more cost

Multi-switches: Lower cost, same performance

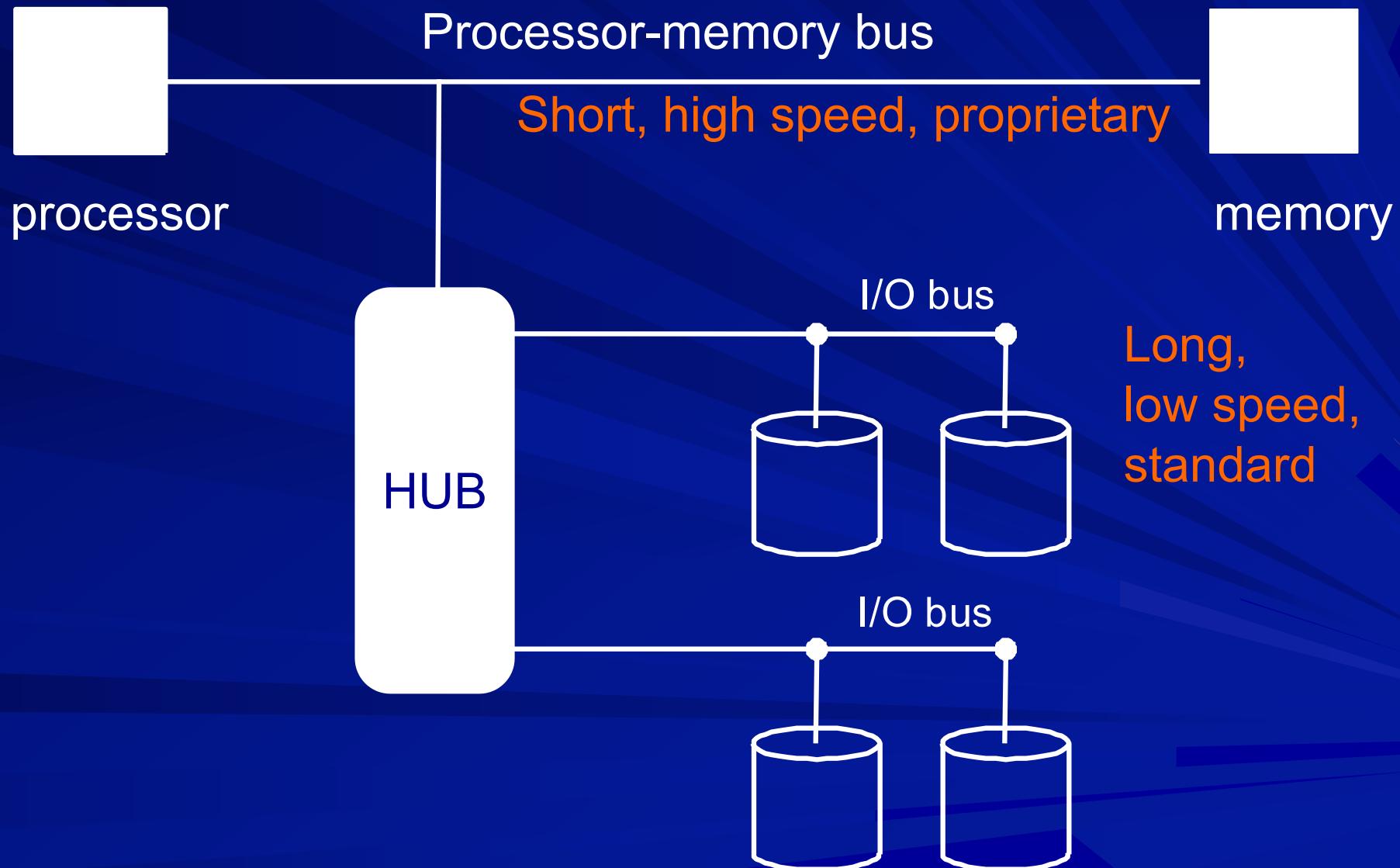
Backplane bus



System with multiple buses



System with multiple buses



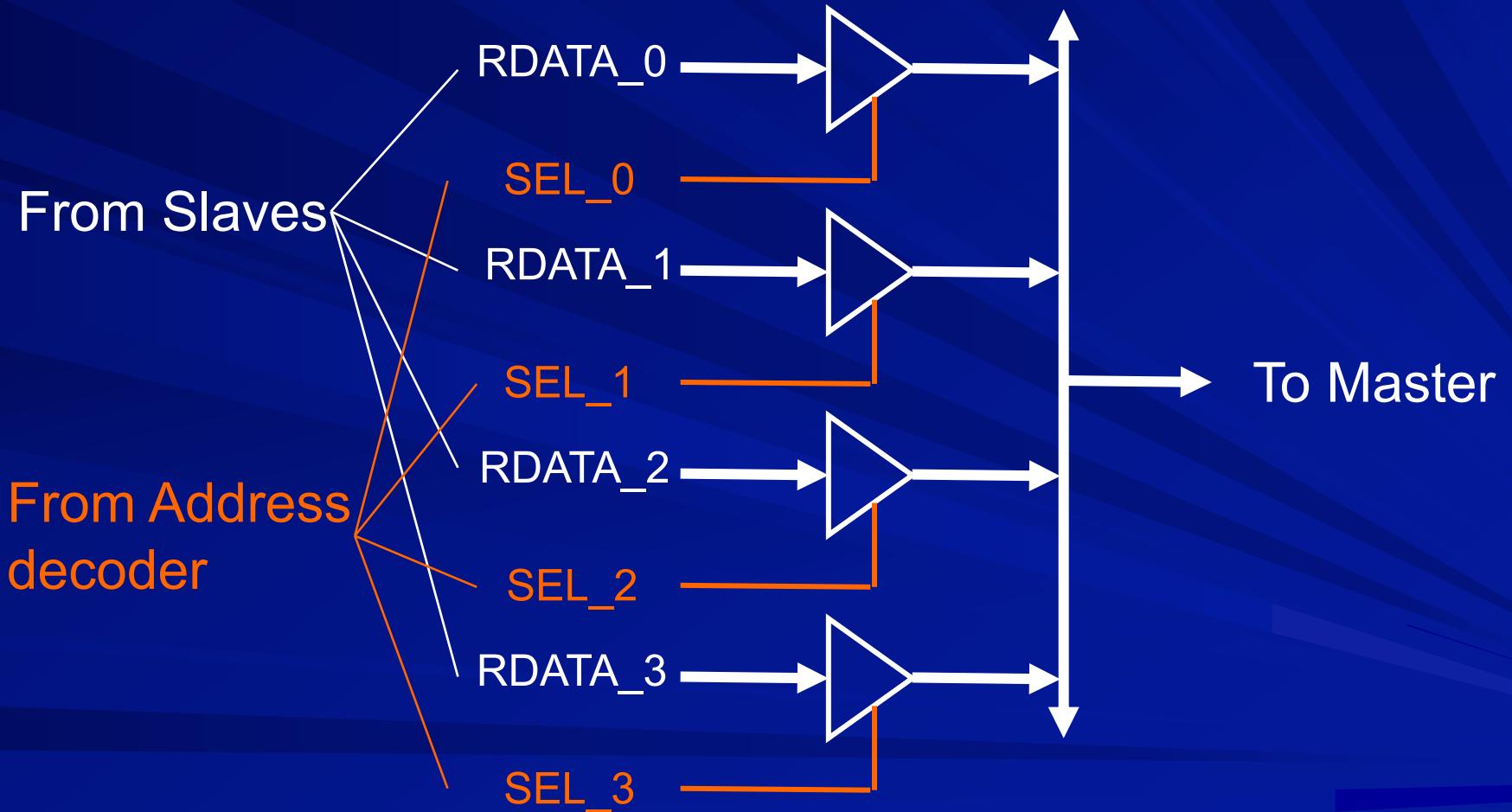
Bus Standards

- Physical / mechanical
 - Pins, connectors, cables
- Electrical
 - Voltage / current levels, impedances
- Logical
 - Definition of signals
 - Timings and protocols

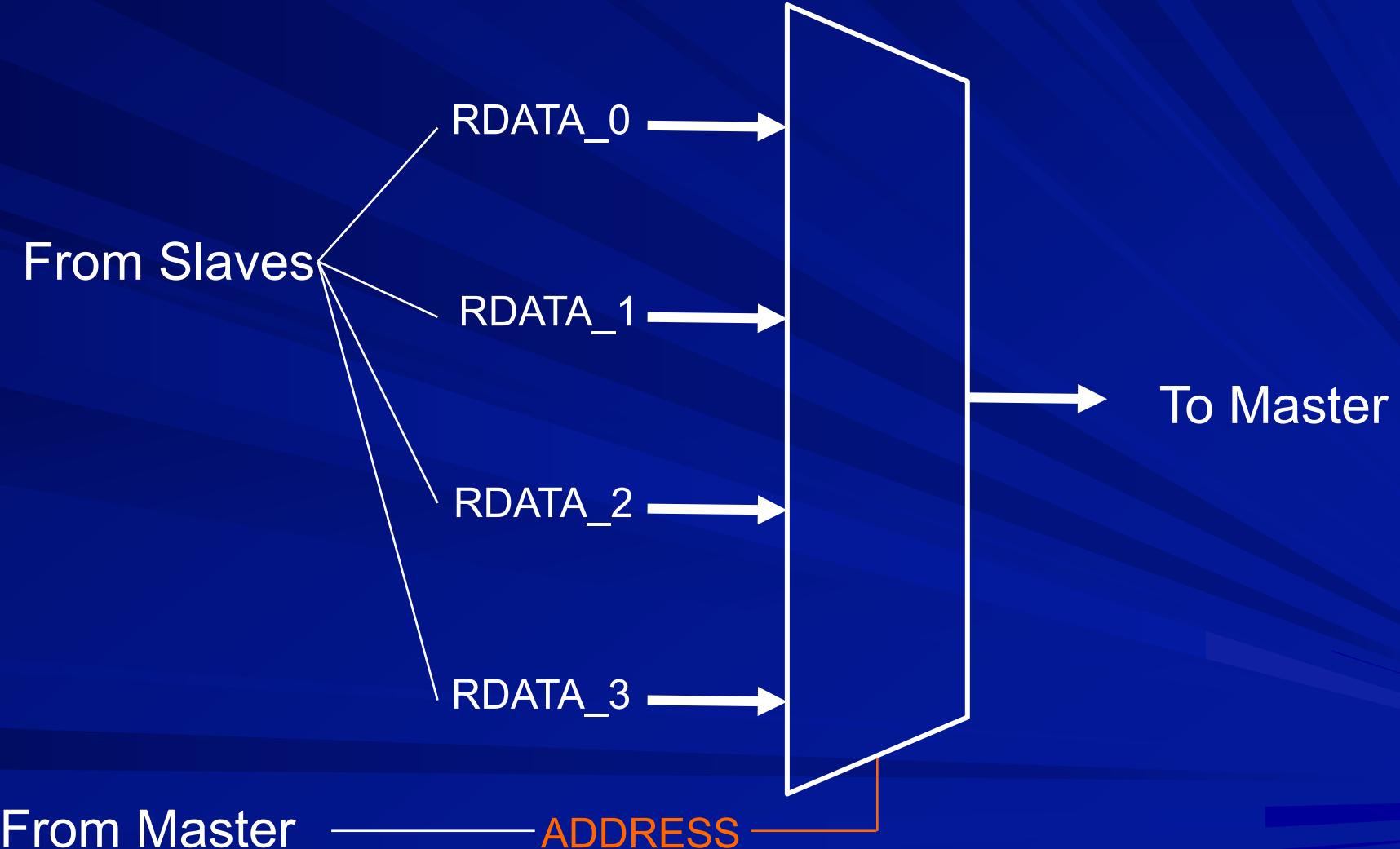
Subsystems on the buses

- Master
 - Initiates transfer
- Slave
 - Responds to master
- Bridge /
bus adapter
 - Connects two buses
- Hub
 - Connects many buses
- Arbiter
 - Resolves master requests
- Decoder
 - Selects slaves

Tri-state Bus



Multiplexed Bus



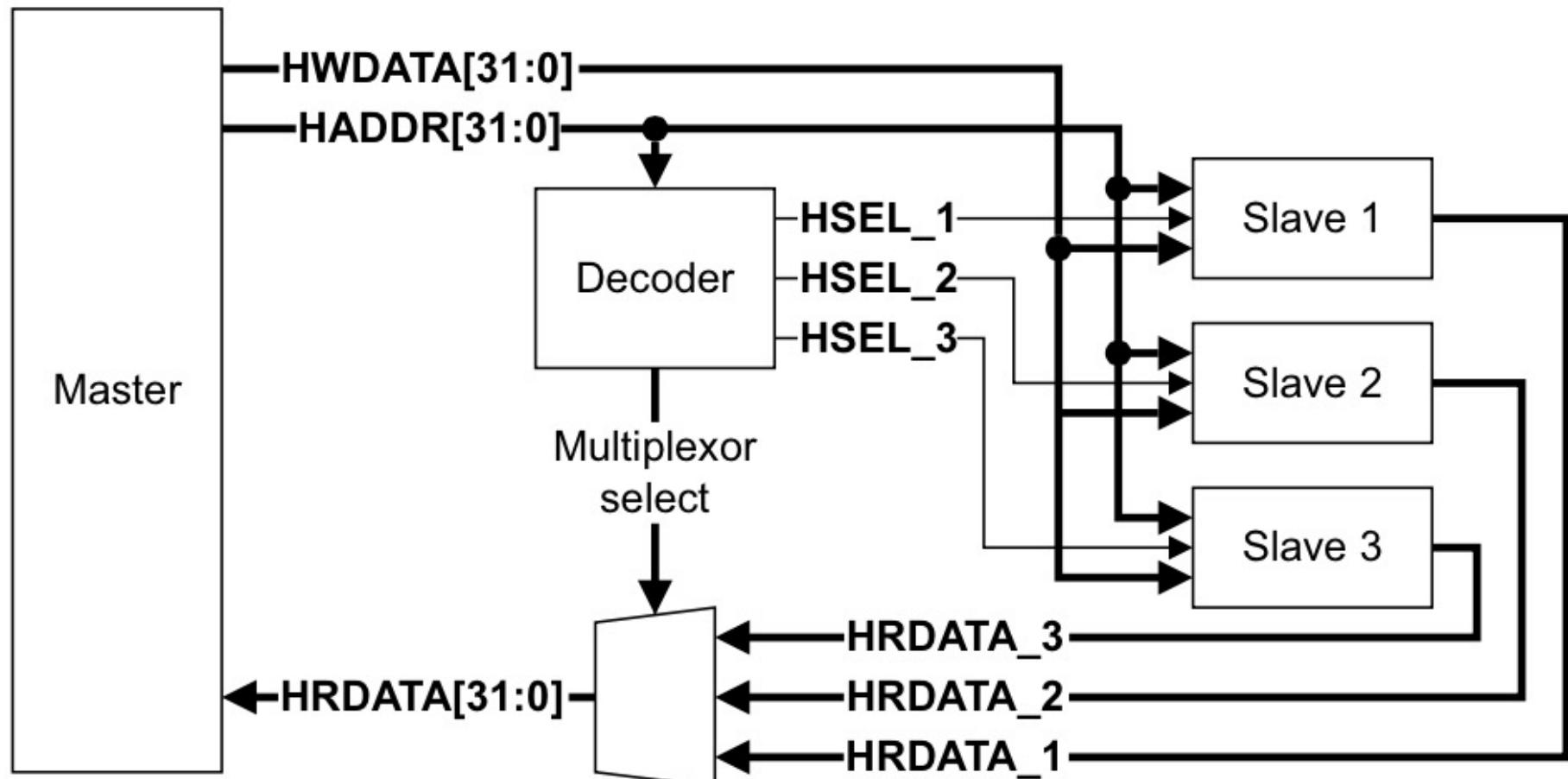
AMBA : Advanced Microcontroller Bus Architecture

- ARM open standard for on-chip buses
- For System-on-Chip (SoC)
- Variants
 - AHB : Advanced High speed Bus
 - APB : Advanced Peripheral Bus
 - AXI : Advanced eXtensible Interface
 - AHB-Lite : subset of AHB

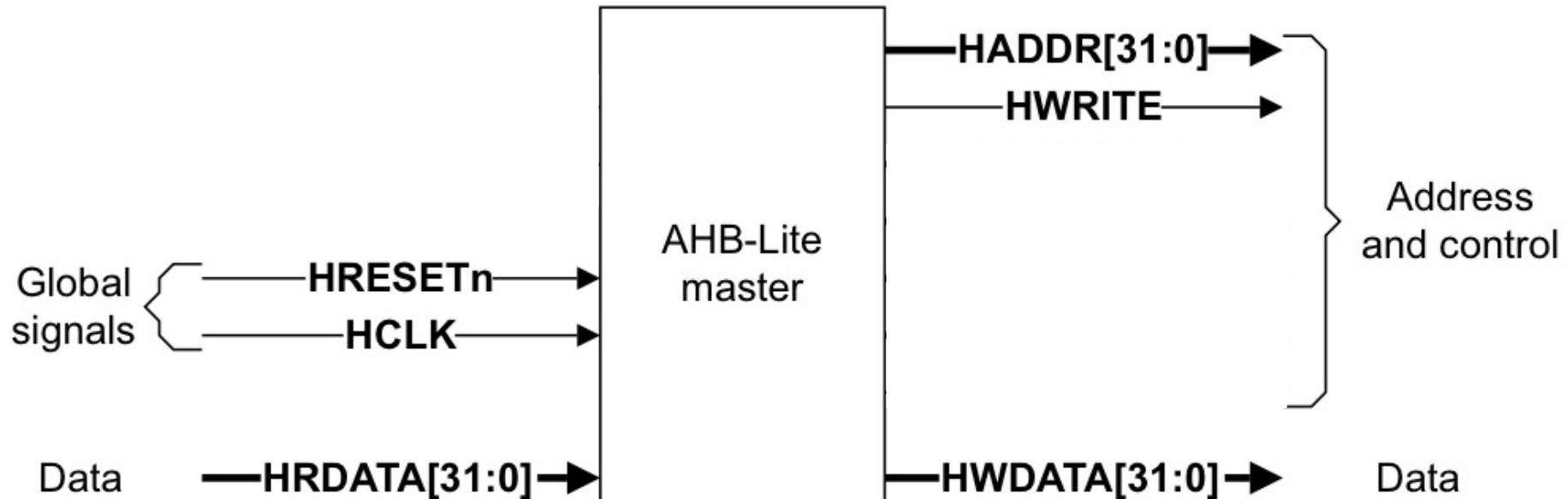
AHB-Lite

- Single master, multiple slaves
- Parallel
- Multiplexed (not tri-state)
- Separate data, address, control
- Synchronous
- Pipelined
- Burst transfer supported
- Split transaction not supported

AHB-Lite Block Diagram

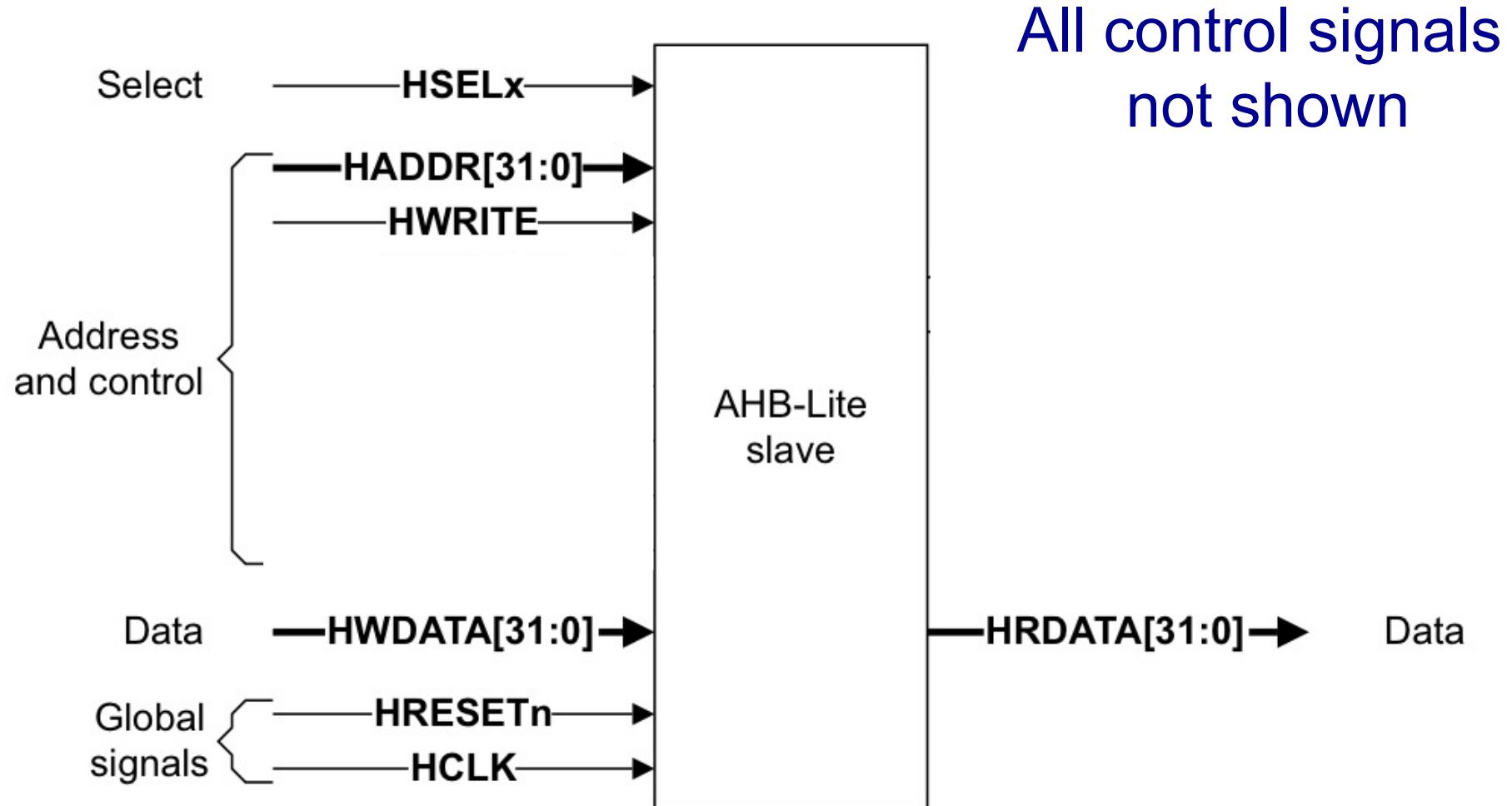


Master Interface



All control signals not shown

Slave Interface



THANKS