COL215L: Digital Logic & System Design

Lecture 20: Finite State Machines

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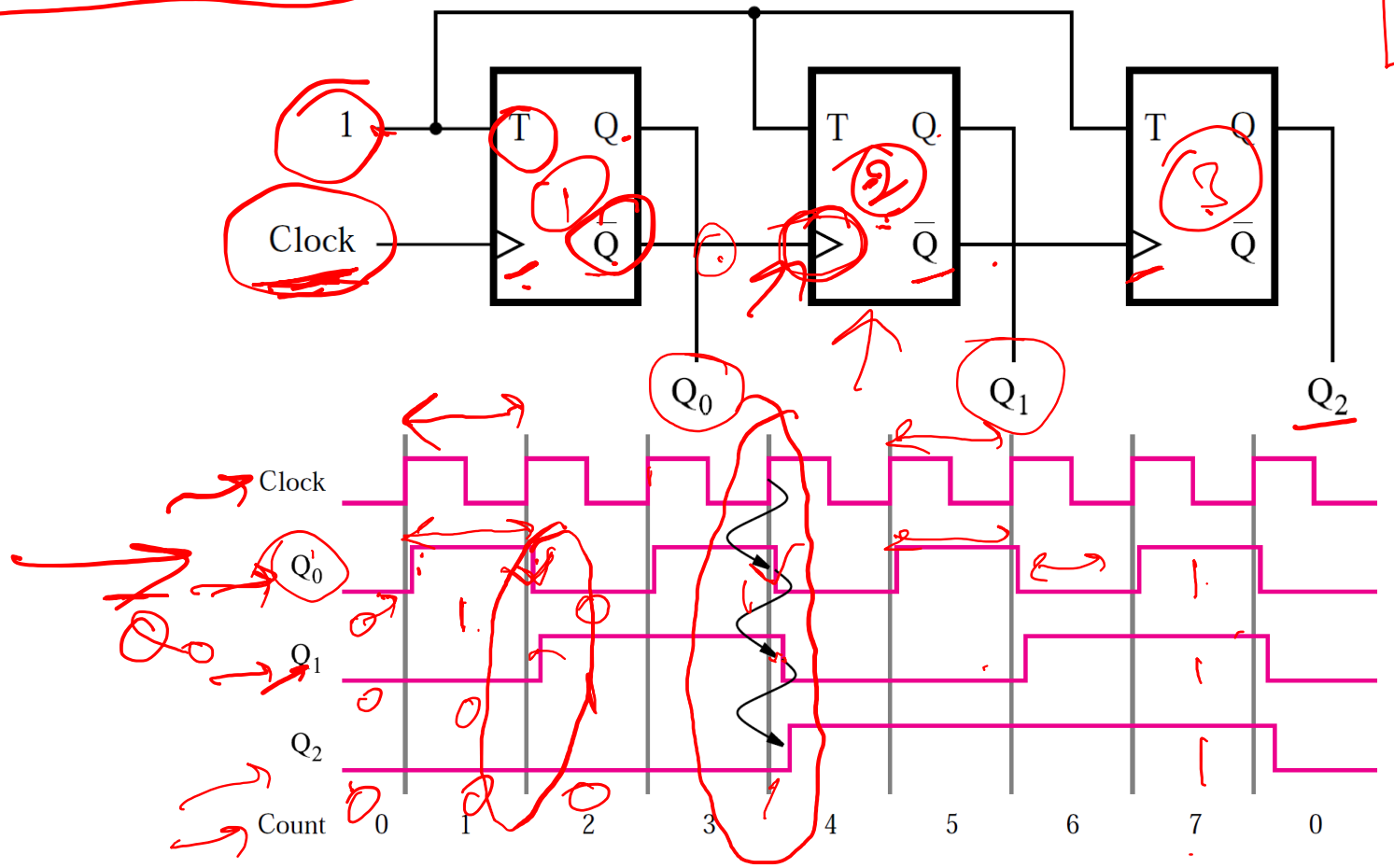
Asynchronous Counter

- Up-Counter with T Flip-Flops



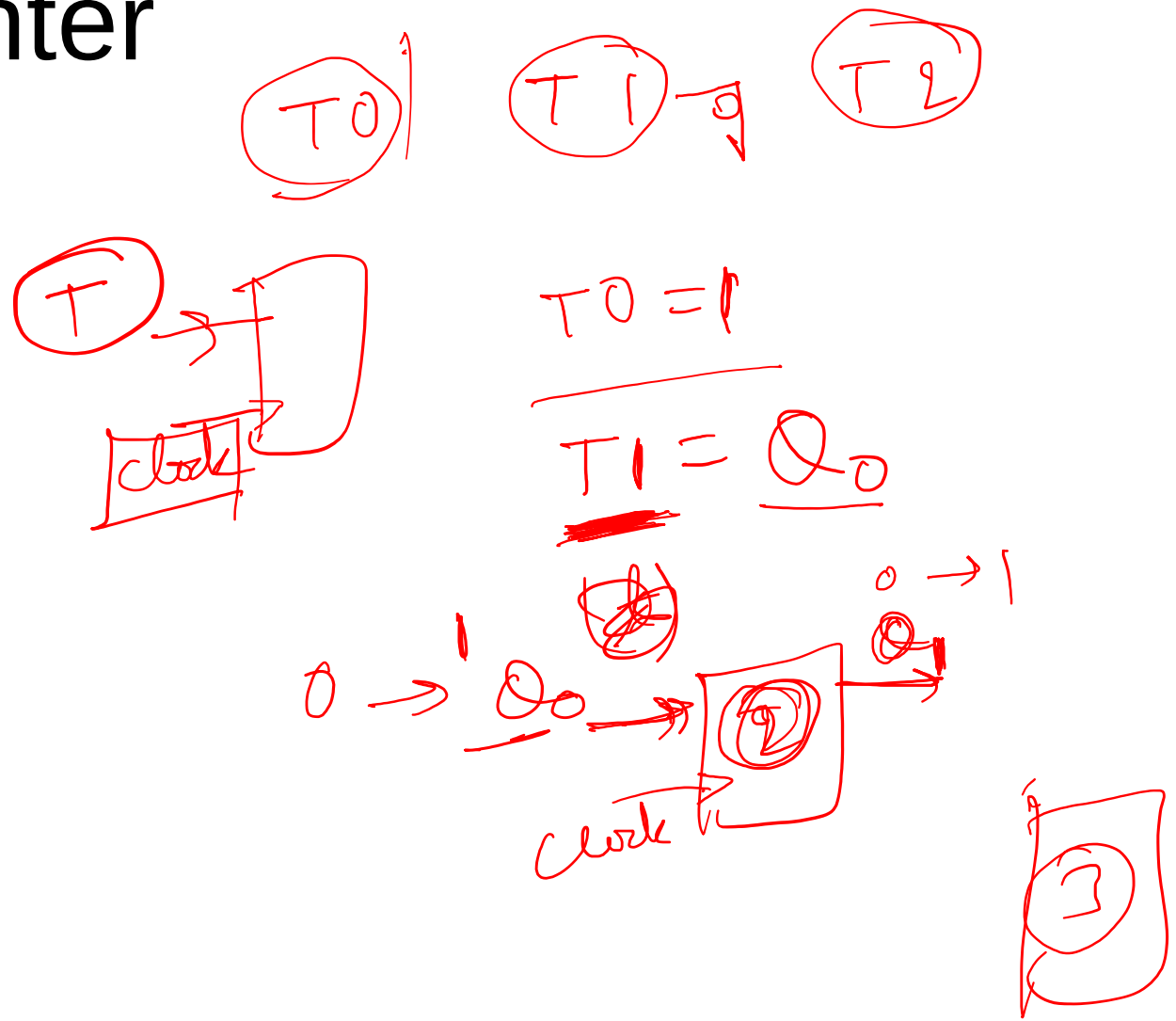
T	Q(t + 1)
0	Q(t)
1	$\overline{Q}(t)$

Synchronous Counter

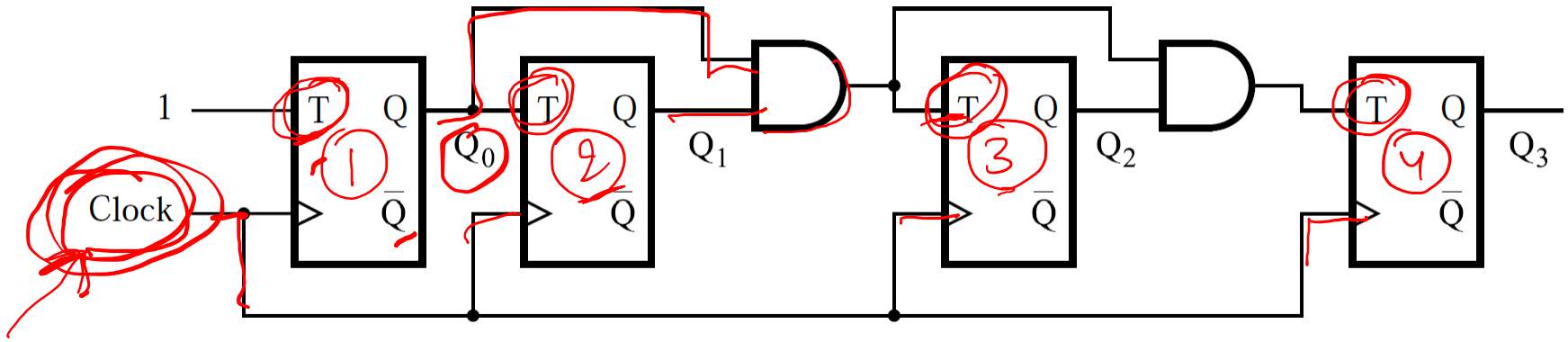
Clock cycle	Q_2 Q_1 Q_0
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1
8	0 0 0

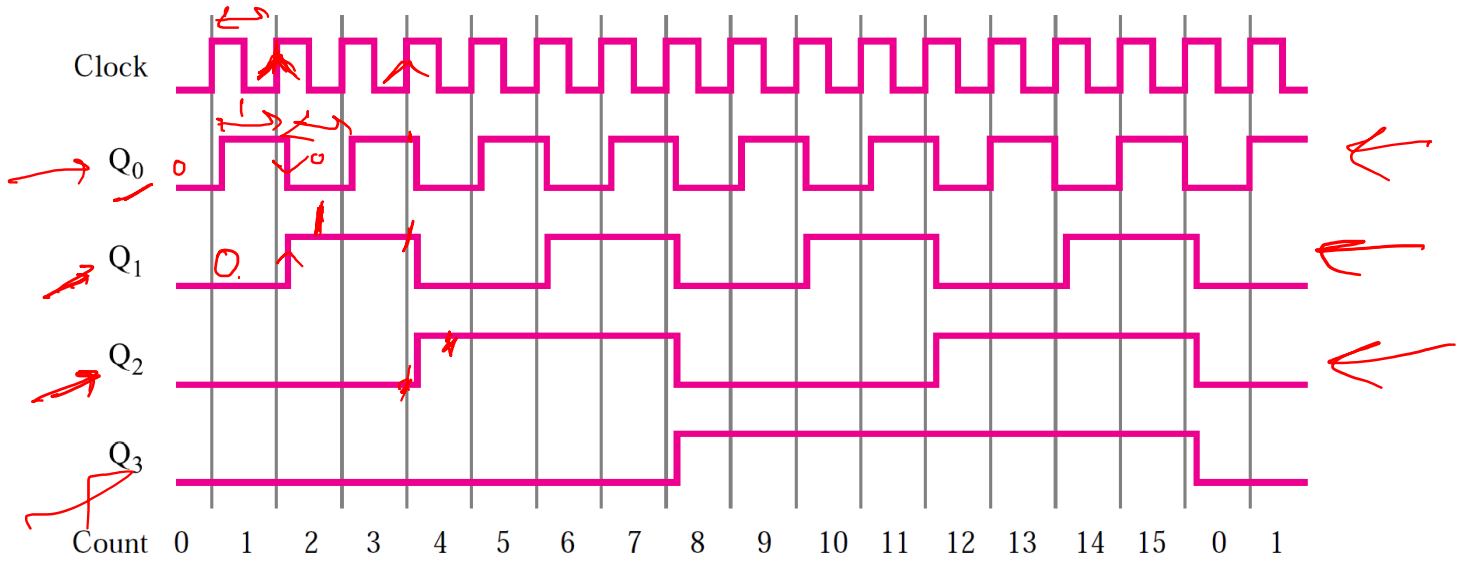
Q_1 changes

Q_2 changes

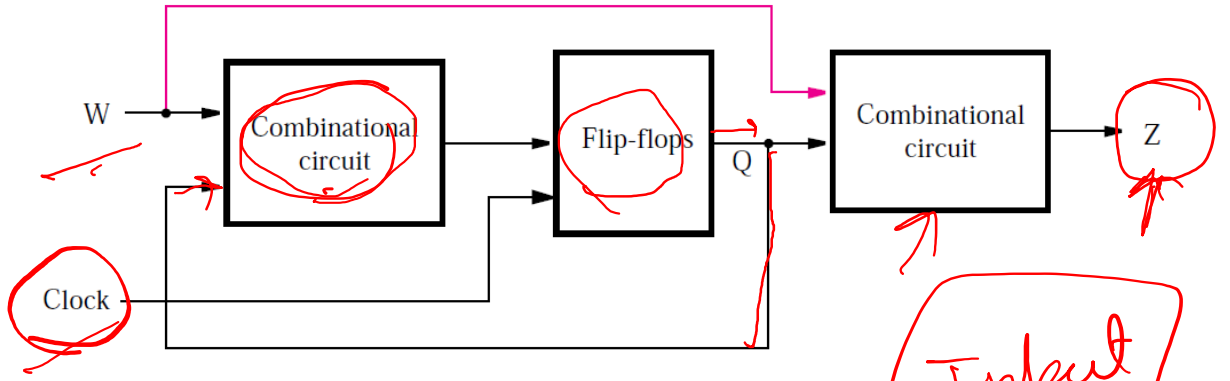


Synchronous Counter (Cont.)

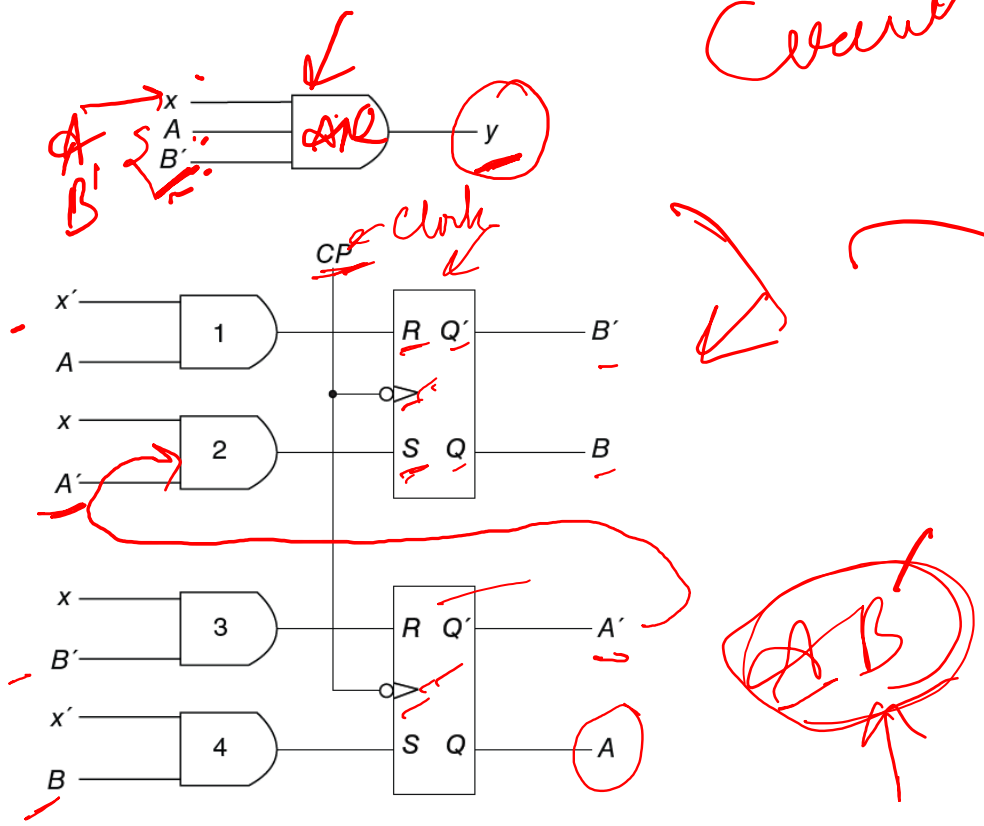




Sequential Circuits (Revisited)



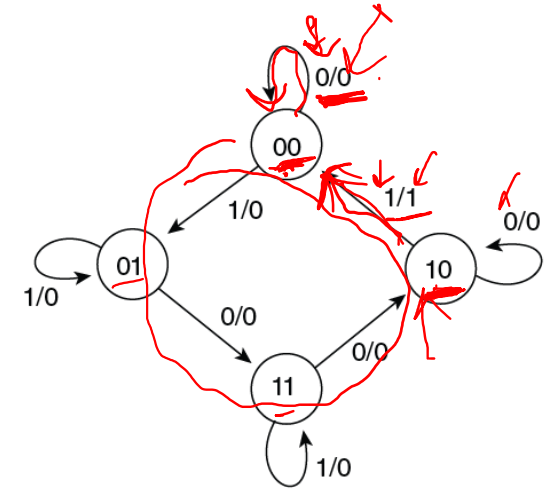
Example



Present State	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	AB	AB	y	y
00	00	01	0	0
01	11	01	0	0
10	10	00	0	1
11	10	11	0	0

State Table and Diagram

Present State	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	AB	AB	y	y
00	00	01	0	0
01	11	01	0	0
10	10	00	0	1
11	10	11	0	0



Table

Diagram

$y = x \cdot A \cdot B'$