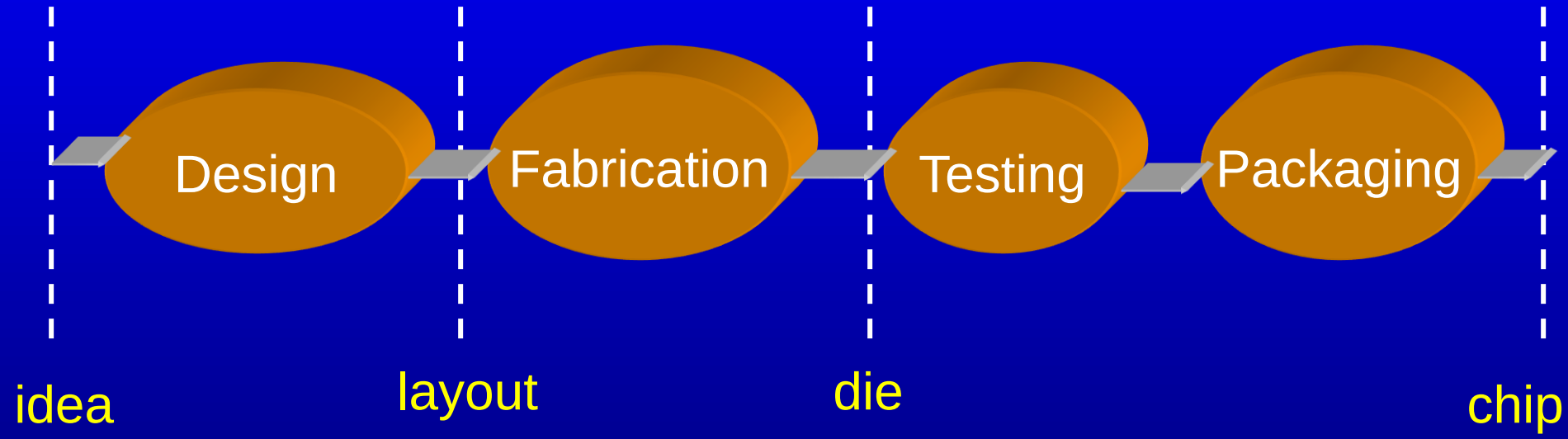
Synthesis of Digital Systems

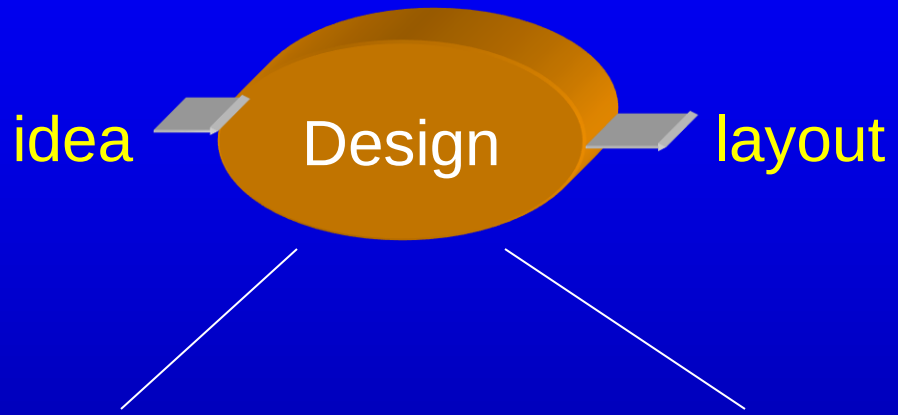
Part 1: Chip Design Flow

Preeti Ranjan Panda
Department of Computer Science and Engineering
Indian Institute of Technology Delhi
panda@cse.iitd.ac.in

“idea” to chip and system

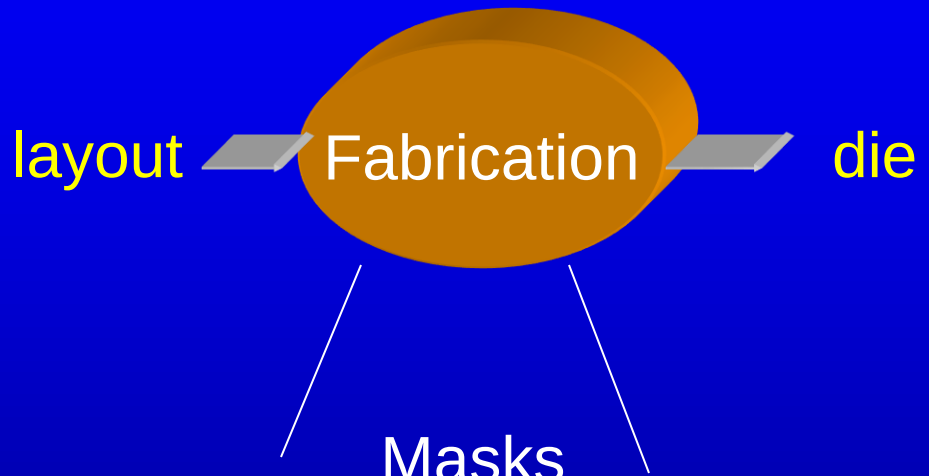


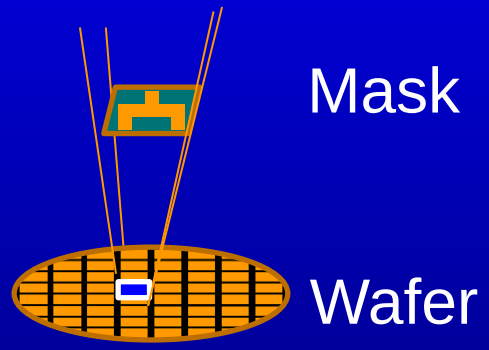
Design Stage



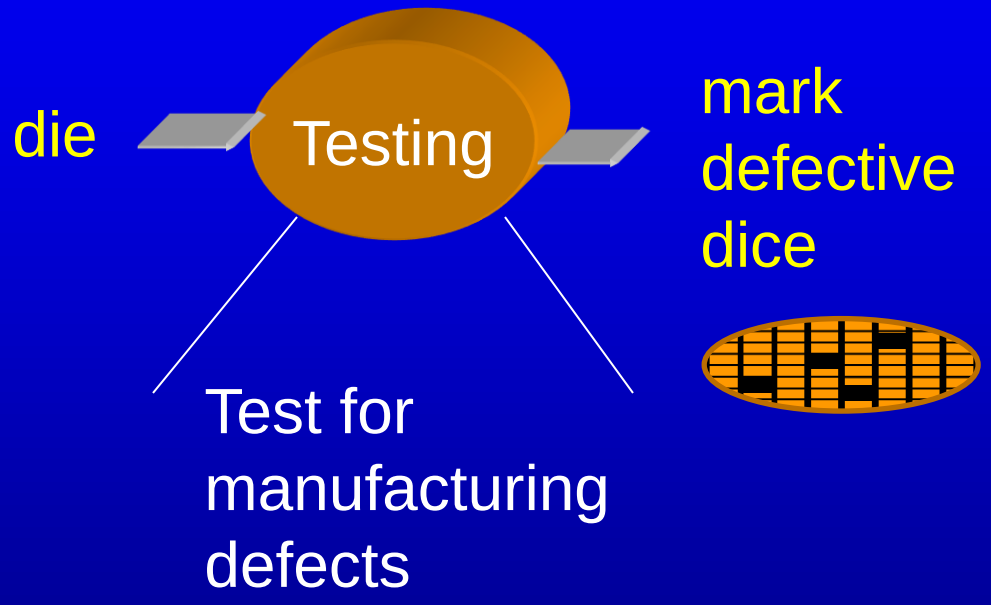
Specification
Modelling
Implementation
Verification/Simulation

Fabrication Stage

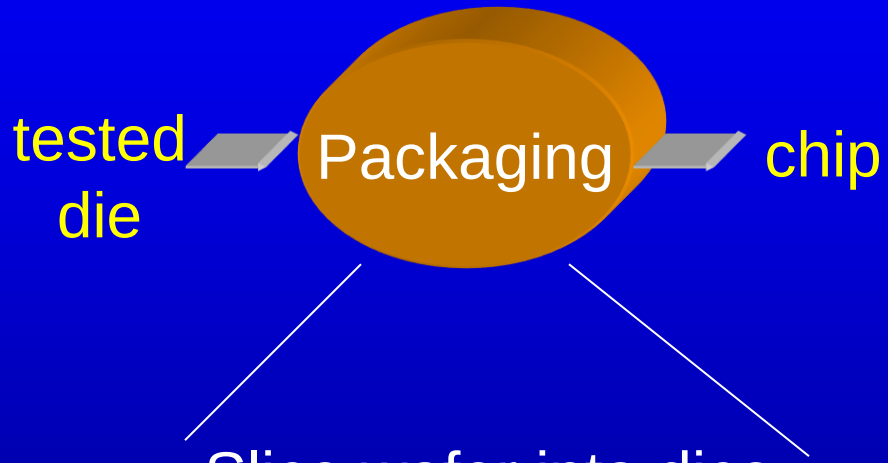




Testing Stage

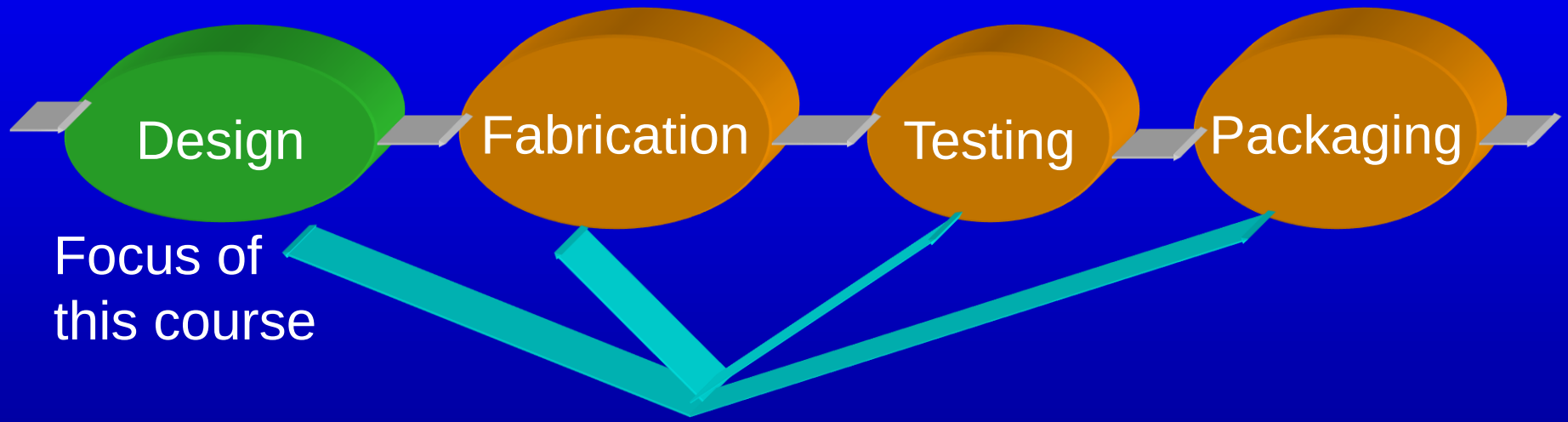


Packaging Stage



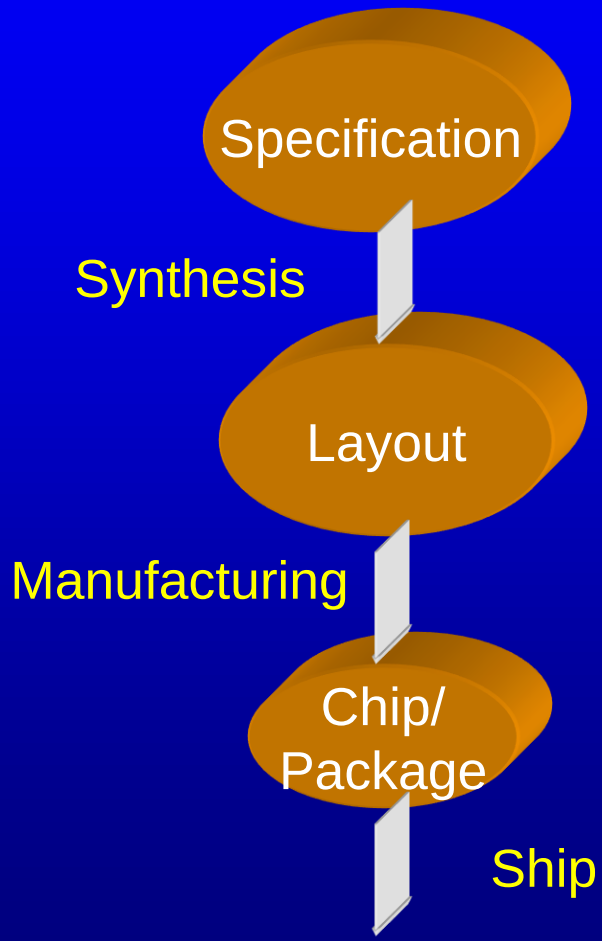
Slice wafer into dice
Wrap in package

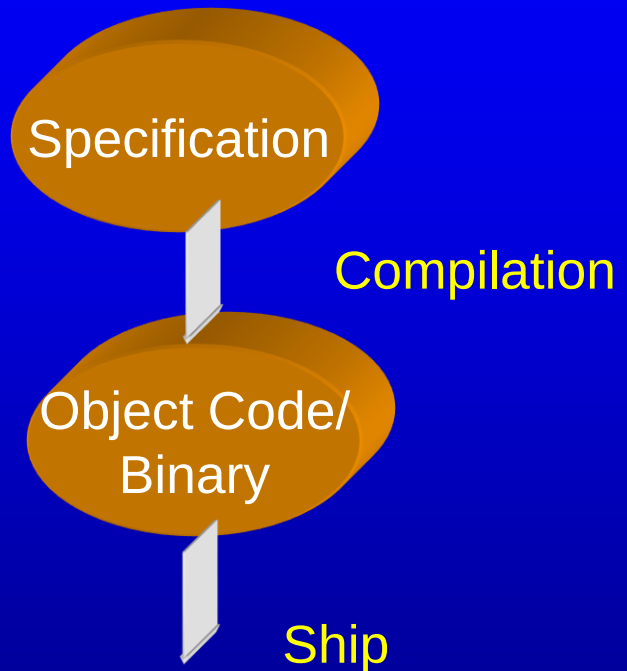
Design Automation: All Steps Heavily Automated



Computer Aided Design for VLSI
or
(Electronic) Design Automation

Parallel between HW and SW flows





Front-end of Compiler and
Synthesis tool are very similar

Modelling

- Representation of abstract view of the system
- Varying abstractions
  - Functionality
  - Timing
  - Power and energy

Modelling: level of detail

- System Level (or Electronic System Level – ESL)
  - abstract objects (transactions, packets,...)
  - abstract properties (traffic rates, congestion, deadlock)
- Behavioural Level
  - no clock cycle level commitment
- Register-Transfer Level (RTL)
  - operations committed to clock cycles
- Gate level
  - structural netlist

CAD in Specification / Modelling

- Layout and Schematic Editors
- Graphical FSM Capture Tools
- High-level Analysis Tools

Implementation: Synthesis

- HDL $\rightarrow$ Layout
  - HDL $\rightarrow$ Gates
  - Gates $\rightarrow$ Layout

CAD in Synthesis

- System Synthesis: Hardware vs. Software decisions
- Behavioural Synthesis
  - Behavioural HDL $\rightarrow$ RTL HDL
- RTL Synthesis
  - RTL HDL $\rightarrow$ Gates
- Layout Synthesis
  - Gates $\rightarrow$ Layout (Placement, Routing)

Verification

- Confirm that
  - specification is correct
  - implementation satisfies specification
  - timing constraints are met

CAD in Verification

- Simulation
  - Execute the specification
  - Test data provided by designer
  - Check against expected output
- Formal Verification
  - Check equivalence between specification and implementation
    - without simulation
  - Check for satisfaction of properties

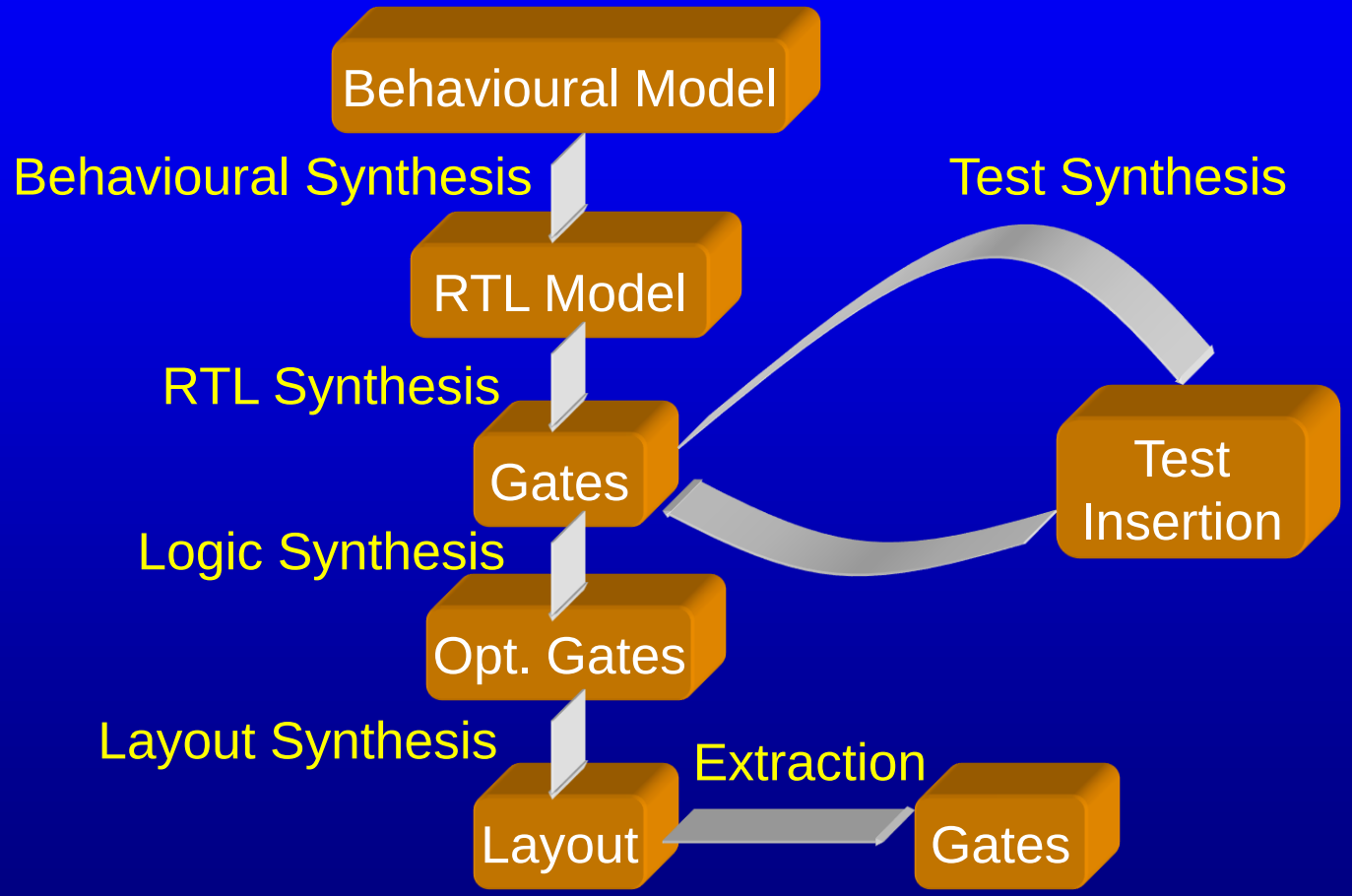
Testing

- Generate test data for chip
- Building test circuitry on-chip

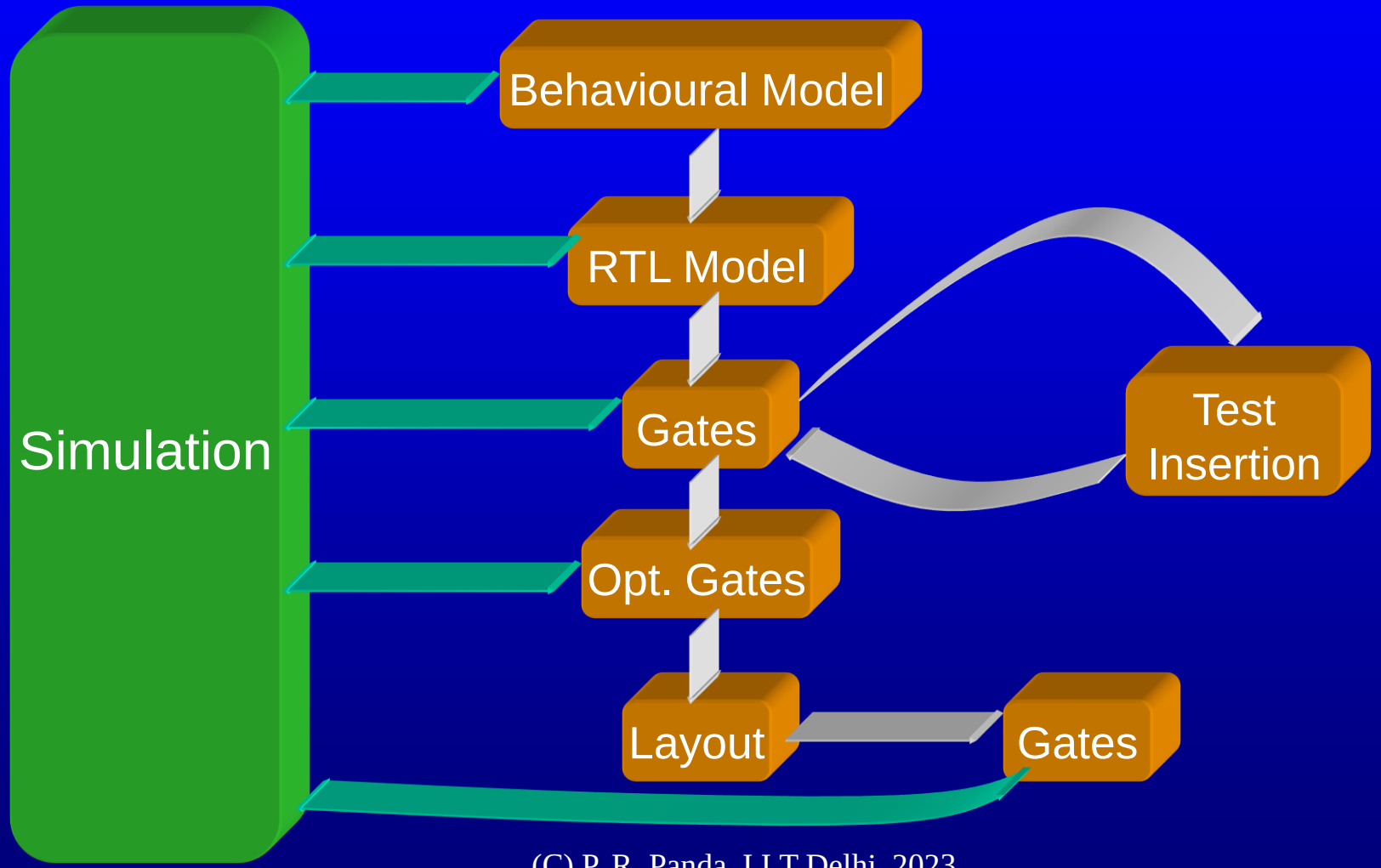
CAD in Testing

- Automatic Test Pattern Generation
- Scan insertion

Design Flow



Design Flow: Simulation



Design Flow: Verification