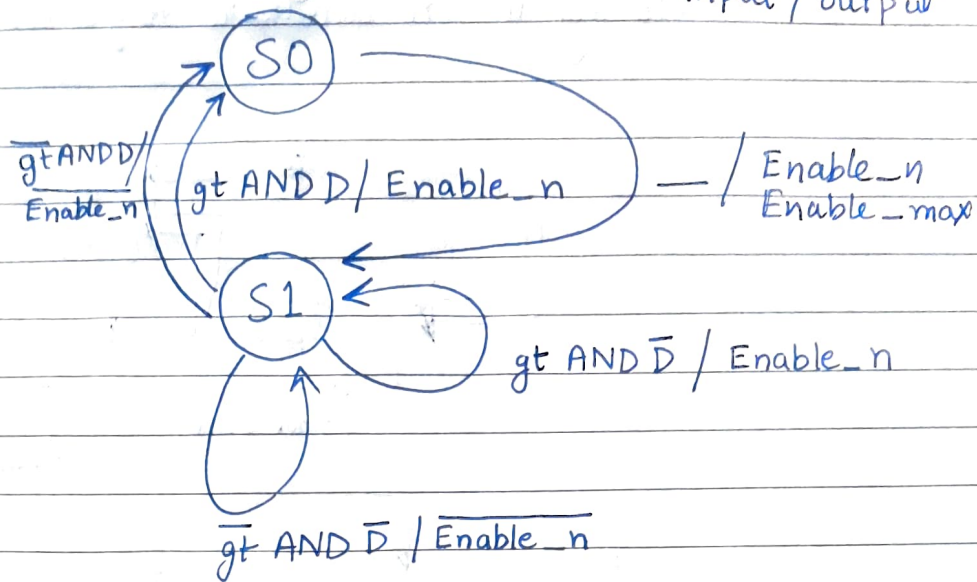


## Tut 7

①

(i)



$gt \rightarrow 1$  when input > stored value

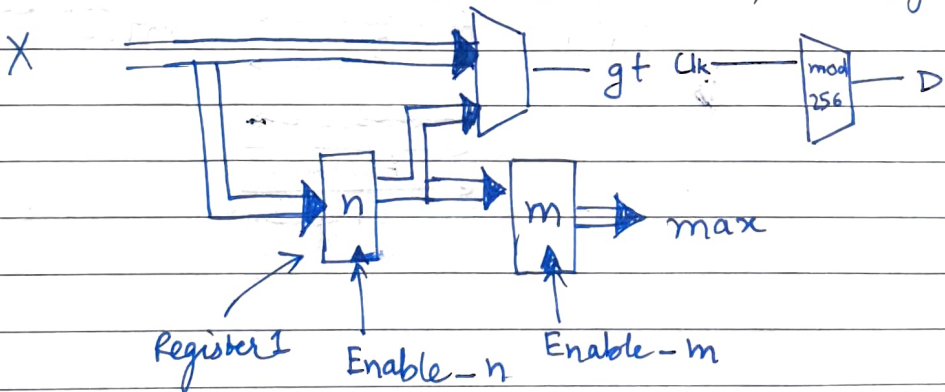
$D \rightarrow 1$  when counter hits 255

$Enable\_n \rightarrow 1$  then register 1 stores input.

$Enable\_max \rightarrow 1$  then read the value in Register 1 & keep in Register 2

Data Part: We need 2 registers, 1 comparator.

We also need a counter, with logic to turn  $D=1$  at 255

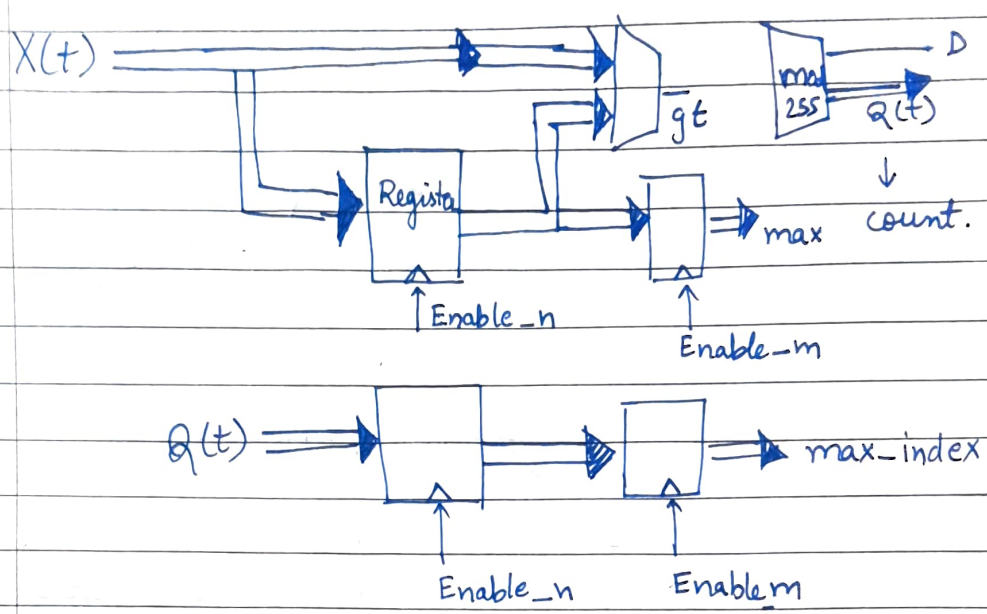


Classifying Status signals & control signals:

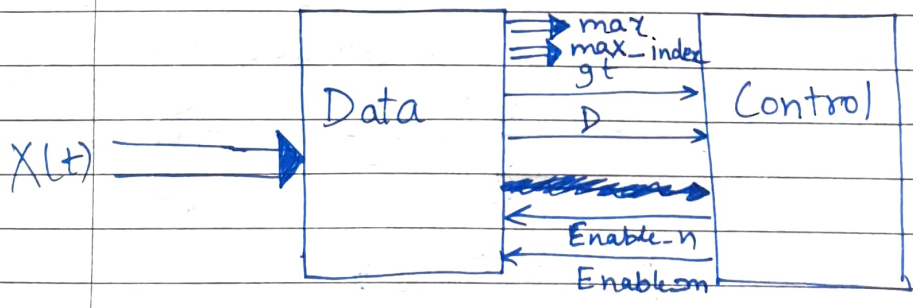
$D$  &  $gt$  are generated by the datapath, so they are Status signals.

$Enable$  signals are given by control so they are control.

(ii) Can be achieved by using the counter output and storing it in another register.

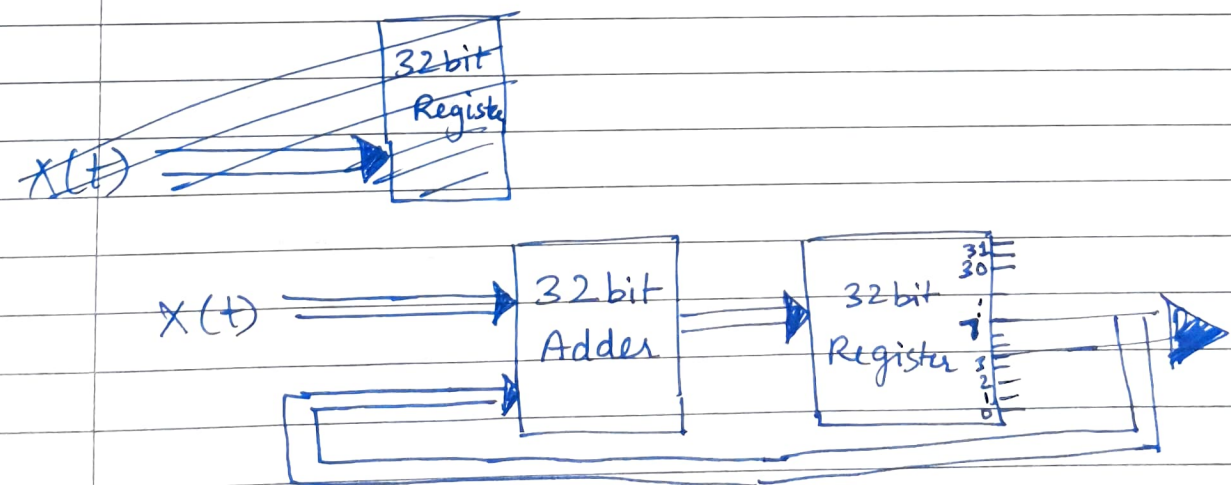


State machine will be same, since <sup>only</sup> data part is the ~~same~~ modified. Also, new signal  $Q(t)$  is completely internal.



— / — / —

(iii) Sum of 256 16 bit numbers cannot exceed  $2^{16} \times 256 = 2^{24}$ .



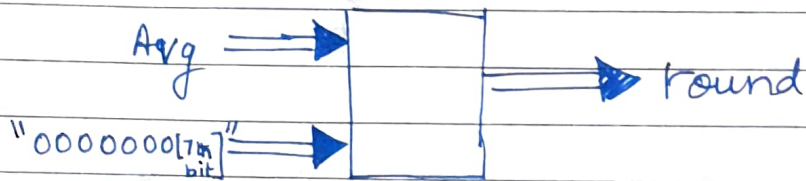
The diagram illustrates a digital circuit component, likely a register or adder, with the following components and connections:

- 32-bit Register:** A rectangular block labeled "32 bit Register". It receives an input signal  $X(t)$  from the left.
- 32-bit Adder:** A rectangular block labeled "32 bit Adder". It receives two inputs:  $X(t)$  from the left and a feedback signal from the output of the 32-bit Register.
- 32-bit Register (Output):** A rectangular block labeled "32 bit Register" that receives the output of the 32-bit Adder. It has 32 output lines labeled 0 through 31 on its right side.

\_/\_/\_

(iv) Rounding means if output is ...00110.1  
then in our <sup>avg</sup> answer, we add 1,  
i.e. 00111<sup>↑</sup>, otherwise avg is the  
answer.

So we can add the 7th bit of the output to  
bits 8 to 23.



rest all will be same.