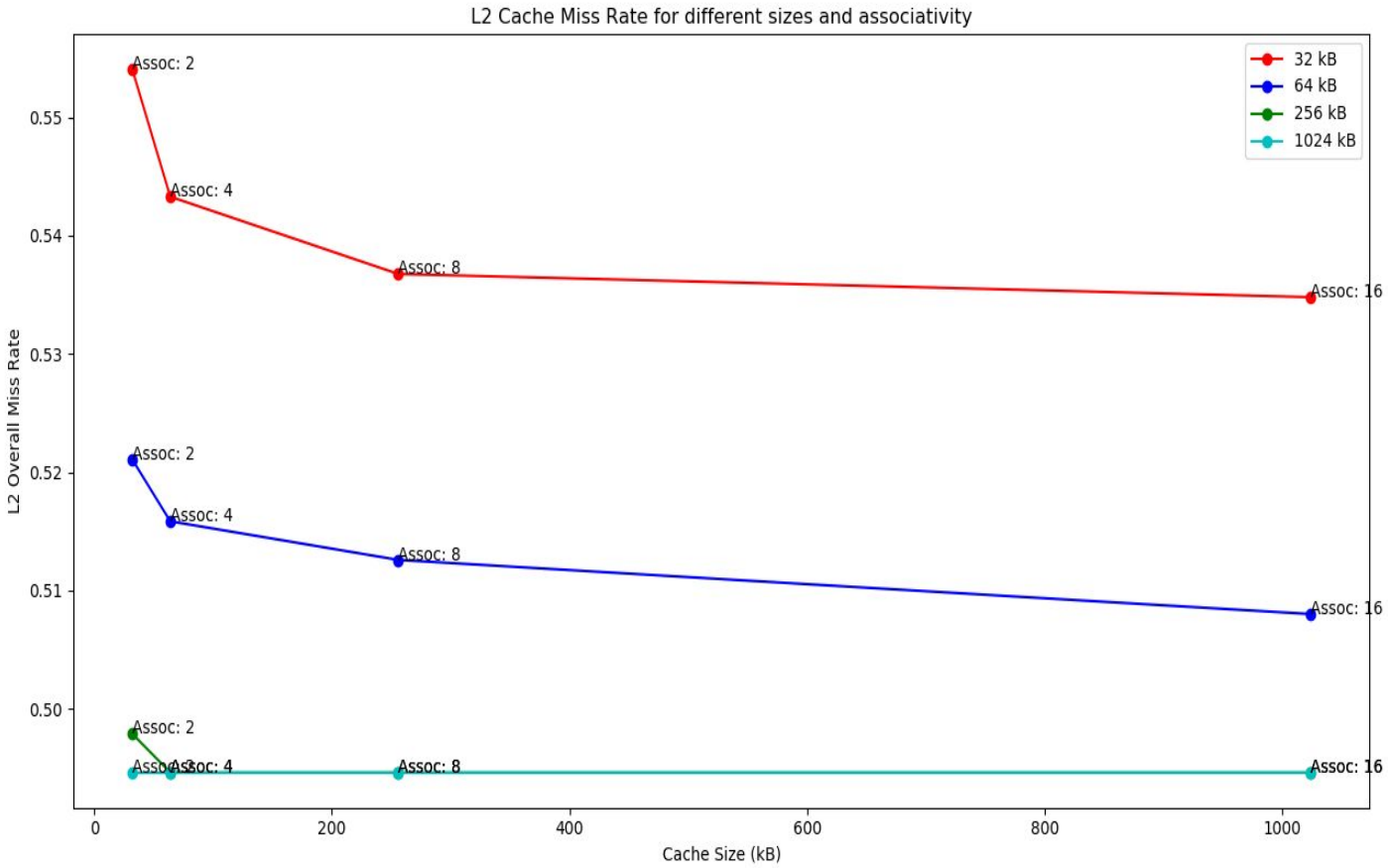
Assignment- 1

Harshit Rai
2017152

Question- 2
B)

Size (kB)	Associativity	L2 Cache Miss Rate
32	2	0.554067
32	4	0.543287
32	8	0.536753
32	16	0.534793
64	2	0.521072
64	4	0.515844
64	8	0.512578
64	16	0.508004
256	2	0.497877
256	4	0.49461
256	8	0.49461
256	16	0.49461
1024	2	0.49461
1024	4	0.49461
1024	8	0.49461
1024	16	0.49461



C) From the graph we see that as the cache size increases the cache miss rate decreases. The miss rate when associativity=2 is higher as compared to the miss rate when associativity=16. Also, as the associativity increases, the cache miss rate decreases. The miss rate when cache size=32 kB higher as compared to the miss rate when cache size=1024 kB. We are seeing this particular trend because as the cache size increases, more space will be available. Therefore there will be lesser chances of conflicts between the memory addresses.

Higher associativity means more complex hardware. However, for large cache sizes, increasing the associativity does not affect the miss rate. We can see this happen when the cache size=1024 kB, increasing the associativity does not change the L2 cache miss rate. It is constant.