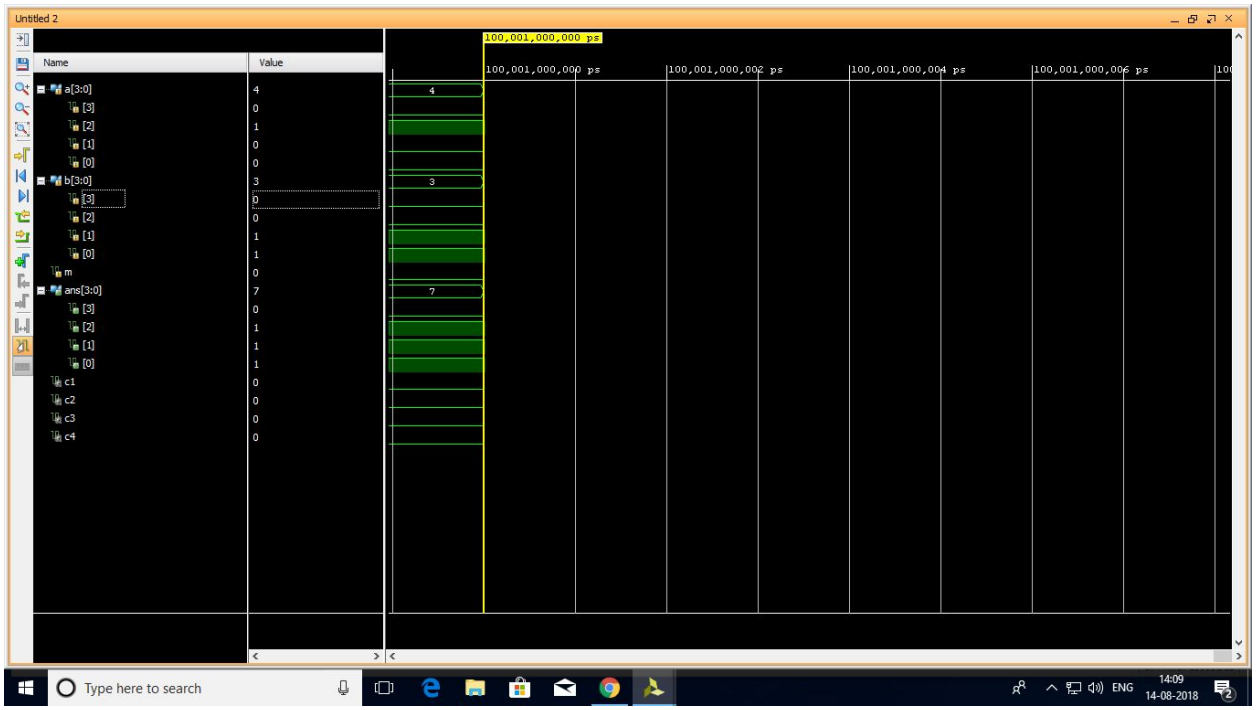
LAB 2 (4-bit adder/subtractor)

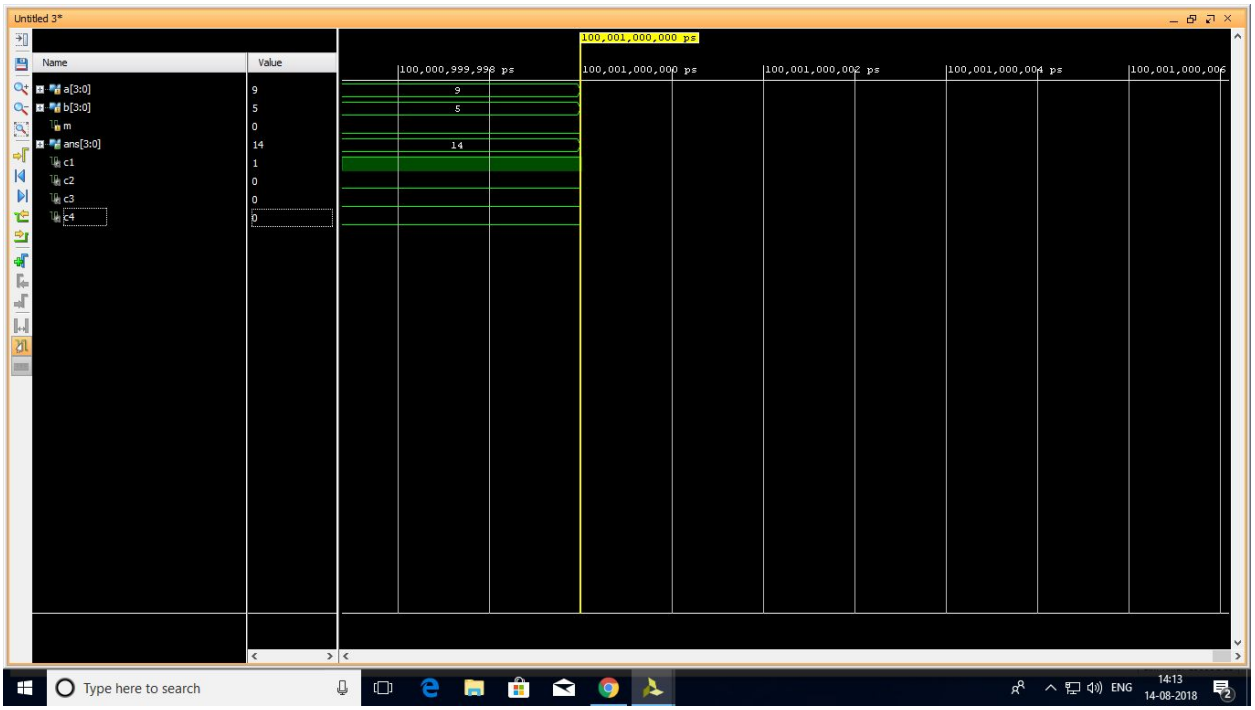
Verilog code

```
module add_sub_4(
input [3:0] a,
input [3:0] b,
input m,
output [3:0] ans
);

 wire c1,c2,c3,c4;

full_adder fun1(.a(a[0]),.b(b[0]^m),.c(m),.sum(ans[0]),.carry(c1));
full_adder fun2(.a(a[1]),.b(b[1]^m),.c(c1),.sum(ans[1]),.carry(c2));
full_adder fun3(.a(a[2]),.b(b[2]^m),.c(c2),.sum(ans[2]),.carry(c3));
full_adder fun4(.a(a[3]),.b(b[3]^m),.c(c3),.sum(ans[3]),.carry(c4));

endmodule
```

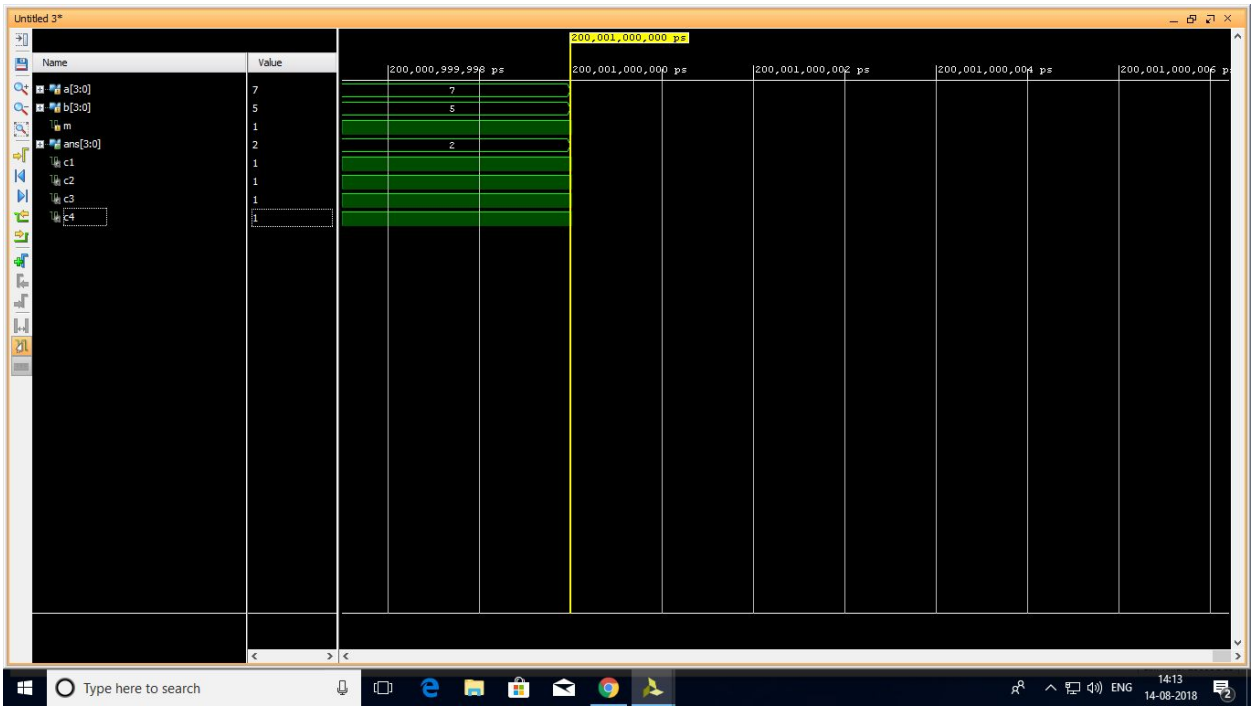
Output Waveform



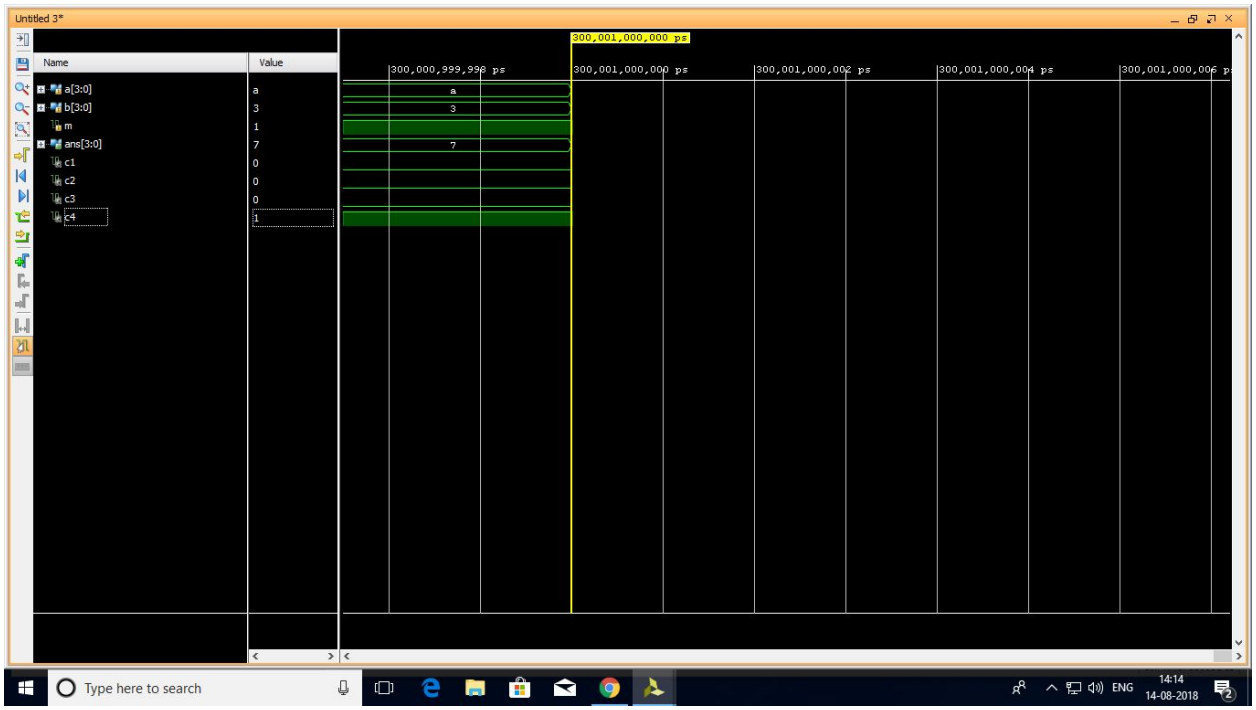
a=4, b=3, m=0, ans=7



a=9, b=5, m=0, ans=14



a=7, b=5, m=1, ans= 2



a=10, b=7, m=1, ans=3