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MANIPAL INSTITUTE OF TECHNOLOGY
(Constituent Institute of Manipal University)
MANIPAL-576104

I SEMESTER M.TECH (COMPUTER SCIENCE AND ENGINEERING) DEGREE
END-SEMESTER EXAMINATION-NOVEMBER/DECEMBER 2014
SUBJECT: HIGH PERFORMANCE COMPUTER SYSTEMS (CSE 507)
DATE: 27-11-2014

TIME: 3 HOURS MAX.MARKS: 50

Instructions to Candidates

- **Note:** Answer any **FIVE** full questions.

1A. Starting from basic principles derive the expression for the clock period τ, speed up S_k, throughput W, efficiency η of linear pipeline. This pipeline has a processor with clock frequency of 50 MHz executing a program with 15000 instructions. An assumption is done such that 5 stages of instruction pipelining are done for this linear pipeline and one instruction is issued per clock cycle. Calculate the above derived parameters for this linear pipeline.

1B. Derive the relationships among the bandwidths of the major subsystems in a uniprocessor system. **((4+2)+4)**

2A. With complete detailed design for mesh connected ILLIAC network and PM2I network, prove that ILLIAC network is a subset of plus-minus-2I network for N=16 where N is the number of nodes.

2B. Construct an a^n X b^n Delta network using *a*-shuffle as the link pattern between every consecutive stages of the network. From this, derive a 4^2 X 3^2 Delta network. **(5+5)**

3A. Write down the formula to calculate the time to strike out the multiples of prime *k* in control parallel approach algorithm. Discuss the problems and inefficiencies with the control parallel approach. Draw the diagram that supports data parallel approach in finding the prime numbers up to 40 using 4 processors.

3B. Write a parallel algorithm for shuffle exchange processor array model for finding the sum of 16 values. With appropriate diagram on this SIMD model illustrate how this algorithm works. **((1+1.5+1.5) + 6)**

4A. Write a parallel algorithm for matrix multiplication on UMA multiprocessor system. Discuss your analysis of parallelism for two 3 x 3 matrices.

4B. Draw a general bitonic sorting network using building block $\oplus$BM[*k*] and ΘBM[*k*] of input size *k*. Network should be capable to deal with 8 random numbers as input to keep them in

descending order. (Note: There is no need to show any number manipulation in the network). Further how do map it on to hypercube network? Explain with the diagrams. **(5+5)**

5A. Give the general MPI program structure. Write an MPI program to compute π value using *p* number of processes.

5B. Write a short note on OpenCL specification. Discuss the OpenCL APIs connected with the following:

i) Write host data to the device buffers
ii) Create the Kernel **((1+4)+(2+3))**

6A. With neat diagram discuss the abstract memory model defined by OpenCL. Write an OpenCL kernel program for matrix-matrix multiplication.

6B. Write a complete CUDA program for vector-vector addition. **((2.5+2.5)+5)**