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FACTA UNIVERSITATIS
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DOI: 10.2298/FUEE1404561N

RECENT RESEARCH IN VLSI, MEMS AND POWER DEVICES WITH PRACTICAL APPLICATION TO THE ITER AND DREAM PROJECTS

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Abstract. *Several MEMS (Micro Electro-Mechanical Systems) devices have been analysed and simulated. The new proposed model of SiC MPS (Merged PIN-Schottky) diodes is in full agreement with the real MPS devices. The real size DLL (Dynamic Lattice Liquid) simulator as well as the research on modelling and simulation of modern VLSI devices with practical applications have been presented. Based on experience in the field of ATCA (Advanced Telecommunications Computing Architecture) based systems a proof-of-concept DAQ (data acquisition) system for ITER (International Thermonuclear Experimental Reactor) have been proposed.*

Key words: *MEMS, power devices, SiC, DLL, VLSI, nuclear fusion.*

1. EDUMEMS PROJECT

The EduMEMS (Developing Multidomain **MEMS** Models for **Edu**cational Purposes) project started in 2011 and Lodz University of Technology acts as project coordinator. The project consortium includes two Polish universities (Lodz and Wroclaw University of Technology), one French and one Belgian partners (LAAS-CNRS laboratory and Ghent University) and two Ukrainian universities (Lviv Polytechnic National University and National Technical University of Ukraine in Kiev). The main goal of the project is to

Received October 6, 2014
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bring together scientists from different areas of research (mechanics, electronics, optics, fluidics) to work together on interdisciplinary MEMS modelling and design.

MEMS operate in the microscale and most MEMS devices involve phenomena from multiple domains. Therefore, to provide in-depth quality research of MEMS, specialists from all these domains have to cooperate. Thanks to the project, researchers can go to the partner universities and work there with specialists in a given field. Such newly founded research groups guarantee that the performed design, analysis and simulations take into consideration and adequately model all phenomena which arise in MEMS devices. One have to underline that the common research in MEMS area have been conducted already by LUT and LAAS in the frame of BARMINT project [1].

During the project, several MEMS devices have been analyzed and simulated, new modelling methodologies have been proposed and new device models have been invented. In particular, the following topics have been researched:

- modelling of uncooled microbolometer
- modelling of micromembrane
- modelling of RF temperature sensor
- modelling of microfluidic flow

In this paper we describe in detail the work performed on first two devices, namely microbolometer and membrane.

1.1. Modelling and simulation of uncooled microbolometer

Bolometers are used to measure radiation, in particular they are used in thermal cameras to measure infrared radiation [2]. Their principle of operation is that the radiation heats up an active element which changes its resistance due to the temperature change. The resistance change can be then measured and based on the result, the intensity of radiation is calculated. Thermal cameras usually use arrays of microbolometers in which each one represents one pixel. After reading the radiation coming on all pixels, the camera is able to provide the entire thermal image of observed scene.

The detailed description of microbolometer operation is beyond the scope of this paper. Here, we will concentrate on modelling electrical and thermal phenomena in these devices. Let us first discuss the thermal domain. The role of the microbolometer is to provide the highest possible temperature change for a given radiation. Thus, the surface of the device should be as large as possible and made of material which has a high temperature coefficient of resistance (TCR). Moreover, the heated surface of this material should be thermally separated from the chip surface so that the absorbed heat does not heat up the entire chip. As far as the electrical domain is concerned, the designer has to ensure that it is possible to measure the resistance of the heated element. This most often involves applying a given current through the element and measuring the voltage. Thus, the used material should be a conductor. All mentioned requirements are met in the structure of MEMS-based microbolometer (see Fig. 1).

It can be seen that the structure is composed of a bridge suspended over the substrate and supported by thin legs. Thanks to this structure, the bridge is thermally isolated from the substrate. The isolation is of course not perfect and depends on the size of the supporting legs. It can be also observed that there is a thin layer of active material which has a serpentine shape and goes from one leg to another. This layer is the active

material: the one whose resistance will be measured. Consequently, it is made of thin conductor with high TCR. Several materials have been proposed for the role of active material, namely vanadium oxide, titanium, amorphous silicon etc. This thin layer is encapsulated in the membrane whose role is to maximize the device surface and to absorb as much radiation as possible. Naturally, the membrane should be made of isolator (silicon nitride is most often used) so that it does not interfere with the current flowing through the active layer.

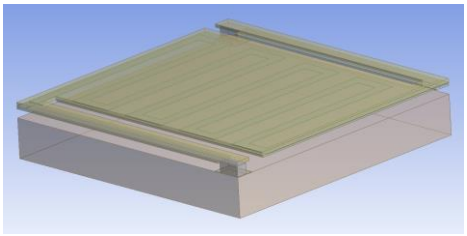

Fig. 1 Typical microbolometer structure

Electro-thermal simulation of microbolometers has to include the coupling between electrical and thermal domain. The reason is that Joule heat dissipated in the active layer is a function of resistance but also the resistance is a function of temperature (so basically a function of dissipated heat). Therefore, accurate and fast simulation of such structures is difficult. Of course, one can use Finite Element Model based tools like ANSYS [3] or COMSOL [4] to obtain detailed simulation results. During the project, we performed thorough simulations of various microbolometer shapes, tested various layer dimensions and used various materials. A sample simulation result for titanium-based 50×50 µm microbolometer is presented in Fig. 2. It presents the maximal transient temperature reached in microbolometer due to the applied current pulse. Note that on one hand, pulse amplitude should be as small as possible to reduce Joule heating. However, on the other hand, the bias current should be as high as possible to increase the sensitivity. Consequently, our simulation give concrete answer to the designer which has to make this trade-off. For example, it shows that in case of this particular microbolometer, a current pulse of 0.2 mA amplitude and 100 µs duration will cause the temperature rise up to 26°C. On the other hand, a current of 0.25 mA and 150 µs will increase the temperature to 30.2°C [5].

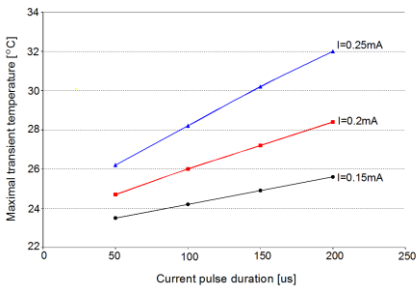

Fig. 2 Maximal transient temperature due to the applied current pulse

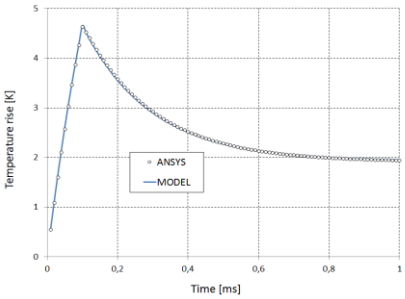

Fig. 3 Response of a microbolometer for a constant radiation and current pulse

However, the simulation time may be quite long in this case, which is sometimes prohibitive. In some cases, designers are in need of faster and simpler models. Therefore, a significant amount of work has been performed to design an analytical, electro-thermal model of a microbolometer, which allows obtaining results very close to those calculated by ANSYS in a much shorter time. Fig. 3 shows the response of a microbolometer for a constant radiation and current pulse for both ANSYS model and simplified, analytical model [6].

It shows that the designed model gives basically identical results to those obtained using complex ANSYS model. Needless to say, the simulation time using our model is much shorter, especially in case of transient simulation with a significant number of time points. We have performed similar comparisons for various microbolometers (various sizes, materials, shapes) and the maximal error of our model with respect to ANSYS model was found to be 3%.

1.2. Modelling and simulation of micromebrane

Membranes are commonly used in many micromachined applications. They are used as a mechanical part of a device that allow converting external force into electrical signal (via membrane deflection) as well as generating force by applying electrical signal. Wide spectrum of application defined many constructions of membranes (number of layers, materials used in fabrication) and wide range of membrane shapes and dimensions. Therefore, the simulation of a membrane became crucial step in device production. Very often FEM analysis is used in MEMS simulation. Although, it can be very detailed, the time consumption is rather high. As the simulation has to be run repeatedly, numerical simulation can be very inconvenient. Then, the analytical modelling can be a very good alternative, especially when the model is very accurate and allows combining mechanical domain with other ones [7].

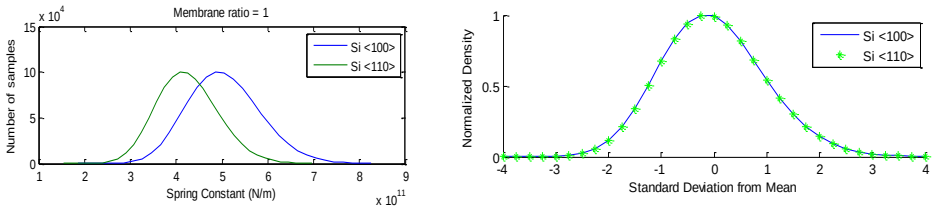

Fig. 4 Membrane stiffness distribution for square membrane

One of the highest benefits of analytical modelling can be achieved in statistical simulation. Even we found optimal parameters of the membrane that give the desired performance of the device, the fabrication process does not guarantee that the real device will meet this requirements. Many fabrications steps have some tolerances that affect the device performance. The investigation of this influence can be performed using Monte Carlo analysis. Component tolerances are used in generation of parameters distribution and then the simulation is run many times for each case to obtain the distribution of the device performance. A sample simulation was performed for a silicon membrane with dimension of 200 µm width and 4 µm of thickness and various lengths (from square membrane to rectangular). It was assumed that the fabrication process influences on

membrane dimensions and residual stress within it. The distribution of input parameters was generated using the normal distribution and tolerances provided by typical equipment used in fabrication process. The sample results for square membrane are presented in Fig. 4.

It presents the distribution of the membrane stiffness for two crystallographic orientations. It can be seen that rather negligible input tolerances affects the membrane properties significantly. The deviation from the mean value can reach 3 standard deviation and "only" 70% of membranes are located within one standard deviation. Depending on our requirements, the tolerances of fabrication process may lead to fabrication of useless devices. Therefore, the statistical simulation can be very useful in estimation of yield production.

In many applications the membranes are fabricated using wafer bonding technique [8]. The bonding process usually requires high temperature annealing of the structure to strengthen the bond. If two different materials are bonded, the residual stress appears in the structure which is usually undesired because it changes the response of the membrane. The evolution of MEMS fabrication technology allows nowadays performing bonding process in stress free temperature. However, this technique does not guarantee that the residual stress will not appear. It can only reduce its value significantly. It has to be mentioned that the device operates in variable temperatures that influence on residual stress value. Therefore, it is desired to investigate this influence in a typical range of operational temperature of a device. The simulation was performed for a structure that consists of silicon membrane fabricated on Pyrex surface by bonding performed in 270°C (that is known as stress free temperature). It was found that the residual stress disappears when the structure is returned to about 13°C as near this temperature the deflection of unloaded membrane changes direction. Then, the influence of operational temperature was investigated for temperatures in range of 0-50°C. The figures below show the change of membrane stiffness and normal stress in the centre of membrane edge (see Fig. 5).

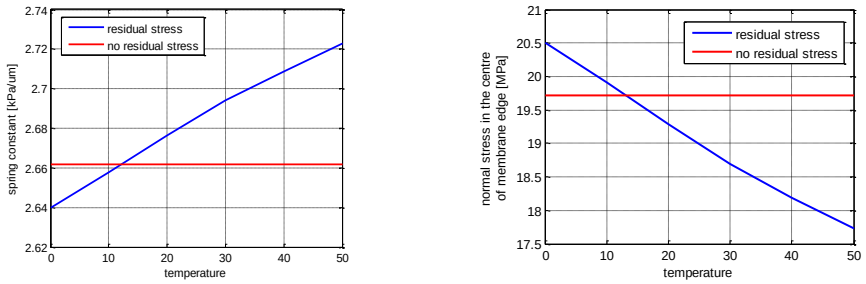

Fig. 5 Membrane stiffness and normal stress within the membrane as a function of temperature

Comparing to the membrane with no residua stress, the membrane stiffness varies up to is 2.3%. Although, this change seems to be negligible, in case of capacitive read-out the capacitance will vary up to 10%. On the other hand, the stress within the membrane varies up to 10% also. In case of piezoresistive read-out, the response will be different by the same value.

2. BEHAVIORAL ELECTRO-THERMAL MODELS OF MERGED SIC DIODE

Silicon carbide devices are the most promising semiconductor devices for power applications [9]. They offer excellent thermal properties and low on-state resistance together with high voltage capability. This has made possible the manufacturing of high voltage unipolar devices reaching very high operating frequencies. As a consequence, the most frequently used SiC devices are **M**erged **P**IN-**S**chottky (MPS) diodes [10].

The MPS diode models provided by device manufacturers - the classical SPICE embedded diode model, as well as physical models are all unable to accurately reproduce temperature-dependent device behaviour of these devices in a relatively wide range of operating temperatures [11]. However, accurate models are required in order to provide engineers with a reliable tool for design of robust state-of-the-art power conversion appliances. Consequently, a simple and accurate electro-thermal model of the MPS diode is necessary.

Behavioural models have great potential in this regard, in particular when unipolar devices are concerned. Electrical phenomena in Schottky diodes during conduction and switching are generally simpler as compared to PIN diodes, which renders behavioural modelling feasible. However, SiC MPS diodes exhibit nonlinear behaviour when temperature influence is involved [12] what requires the development of dedicated models [10]. Moreover, even though switching processes are very short as compared to thermal time constants, they may soon become more important as switching frequencies are increased.

Until now, **C**ompact **T**hermal **M**odels (CTMs) were obtained either by detailed investigation of the device structure, whose physical and geometrical parameters are often unavailable, either by application of the **N**etwork **I**dentification by **D**econvolution (NID) method, based on analysis of a single transient temperature measurement processed appropriately [13]. To develop the electro-thermal MPS model, a novel model generation approach can be applied which is based on the NID method and time constant spectrum examination. It offers greater simplicity and better numerical properties while preserving the physical meaning of the obtained CTM [14].

The thermal model is coupled with the electrical part to form the complete electro-thermal model. The proposed approach is demonstrated for the CSD20030 common-cathode dual MPS rectifier manufactured by Cree. It is demonstrated that the behavioural approach enables the derivation of an accurate unipolar power semiconductor device model without any knowledge about its technological parameters. This has a great practical impact as such data are normally not revealed by device manufacturers.

The first SiC diodes made available by device manufacturers were subjected to tests which showed serious inconsistencies between simulated and measured behaviour (see [10,15] and also [11]). The research presented in [10, 15] shows that classical Shockley's equation [17] cannot be used for electric domain description. In the authors' opinion, these inconsistencies may be due to these devices being manufactured as merged PIN-Schottky diodes with additional p-islands [18]. In a regression-based analysis of the MPS electro-thermal model [19], the temperature T is linearly or quadraticly related to internal resistance series resistance R_s and intrinsic voltage drop V_{intrsc}. Analyses of measured quantities variability lead to the following relationship describing the static behaviour of the diode under forward bias:

$$V_{fwd}(I_{fwd},T) = (p_1+p_2\cdot T)\cdot\ln I_{fwd} + (p_3+p_4\cdot T) + I_{fwd}\cdot p_5\cdot[1+p_6\cdot(T-27°\mathrm{C})+p_7\cdot(T-27°\mathrm{C})^2] \quad (1)$$

where $p_1,\ldots, p_7$ are empirical constant coefficients. Equation (1) is equivalent to the form suitable for numerical simulations [16]:

$$I_{fwd}(V_{fwd},T) = \exp\frac{V_{fwd} - V_{intrsc}(T) - R_s \cdot I_{fwd}(V_{fwd},T)}{V_r(T)} \tag{2}$$

where $V_r(T) = p_1 + p_2 \cdot T$, $V_{intrsc}(T) = p_3 + p_4 \cdot T$, $R_s(T) = p_5 \cdot [1 + p_6 \cdot (T - 27\ °C) + p_7 \cdot (T - 27\ °C)^2]$.

A similar analysis was performed for the reverse bias, leading to the formula (valid almost for all the diodes)

$$I_{rev}(V_{rev},T) = \beta(T) \cdot \exp[V_{rev} \cdot \alpha(T)]. \tag{3}$$

where $\alpha(T)$ and $\beta(T)$ have linear character. In the case of the antysymmetric current character of temperature influence on behaviour of this diode below and over 75 °C (e.g. for CSD04060 diode), an exponential and a hyperbolic relationships had to be used to represent the way the current varies with temperature [16]:

$$I_{rev}(V_{rev},T) = \exp\frac{a + b \cdot V_{75} + c \cdot V_{75}^2}{1 + d \cdot V_{75} + e \cdot V_{75}^2} \tag{4}$$

where V_{75} is the reverse voltage drop V_{rev} at T = 75 °C

$$V_{75} = \frac{V_{rev} + f + g \cdot T}{1 + h \cdot T} \tag{5}$$

and a to h are empirical constant coefficients.

The SiC MPS diode total capacitance is not significant for forward polarization except under very high switching frequencies. However, the junction capacitance for low reverse voltages can be presented using the space charge layer capacitance equation:

$$C_j(V_d) = C_{j0} \cdot |V_d + V_j|^{1 - Mj} \tag{6}$$

where C_{j0} is the capacitance of an unbiased junction (V_d = 0), V_j is the junction potential, and M_j is the junction grading coefficient.

Thermal behaviour of semiconductor devices and cooling assemblies can be predicted by **C**ompact **T**hermal **M**odels (CTMs), which can be derived adopting the structural or the behavioural approach [20], [14], [23]. The detailed SPICE behavioural model of Infineon and Cree MPS devices are presented in [10], [21], [16], [15]. The electro-thermal model is in full agreement with the real MPS devices behaviour. The proposed model of SiC MPS diodes is in full agreement with the real MPS devices behaviour in forward and reverse characteristics with the measurements of real devices (Fig. 6, Fig. 7) and definitely produced much better results than the models provided by the device manufacturers.

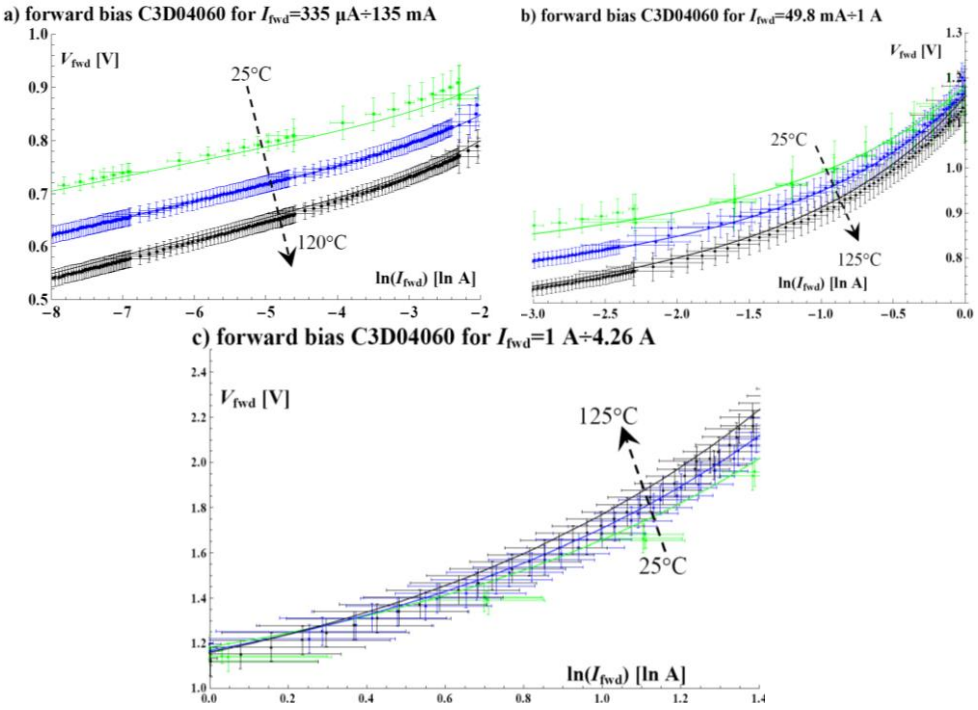

Fig. 6 Comparison of the measured SiC diode forward characteristics with the proposed model. Temperatures: 25°C (green), 75°C (blue), 125°C for C3D04060 (black). Y-axis: V_{fwd} [V]; X-axis: ln(I_{fwd}); The measurement deviation is presented using error bars. ([20]).

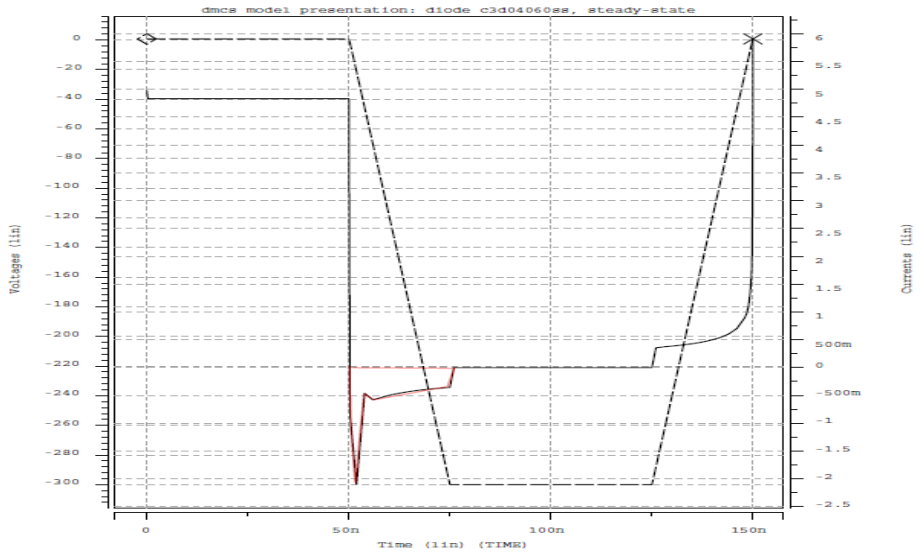

Fig. 7 The example dynamic behaviour of C3D04060 diode (source [20]).

3. FROM DLL SIMULATOR TO DREAM SUPERCOMPUTER

3.1 Introduction – historical outline

Necessity is the mother of invention. This very well-known saying perfectly renders the idea of **D**ynamically **RE**configur**A**ble poly**M**orphic supercomputer (DREAM). The idea was born in 2010, in Department of Microelectronics and Computer Science at Lodz University of Technology in Poland.

The conception of this idea took place at the same University about ten years earlier, when two scientists from Department of Molecular Physics – working on simulations of some phenomena in polymers – desired to accelerate their calculations. For their simulations they were using **D**ynamic **L**attice **L**iquid (DLL) algorithm, which – as it was expected and finally proved – can be efficiently parallelised. In order to materialize their desire, the physicists-inventors started to draw the schematics of an electronic device – composed of discrete elements – dedicated to execute DLL algorithm in a fully parallel manner. Soon they realised, that the task is very ambitious and in the era of integrated circuits the approach based on discrete components is not efficient. However, the solution based on dedicated **A**pplication **S**pecific **I**ntegrated **C**ircuits (ASICs) would be relatively expensive and inflexible. The idea to build a parallel computing machine equipped with a typical microprocessor was also not very promising. The simulations of polymers by means of DLL algorithm require many – though very simple – logic units called nodes. Each node (representing e.g. one monomer) corresponds to a lattice point of the **f**ace **c**ubic **c**entred (fcc) network. Assigning one node to one microprocessor would result in a huge number of inefficiently used computing cores.

The solution to this stalemate came from the friendly Department of Microelectronics and Computer Science and was – as most inventions – very simple: instead of discrete elements, dedicated ASICs or microprocessors, the reconfigurable devices such as FPGAs (Field Programmable Gate Arrays) must be used [22, 23]. In such elements it is possible to implement many nodes (lattice points) and to simulate their behaviour simultaneously. In this way the size of the simulator can be significantly reduced. Furthermore, the internal architecture of computing elements can be optimized to efficiently achieve the functionality of e.g. simulated monomers.

3.2 First prototype – μDLL simulator

In order to prove the feasibility and efficiency of the proposed solution, both departments – in close cooperation – developed a prototype of a simulator dedicated to DLL algorithm. The prototype was named μDLL simulator. Its capacity, defined as a number of implemented nodes, is insufficient to perform any full-scale simulation. The purpose of building this prototype was just to prove the concept of parallel DLL algorithm execution in an array of FPGAs.

μDLL simulator (Fig. 8) is composed of 7 PCBs (Printed Circuit Boards). 6 of them contain 3 FPGAs (XC3S4000) each and constitute resources for the simulation nodes. The 7-th board is equipped with 2 FPGAs (XC2S150E) and it is responsible for synchronizing the simulation and for the communication of the whole system with a PC (Personal Computer). This board initializes the simulation and collects the simulation results.

The implementation of the DLL algorithm in μDLL simulator is described in details in [22]. Below the most general aspects of this implementation are presented in order to simplify the understanding of the μDLL simulator construction.

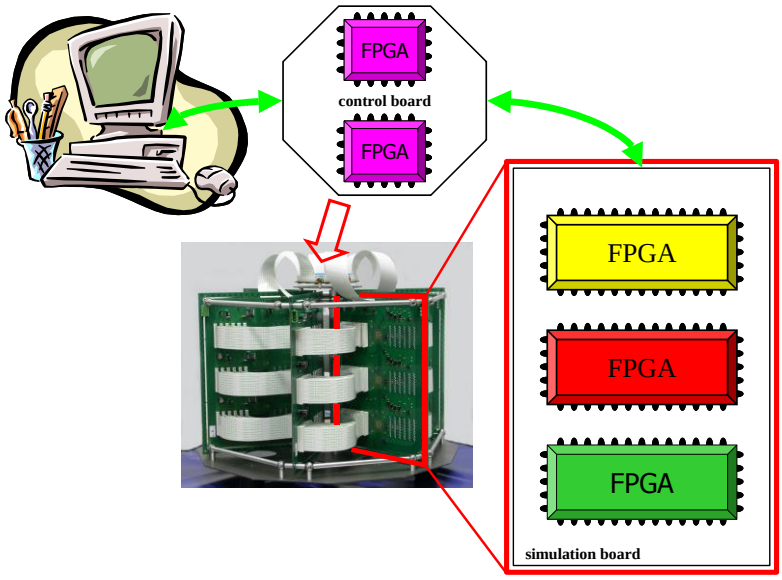

Fig. 8 μDLL simulator

In each FPGA on the simulation board a 2×6 array of nodes is implemented, thus the board represents a two-dimensional array containing 36 (6×6) nodes (9). 6 boards correspond to a three-dimensional array containing 216 (6×6×6) nodes.

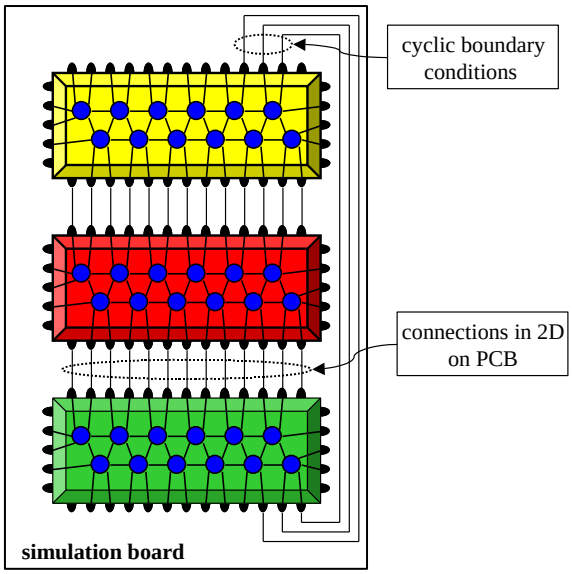

Fig. 9 Nodes and connections on simulation board

The lattice of nodes in μDLL simulator represents the face cubic centred (fcc) network with the coordination number of 12. In other words: during the simulation process each node exchanges the data with the closest 12 neighbours: 6 on the same board, 3 on the next board and 3 on the previous board. For this exchange in μDLL simulator the dedicated wires are designed.

Although the μDLL simulator proved the idea of parallel implementation of DLL algorithm in an array of FPGAs, its construction was fixed and could not be extended to perform the realistic physical or chemical simulations. In practical applications the DLL model should have about 10^6 (100×100×100) nodes.

3.3 Second prototype – mDLL simulator

The very promising results of implementation of the DLL algorithm in μDLL simulator encouraged the authors to design a new simulation board, which could constitute a basic building block of the full-scale DLL simulator. Therefore the second prototype of DLL simulator (Fig. 10) was designed and developed.

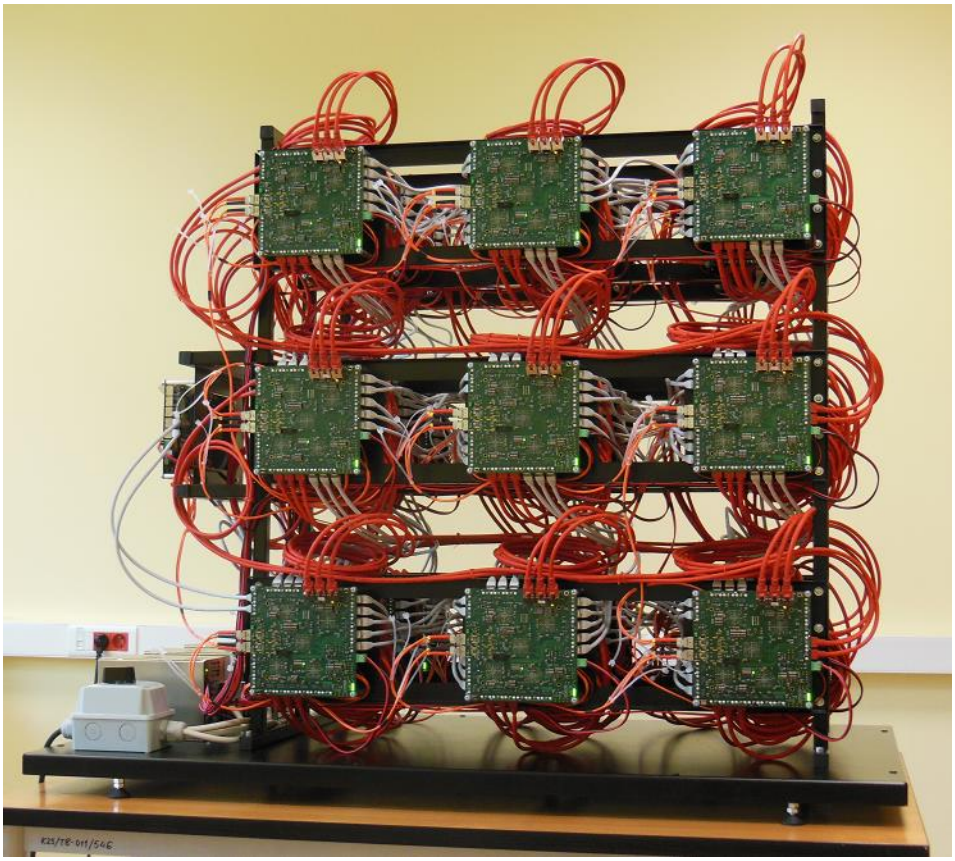

Fig. 10 mDLL simulator

The second prototype – mDLL simulator finished in 2012 – is composed of 27 simulation boards and one control board serving the same functionality as in μDLL simulator. It is still too small for practical applications but it allows testing the functionality of simulation board, which can be many times duplicated and used in the construction of a powerful computing machine.

Each simulation board contains 5 FPGAs: 4 of them, called simulation FPGAs (XC6SLX75), constitute resources for the nodes of the DLL algorithm and the 5-th FPGA (XC6SLX45T), called control FPGA, manages the operation of the simulation FPGAs (Fig. 11).

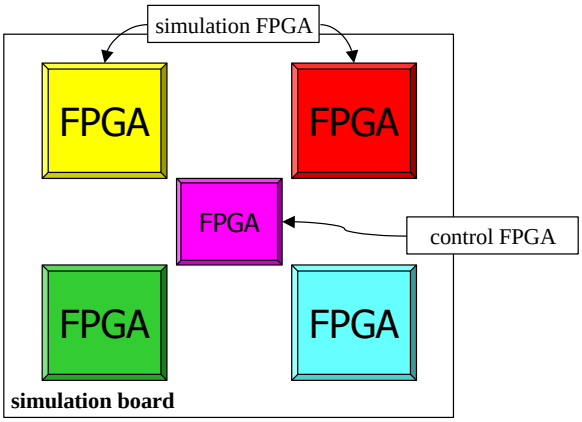

Fig. 11 Simulation board in second prototype

The simulation boards are connected in panels. To reduce the number of wires connecting the simulation boards in panel – which is very important in any big computational machine due to the feasibility and reliability reasons – the nodes in the mDLL simulator are not directly connected, as it was in μDLL simulator. The outputs of nodes, which must be transferred outside the FPGA, are grouped and transmitted serially. On the receiver side they are deserialised, ungrouped and delivered to appropriate inputs of the destination nodes. Sending the outputs and receiving the inputs of each node is performed simultaneously, using dedicated transfer protocol to achieve high data throughput.

The implementation of DLL algorithm on mDLL and μDLL simulators differs mainly in the organization of nodes in the simulation FPGA and in the communication among the nodes placed in different chips. In μDLL a dedicated one-bit routing path was devoted to each connection among such nodes. In mDLL the connections are merged in groups and transferred using fast serial links.

The number of nodes in one FPGA is configurable. For simple simulations it is possible to reduce the architecture of a node and to include more nodes in one chip.

3.4 DREAM supercomputer

The works on μDLL and mDLL simulators revealed the feasibility and efficiency of the FPGA-based DLL simulator. It gave an impulse to build such a simulator in a full scale within the confines of BioNanoPark+, which is currently coming into existence in

Lodz. Simultaneously, very positive conclusions, which emerged during the μDLL and mDLL development encouraged the constructors of both prototypes to find more applications for the powerful and flexible computing machine being constructed (the DLL simulator in BioNanoPark+ will be composed of over 25 000 FPGAs).

In this way the idea of Dynamically REconfigurAble polyMorphic (DREAM) supercomputer appeared. The fundamental aspect of this idea is to provide the scientists with the possibility to use the DREAM FPGAs without the need to define their functionality by means of HDL, as it is in case of μDLL and mDLL. Therefore an automatic conversion (compilation) from high level programming language (e.g. C++) to FPGA configuration bit-stream has been proposed. Furthermore, in order to equip the DREAM supercomputer with some extraordinary features supporting unconventional simulations, the bio-inspired mechanisms are planned to be implemented in it. These mechanisms (such as dynamic routing or self-replacement) will transform the set of FPGAs and cables into the fault tolerant, evolvable hardware ready to adopt itself to the problem to be solved.

4. ASIC Design for Commercial Applications

4.1. Industry oriented ASIC design and research

DMCS undertakes numerous industry-oriented activities. Application Specific Integrated Circuit (ASIC) design oriented cooperation with external enterprises begun with series of contracts with Tritem Microsystems GmbH company, conducted in cooperation with Institute of Electron Technology in Warsaw. DMCS team participants had valuable opportunity of working in typical commercially oriented ASIC design facilities abroad, owned by a major player on a IC-based solution market. Such experience is a big asset, especially in country like Poland, that generally lacks its own industrial design centres and modern foundries.

Result of the mentioned cooperation was a set of ASICs ready to preproduction phase tests. Some of these designs were introduced to mass production and are available on market, nowadays.

4.2. Continuation of industry-oriented research

DMCS staff got insight into work organisation, commercial design resource management and design methodology, during the abovementioned projects. Also, our staff had opportunity of undertaking real life design challenges. Thus, new ideas emerged during the projects. Some of them were checked and introduced during commercial projects, some we evaluated much later, though providing very interesting results.

One specific solution introduced during commercially oriented projects is a high voltage unity-gain voltage buffer. It was designed as a hybrid of two typical complementary voltage buffers – source follower and gate follower structures (Fig. 12). Very useful property set of this new structure enabled application of several untypical signal processing solution in HV integrated environments [24]. The buffer (Fig. 13) was granted a patent by Polish Patent Office in 2012 [25]. This is a rare achievement because what was patented was not a layout of the structure but scheme of transistor-level electrical connections and their applications in forming functionality of the buffer.

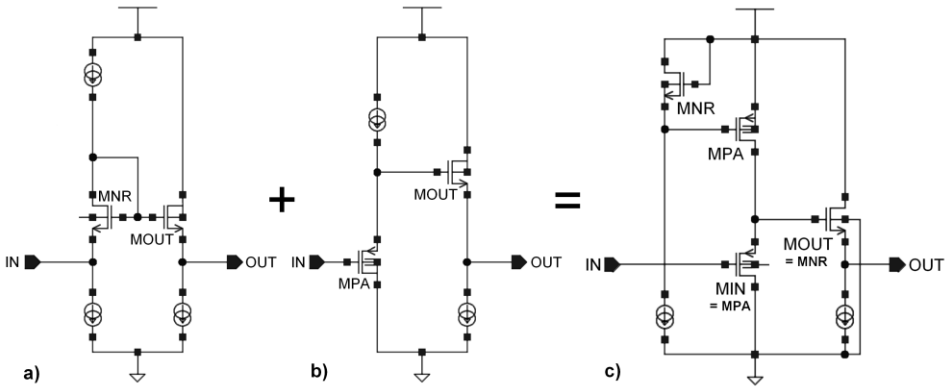

Fig. 12 Operation rule of the patented unity-gain buffer;
a) source follower, b) gate follower, c) combined follower

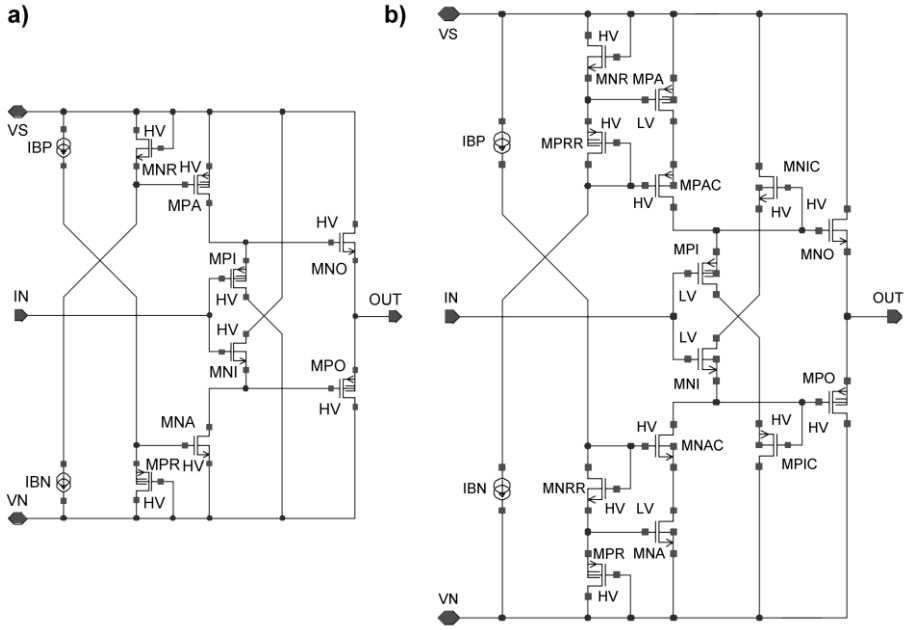

Fig. 13 The patented unity-gain high-voltage buffer;
a) simplified version, b) high-quality full version

When industry oriented projects and ASIC designs were completed, several design ideas were further studied and advanced. Several interesting circuits were elaborated and published in ISI list journals.

Much stress was put on overcoming problems with precise signal processing in high-voltage ASICs. Effective means of current-mode circuitry insertions into voltage-mode signal paths were studied and implemented. It must be stressed that simplicity and

precision of devised solutions was possible due to application of previously patented voltage buffer.

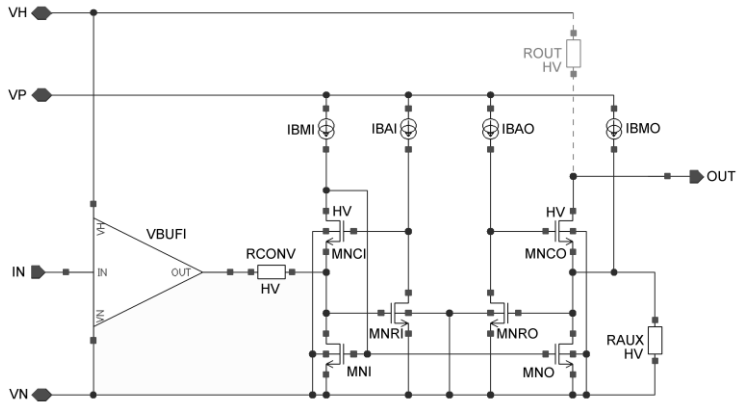

Fig. 14 Voltage/current/voltage converter for current-mode circuitry integrated into high-voltage voltage-mode signal paths

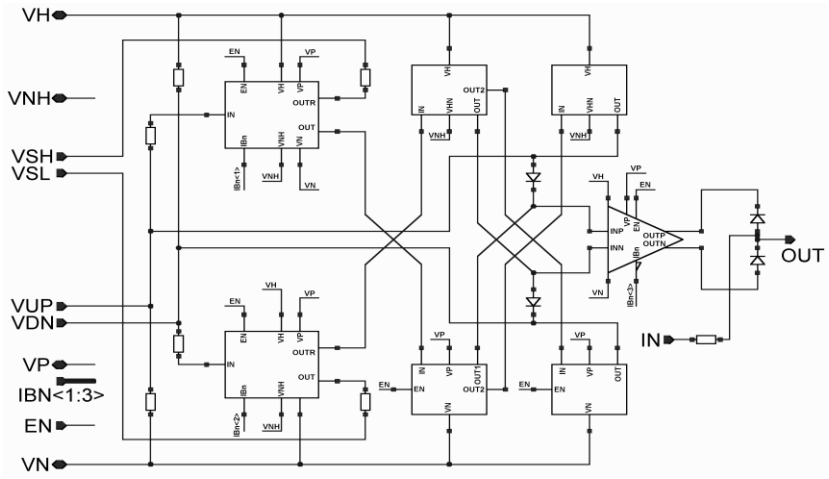

Fig. 15 Current-mode trapezoidal waveform generator and edge-rounded for high-voltage systems [29], based on unity-gain buffer [24] and current-mirrors (shown as boxes)

Set of simple but efficient voltage/current and current/voltage integrated converters was introduced [26] (and presented in Fig. 14) along with several function current-mode function blocks applicable to high-voltage CMOS and SoI integrated systems. These function blocks include current-mode versions of waveform invertors, amplifiers and DC-level shifters [26], [27]. They all can be placed inside high-voltage signal paths owing to design of voltage/current/voltage conversion system with use of no more than the devised

buffer combined with simple but efficient voltage/current/voltage converter tailored precisely for CMOS/SoI integrated systems [27].

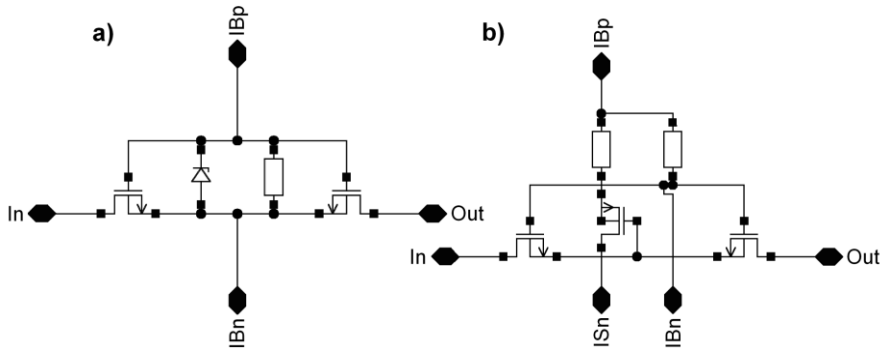

Fig. 16 Current-mode high-voltage switches for voltage (a, b) and current (c) applications

Set of current-mode trapezoidal waveform generators with fully controlled waveform parameters were studied and published [28]. Universal current-mode low-voltage and high-voltage trapezoidal waveform generators with edge-rounding functionality were invented and published [29]. This circuitry makes possible precise control over frequency, voltage-range and slew-rate control of the waveform in high-voltage integrated systems with use of nothing more than unity gain buffers and current mirrors (Fig. 15). For high-voltage signal switching applications, set of application-optimized high-voltage current-controlled switches for voltage and current signal paths has been devised and studied [30]. Some of them are presented in Fig. 16.

4.3. Continuation of industry-oriented research

DMCS continues commercially-oriented ASIC design activities. Proven and new industry entities enter various cooperation schemes with our Department.

Together with Institute of Electron Technology and Tritem Microsystems GmbH, our Department has applied for funds to build and test prototype system for remote and wireless identification, access control and supervisory. Several previously designed circuits are planned to be used for design of ASIC circuits related to this activity.

DMCS has also cofounded a consortium with Astri Polska Ltd and Center of Space Research of Polish Academy of Sciences, and has been applying for **E**uropean **S**pace **A**gency (ESA) funds to build ASICs for use in space industry. ESA expressed its interest and the consortium has been granted initial funds for in-depth feasibility study on a specialized ASIC for space applications.

Also, a three-year scientific project related to the study on modelling and simulation of the electro-magnetic phenomena in modern 3D integrated systems has been recently granted. Though this is a scientific project, it is expected to implement several functional blocks initially developed for commercial applications.

DMCS takes part in a number of projects at application stage where it is expected to design, implement and test various complex systems in the form of ASICs.

5. Development of Diagnostic Use Cases for the ITER Organisation

5.1. The ITER Organisation diagnostic and control systems

As the global energy consumption increases, the provision of efficient and clean energy sources becomes an urging necessity. One of the most promising way of energy production is the use of the nuclear fusion in thermonuclear reactors, such as tokamaks in which the plasma is confined in a toroidal shape using magnetic fields. Both the substrates and products of the Deuterium-Tritium fusion are not radioactive and are environmentally friendly.

The project of building the world's largest thermonuclear reactor is called ITER. It is a result of international cooperation of the European Union, India, Japan, Korea, Russia, China and the United States. It is built on the experience gained from the latest experiments, like Joint European Torus (JET) and Tore Supra and it will be the most technologically advanced tokamak so far. It is assumed to be able to produce 500 MW of energy with efficiency coefficient of at least 10. The machine is now being constructed at ITER, Cadarache, France. As the site construction process progresses, the need for development of sophisticated control and monitoring system is emerging. The technology being the result of the ITER project will be able to be commercialized in 2050, but the tokamak assembly should start in 2015 and till then the concept for its instrumentation shall be finished. Building and operating of the machine requires multidisciplinary effort not only by the physicists but also by the engineers. Since EU tends to reduce CO_2 production the new technology of energy production is especially crucial.

The control systems of modern tokamaks utilize a variety of telecommunication standards. JET, the largest fusion device in Europe, is operated via an old ATM network. Tore Supra is backboned by the SCRAMNet real-time shared memory and the VME standard. In both machines the data acquisition is performed with PXI, Eurocard, cPCI, VME and AdvancedTCA (ATCA) systems. Among these architectures, the PCI eXtensions for Instrumentation (PXI) gained popularity and is also considered one of the fundamental standards of the ITER project. The I&C systems of ITER require an architecture providing a higher Reliability, Availability, Maintainability and Inspectability (RAMI) than can be achieved with PXI. The xTCA (ATCA and MTCA) standards [31] [32] [33] [34] [35] seem to fulfil this requirement and are being successively added to the ITER PCDH catalogue.

The advantage of the PXI architecture (National Instruments) is wide availability of various I/O and processing modules, especially on markets not reached by competitive technologies. Also the LabVIEW graphical programming environment is easy to use for people with limited programming experience.

Although the PXI architecture is widely adopted and well tested, it also has some drawbacks:

- weak support for GNU/Linux and other Unix-like operating systems,
- significant limitation on type and number of backplane interfaces,
- no possibility of providing an effective redundancy scheme,
- lack of support for hardware interlock mechanisms.

The ATCA standard was developed for demanding telecommunication applications and later adapted for physics experiments. It concentrates on providing powerful computing

platform with high reliability. Due to high price of standard compliant components, it gains popularity slowly, mainly in the USA and Europe. The authors have gained experience in the field of ATCA-based systems by building a proof-of-concept DAQ system for ITER composed of off-the-shelf commercial components.

The last considered standard is the MTCA. This standard is similar to PXI, however it offers better performance and flexibility. The Advanced Mezzanine Card (AMC) modules, plugged into MTCA shelf may contain a variety of backplane interfaces, support hot-swap mechanism and offer an advanced monitoring and module management capabilities. Data transmission between the AMC modules takes place over Gigabit Ethernet, PCI Express, SATA, Serial RapidIO and similar high-speed serial interfaces. Due to high reliability and cost-effectiveness the MTCA-based systems are gradually gaining popularity in the industrial and scientific control systems [36] [37] [38] [39].

The potential of MTCA standard was already noticed by the world's leading physics laboratories. In response to this, the PCI Industrial Computer Manufacturers Group (PICMG) announced the establishment of the xTCA for Physics Coordinating Committee, in 2009. The sub-committee provides extensions and modifications to the plain telecommunication standard in order to adapt it for experimental research machines and detectors in such diverse fields as astronomy, high energy, photon, fusion and medical physics. The resulting subsidiary specification, the MTCA.4, is now under active development and receives contributions from a number of well-known laboratories and institutions such as ITER, DESY, CERN and many others. Members of the DMCS team are also involved in development of MTCA.4 standard working actively in PICMG xTCA for Physics since 2009.

The MTCA.4 specification introduces many improvements especially important for ITER [52]. For example, it enables some global scope signals (e.g. timing events, interlocks, additional clocks) to be transferred freely between cooperating modules. Also, it introduces the Micro Rear Transition Module (MRTM) which can effectively double the space available on the module and allows connecting signals from both sides of the chassis.

The PICMG expects that the MTCA.4 will be the common standard for physics experiments of the future. The authors believe that this standard can already offer a well-suited complete solution for ITER, although similar systems have not been built before using this architecture.

The ITER tokamak requires more than 150 various plant systems. Most of them are part of the I&C subsystem that can be logically divided into two layers: central coordination and local plant systems. The primary goal of ITER I&C system is to provide a fully integrated and automated control for the thermonuclear reactor. The most important part of I&C is the data acquisition system, which should collects signals from large number of digital/analogue channels (about 4000) and digital cameras (about 200). Since these signals come from different physical sources, they span a large range of different sampling frequencies (from kHz to GHz), resolutions (from 8 to 24 bits) and signal conditioning techniques (Table 1). Therefore the task of developing such data acquisition system is very demanding and requires pre-processing and processing of data on various hardware platforms (FPGA, GPU, CPU, etc.).

Table 1 Summary of example signal sources and required data processing

Measurement Group	Data IO	Signal Processing
Magnetics	1400 ADC (1 MS/s) 240 ADC (10 MS/s)	FPGA / GPU / CPU
Dosimetry and Fusion Products	50 ADC (100 MS/s)	FPGA / CPU
VIS/IR Cameras	24 cameras (1 kHz frame rate – 8Gb/s per camera)	FPGA / CPU
Optical (ex. LIDAR)	150 ADC (20 GS/s)	FPGA / GPU
Imaging Spectroscopy	~200 cameras and detector arrays (7 Gb/s)	FPGA / CPU
Spectroscopy and neutral particle analyzer	~50 ADC (1 GS/s)	FPGA / CPU
Bolometers	~500 ADC (1 MS/s)	FPGA / CPU

5.2. Diagnostic use cases

Most of the extremely complex ITER diagnostics systems are provided by the Domestic Agencies (DAs) and their partners. On their demand the IO has created several diagnostics use case examples to enhance the understanding of diagnostics Plant System I&C and the associated deliverables. The use cases come complete with documentation and implementation, further helping the DAs, their suppliers and diagnostic responsible officers to meet the ITER diagnostics requirements [40].
The Department of Microelectronics and Computer Science has prepared two of such use cases, one in ATCA and one in MTCA.4 form factor.

5.2.1. Data acquisition use case in the ATCA form factor

The data acquisition system designed and built by the authors is based on the ATCA and AMC standards. All the elements that comply with those standards are off-the-shelf devices. No in-house ATCA or AMC hardware has been made. This is due to ITER policy and is to ensure that such equipment is always available and proper tech support is provided for it. The system block diagram is presented in Figure 17 [41]. All the data communication in the system is based on the 1 and 10 gigabit Ethernet. The input of the system consists of a number of TEWS TAMC900 modules. Every card is divided into two logical submodules each of them sampling up to four channels with a frequency of up to 50 MS/s. Two AMC modules reside in one Emerson ATCA-7301 carrier board that connects to an Emerson ATCA-F120 10 Gb Ethernet switch over backplane. The receiving side of the system consists of an Emerson ATCA-7360 computation blade where the DAQ server runs. The received stream of data is forwarded to an external Data Archiver (backup system) via a 10 GbE connection. Simultaneously, data is sent to a TESLA S1070 computation blade via a PCIe x8 connection. In case of failure of the 10 GbE uplink to the Data Archiver or PCIe connection to the computation blade, data is stored in a dual HDD buffer. The HDD buffer is configured in a software Raid 0 configuration. The data is sent from the HDD buffer immediately when the connectivity is recovered. The photograph of the system is presented in Figure 18. The system is able to continuously process and forward to the archiving system the 800 Mb/s data coming from 5 modules simultaneously without dropping any data.

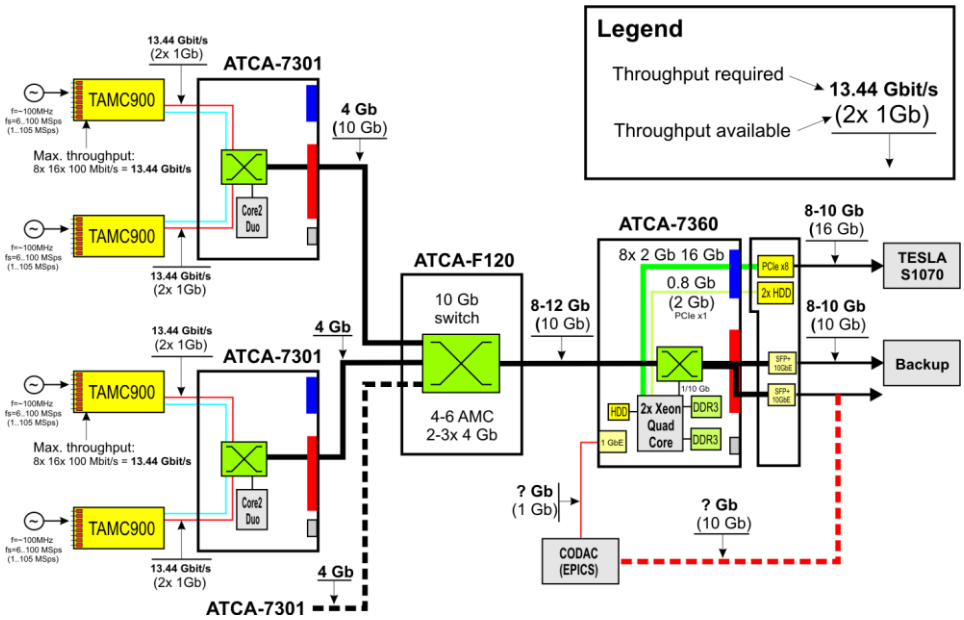

Fig. 17 Block diagram of the DAQ system with estimated throughputs.

Diagnostics systems based on the direct imaging are now widely used in Tokamaks for both the real-time plasma control and off-line physics studies. The visible light emitted by the plasma can be used to monitor the plasma position during the operation, as well as to detect some transient events, such as flying debris that could degrade or interrupt the plasma unexpectedly if not mitigated. The infrared light is also very important to measure the surface temperature of the plasma facing the components subject to high heat fluxes (several MW/m^2) and particle fluxes. The early detection of overheating areas, called hot spots, is of the primary importance for the protection of the machine during the plasma operation to avoid component damage, such as melting, and even leaks of the water-cooling systems installed behind the first wall components. To this end, images are analysed in real-time (up to several ms) to detect, identify and recognize abnormal events which will be provided for the central control systems. Image processing techniques are used to recognize spatiotemporal patterns of the expected thermal events (i.e. qualitative analysis). Then, adequate actions can be taken to decrease the components overheating or to change the plasma state to the safest conditions. Considering the high complexity of the machine geometry and plasma equilibrium, all of the in-vessel surface must be monitored with a resolution high enough to detect every local hot-spot of at most several centimetres in diameter. In the case of ITER, this means that the cameras used for machine protection function must cover up to 640 m^2 from a distance up to 10 meters. Cameras are also used for the understanding of plasma-wall interactions, e.g. to study the turbulence in the edge plasma, close to the vessel. In this case, the temporal resolution can be very high (200 kFPS) and the system must support the streaming as well as the access of large amount of imaging data. Recent applications of imaging networks in Tokamak show that combination of data from several cameras is very promising for the 3D

volume reconstruction (e.g. tomography), provided that data are well calibrated and synchronized.

Fig. 18 Hardware installed in the ITER cubicle – front view

5.2.2. Image diagnostics use case in the MTCA.4 form factor

An Image Acquisition System (IAS) is composed of a digital camera connected to a frame grabber card, image processing module and data transmission system [42][43][44][45][49]. The acquired images are sent to the image processing system. The system distributes data for further processing and archiving. The processed data are sent using low-latency

connection to the machine control or protection system [53]. The buffered images with attached metadata are sent for archiving via the high-throughput connection. The metadata describes collected data (image resolution, bit depth, frame rate, etc.) and precisely defines when the images were created. The global synchronization network delivers a reference clock and a trigger signal that define when the images are acquired and allow calculating timestamps. A block diagram of IAS is presented in Fig. 19. The IAS based on MTCA.4 specification consists of:

- digital cameras connected to frame grabber modules,
- Camera Link receiver mezzanine module [54],
- frame grabber modules with local processing power,
- synchronization and timing distribution module connected to Time Communication Network (TCN),
- image processing module based on external industrial computers with GPUs,
- high-throughput network links to Data Archiving Network (DAN) and Synchronous Data Network (SDN).

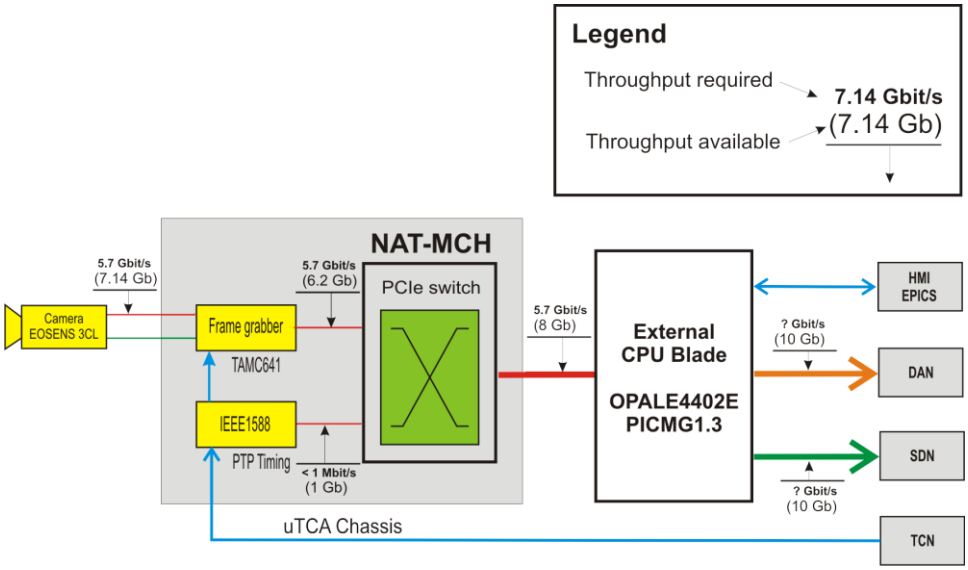

Fig. 19 A block diagram of IAS implemented in MTCA.4.

The flow of the digital data starts with the camera. Data from the camera is transferred to a dedicated frame grabber module, realized as an Advanced Mezzanine Card (AMC) hosted in the MTCA.4-compliant shelf. The shelf is connected to an external CPU module using the PCIe cable link. Video data from the frame grabber is transferred using a DMA directly to the host computer memory. From there, the data are made available through two 10 Gb/s Ethernet connections.

The IAS is installed in the ITER CODAC technical room. The MCH NAT-MCHPHYS fabricated by NAT with the RTM PCIe uplink (PCIe x4, gen. 2) was used. The maximum theoretical bandwidth of the PCIe x4, gen. 1 connection on the frame grabber card is 8 Gb/s. To evaluate the performance of the DMA module on the frame

grabber card, the switch hierarchy, the root complex and the software driver a special performance testing module, sending the test data at the maximum possible speed has been implemented in the firmware. Using this module, the maximum achievable data rate from the single module has been measured as 800 MB/s. This result is fully satisfactory for the system with a single camera as it is equal to the CameraLink theoretical maximum of 6.4 Gb/s. The link between the PCIe switch on the MCH and the external CPU is currently limited to the PCIe x4, gen. 2. This allows transferring payload data with a theoretical throughput up to 1.6 GB/s (12.8 Gb/s). In this configuration image acquisition can be done from two frame grabber cards running almost at full link saturation. The system with two frame grabber cards has also been tested. In this case, the maximum throughput from the single AMC module was limited to about 6.2 Gb/s.

One of the key issue in integration of all control and diagnostic subsystems is distribution of reference clock and precise synchronization. In the tokamak the reference time is distributed via dedicated Time Communication Network (TCN) using the IEEE 1588-2008 protocol, called Precision Time Protocol (PTP). The assumed synchronization accuracy that is ensured by this solution is 50 ns RMS. The application of the PTP-based network causes that every subsystem needs to be equipped with timing receiver capable of receiving reference time from TCN network, generating synchronous clock and trigger signals and provide support for timestamping of external signals. As there are no commercially available solutions that may be used at MTCA-based ITER diagnostic systems, it was necessary to design new MTCA.4-compliant timing module providing support for the PTP and ensuring required synchronization accuracy [46].

The module is based on a recent Spartan-6 FPGA circuit from Xilinx. The programmable device hosts complex microprocessor system built around the MicroBlaze core. The firmware image is too large to fit in the FPGA's integrated memory and is hence stored and executed in the external DDR2 SDRAM. The FPGA bitstream is loaded from the external SPI FLASH memory. The RAM memory is preloaded on system start-up using contents of the SPI FLASH memory. The hardware structure of the PTM module is presented in 20. The PTM-1588 module accesses the timing network using Gigabit Ethernet interface using the regular 8P8C modular connector. The module not only synchronizes its internal counters with the PTM master, but also provides synchronized clocks. The module reference frequency is generated by the Oven Controlled Voltage Controlled Crystal Oscillator (OCVCXO). The clock phase correction is achieved by manipulation of the OCVCXO frequency. Its frequency can be shifted in 10 ppm range using an external tuning voltage provided by the FPGA controlled DAC. The module produces 100 MHz clock and Pulse Per Second (PPS) signal on the front panel output and both 10 MHz and 100 MHz on the backplane. Apart from that, there are 8 programmable lines on the backplane and 2 on the front panel, that can be used for generation of Future Time Events and timestamping of external signals. The module is configured and operated mainly by means of the PCIe interface. The board is manageable through the Intelligent Platform Management Interface (IPMI) protocol thanks to custom developed Module Management Controller (MMC), analogous to the one presented in [47], [48], [50], [51]. This subsystem is responsible for monitoring the module health and maintaining its state. The PTM-1588 board has been tested at ITER, using the GPS-synchronized grandmaster clock Symmetricom Xli and three cascaded Hirschmann MAR1040 switches. At the same time, the PPS output of the grandmaster clock is connected to the front-panel input of the board using the 50 Ohm coaxial cable. The delay of the cable, input and

output drivers has been calibrated by connecting the PPS output to FTE input via a cable and timestamping it locally. The PPS error has been measured for 237230 samples (the test lasted 2.7 days). The RMS value of the error was 11.7 ns.

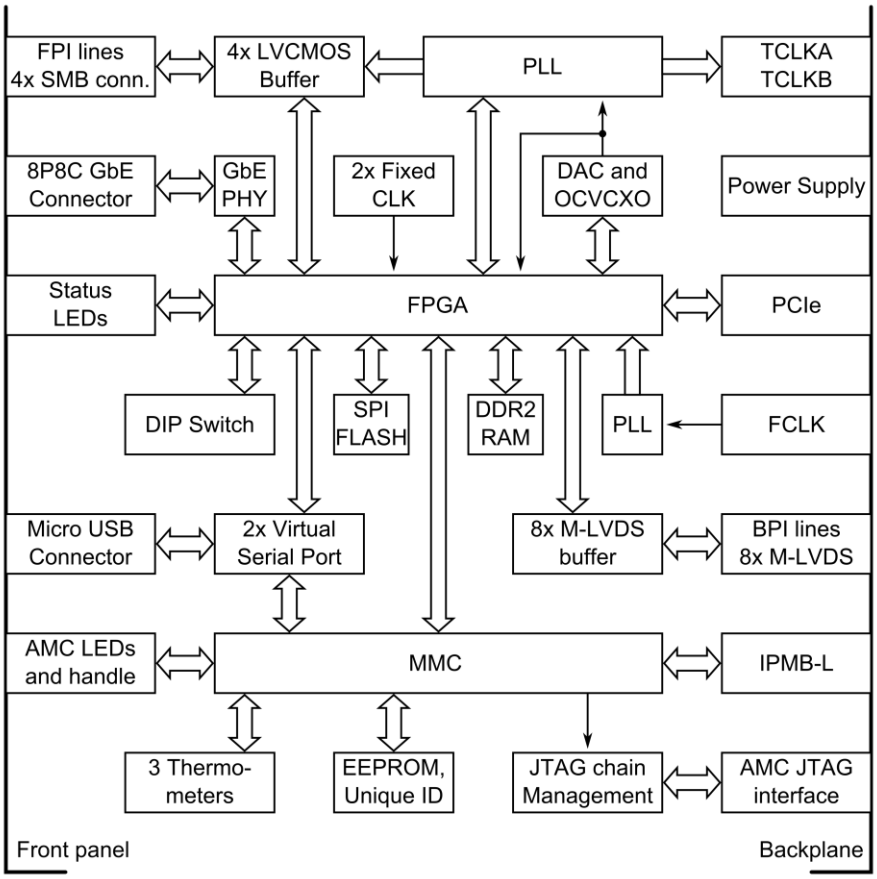

Fig. 20 Precise Timing Module – hardware structure

6. CONCLUSIONS

In this paper some chosen research topics conducted in DMCS TUL have been presented. At first several MEMS (Micro Electro-Mechanical Systems) devices have been analysed and simulated. New modelling methodologies have been proposed and some new device models (microbolometer and micromembrane) have been invented. Next the new model of SiC MPS (Merged PIN-Schottky) diodes has been proposed. To develop the electro-thermal MPS model, a novel model generation approach has been applied which is based on the NID method and time constant spectrum examination. It offers greater simplicity and better numerical properties while preserving the physical meaning of the obtained CTM. The thermal model is coupled with the electrical part to form the

complete electro-thermal model. The proposed approach has been demonstrated for the CSD20030 common-cathode dual MPS rectifier manufactured by Cree. The new proposed model of SiC MPS (Merged PIN-Schottky) diodes is in full agreement with the real MPS devices. These works will be continued in the frame of the European project ADEPT (Advanced Electric Powertrain Technology). Its aim is to produce a virtual development environment for electric propulsion systems for EVs and HEVs (Electrical and Hybrid Electrical Vehicles). It is expected that SiC devices will be heavily applied in these applications to reduce power loss and cooling needs, thus enabling an extension of the vehicle's operating distance range. However, reliable device models are needed for efficient circuit design and optimization. The idea of **D**ynamically **RE**configur**A**ble poly**M**orphic supercomputer (DREAM) was born in DMCS in 2010. The simulations of polymers by means of DLL algorithm require many logic units called nodes. Instead of discrete elements, dedicated ASICs or microprocessors, the reconfigurable devices such as FPGAs (Field Programmable Gate Arrays) have been used. The fundamental aspect of this idea is to provide the scientists with the possibility to use the DREAM FPGAs without the need to define their functionality by means of HDL, as it is in case of μDLL and mDLL. Therefore an automatic conversion (compilation) from high-level programming language (e.g. C++) to FPGA configuration bit-stream has been proposed. DMCS undertakes numerous industry-oriented activities. Several interesting circuits were elaborated and published in ISI list journals. DMCS continues commercially-oriented ASIC design activities. Proven and new industry entities enter various cooperation schemes with our Department. Together with the Institute of Electron Technology and Tritem Microsystems GmbH, our Department has applied for funds to build and test prototype system for remote and wireless identification, access control and supervisory. Several previously designed circuits are planned to be used for design of ASIC circuits related to this activity. DMCS has also cofounded a consortium with Astri Polska Ltd and Space Research Centre of the Polish Academy of Sciences, and has been applying for **E**uropean **S**pace **A**gency (ESA) funds to build ASICs for use in space industry. ESA expressed its interest and the consortium has been granted initial funds for in-depth feasibility study on a specialized ASIC for space applications. A three-year scientific project with potential commercial applications has been recently granted to DMCS. Its research part focuses on modelling and simulation of electro-magnetic phenomena in modern 3D integrated systems. Practical applications will be driven by the implementation of several function blocks designed to fulfil commercial demands. As the last point the project of building the world's largest thermonuclear reactor – ITER has been presented. The control systems of modern tokamaks utilize a variety of telecommunication standards. DMCS proposed to apply xTCA (ATCA and MTCA) standards in order to fulfil the requirement of the project. For the real-time plasma control and off-line physics studies, a diagnostics system based on direct imaging has to be developed. The visible light emitted by the plasma can be used to monitor the plasma position during operation as well as to detect some transient events, such as flying debris that could degrade or interrupt the plasma unexpectedly if not mitigated. The infrared light is also very important to measure the surface temperature of the plasma facing the components subject to high heat fluxes (several MW/m^2) and particle fluxes. Images must be analysed in real-time (up to several ms) to detect, identify and recognize abnormal events which information will be provided for the central control systems. Cameras are also used for the understanding of plasma-wall interactions, e.g. to study the turbulence in

the edge plasma close to the vessel. In this case, the temporal resolution can be very high (200 kFPS) and the system must support the streaming as well as the access to large amounts of imaging data. Recent applications of imaging networks in tokamaks show that a combination of data from several cameras is very promising for the 3D volume reconstruction (e.g. tomography), provided that data are well calibrated and synchronized.

REFERENCES

[1] Esteve D., Alderman J., Cane C., Courtois B., Glesner M., Napieralski A., Rencz M., Samitier J., Troccaz J., Cinquin P., Dillman J.: *"Basic research for microsystems integration"*, Cepadus-Editions, Toulouse, France, 1997, s. 266 ISBN 2-85428-465-8.

[2] Bhan R. K., Saxena R. S., Jalwania C. R., and Lomash S. K.: "Uncooled Infrared Microbolometer Arrays and their Characterisation Techniques", Def. Sci. J.59, pp. 580–590 (2009)

[3] ANSYS® Workbench, http://www.ansys.com

[4] COMSOL® Multiphysics, http://www.comsol.com

[5] Zajac P., Szermer M., Maj C., Zabierowski W., Melnyk M., Matviykiv O., Napieralski A., Lobur M.: "Study of Dynamic Thermal Phenomena During Readout of Uncooled Titanium-based Microbolometer", Memstech, 16-20 April 2013, Polyana, Ukraine, pp. 40-42

[6] Janicki M., Zajac P., Szermer M., Napieralski A.: "Compact thermal modeling of microbolometers", 15th International Conference on Thermal, Mechanical and Multi-physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 7-9 April 2014, Ghent, Belgium, pp. 1-4

[7] Maj C., Olszacki M., Al Bahri M., Pons P.: "Analytical model of electrostatic membrane-based actuators", 10th International Conference on Thermal, Mechanical and Multi-physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 26-29 April 2009, Delft, Netherlands, pp. 1-6

[8] Suni T.: "Direct wafer bonding for MEMS and microelectronics", VTT Publications, Espoo, Finland, 2006

[9] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 645–655, 1993.

[10] Zubert M., Napieralska M., Jabłoński G., Starzak Ł., Janicki M., Napieralski A.: Static Electro-Thermal Model of SiC Merged PiN Schottky Diodes. W: *10th International Seminar on Power Semiconductors ISPS'10*, Prague, Czech Republic, 1-3 Sep 2010, Prague, ed. V.Benda, 2010, s.282. pp.227-232.

[11] J. Zarebski and J. Dabrowski, "SPICE modelling of power Schottky diodes," *Int. J. Numer. Modelling: Electron. Networks, Devices and Fields*, vol. 21, no. 6, pp. 551–561, 2008.

[12] W. Janke and A.Hapka, "Nonlinear thermal characteristics of silicon carbide devices," *Mater. Sci. Eng.*: B, vol. 176, no. 4, pp. 289–292, 2011.

[13] V. Szekely, "On representation of infinite-length distributed RC one-ports," *IEEE Trans. Circuits Syst.*, vol. 38, no. 7, pp. 711–719, 1991.

[14] M. Janicki, J. Banaszczyk, B. Vermeersch, G. De Mey, and A. Napieralski, "Generation of reduced dynamic thermal models of electronic systems from time constant spectra of transient temperature responses," Microelectron. Rel., vol. 51, no. 8, pp. 1351–1355, 2011.

[15] Lukasz Starzak, Mariusz Zubert, Marcin Janicki, Tomasz Torzewicz, Malgorzata Napieralska, Grzegorz Jablonski, Andrzej Napieralski. Behavioral Approach to SiC Merged Diode Electro-Thermal Models Generation. *IEEE Transaction on Electron Devices*. February 2013, Volume 60, No 2:, pp. 630-638

[16] Zubert, M.; Starzak, L.; Jablonski, G.; et al. An accurate electro-thermal model for merged SiC PiN Schottky diodes. *Microelectronics Journal* Volume: 43 Issue: 5, 312-320, May 2012.

[17] V. Zeng. (2012, Jan. 6). High efficiency system design with Infineon power discrete-Infineon CoolMOSTM, OptiMOSTM, IGBT and SiC diode. Infineon. [Online]. Available: *www.infineon.com/cms/cn/corporate/promopages/CSR/8.ppt*

[18] Zubert M., Janicki M., Napieralska M., Jabłoński G., Starzak Ł, Napieralski A.: "Behavioural Electro-Thermal Modelling of SiC Merged PiN Schottky Diodes". *Scientific Computing in Electrical Engineering SCEE 2010. Series: Mathematics in Industry*, Vol. 16, Part III. Subseries: The European Consortium for Mathematics in Industry. Eds.: Michielsen, Bastiaan; Poirier, Jean-René. 1-st Edition., 2011, Springer-Verlag 2012, pp. 223-231

[19] Sabry M.-N., "Compact thermal models for electronic systems," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 1, pp. 179–185, 2003.

[20] M. Zubert, L. Starzak, G. Jabłoński, M. Napieralska, M. Janicki, A. Napieralski. „Novel SPICE Dynamic Model of SiC Merged PiN Schottky Diodes". *2011 Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)*, 16-18 June 2011, pp. 541 – 544

[21] Janicki, Z. Kulesza, T. Torzewicz, and A. Napieralski, "Automated stand for thermal characterization of electronic packages," in *Proc. 27th IEEE Semiconductor Thermal Measurement, Modeling and Management Symp*., San Jose, CA, 2011, pp. 199–202.

[22] Jung J., Polanowski P., Pakuła T., Kiełbik R., Napieralski A., Ulański J., „Hardware implementation of Dynamic Lattice Liquid model as a way of investigation of very complex molecular systems", Proceedings of the 6th Hellenic Conference on Polymers, Patras, Greece, November 2006, pp. 285-286

[23] Polanowski P., Jung J., Kiełbik R.: "Special Purpose Parallel Computer for Modelling Supramolecular Systems based on the Dynamic Lattice Liquid Model", Computational Methods In Science And Technology 16(2), 2010, ISSN 1505-0602, pp. 147-153.

[24] Jankowski M., Napieralski A.: High-Voltage high input impedance unity-gain voltage buffer, Microelectronics Journal, 2013, vol. 44, no. 7, p. 576-585

[25] Patent issued by Polish Patent Office "Uklad bufora napieciowego," (eng. "Voltage Buffer Circuit"), inventor: Jankowski Mariusz, designee: Automatix spółka z o.o., exclusive right kind and number WYN: (11) 212837, granted: 19 June 2012, published: 22 June 2012.

[26] Jankowski M., Napieralski A.: Novel Structure of CMOS Voltage-to-Current Converter for High Voltage Applications, Nanotech Conference & Expo 2012, June 18-21 2012, Santa Clara, California, USA

[27] Jankowski M., Napieralski A.: Current-mode signal processing implementation in HV SoI integrated systems, Microelectronics Journal, Volume 45, Issue 7, July 2014, Pages 946–959

[28] Jankowski M., Jabłoński G.: Adjustable Generator of Edge-Rounded Trapezoidal Waveforms. International Journal of Electronics and Telecommunications, 2012, vol. 58, no. , p. 213-218

[29] Jankowski M., Napieralski A.: High-voltage trapezoidal waveform generator with edge-rounding functionality implementations, Proceedings of the 21st International Conference Mixed Design of Integrated Circuits & Systems (MIXDES), 19-21 June 2014, pp. 224 – 229

[30] Jankowski M., Napieralski A.: Current-controlled switches for HV SoI processes, Microelectronics Journal, Volume 45, Issue 7, July 2014, Pages 931–945

[31] S. Simrock, L. Bertalot, M. Cheon, C. Hansalia, D. Joonekindt, G. Jablonski, Y. Kawano, W.-D. Klotz, T. Kondoh, T. Kozak, P. Makijarvi, D. Makowski, A. Napieralski, M. Orlikowski, M. Park, S. Petrov, A. Piotrowski, P. Predki, I. Semenov, D. Shelukhin, V. Udintsev, G. Vayakis, A. Wallander, M. Walsh, S. Wu, S. Yang, and I. Yonekawa, "Evaluation of the ATCA fast controller standard for ITER diagnostics," Fusion Engineering and Design, vol. 87, no. 12, pp. 2100 – 2105, 2012.

[32] D. Makowski, W. Koprek, T. Jezynski, A. Piotrowski, G. Jablonski, W. Jalmuzna, K. Czuba, P. Predki, S. Simrock, and A. Napieralski, "Prototype Real-Time ATCA-Based LLRF Control System," Nuclear Science, IEEE Transactions on, vol. 58, no. 4, pp. 1553 –1561, aug. 2011.

[33] A. Piotrowski and D. Makowski, "PCIExpress Hot-plug Mechanism in Linux-based ATCA Control Systems," Wroclaw, Poland, June 2010.

[34] D. Makowski, W. Koprek, T. Jezynski, A. Piotrowski, G. Jablonski, W. Jalmuzna, and S. Simrock, "Interfaces and communication protocols in ATCA-based LLRF control systems," in Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE, Oct. 2008, pp. 32–37. [3]

[35] D. Makowski, W. Koprek, T. Jezynski, A. Piotrowski, G. Jablonski, W. Jalmuzna, K. Czuba, P. Predki, S. Simrock, and A. Napieralski, "Prototype Real-Time ATCA-Based LLRF Control System," Nuclear Science, IEEE Transactions on, vol. 58, no. 4, pp. 1553 –1561, aug. 2011.

[36] J. Branlard, G. Ayvazyan, V. Ayvazyan, M. K. Grecki, M. Hoffmann, T. Jezynski, I. M. Kudla, T. Lamb, F. Ludwig, U. Mavric, S. Pfeiffer, H. Schlarb, C. Schmidt, H. C. Weddig, B. Yang, K. Oliwa, W. Wierba, W. Cichalewski, K. Gnidzinska, W. Jalmuzna, D. R. Makowski, A. Mielczarek, A. Napieralski, P. Perek, A. Piotrowski, T. Pozniak, K. Przygoda, S. Korolczuk, J. Szewinski, P. Barmuta, S. B. Habib, L. Butkowski, K. Czuba, M. Grzegrzolka, E. Janas, J. Piekarski, I. Rutkowski, D. Sikora, L. Zembala, and M. Zukocinski, "The European XFEL LLRF System," in International Particle Accelerator Conference, New Orleans, USA, May 2012.

[37] A. Mielczarek, D. Makowski, G. Jablonski, A. Napieralski, P. Perek, P. Predki, T. Jezynski, F. Ludwig, and H. Schlarb, "uTCA-based Controller," in Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference, June 2011, pp. 165 –170.

[38] I. Rutkowski, K. Czuba, D. Makowski, A. Mielczarek, H. Schlarb, and F. Ludwig, "Vector Modulator Card for MTCA-Based LLRF Control System for Linear Accelerators," Nuclear Science, IEEE Transactions on, vol. 60, no. 5, pp. 3609–3614, Oct 2013.

[39] D. Makowski, G. Jablonski, P. Perek, A. Mielczarek, P. Predki, H. Schlarb, and A. Napieralski, “Firmware Upgrade in xTCA Systems”, Nuclear Science, IEEE Transactions on, vol. 60, no. 5, pp. 3639–3646, Oct 2013.

[40] S. Simrock, L. Abadie, R. Barnsley, L. Bertalot, P. Makijarvi, J. Y. Journeaux, R. Reichle, D. Stepanov, G. Vayakis, I. Yonekawa, A. Wallander, M. Walsh, P. Patil, D. Makowski, and V. Martin, “Diagnostics use case examples for ITER plant instrumentation,” in International Conference on Accelerator and Large Experimental Physics Control Systems, ICALEPCS, 2013, June 2013.

[41] A. Piotrowski, M. Orlikowski, T. Kozak, P. Predki, G. Jablonski, D. Makowski, and A. Napieralski, “Performance Optimisation in Software for Data Acquisition Systems,” Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference, pp. 189 – 194, June 2011, ISBN 978-1-4577-0304-1.

[42] A. Mielczarek, P. Perek, D. Makowski, M. Orlikowski, G. Jablonski, and A. Napieralski, “AMC frame grabber module with PCIe interface,” Mixed Design of Integrated Circuits and Systems (MIXDES), 2013 Proceedings of the 20th International Conference, pp. 137 – 142, June 2013, ISBN 978-83-63578-00-8.

[43] P. Perek, M. Orlikowski, G. Jablonski, A. Mielczarek, D. Makowski, K. Zagar, and S. Isaev, “Software Components of MTCA-based Image Acquisition System,” Mixed Design of Integrated Circuits and Systems (MIXDES), 2013 Proceedings of the 20th International Conference, pp. 137 – 142, June 2013, ISBN 978-83-63578-00-8.

[44] Perek P., Wychowaniak J., Makowski D., Orlikowski M., Napieralski A., “Image Acquisition and Visualisation in DOOCS and EPICS Environments”, Int. J. Microelectron. Comput. Sci., 2012, vol. 3 no. 2, pp. 60-66, ISSN 2080-8755

[45] Mielczarek A., Makowski D., Jablonski G., Perek P., Napieralski A., “Image Acquisition Module for uTCA systems”, Mixed Design of Integrated Circuits and Systems (MIXDES), 2012 Proceedings of the 19th International Conference, 24-26 May 2012, pp. 156-160, ISBN 978-1-4577-2092-5

[46] G. Jabłoński, D. Makowski, A. Mielczarek, M. Orlikowski, P. Perek, A. Napieralski, P. Makijarvi, and S. Simrock, “IEEE 1588 Time Synchronization Board in MTCA.4 Form Factor,” in Real Time Conference (RT), 2014 19th IEEE-NPSS, 2014.

[47] P. Perek, A. Mielczarek, P. Predki, D. Makowski, and A. Napieralski, “Module Management Controller for MicroTCA-based Controller Board,” International Journal of Microelectronics and Computer Science, vol. 3, no. 1, 2012, pp. 25–31, 2012, ISSN 2080-8755.

[48] D. Makowski, A. Mielczarek, P. Perek, M. Fenner, F. Ludwig, M. Uros, J. Szewinski, and A. Schlarb, H. Napieralski, “Standardized Solution for Management Controller for MTCA.4,” in Real Time Conference (RT), 2014 19th IEEE-NPSS, 2014.

[49] Perek P., “High-performance Image Processing System for Plasma Diagnostics”, Proceedings of the XV International PhD Workshop OWD 2013, Wisła, Poland, pp. 328-331

[50] T. Kozak, P. Prędki, D. Makowski, "Real-Time IPMI Protocol Analyzer," *Nuclear Science, IEEE Transactions on* , vol.58, no.4, pp.1857,1863, Aug. 2011

[51] P. Prędki, D. Makowski, A. Napieralski, "Intelligent Platform-Management Controller for Low-Level RF Control System ATCA Carrier Board," *Nuclear Science, IEEE Transactions on* , vol.58, no.4, pp.1538,1543, Aug. 2011

[52] D. Makowski, A. Mielczarek, P. Perek, A. Napieralski, L. Butkowski, J. Branlard, M. Fenner, H. Schlarb, B. Yang, " High-Speed Data Processing Module for LLRF" in Real Time Conference (RT), 2014 19th IEEE-NPSS, 2014.

[53] D. Makowski, A. Mielczarek, P. Perek, G. Jabłonski, M. Orlikowski, A. Napieralski, P. Makijarvi, S. Simrock, V. Martin, "High-Performance Image Acquisition and Processing System with MTCA.4" in Real Time Conference (RT), 2014 19th IEEE-NPSS, 2014

[54] A. Mielczarek, D. Makowski, G. Jabłoński, P. Perek, M. Orlikowski, "FMC Video Acquisition Module with Camera Link Interface", International Journal of Microelectronics and Computer Science 2012, Volume 3, Number 3, ISSN: 2080-8755