

CS224: Assignment 8

Weightage: 10%

Date of Demonstration: 22nd April 2025 (2PM-5PM) in H/W Lab.

Problem Statement: Implement a subset of the MIPS processor.

Description: Design a processor implementing a subset of core MIPS instruction set

Reference: [P&H] Computer Organization & Design: The HW/SW interface – by Patterson & Hennessy

Design a single cycle 32-bit MIPS implementation that includes a subset of the core MIPS instruction set

- The memory reference instructions: load word (lw) and store words (sw)
- The arithmetic-logical instructions: add, sub, and, or, and set-less-than (slt)
- Control transfer instructions: branch equal (beq) and jump (j)
- Instruction for supporting subroutine: jump and link (jal)

[Note: Refer to the P&H book for detailed instruction formats and meaning]

Design the data-path (Instruction memory (only read access), Data memory (read and write), Register file (32 numbers of 32 bit registers), ALUs, MUXes, Shifter, and Sign Extender, Program counter etc), and controller of the processor (executes one instruction in a single cycle).

Implement all data-path units as separate Verilog modules to design the processor datapath in modular fashion. To test, set a specific value to the data and instruction memories and execute the instruction. Behavioral level implementation is not allowed in this Assignment. Note that the instruction set is complete i.e., any meaningful program can be written with these 10 instructions. The test cases must have some meaningful programs covering usage of all instructions. No FPGA or breadboard level demo is needed. Only simulation results will be sufficient.

Evaluation:

1. **The Verilog Implementation of the processor. The quality of the implementation.**
2. **The Test bench covering various scenarios.**

Guidelines:

- All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration.
- The grading will be based on (a) Correctness, (b) Quality of design (c) Cleanliness/modular design, (d) Use of proper Comment/Naming/Labeling of the design components and (e) Questionnaire and explanation and (e) correctness of your Verilog implementation.
- The Verilog implementation will also be checked during evaluation.
- You may find similar implementation in the internet. You can use them as a reference but you should write your own Verilog.

Submission:

You need to submit following items in a zip folder. For each group, one of the member must submit the report. One submission per group. We will share the marks in teams against your submission each Assignment.

1. A PDF file containing (i) clear diagram of the design (ii) Logic behind the circuit obtained. The report must be available during Lab evaluation.
2. Verilog code of your design
3. Test bench file