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# DEMC Assignment

## Magnitude comparator:

- It is a combinational circuit that compares 2 numbers 'A' & 'B' and determine their relative magnitude. The outcome of the comparator is specified by 3 binary variables that indicate whether A > B, A = B & A < B.
- Any Magnitude comparator takes 2 inputs of any length & produce 3 outputs.

## Types of comparators:

### ① 1-bit comparator:-

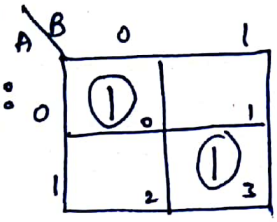
It is used to compare 2, 1-bits of A & B.

Truth table:

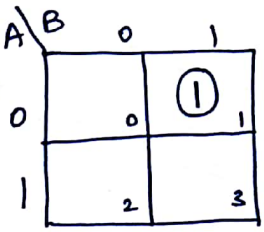
| A | B | A = B | A < B | A > B |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |

K-Map:

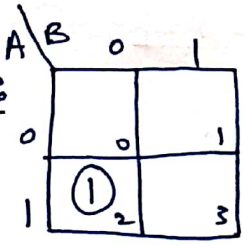
A = B:




A < B:




A > B:



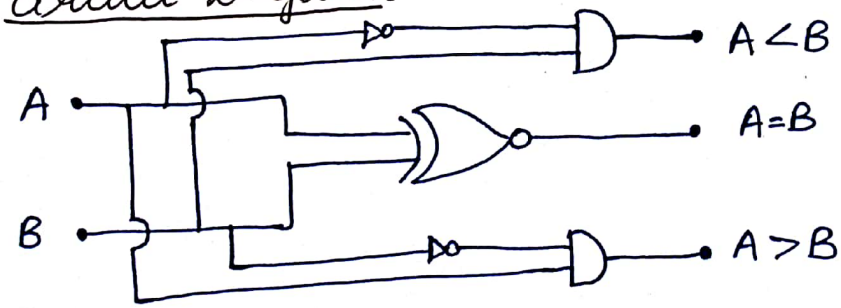

A = B: $\bar{A}\bar{B} + AB$

A < B: $\bar{A}B$

A > B: $A\bar{B}$

A = B: $A \odot B$

Circuit diagram:



## ② 2-bit comparator:-

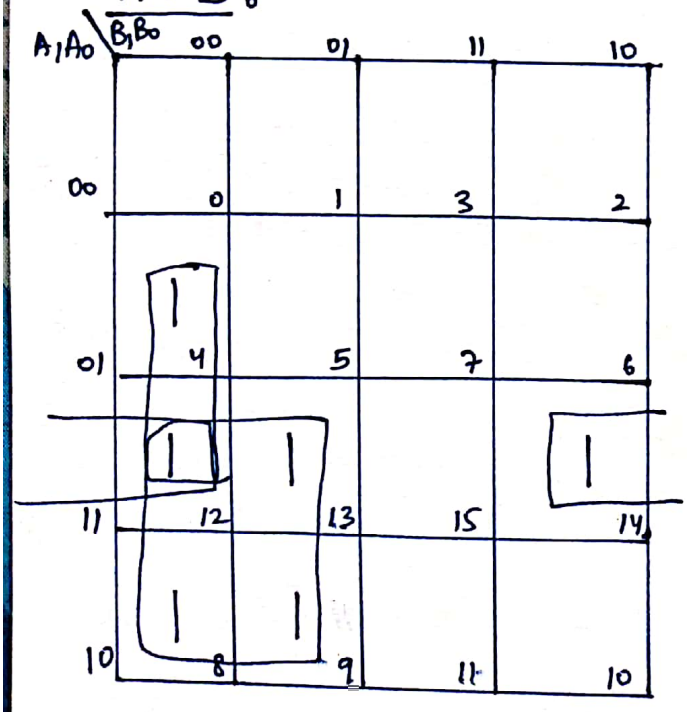
It is used to compare two 2-bits of A & B.

Truth table:

| $A_1$ | $A_0$ | $B_1$ | $B_0$ | A>B | A=0 | A<B |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

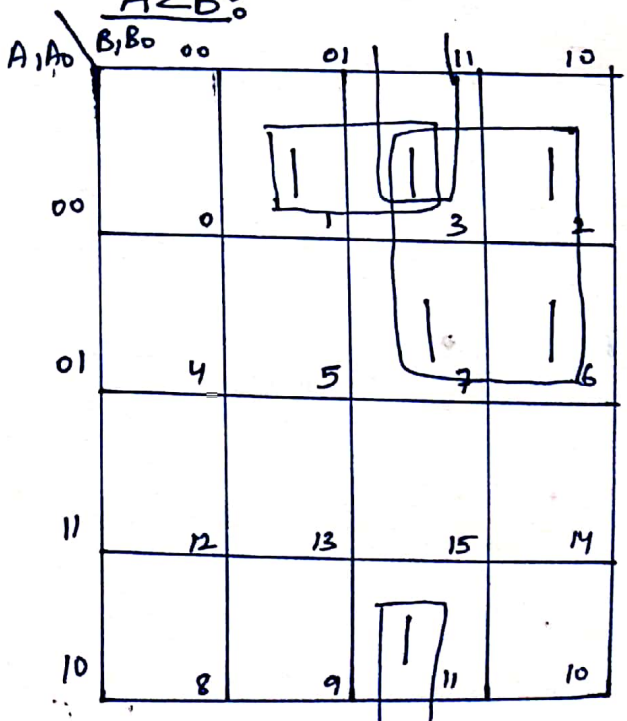
K-Map:

A>B:




$A_1\overline{B_1} + A_1A_0\overline{B_0} + A_0\overline{B_1}\,\overline{B_0}$

A<B:




$\overline{A_1}\,\overline{A_0}B_0 + \overline{A_1}B_1 + \overline{A_0}B_1B_0$

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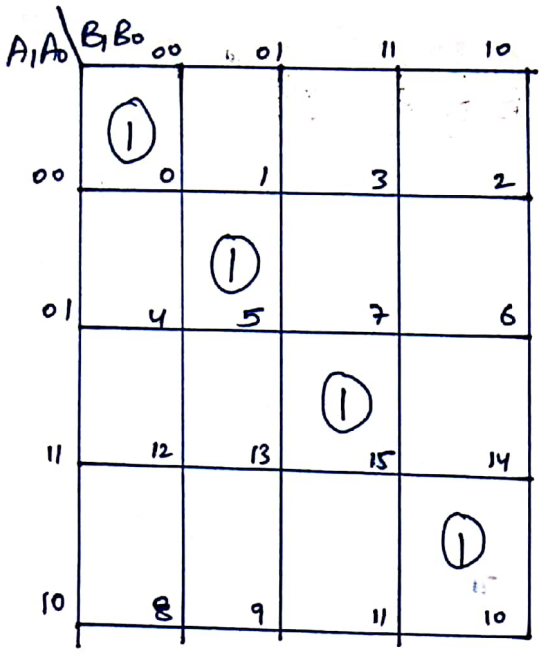
## A = B:



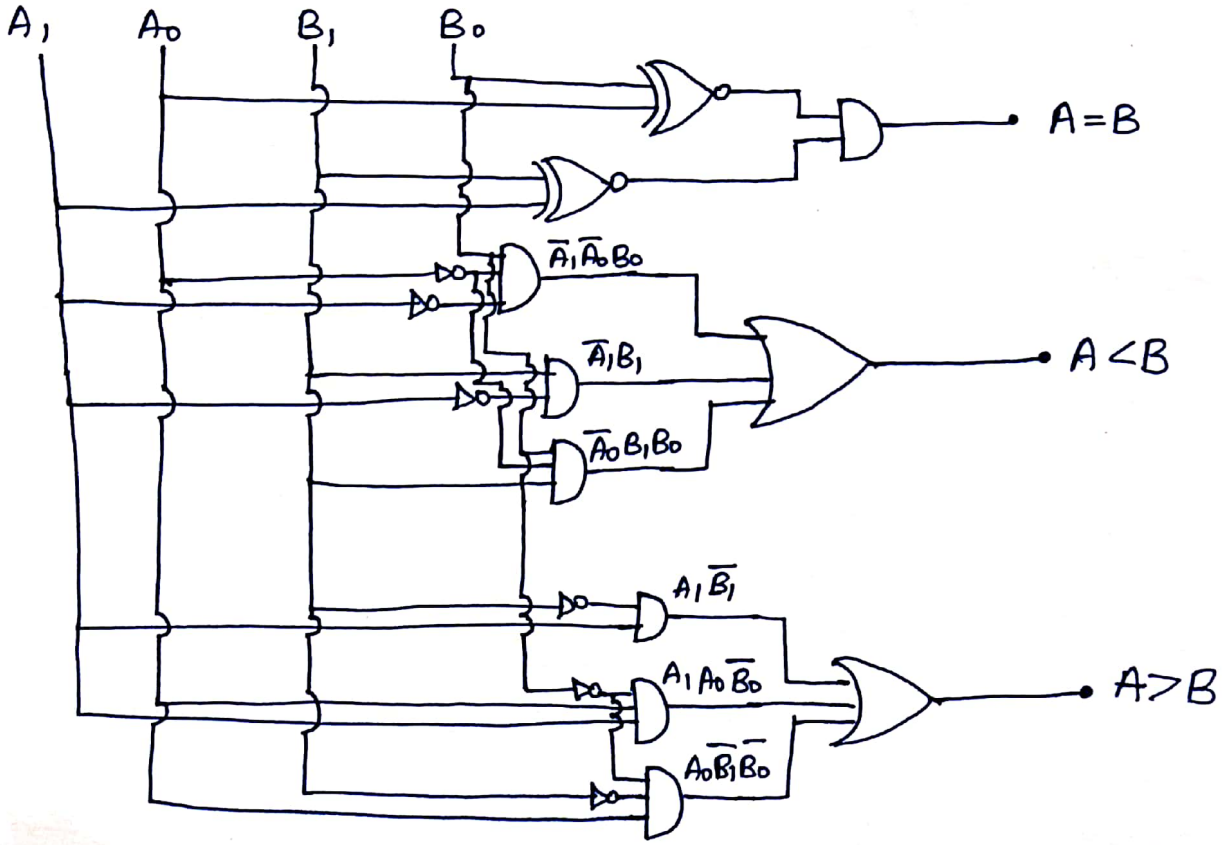

$\Rightarrow \overline{A_1}\,\overline{A_0}\,\overline{B_1}\,\overline{B_0} + \overline{A_1}A_0\overline{B_1}B_0 + A_1A_0B_1B_0 + A_1\overline{A_0}B_1\overline{B_0}$

$\Rightarrow \overline{A_1}\,\overline{B_1}\,(\overline{A_0}\,\overline{B_0} + A_0B_0) + A_1B_1\,(A_0B_0 + \overline{A_0}\,\overline{B_0})$

$\Rightarrow (\overline{A_0}\,\overline{B_0} + A_0B_0)\,(\overline{A_1}\,\overline{B_1} + A_1B_1)$

$\Rightarrow (A_0 \odot B_0)\,(A_1 \odot B_1)$

## Circuit diagram:



# Priority Encoder:

- It encodes the information from $2^n$ input lines into an n-bit code.
- It produces a binary code equivalent to the input which is high.

## 4:2 priority encoder:

Truth table:

| $I_3$ | $I_2$ | $I_1$ | $I_0$ | $Y_1$ | $Y_0$ | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | → invalid |
| 0 | 0 | 0 | 1 | 0 | 0 | |
| 0 | 0 | 1 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 1 | 0 | 1 | |
| 0 | 1 | 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 1 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | |
| 1 | 0 | 0 | 1 | 1 | 1 | |
| 1 | 0 | 1 | 0 | 1 | 1 | |
| 1 | 0 | 1 | 1 | 1 | 1 | |
| 1 | 1 | 0 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | 1 | 1 | |
| 1 | 1 | 1 | 0 | 1 | 1 | |
| 1 | 1 | 1 | 1 | 1 | 1 | |

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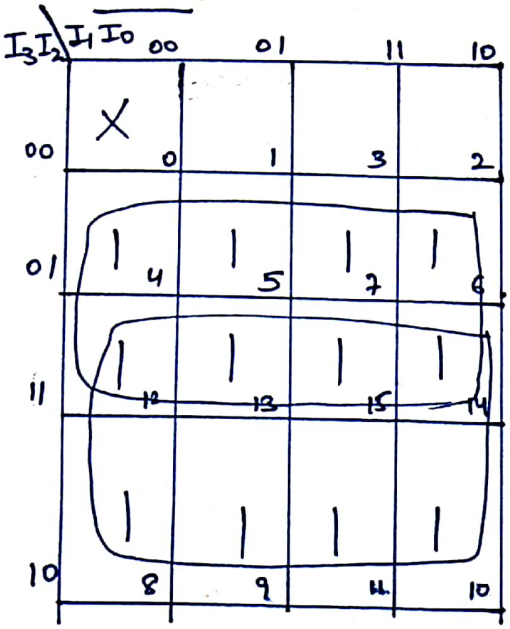
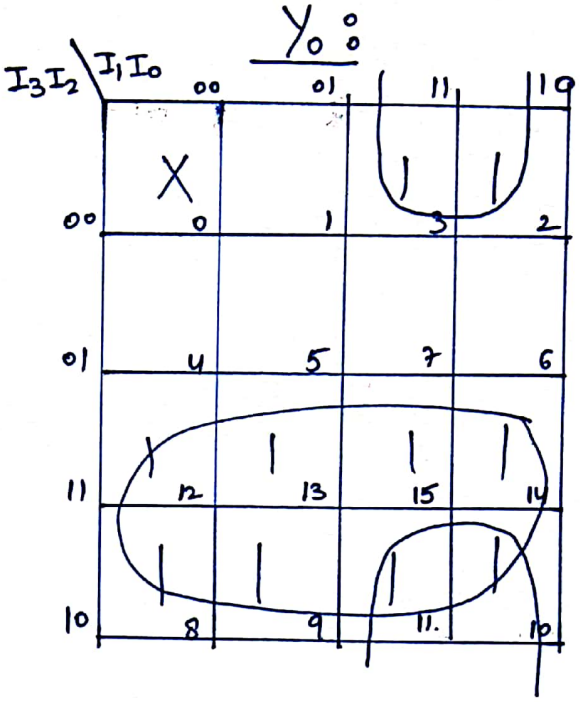
## K-map:

$Y_1$ :




$I_2 + I_3$

$Y_0$ :




$I_3 + \overline{I_2} \cdot I_1$

## Circuit Diagram: