

10°

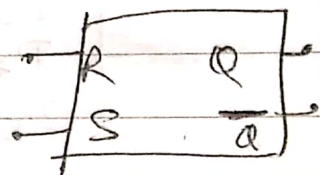
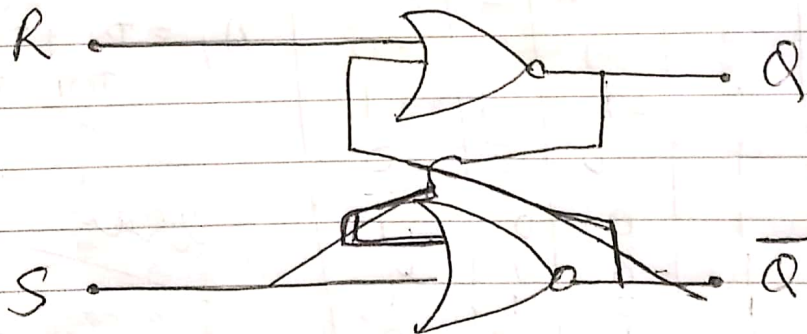
Sequential circuits

①

Latch :-

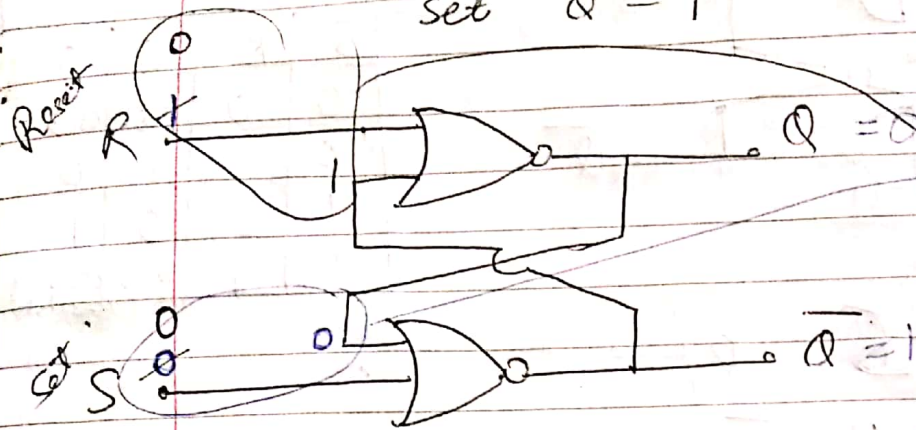
S-R Latch :-

Using NOR



Reset $Q = 0$
Set $Q = 1$

If $R = 1$ Output = 0
If $S = 1$ Output = 1



NOR		T
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If Input = 1 output is 0

Case I:-

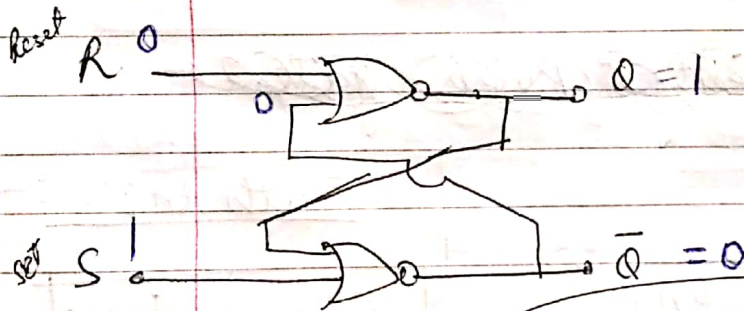
$S = 0, R = 1$
 $Q = 0, \bar{Q} = 1$

Memory as we have the previous output.

$S = 0, R = 0, Q = 0 \text{ \& } \bar{Q} = 1$

Case II:-

$S = 1, R = 0, Q = 1 \text{ \& } \bar{Q} = 0$



$S = 0, R = 0, Q = 1$
 $\bar{Q} = 0$

Memory

Case III:-

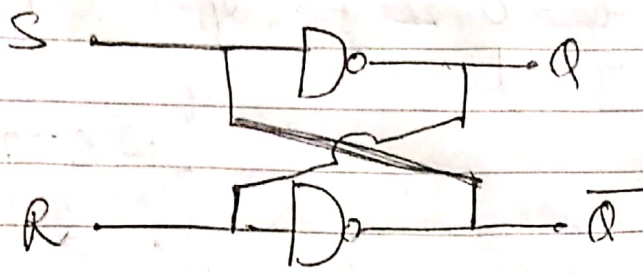
$S = 1, R = 1, Q = 0, \bar{Q} = 0$

Not used

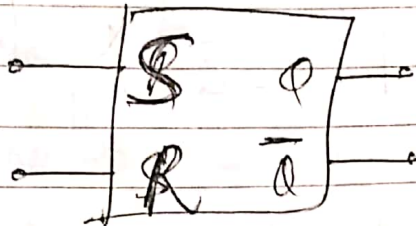
$S = 0, R = 0, Q = 0 \text{ \& } \bar{Q} = 1$
 $Q = 1 \text{ \& } \bar{Q} = 0$

S	R	Q	\bar{Q}
0	0	Memory as before / No change.	
0	1	0	1
1	0	1	0
1	1	Not used / Invalid cond ⁿ .	

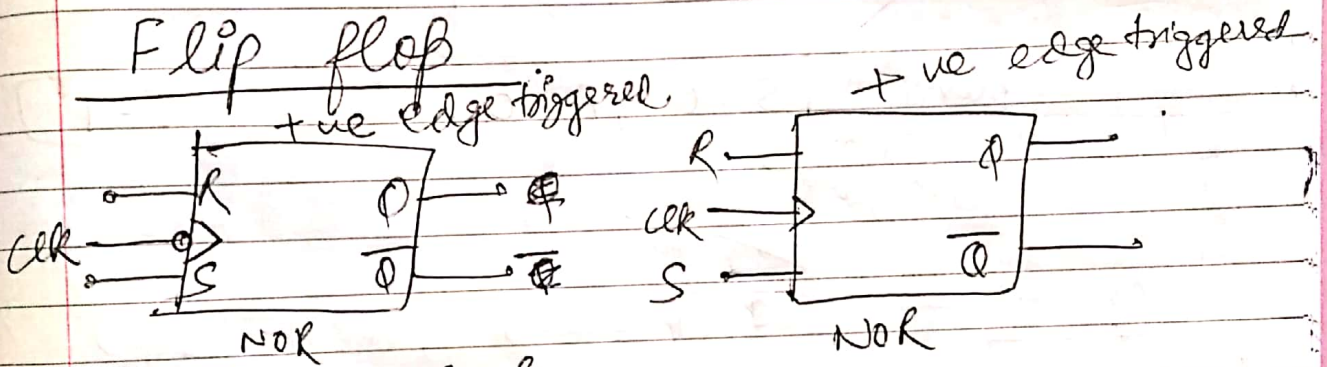
SR-latch - using NAND



S	R	Q	Q̄
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Memory state	



Flip flop



(i) S-R ~~flip flop~~ ~~using NOR gates~~

Characteristic table

clk	S	R	Q _n	Q _{n+1}	
↑	0	0	0	0	no change.
↑	0	0	1	1	
↑	0	1	0	0	Reset condition
↑	0	1	1	0	
↑	1	0	0	1	set condition
↑	1	0	1	1	
↑	1	1	0	X	invalid
↑	1	1	1	X	
↓	anything			No change.	

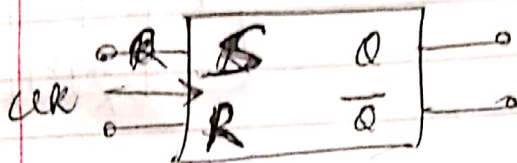
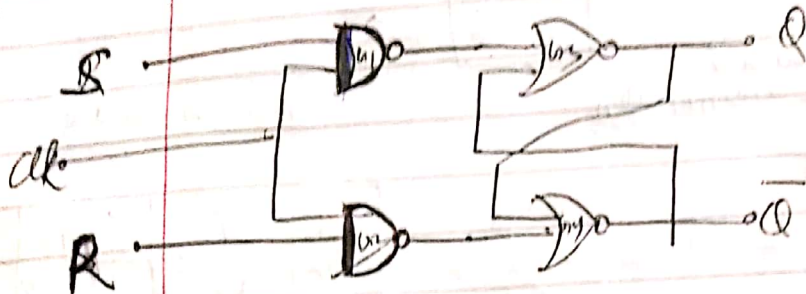
Truth table

S	R	Q _{n+1}
0	0	No change (Q _n)
0	1	0 (Reset)
1	0	1 (Set)
1	1	Invalid (Race condition)

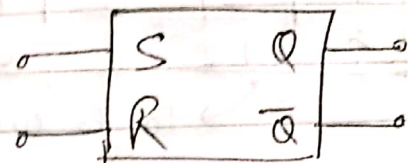
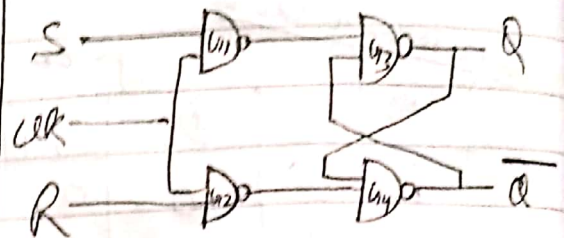
Excitation table

Q _n	Q _{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

circuit diag using NOR



circuit diag using NAND



characteristic table
20. D flip flop :-

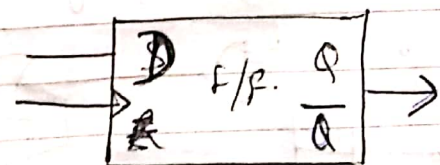
clk	D	Q _n	Q _{n+1}
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1
↓	anything		No change

excitation table

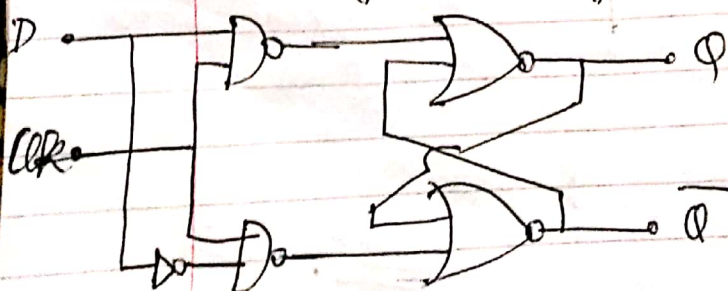
Q _n	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Truth table

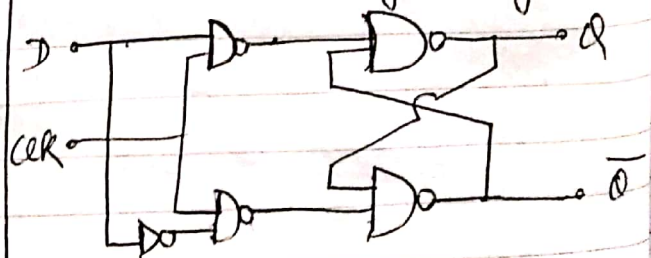
	D	Q _{n+1}
↑	0	0
↑	1	1
↓	anything	No change



circuit diagram using NOR

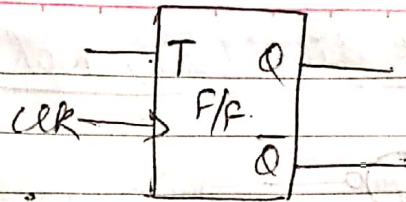


circuit diag using NAND



(3)

T flip flop :-



Characteristic table

Truth table

clk	T	Q_n	Q_{n+1}
↑	0	0	0
↑	0	1	1
↑	1	0	1
↑	1	1	0

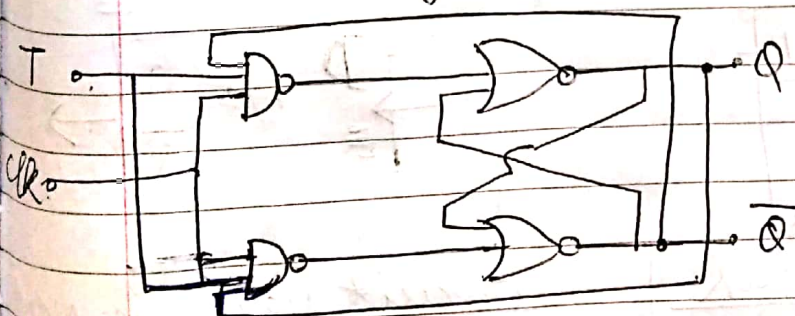
clk	T	Q_{n+1}
↑	0	Q_n no change
↑	1	Q_n Toggle
↓	anything	No change

Toggle on nahi hai so $Q_{n+1} = Q_n$
Toggle on hai so Q_{n+1} will be reverse of Q_n
↓ anything no change

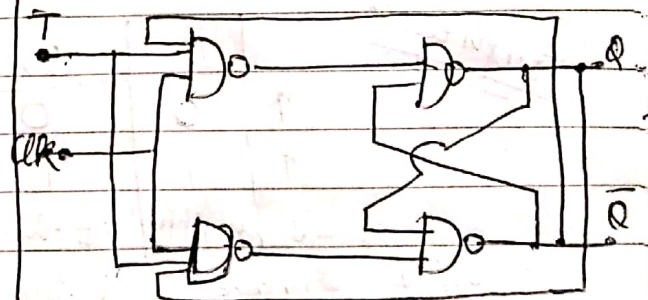
Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

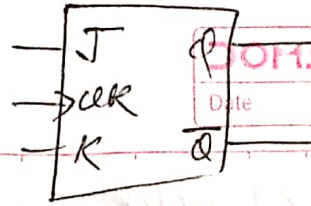
Circuit diag using ~~NAND~~ NOR



Circuit diag using NAND



④ JK flip flop :-
 → prefers over SR.



characteristic table
 → work as Reset

clk	J	K	Q_n	Q_{n+1}
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	0
↓		anything		no change

Annotations for characteristic table:
 - For (0,0): no change
 - For (0,1): Reset
 - For (1,0): Set
 - For (1,1): Toggle condition

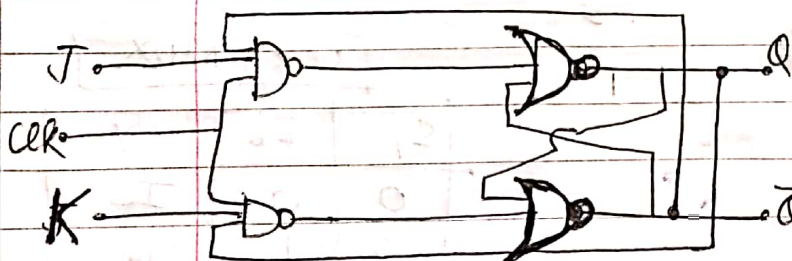
Truth table

clk	J	K	Q_{n+1}
↑	0	0	Q_n (no change)
↑	0	1	0 (Reset)
↑	1	0	1 (Set)
↑	1	1	\bar{Q}_n (toggle)
↓	anything		no change

excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

circuit diagram using NOR



circuit diagram using NAND

