

DECLARATION

I hereby declare that the Summer Training Report entitled(Implementation of Softcore RISC Processors in FPGA) is an authentic record of work completed as requirements of Summer Training () during the period from 21stJune'24 to 02ndAug'24 in Instruments Research & Development Establishment DRDO, under the supervision of **Mr. Vaibhav Saini (Scientist F, IRDE Dehradun)**.

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