Nirma University
Institute of Technology
B. Tech in Electronics and Communication Engineering
Semester – V
2EC501 – VLSI Design
Special Assignment (Marks 30)

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Submitted to: prof. Akash sir, Piyush sir and Usha mam

Problem Statement:

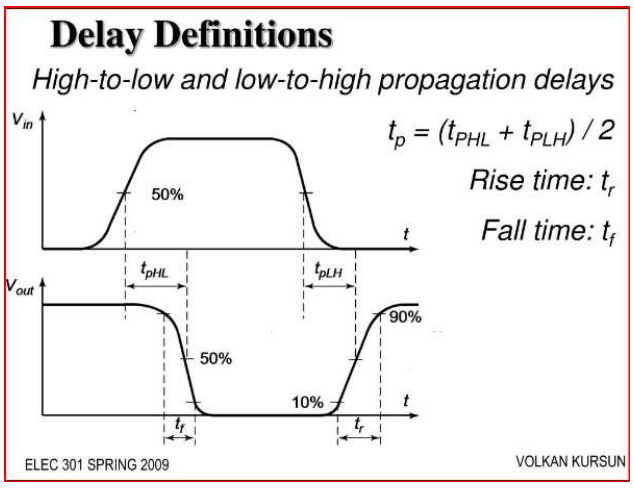
To design a two input AND gate with CMOS with propagation delay 2ns. Prepare the gate using 180nm technology. Assume that all the transistors have been sized to give a worst-case output resistance of 20 K for the worst-case input pattern.

Theory:

A CMOS gate consists of a PMOS (pull-up network) which is connected to VDD (input 1), and a NMOS (pull-down network) connected to GROUND (input 0). The two input AND gate can be realized from 2 input NAND gate and the output of NAND gate connected to the input of MOS inverter. In the two input NAND gate, the two PMOS are connected in parallel and two NMOS are connected in series.

Propagation delay:

Propagation delay (tp) is the time required for the gate to respond to change it's input. It is measured between the 50% transition points of the input and output waveforms.



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* PROPOGATION DELAY:

T_{PHL} → time delays as the output changes from high to low.

T_{PLH} → time delays as the output changes from low to high.

$$T_P = \frac{T_{PLH} + T_{PHL}}{2}$$

required T_P = 2ns

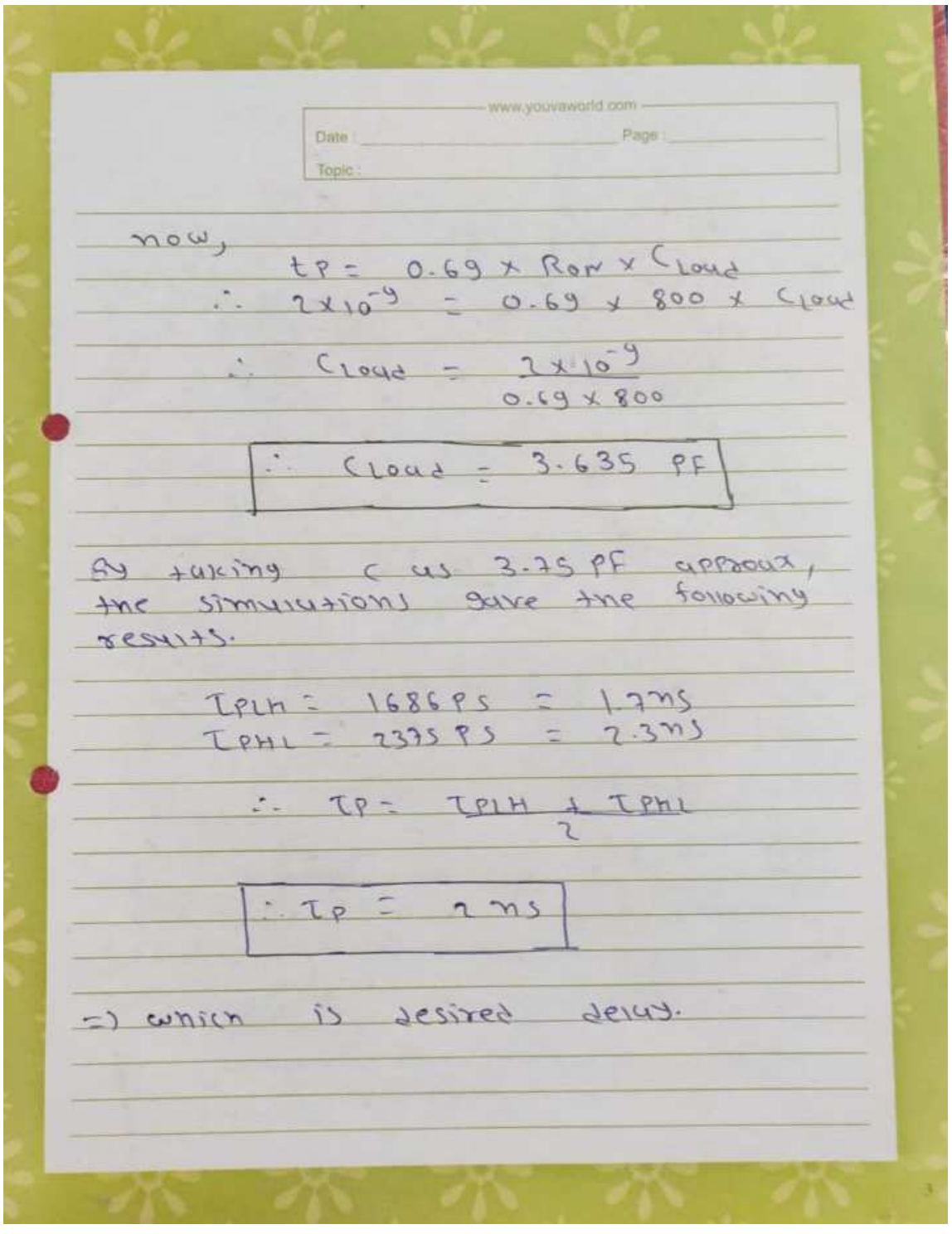
let, $T_{PHL} = T_{PLH}$

The current I_{DS} shows aster simulating 1.5 mA.

$\therefore V_{DS} = R_{ON} I_{DS}$

$\therefore \frac{1.2}{1.5 \times 10^{-3}} = R_{ON}$

$\therefore R_{ON} = 800\ \Omega$



now,

$$t_P = 0.69 \times R_{on} \times C_{load}$$

$$\therefore 2 \times 10^{-9} = 0.69 \times 800 \times C_{load}$$

$$\therefore C_{load} = \frac{2 \times 10^{-9}}{0.69 \times 800}$$

$$\therefore C_{load} = 3.635\ pF$$

By taking C as 3.75 pF approx, the simulations give the following results.

$T_{PLH} = 1686\ ps = 1.7\ ns$

$T_{PHL} = 2395\ ps = 2.3\ ns$

$$\therefore T_P = \frac{T_{PLH} + T_{PHL}}{2}$$

$$\therefore T_P = 2\ ns$$

=) which is desired delay.

Questions:

1. **Find out the optimized Boolean equation (If not given).**

TRUTH TABLE

A	B	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

F = A.B

2. Draw the optimized gate level circuit diagram.

F = A.B

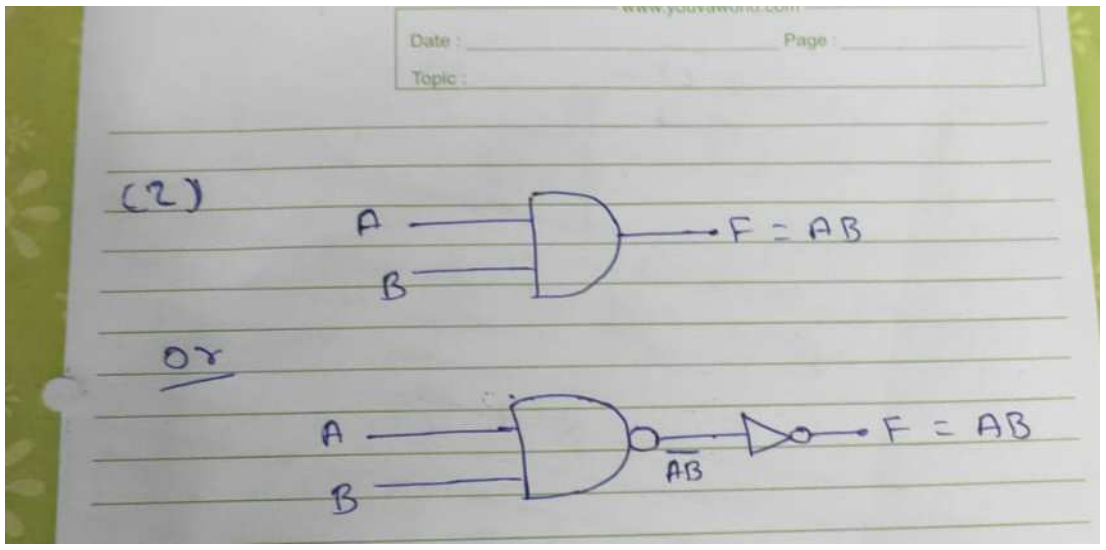


Figure 1

3. Draw the transistor level schematic for CMOS/MOS implementation.

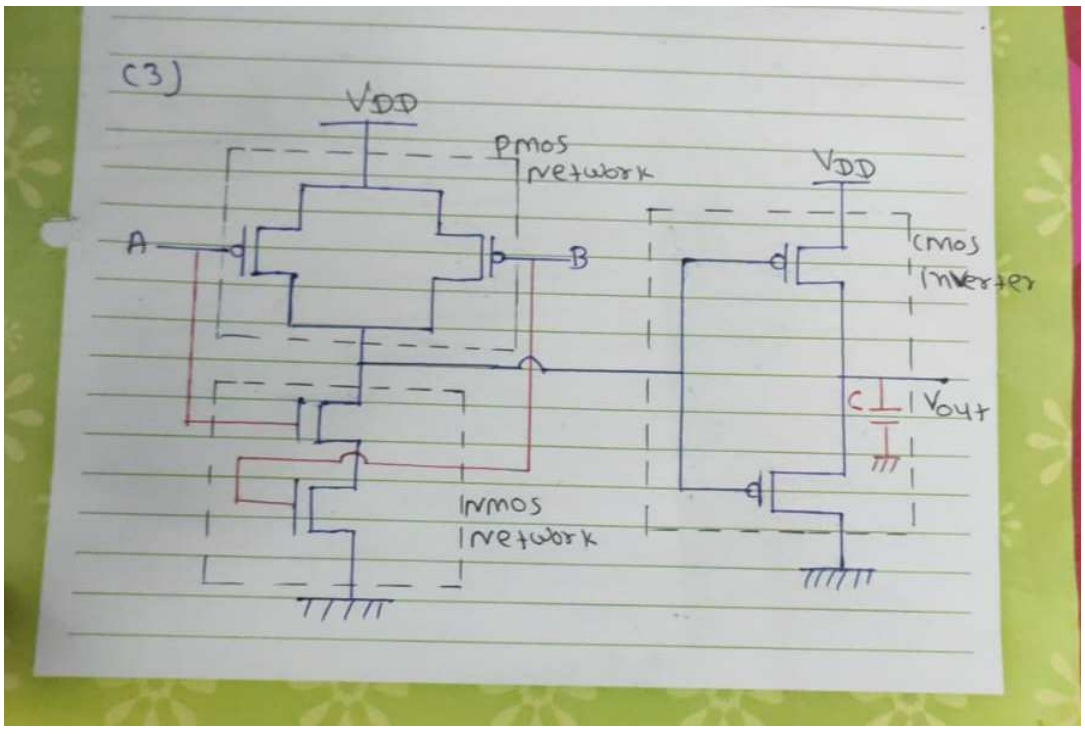


Figure 2

This figure 1 demonstrates the static two-input AND gate in CMOS technology. The two-input AND gate shown in the figure is built from six transistors. The parallel connection of the two p-channel transistors between VDD and the gate-output ensures that the gate-output is driven high (logical 1) when both gate input A and B is high (logical 1).

4. Draw stick diagram for above implementation level using proper color code

Colour Code:
P diffusion: **Yellow**
Metal 1: **Blue**
N diffusion: **Green**
Poly-silicon: **Red**
Contacts & Taps: **Black**

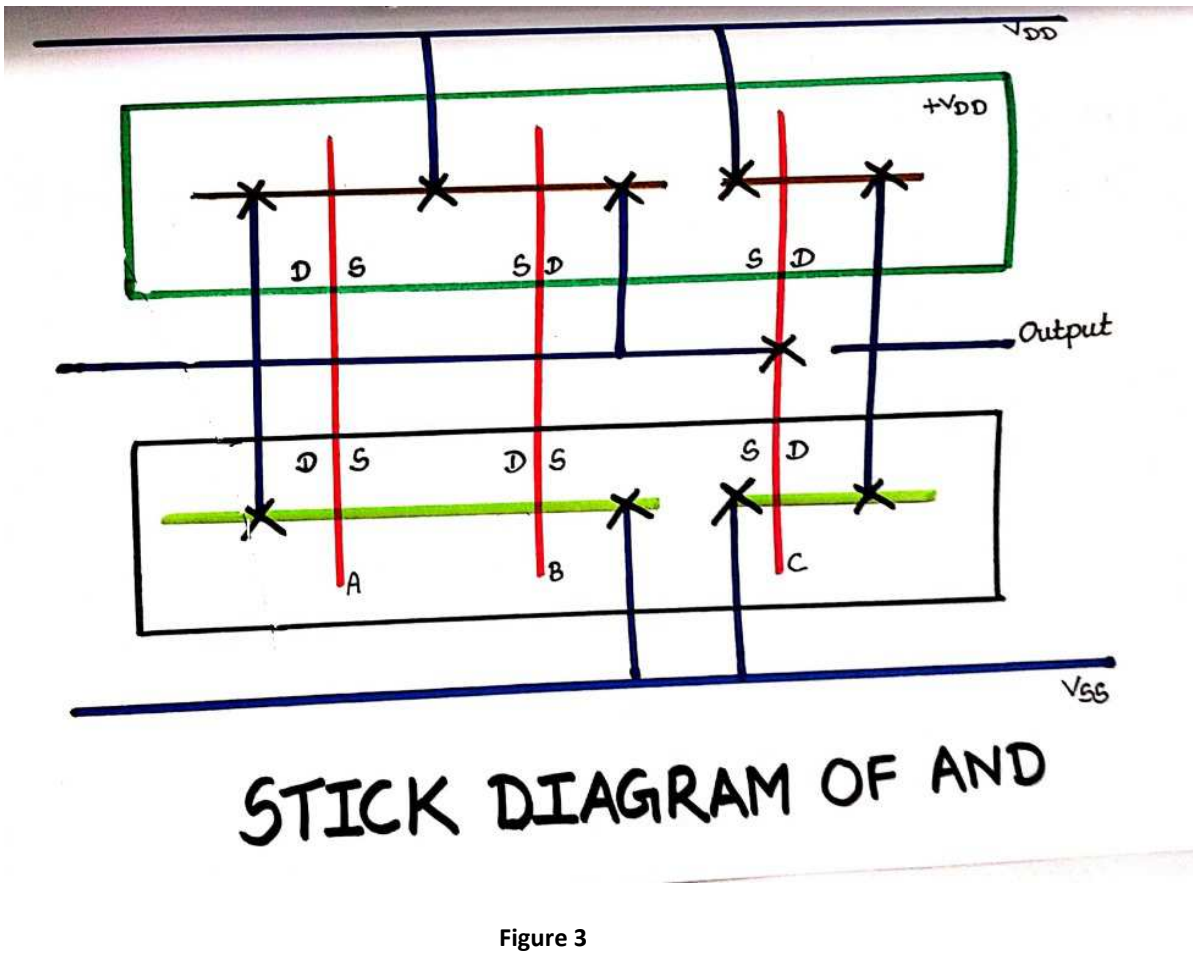


Figure 3

5. State the various level of V_{OL} corresponding to various transistor statuses

Since, the given circuit is CMOS based. As it is known that, in CMOS, minimum output voltage occurs when input is high (Vin = VDD), also pMOS is OFF, nMOS is ON, hence nMOS pulls V_{out} to Ground. Therefore, V_{OL} = 0 V Hence for various level of status, V_{ol} can't be computed.

6. Find an equivalent CMOS inverter circuit.

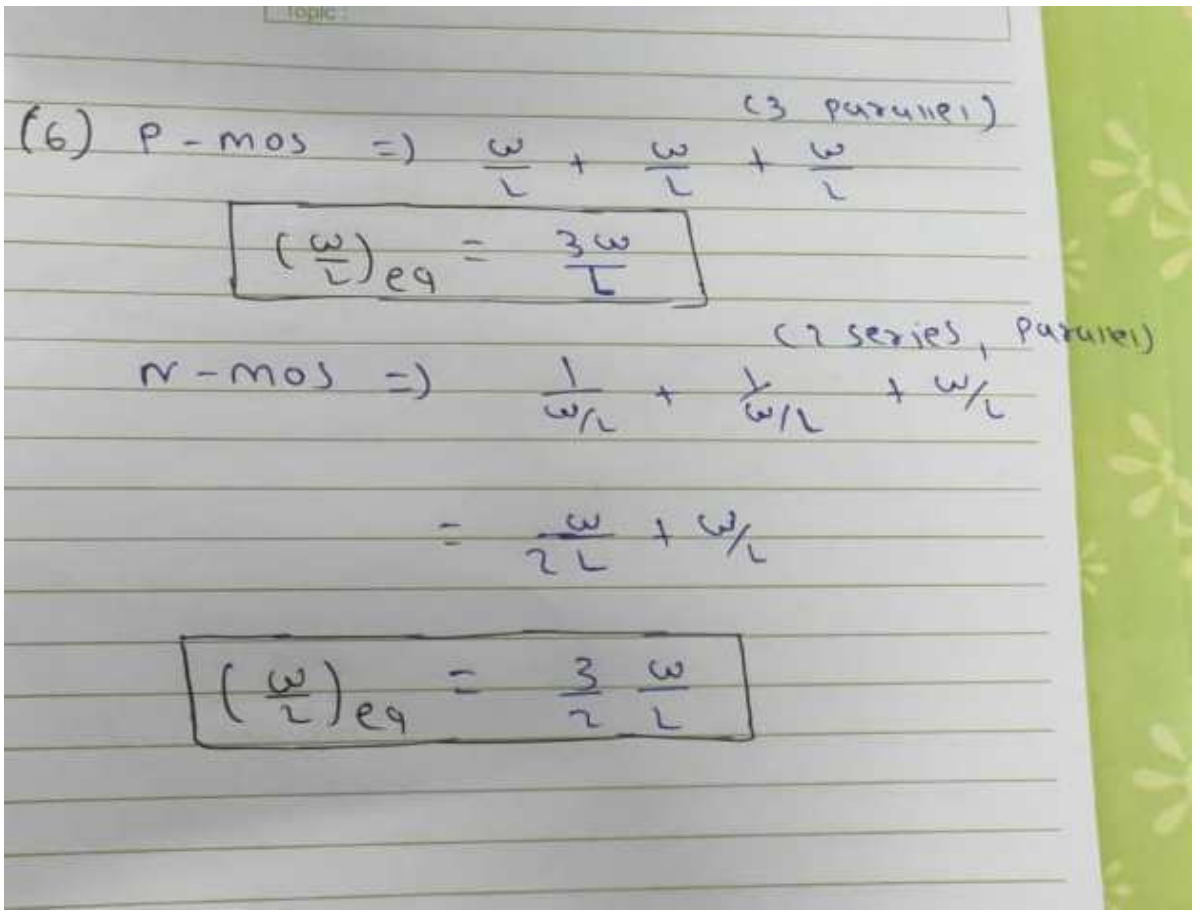


Figure 4

$(W/L)_{p\ channel} = (W/L) + (W/L) + (W/L) = 3(W/L)$ (all 3 in parallel)

$(W/L)_{n\ channel} = ½(W/L) + (W/L) = 3/2\ (W/L)$ (2 series, 1 parallel)

7. For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

Vol will be lowest when the W/L equivalent of driver is highest.
For lowest Vol, all 3 nMOS should be in ON state, hence A=1, B = 1. On replacing these nMOS by resistors.
Value of resistance corresponding to this input pattern:
R = (20 + 20) || 20
R = 40 || 20
R = 13.33 Kilo ohm
Hence, for 13.33 Kilo ohm, the output is low.

8. For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

For, output to be high, all the pMOS should be in ON state.
Hence the input A and B will be 0. On replacing these pMOS with resistors, Value of resistance corresponding to this input pattern:

1/R = 1/20k + 1/20k +1/20k
R = 6.67 Kilo ohm
Hence, for R = 6.67 Kilo ohm, the output is high.

9. Prepare the layout using Microwind tool.

Design is made using 0.12 µm foundry.

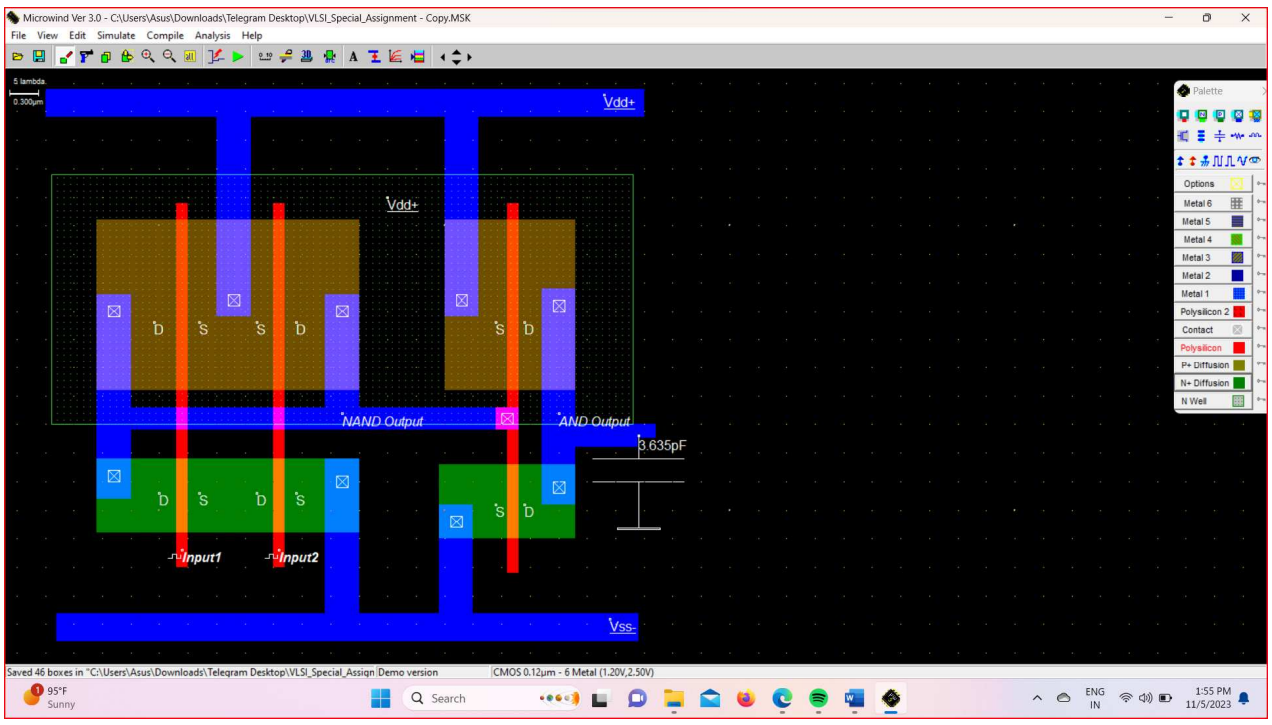
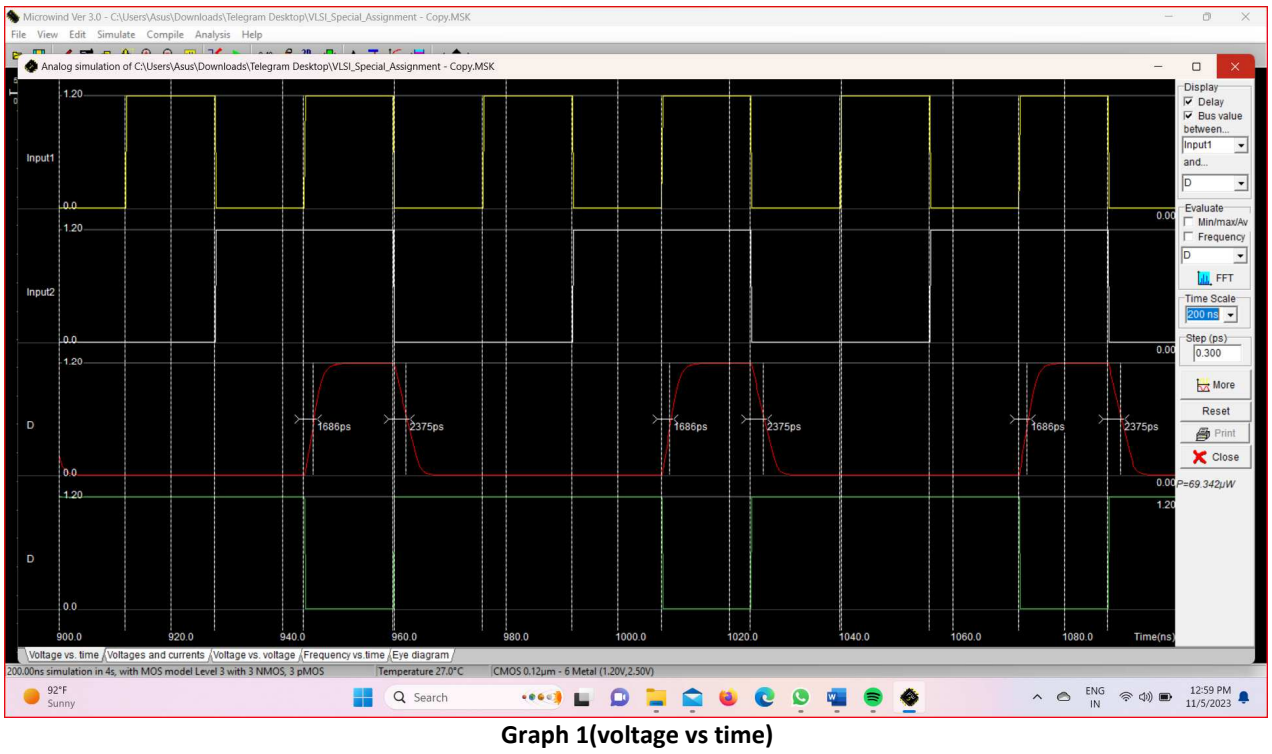


Figure 5

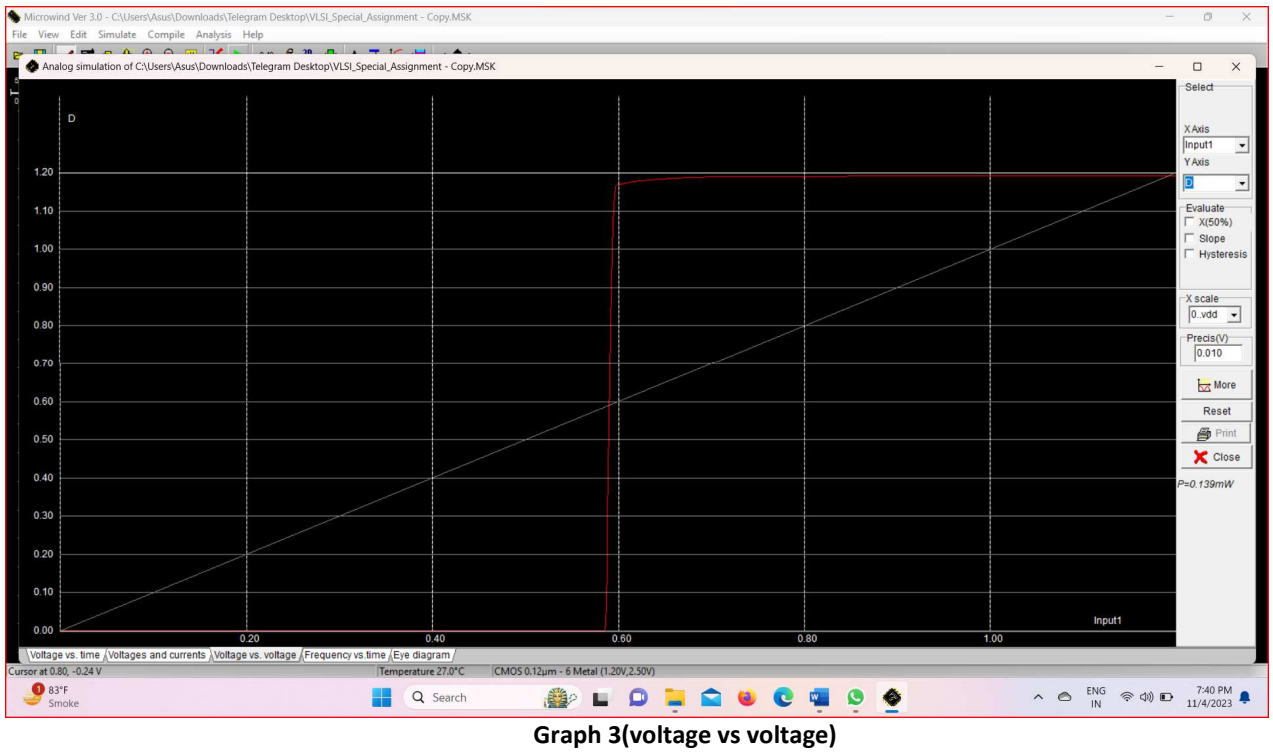
Here, AND gate is made using CMOS. Here, two inputs A and B are taken as clock and Vout is obtained as output. Here, the rise time and fall time of input clock is increased to achieve the propagation delay of 2ns.

10. Simulate it for various combinations of inputs.



Graph 1(voltage vs time)

Graph 2(voltages and currents)



Graph 3(voltage vs voltage)

TRUTH TABLE

A	**B**	**V_{out}**
0	0	0
0	1	0
1	0	0
1	1	1

It can be observed that from the figure,
For input A= 0, B=0 output from the simulation and Boolean equation is 0.
For input A=0, B=1output from the simulation and Boolean equation is 0.
For input A=1, B=0output from the simulation and Boolean equation is 0.
For input A=1, B=1output from the simulation and Boolean equation is 1.
From the graph 2, it can be observed that Vol is 0 and Voh is equal to vdd that is 1.2V. Hence, the ideal output for CMOS AND gate is obtained. Here, 2ns propagation delay is also achieved by adjusting the values of rise time and fall time of input clock.

11. Measure the rise time, fall time, propagation delay and other parameters.

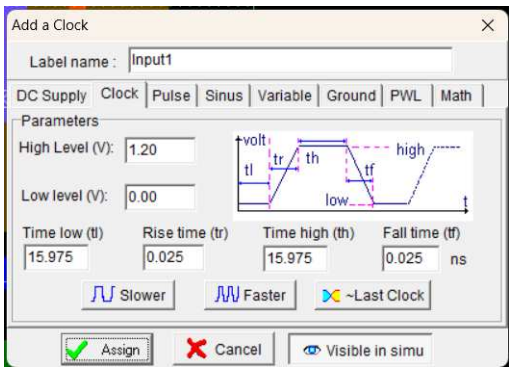
The propagation delay times τ_{PHL} and τ_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. By definition, τ_{PHL} is the time delay between the $V_{50\%}$-transition of the rising input voltage and the $V_{50\%}$ -transition of the falling

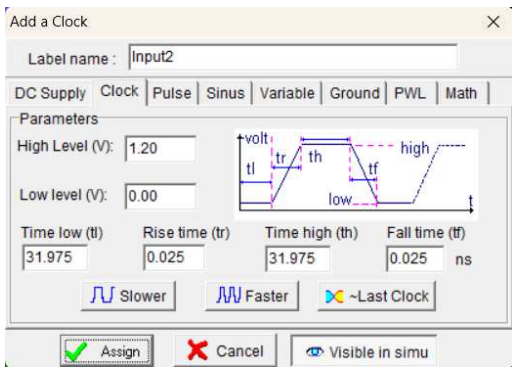
output voltage. Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ -transition of the falling input voltage and the $V_{50\%}$-transition of the rising output voltage.
τ_{PHL} - the time required for the output voltage to fall from V_{OH} to the $V_{50\%}$ level.
τ_{PLH} - the time required for the output voltage to rise from V_{OL} to the $V_{50\%}$ level.

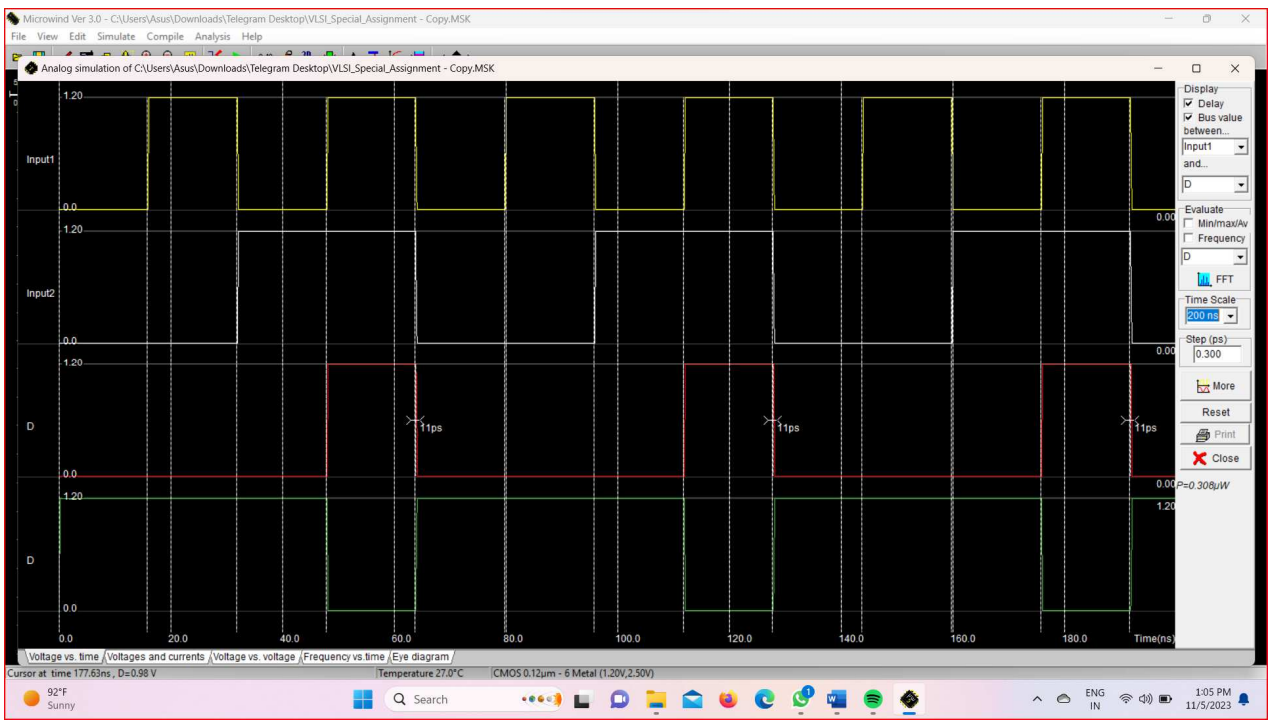
The average propagation delay τ_P of the inverter characterizes the average time required for the input signal to propagate through the inverter.

The rise time **τ_{rise}** is defined here as the time required for the output voltage to rise from the $V_{0\%}$ level to $V_{90\%}$ level. Similarly, the fall time **τ_{fall}** is defined here as the time required for the output voltage to drop from the $V_{90\%}$ level to $V_{10\%}$ level.

- Without external capacitor(3.635pF):

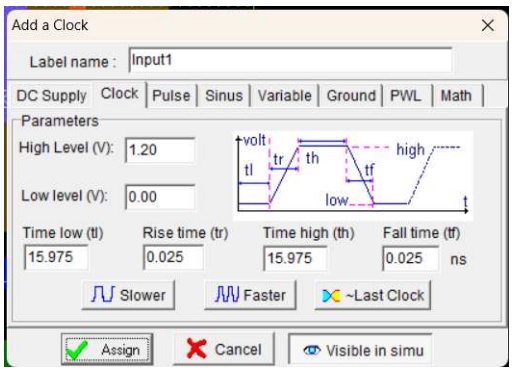


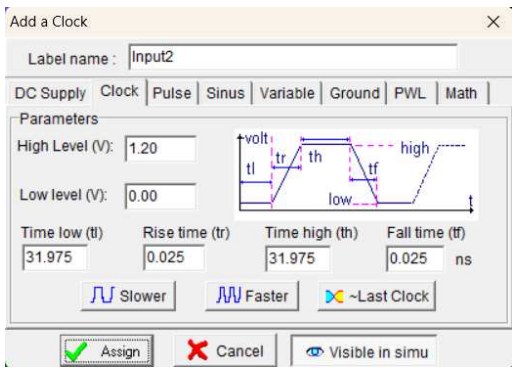


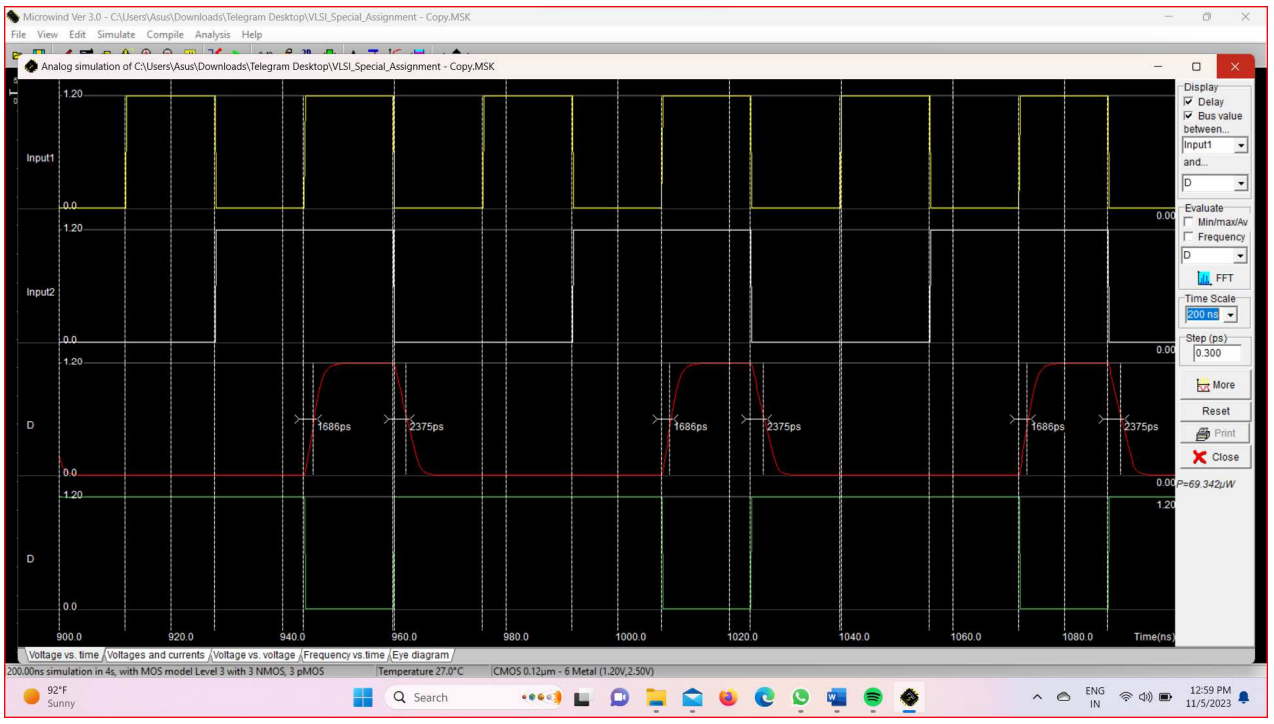


Rise time τ_{rise} = 0.025 ns
Fall time τ_{fall} = 0.025ns

- With external capacitor(3.635pF):







Propagational delay high-low, τ_{PLH} = 1.7ns
Propagational delay low-high, τ_{PHL} = 2.3ns
Total Propagational delay = $(\tau_{PLH} + \tau_{PLH})/2$ = 2ns
Rise time τ_{rise} = 0.025 ns
Fall time τ_{fall} = 0.025ns

Observation:

The propagation delay in the case without virtual external capacitance was much less than the propagation delay in the case with virtual external capacitance, which is because the circuit takes too long to discharge due to high value of external capacitor, and also because the output in this case is a little distorted and not as precise as it was in the previous case, which is due to the fact that the input changes more quickly than the time it takes the circuit to discharge due to the external capacitance, leading to a longer propagation delay and a distorted output.

Conclusion:

In this assignment, AND gate using CMOS having propagation delay of 2ns was implemented on microwind. On implementing AND gate using CMOS, it gives low static power utilization and huge noise immunity due to which these devices do not generate waste heat as compared with other types of logic circuits. Also, the propagation delay of 2ns was acquired adjusting values of rise time and fall time of input clock. The stick diagram of CMOS AND gate was also made using the paper colour code. Also, the values of resistance of CMOS was also found when input was high and low. Also, the ideal values of VOH and VOL was obtained as CMOS is used. Hence, it can be said that the CMOS provide much better output performance than any other circuits.