Objective :

The objective of this experiment is to encode a pseudorandom binary sequence (PRBS) signal using another PRBS as a spreading code to generate a Direct Sequence Spread Spectrum (DSSS) signal.

1. Accept a **message signal** from an **Arbitrary Function Generator (AFG)**.
2. Generate a **frequency-modulated (FM)** signal with a variable carrier frequency and adjustable modulation index.
3. Demodulate the FM signal using a **Phase-Locked Loop (PLL)** to retrieve the original message signal.
4. Provide user-adjustable settings for the modulation index and the PLL's free-running frequency.

Purpose of the Circuit for PRBS Encoding and DSSS Generation Experiment

1. **Demonstrate Principles:**
    - Illustrate the principles of encoding a PRBS signal with another PRBS signal to generate a DSSS signal, including the modulation and demodulation processes.
2. **Test Platform:**
    - Serve as a platform to evaluate the performance of communication systems using DSSS signal processing, providing insights into system behavior under various conditions.
3. **Parameter Exploration**:
    - Enable users to explore the effects of parameters such as modulation index and PLL settings on the behavior of the DSSS system, enhancing understanding of signal processing dynamics.

Working Conditions of the PCB for PRBS Encoding and DSSS Generation Experiment

1. **Frequency Ranges:**
    - Carrier Frequency: Adjustable from 100 kHz to 1 MHz, suitable for the DSSS signal generation.
    - Message Signal Frequency: Up to 20 kHz, accommodating audio signals or other low-frequency data.
2. **Supply Noise Management:**
    - Decoupling Capacitors and PCB Layout: Essential for mitigating power supply noise and crosstalk, ensuring clean signal transmission and accurate PRBS

encoding/decoding.

3. **PCB Dimensions:**
    - Compact Design: Ensures sufficient spacing for cooling and signal isolation, crucial for maintaining signal integrity and preventing interference in the DSSS system.

Constraints on Input and Output Signals

1. Input Signal Features:

- Message Signal: The PRBS signal, represented as an analog waveform, with a peak-to-peak amplitude constrained to ±5V for proper signal conditioning.
- Modulation Control: The modulation index is adjusted via an analog control, such as a potentiometer, influencing the frequency shift in the signal encoding process.
- PLL Adjustment: The Phase-Locked Loop (PLL) is tuned to ensure precise synchronization with the frequency of the PRBS signal, allowing for accurate signal spreading.

2. Output Signal Features:

- FM Signal: The encoded signal is output as a frequency-modulated waveform, with its amplitude governed by the carrier's oscillator power, ensuring a robust transmission of the PRBS.
- Demodulated Signal: The received signal is demodulated to retrieve the original PRBS message, with minimal distortion, ensuring faithful reproduction of the input data.

Load Impedance Requirements for PRBS Encoding and DSSS Generation

1. Modulated Signal Output:
    - 50 Ω impedance for compatibility with oscilloscopes.
2. Demodulated Signal Output:
    - > 1 kΩ impedance for interfacing with audio amplifiers or data acquisition systems.

Inputs and Outputs

Inputs:

1. Message signal (PRBS data):
    - Digital PRBS signal as the input data to be encoded.
    - Type: Digital, ±5 V peak-to-peak.
2. Modulation control (Spreading factor):
    - Adjusts the chip rate or spreading factor for DSSS.
    - Type: Analog, 0–5 V control.
3. PLL adjustment (Clock synchronization):
    - Tunes synchronization between PRBS generators.
    - Type: Analog, 0–10 V control.

Outputs:

1. DSSS Output (Spread signal):
    - Spread-spectrum signal for transmission or further use.
    - Type: Modulated DSSS signal.
2. Demodulated Output (Recovered data):
    - Original PRBS data signal after de-spreading.
    - Type: Digital PRBS signal.

This setup parallels FM modulation, where the PRBS signals are equivalent to the message and carrier signals.

Voltage Requirements for PRBS Encoding and DSSS Generation Experiment

1. **Power Supply Requirements**:
   - **±12 V DC**: Needed for analog components such as operational amplifiers, Voltage-Controlled Oscillator (VCO), and Phase-Locked Loop (PLL) used in the modulation and demodulation processes.
   - **5 V DC**: Required for digital control interfaces or auxiliary circuits that manage the PRBS encoding and decoding.
2. **Onboard Regulation**:
   - A **12 V DC input** can be regulated to provide both **±12 V** and **5 V** using linear regulators, ensuring stable power supply for all components involved in generating and processing the DSSS signal.

Power Consumption for PRBS Encoding and DSSS Generation Experiment

1. Carrier Oscillator Stage:

- Approximately 200 mW: Required for the VCO that generates the carrier signal for the DSSS system.

2. Modulator and Demodulator Stages:

- Around 300–400 mW combined: Consumed by the circuits responsible for modulating the PRBS signal to create the DSSS signal and demodulating it back.

3. Control Circuitry:

- About 50–100 mW: Needed for the control and auxiliary circuits that handle PRBS encoding and decoding adjustments.

4. Estimated Total Power:

- Roughly 1–2 W: Total power usage under typical operating conditions, ensuring all components function properly for the DSSS signal generation and processing.

Stages of the Circuit and Tapping Points for PRBS Encoding and DSSS Generation Experiment

1. **Modulation Stage:**
    - Combining Signals: Encodes one PRBS signal with another to generate the DSSS signal.
    - Adjustable Controls: Includes settings for modulation parameters.
    - Tapping Point: Output of the modulated DSSS signal for verification and analysis.
2. **Carrier Signal Generation:**
    - **Voltage-Controlled Oscillator (VCO): Generates the carrier signal for the DSSS system.**
    - **Tapping Point: Output of the VCO for frequency calibration and monitoring.**

3. Demodulation Stage:
    - **Phase-Locked Loop (PLL)**: Demodulates the DSSS signal to recover the original PRBS signal.
    - **Low-Pass Filter**: Recovers the original message signal from the demodulated output.
    - **Tapping Points**:
        1. **PLL Input**: For observing the incoming DSSS signal.
        2. **Loop Filter Output**: For monitoring PLL dynamics and performance.
        3. **Final Demodulated Signal Output**: For verifying the recovered PRBS signals.

Components Used in PRBS Encoding and DSSS Generation Experiment

1. **Modulator:**
   - Voltage-Controlled Oscillator (VCO): Provides the carrier signal for the DSSS system.
   - Summing Amplifier (LM741): Combines the two PRBS signals to produce the DSSS signal.
2. **Demodulator:**
   - PLL IC (LM565): Utilized for phase locking and demodulating the DSSS signal to retrieve the original PRBS signal.
   - RC Low-Pass Filter: Filters the demodulated output to recover the original message signal.

Simulations and Testing for PRBS Encoding and DSSS Generation Experiment

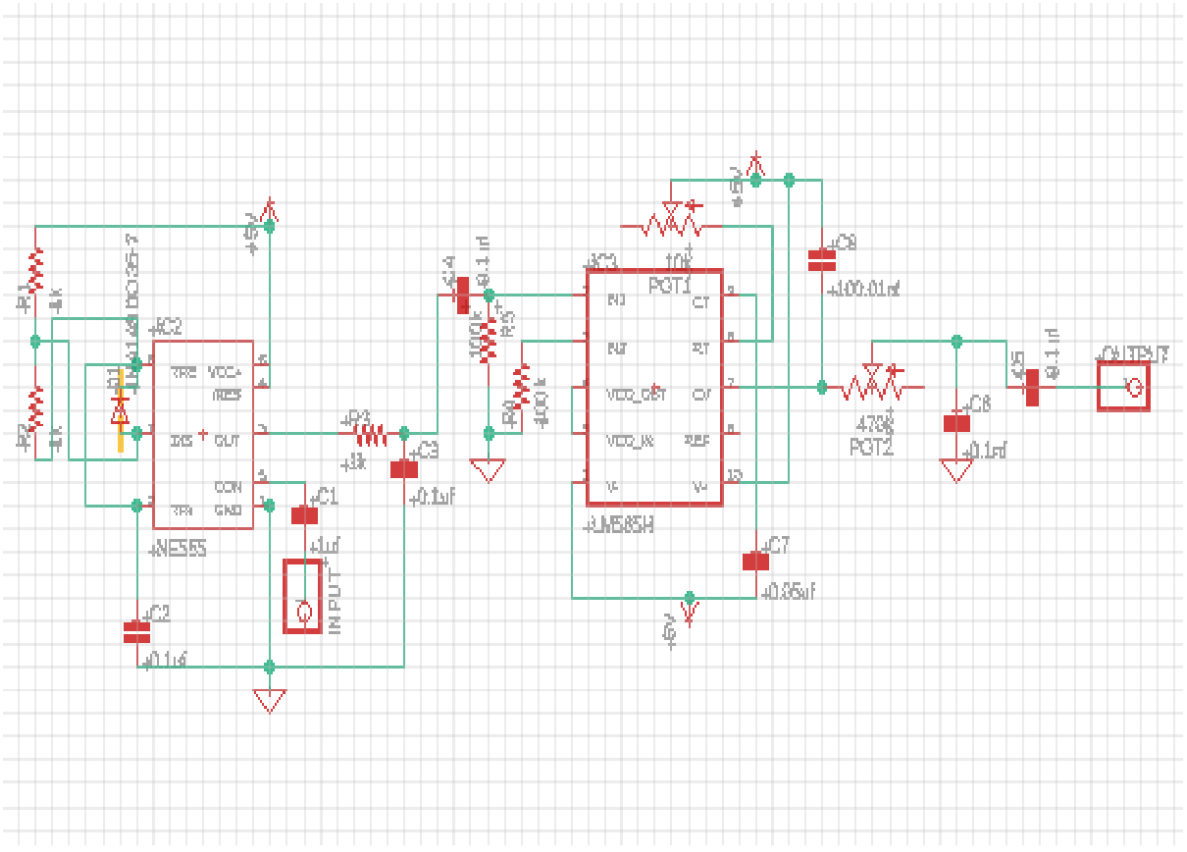
1. **Simulations:**
   - MATLAB: Use MATLAB to verify the functionality of the modulator and demodulator circuits for the DSSS signal.
   - Parameter Analysis: Analyze key parameters such as frequency deviation, demodulated signal fidelity, and PLL locking range to ensure accurate signal processing.

2. **Testing Procedure:**
   - **Message Signal Connection**: Connect the PRBS message signal from an Arbitrary Function Generator (AFG) to the modulator input.
   - **Observation**: Use an oscilloscope to observe the modulated DSSS signal output.
   - **Demodulation Verification**: Input the DSSS signal to the demodulator and verify the recovered PRBS signal against the original message signal to ensure fidelity.

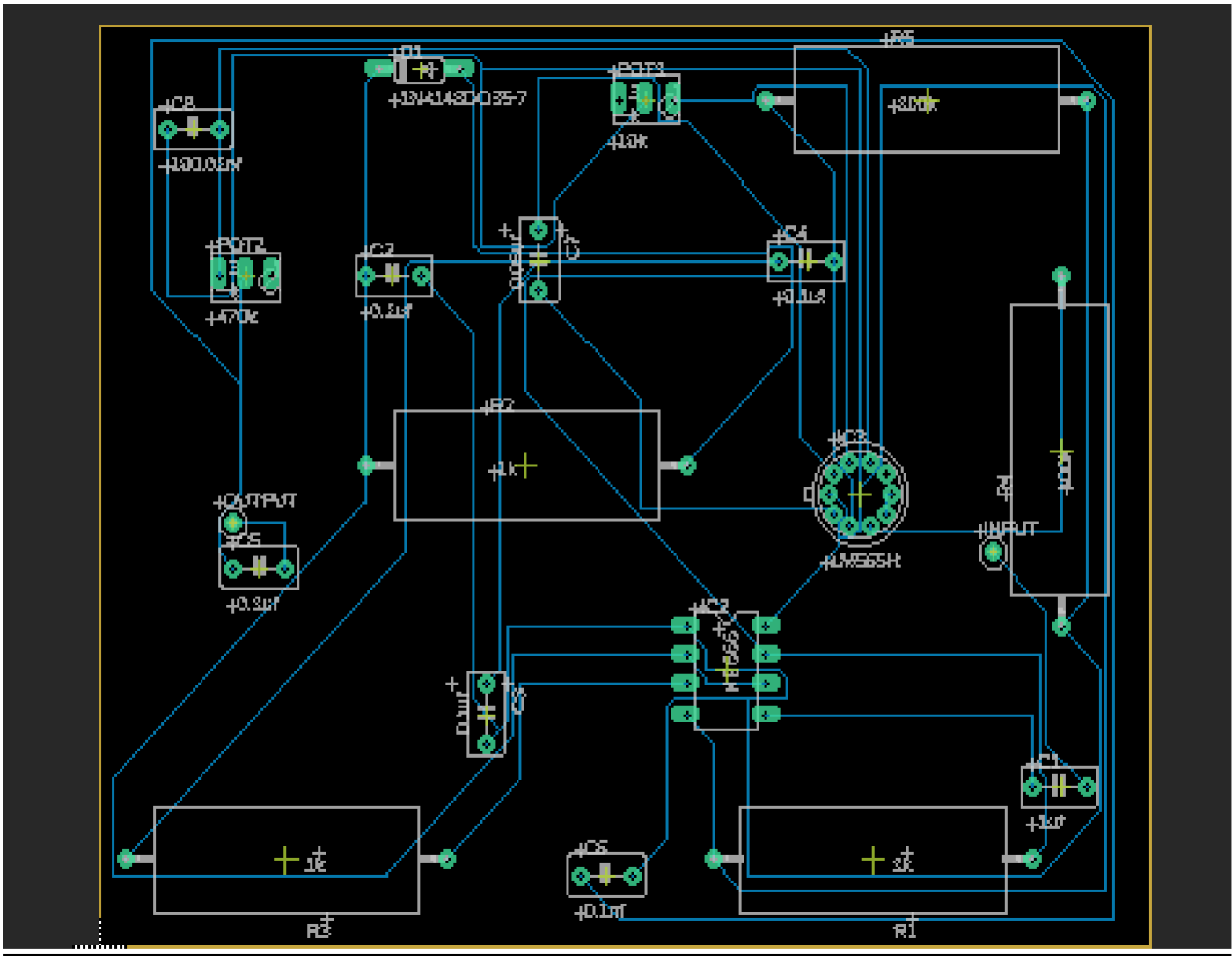
Schematic diagram

This schematic diagram is generated through eagle software.

FM modulation and demodulation

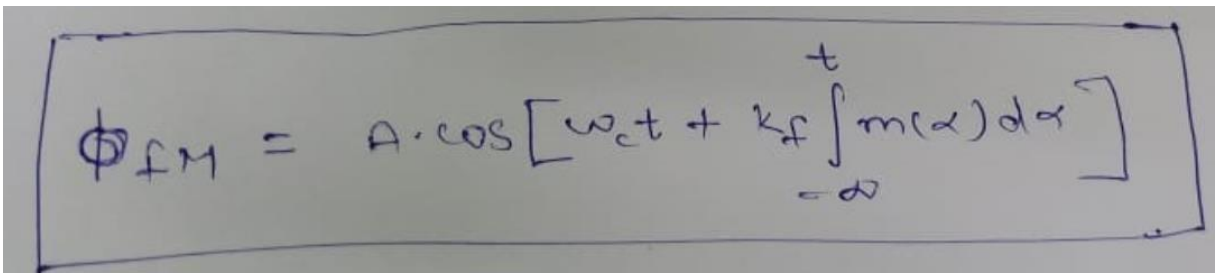


Schematic diagram after routing

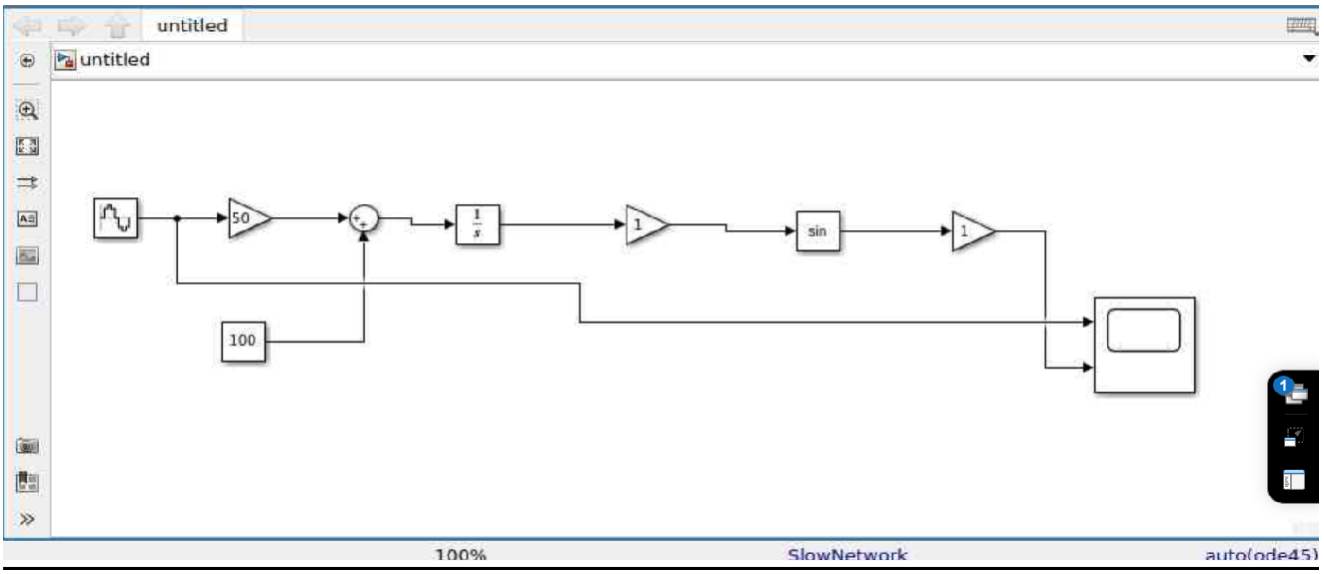


Output simulation by MATLAB

By applying this Equation

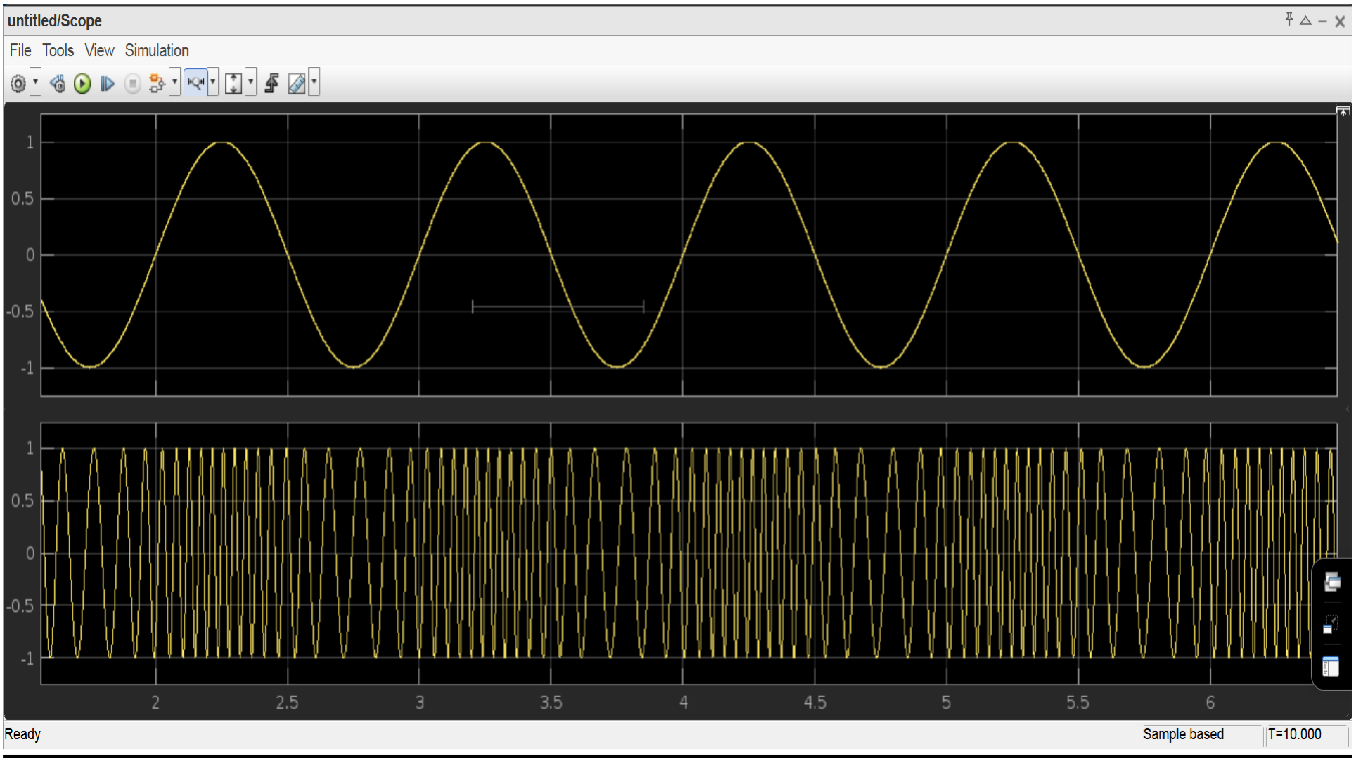


MATLAB simulation



Output wave form after Modulation and Demodulation

Generated through MATLAB



Conclusion

This circuit demonstrates the working of frequency modulation (FM) and demodulation. The modulator generates an FM signal by varying the carrier frequency based on the input message signal, while the demodulator uses a Phase-Locked Loop (PLL) to recover the original message signal. The design includes adjustable features, such as changing the modulation index and the PLL settings, to understand and experiment with the principles of FM communication effectively.