

Leakage Controlled Transistor (in 45nm technology)

Previous Works:

- Lowering the supply voltage (VDD) is the most effective way to reduce the power dissipation as it depends quadratically on VDD. But as VDD reduces, it approaches the threshold voltage of the devices due to which circuit delay will increase and thus degrades its performance. At the same time it is possible to maintain the performance by decreasing the threshold voltage (VTH) but then subthreshold leakage current and power increases exponentially. Therefore, VDD and VTH have to be optimized to achieve the required performance and low power.
- As the feature size reduces, shorter channel length results in sub threshold leakage current through a transistor when it is off. Thinner gate oxides have led to an increase in gate leakage current. Therefore, static power consumption i.e. leakage power dissipation becomes an important portion of total power consumption. In 180 nm and below technologies, leakage accounts for 30-40% of total power.
- There are various techniques to reduce power dissipation in a circuit. Some of them are: Body Biasing, Source Biasing, Voltage Scaling, Sleep Transistor and Transistor Stacking Technique. In this section we will discuss transistor stacking technique in detail.
- Input vector control puts the circuit into low-leakage standby state when idle and restores to correct state when active with the help of additional logic circuitry. This requires special latches to remember the correct state of the circuit, thereby, increasing the area overhead by five times in the worst-case. Also, the amount of time for which the unit remains in idle state should be long enough so that the dynamic power consumed in forcing the circuit to low-leakage state and the leakage power dissipated in the standby state together is less than the leakage power without the technique.
- Power gating and multiple threshold CMOS (MTCMOS) techniques turn off the devices by cutting off their supply voltage using sleep transistors.
 - The sleep transistor is turned on when the circuit is active and turned off when the circuit is in idle state with the help of sleep signal.
 - There is a significant increase in the delay of the circuit when active, due to the presence of the sleep transistor on switching path. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors.
- Another variation called dual technique uses low threshold transistors for gates on the critical path and high threshold transistors for gates not in the critical path. Additional mask layers for each value of threshold voltage are required for fabricating the transistors

selectively according to their assigned threshold voltage values, giving rise to complex fabrication process.

- Forced stacking introduces an additional transistor for every input of the gate in both N- and P-networks to ensure two transistors to be Off for every Off-input of the gate. - However, the loading requirements due to forced stacking reduces the drive current of the gate significantly and hence, the switching speed. A blend of sleep transistors and the stacking effects are used to reduce leakage power.
- This method identifies a circuit input vector for which the leakage current of the circuit is the lowest possible. The sleep signal-controlled transistors are inserted away from the critical path where only one transistor is Off when low leakage input vector is applied to the circuit. Hence, this technique is input vector dependent. Moreover, as this technique uses sleep transistors, it needs additional control hardware consuming power in both idle and active states.
- All the existing techniques except forced stacks, do not effectively control the leakage currents when the circuit is in its active state.
- New technique called LECTOR (Leakage Control Transistor) is designed CMOS circuits aimed at leakage power reduction. This technique control does not distinguish between active and idle states of the circuit and effectively control the leakage currents during all states of the circuit operation.

Leakage Control Transistor Logic:

The transistor stack is a leakage reduction technique which works both in active and standby mode. It is based on the observation that two off-state transistors connected in series cause significantly less leakage than a single device. The leakage current of the stack is even smaller than the leakage of a single device with double channel length. Doubling the channel length reduces the off-current by a factor of two. However, in modern deep sub-micron devices the threshold voltage may decrease for longer channels due to the reverse short channel effect. Therefore, leakage reduction is less effective.

Sub-threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as the “stacking effect” or “self- reverse bias”. Leakage currents in NMOS or PMOS transistors depend exponentially on the voltage at the four

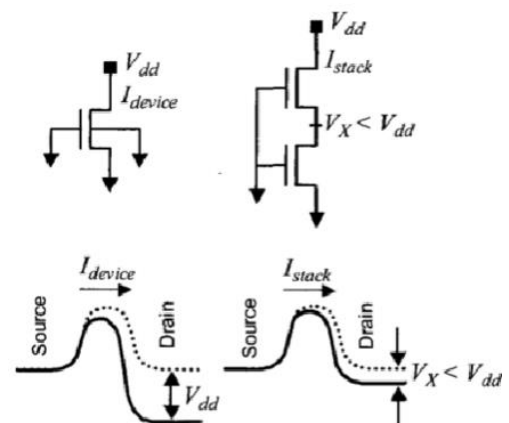


Fig. 1 Leakage current difference between single off device and a stack of two off devices. As illustrated by the energy band diagram, the carrier height is modulated to be higher for the two-stack due to smaller drain-to-source voltage resulting in reduced leakage.

Figure 1

terminals of transistors. V_G is “0” thus increasing V_S of NMOS transistor reduces sub-threshold leakage current exponentially.

When both transistors M_1 and M_2 are turned off, the voltage at the intermediate node (V_M) is positive due to small drain current. Positive potential at the intermediate node has the three following effects:

- Due to the positive source potential V_M , gate to source voltage (V_{GS1}) of transistor M_1 becomes negative; hence, the sub-threshold current reduces substantially.
- Due to $V_M > 0$, body to source potential (V_{BS1}) of transistor M_1 becomes negative, which results in an increase in the threshold voltage (larger body effect) of M_1 , and thus reducing the sub-threshold leakage; further the drain to source potential (V_{DS1}), results in increase of threshold voltage (less drain-induced barrier lowering) of M_1 , reducing sub-threshold voltage.
- If only one NMOS device is off, the voltage at the source node of off transistor would be virtually zero because all other on transistors will act as short circuit. Thus, there is no self-reverse biasing effect, and the leakage across the off transistor is large. But if more than one transistor is off, the source voltages of the off transistor, except the one connected to ground by transistors, will be greater than zero, and the leakage will be determined by the most negatively self-reverse biased transistor (because sub-threshold leakage is an exponential function of gate-source voltage). The reverse bias makes the leakage across the off transistor very small.

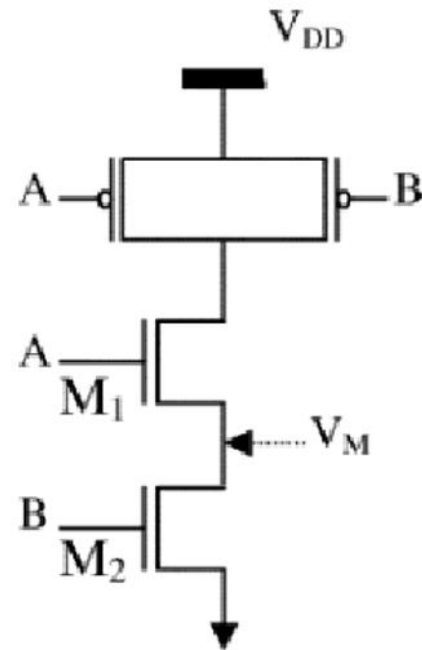


Figure 2: LCT TECHNIQUE

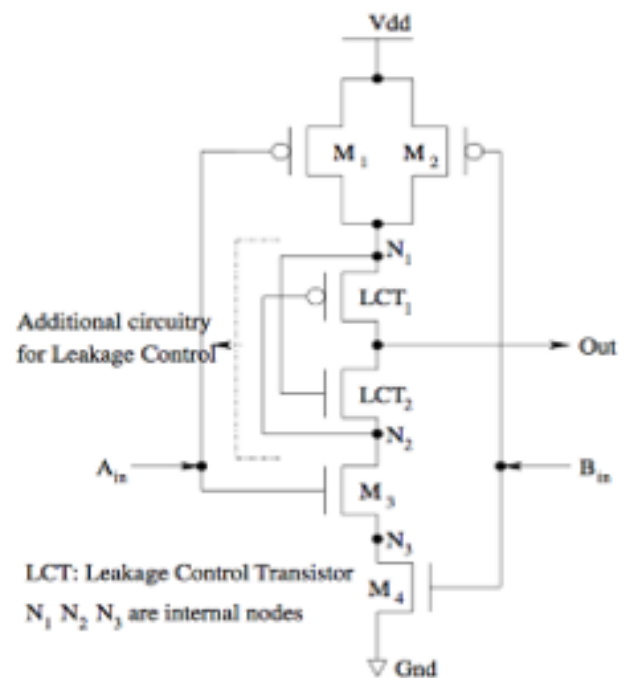


Figure 3: LCT NAND GATE

to ground is far less leaky than a state with only one transistor Off in any supply to ground path”.

In our method, we introduce two Leakage Control Transistors (LCTs) in each CMOS gate such that one of the LCT's is near its cut-off region of operation. We illustrate LEakage Control TransistOR technique (LECTOR) with the case of a NAND gate. A CMOS NAND gate with the addition of two leakage control transistors is shown in given figure (later referred to as LCT NAND gate).

Two leakage control transistors LCT1(PMOS) and LCT2(NMOS) are introduced between the nodes N1 and N2 of the pull-up and pull-down logic of the NAND gate. The drain nodes of the transistors and are connected to form the output node. The source nodes of the transistors are connected to nodes N1 and N2 of pull- up and pull-down logic. The switching of transistors LCT1 and LCT2 are controlled by the voltage potentials at nodes N2 and N1 respectively. This wiring configuration ensures that one of the LCT's is always near its cut-off region, irrespective of the input vector applied to the NAND gate.

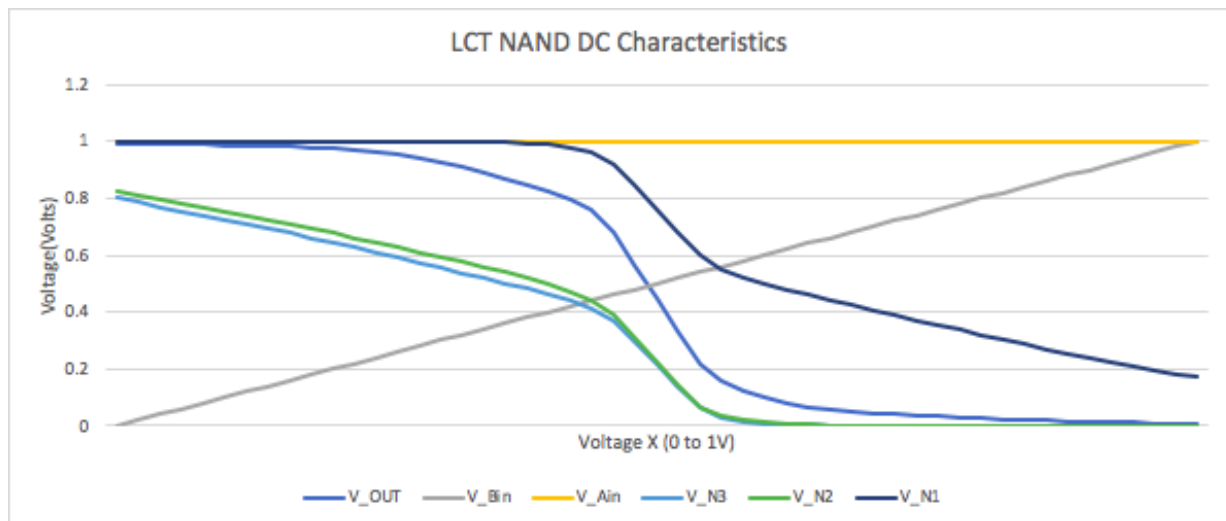


Figure 4: DC CHARACTERISTICS OF LCT NAND GATE

This can be seen from the DC characteristics of the LCT NAND Gate shown above, obtained from simulations, when the input A_{in} is fixed at 1V and B_{in} is varied from 0V to 1V. The values of V_{N1} and V_{N2} indicate the Near Cut-off operation for the LCT transistors.

Circuits and Architectures

1. LCT NAND Gate

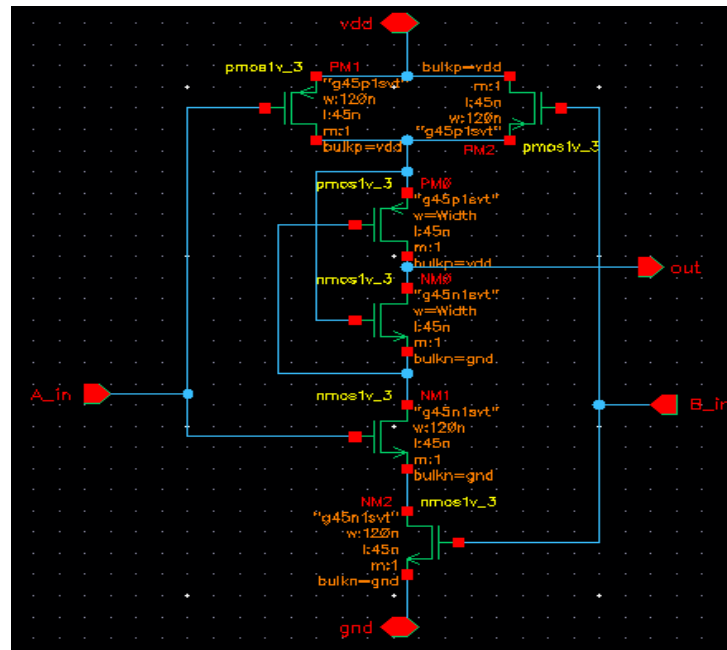


Figure5: LCT NAND GATE SCHEMATIC

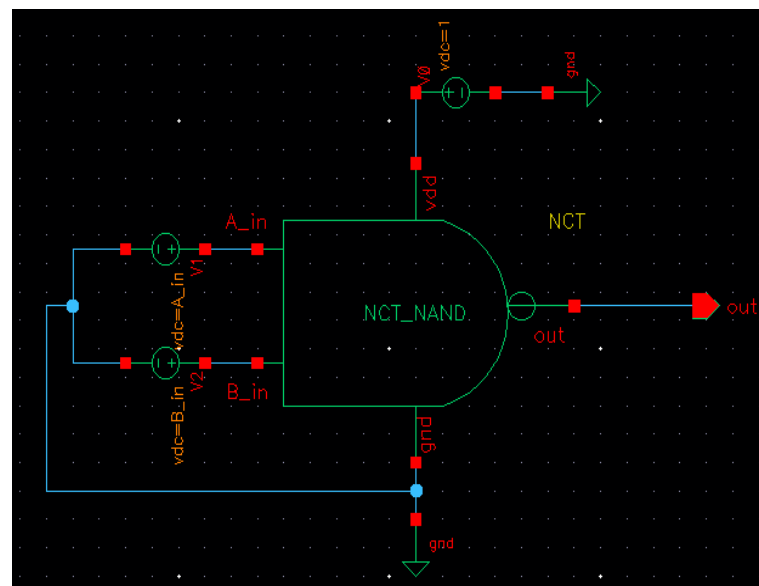


Figure6: LCT NAND GATE SYMBOL

2. LCT Half Adder

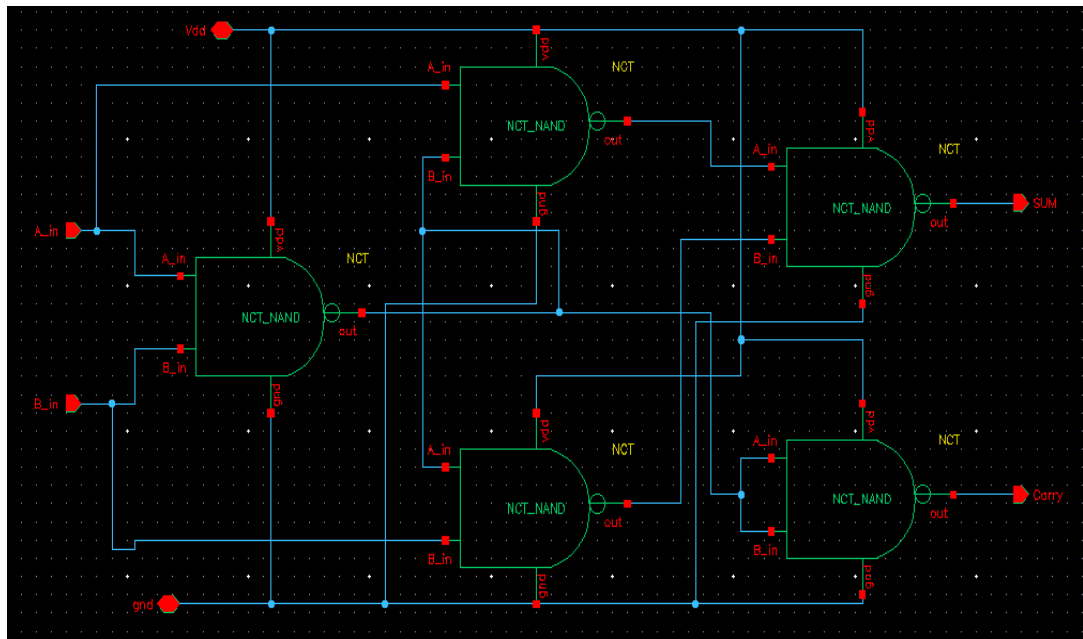


Figure 7: LCT HALF ADDER SCHEMATIC

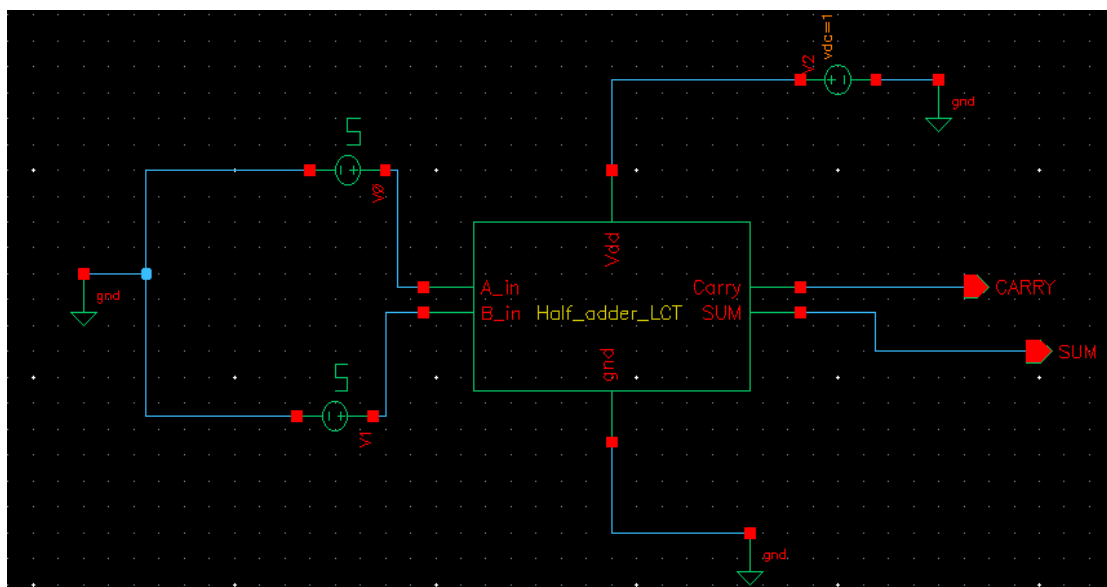


Figure 8: LCT HALF ADDER SYMBOL AND TEST CIRCUIT

3. LCT Multiplier

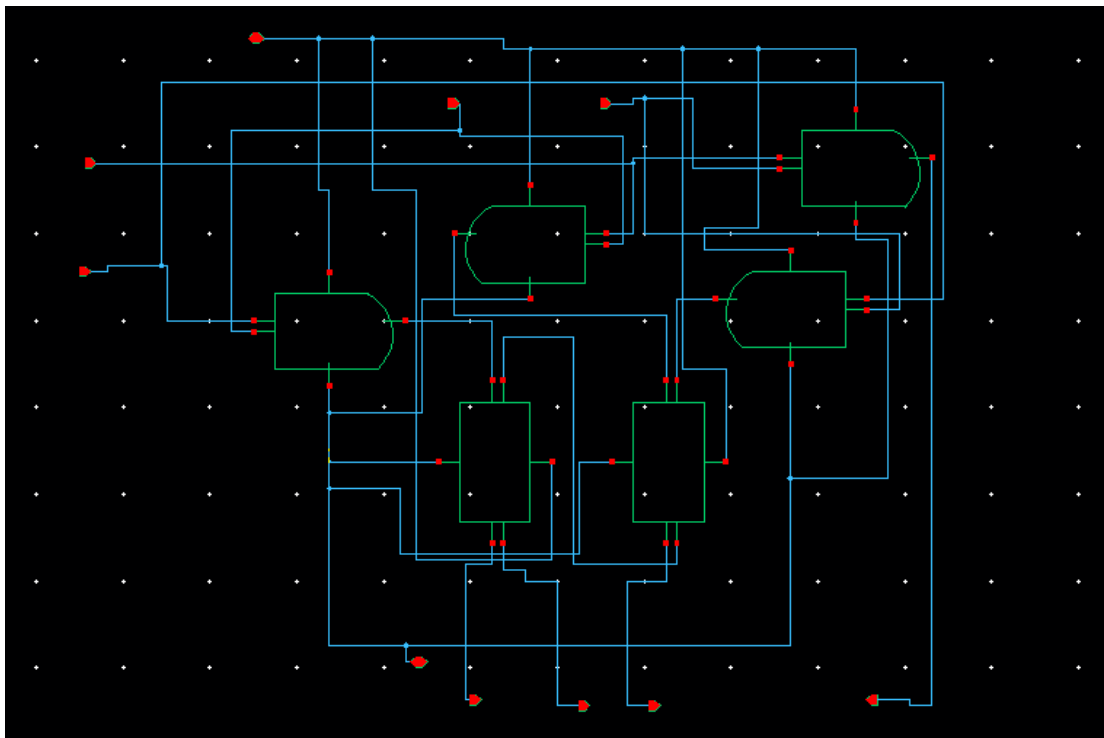


Figure 9: LCT MULTIPLIER SCHEMATIC

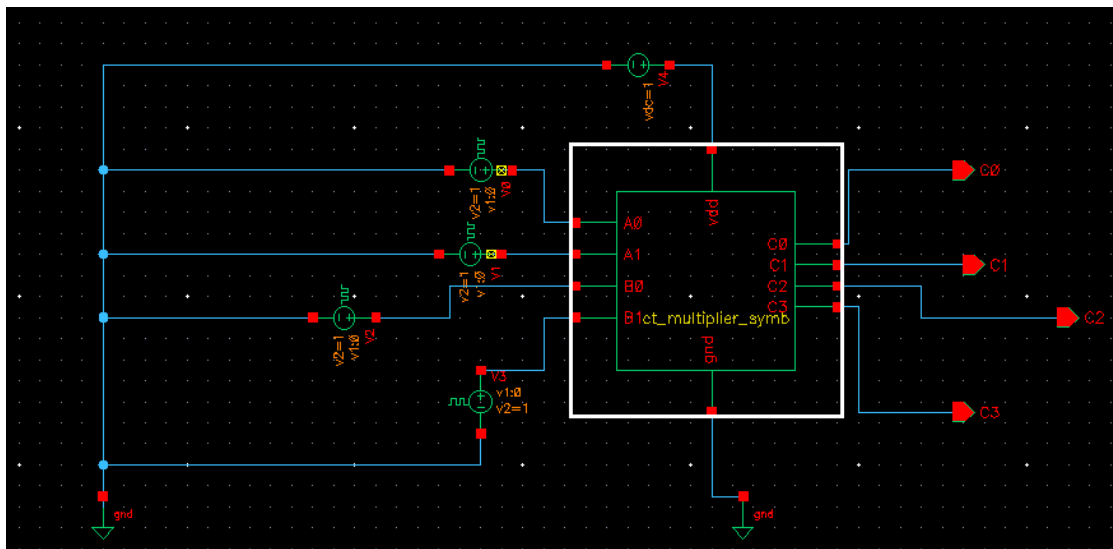


Figure 10: LCT MULTIPLIER SYMBOL AND TEST CIRCUIT

4. LCT Inverter & AND Gate

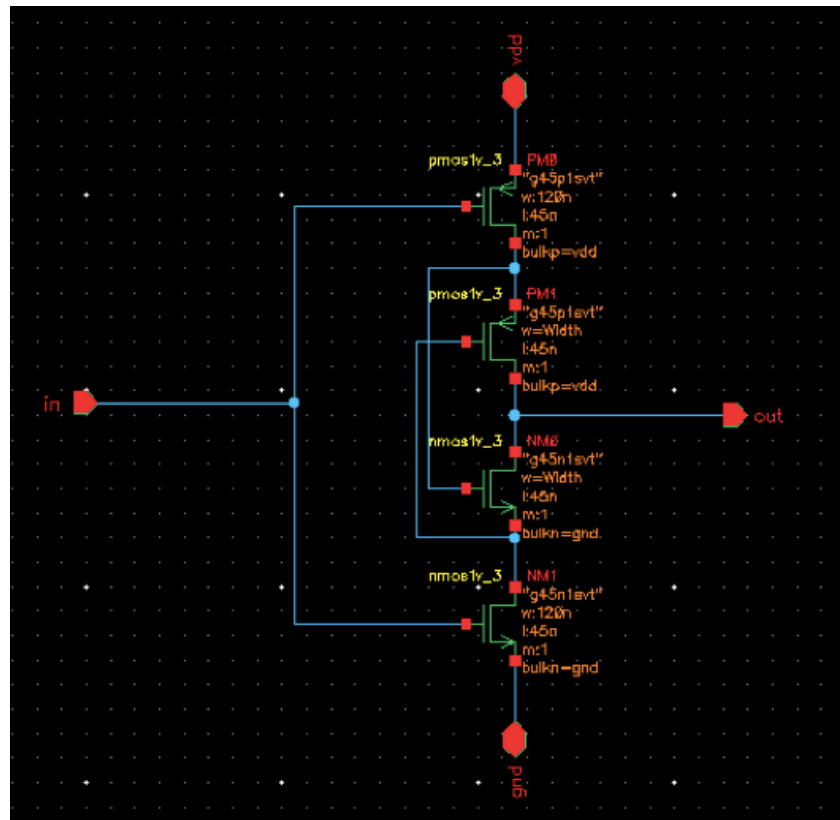


Figure 11: LCT INVERTOR

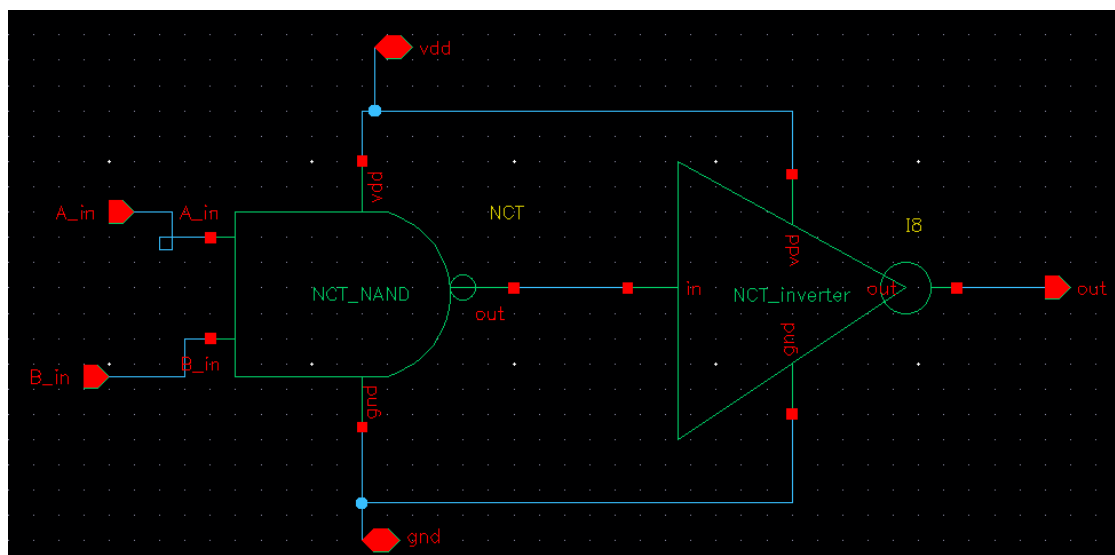


Figure 12: LCT AND GATE

Methodology and Simulation Results:

- We have performed all the analysis on 45nm technology with supply voltage as 1V considering the threshold voltage $V_{TO} = 0.39V$ because it produces most accurate logic levels
- We made a conventional NAND gate using CMOS transistors and then implemented LCT technique on a basic NAND gate.
- Found the power dissipated and delay for conventional and LCT NAND gate by changing the values of input vectors i.e. A_in and B_in for 4 cases (0,0), (0,1), (1,1), (1,0) and varied the width of LCT Transistors as 120n, 180n, 240n, 300n keeping ratio of widths of LCT transistors and normal transistors as 1, 1.5, 2, 2.5.
- As you can see from the data obtained that Power dissipated increases as we move from LCT to 2.5 LCT hence the power savings decrease along with decrease in delay. Also, (1,1) has the maximum power dissipation, case where A_in and B_in are (0,0) has minimum power dissipation.

			Nand Gate								
			We use DC Voltage Source for Ain and Bin								
45 nm technology	(0,0)	(0,1)	(1,0)	(1,1)	TPHL(ns)	TPLH(ps)	Delay=(TPHL+TPLH)/2 (ns)		Power Savings(%)		
	Leakage Power Dissipation(nW)										
Conventional	1.07909	1.17889	1.48696	1.67909			20.0124	(0,0)	(0,1)	(1,0)	(1,1)
LCT	0.60406	0.634062	0.834066	0.934071	40.04995	30.179	20.0401	44.02135	46.21534	43.90797	44.3704
1.5-LCT	0.675347	0.754071	0.894736	1.034742	40.04113	31.6377	20.0364	37.41514	36.03551	39.82784	38.37483
2-LCT	0.7473	0.8052	0.9939	1.193705	40.03324	33.028	20.0331	30.7472	31.69846	33.15893	28.90764
2.5 LCT	0.775999	0.831899	1.05254	1.206901	40.03027	34.552	20.0324	28.08761	29.4337	29.21531	28.12172

Figure 13: NAND GATE ANALYSIS

- Made symbols for LCT NAND for test circuit and future use and tabulated and compared the results.
- Further implemented LCT Technique on a half adder circuit using LCT NAND symbol created before and performed the same analysis comparing the performance in terms of power and delay of conventional half adder circuit with that of LCT half adder for various ratio of widths of LCT transistors and normal transistors as 1, 1.5, 2, 2.5.

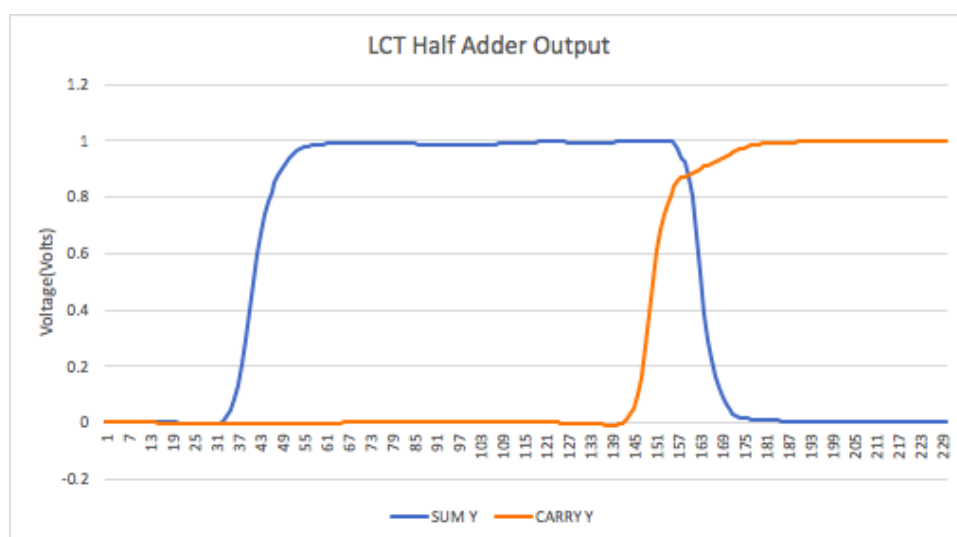


Figure 14

Input Data for checking functionality: Two Vbit Sources used as Input with bitstream as 0,0,1,1 and 0,1,0,1 respectively along with Vdc with dc voltage=1V.

- The output we get on doing transient analysis is sum is 0,1,1,0 and carry is 0,0,1,1 which matches with the truth table values of half adder, hence are circuit is working fine.
- We can see that in the case of half adder too, the power dissipated increases for increase in the ratio of width of LCT transistor to that of a normal transistor implying that power savings in % decrease with decrease in delay.

We use Vpulse with Voltage 1=0V ; Voltage 2=1V; DC Voltage=1V				
		Half Adder		
	Power Dissipation(nW)	% Saving	Delay (ns)	
			Sum	Carry
Conventional	8.5095		0.211308	0.393695
LCT	4.98105	41.4648334	0.305468	0.45361
2-LCT	5.3452	37.1854986	0.297214	0.41065
2.5-LCT	5.8567	31.1745696	0.258677	0.40759

Figure 15: HALF ADDER ANALYSIS

- Implemented and made symbols of LCT Inverter to create LCT AND gate to be used in the LCT multiplier circuit along with the previously created symbols of LCT half adder.
- Performed the analysis comparing the performance in terms of power and delay of conventional Multiplier circuit with that of LCT Multiplier Circuit for various ratio of widths of LCT transistors and normal transistors as 1, 1.5, 2, 2.5.

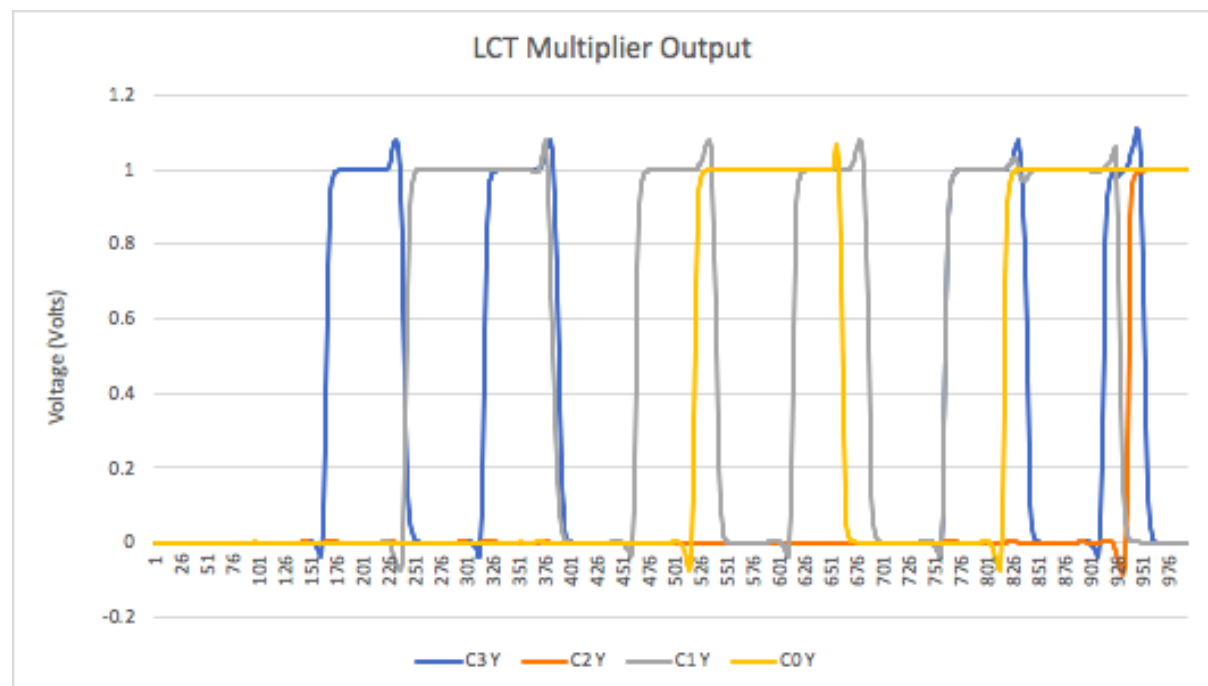


Figure 16

Input Data for checking functionality: Vdc with dc voltage=1V and Four Vbit Sources used as Input with bitstream as follows:

A0= 0,0,0,0,0,0,0,0,1,1,1,1,1,1,1

A1= 0,0,0,0,1,1,1,1,0,0,0,0,1,1,1

B0= 0,0,1,1,0,0,1,1,0,0,1,1,0,0,1

B1= 0,1,0,1,0,1,0,1,0,1,0,1,0,1,0

Outputs: C3,C2,C1,C0

x_0	x_1	x_2	x_3	f_0	f_1	f_2	f_3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

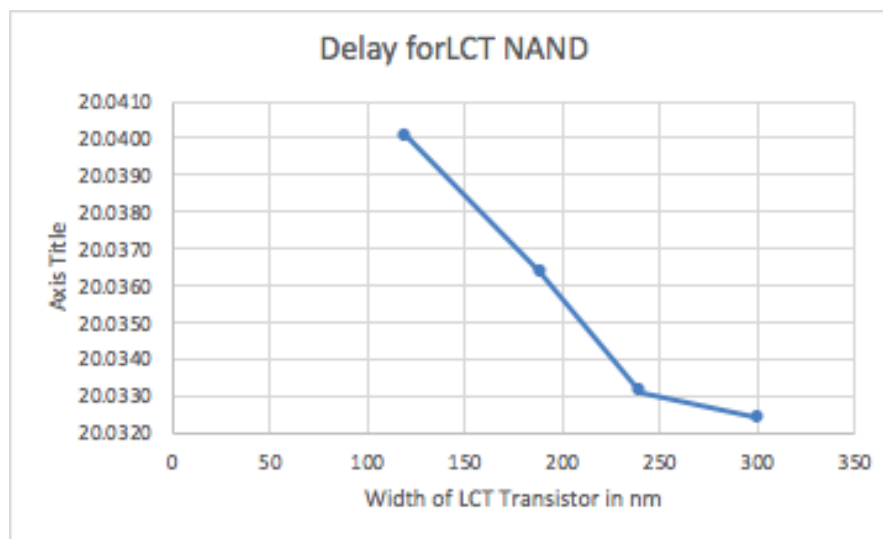
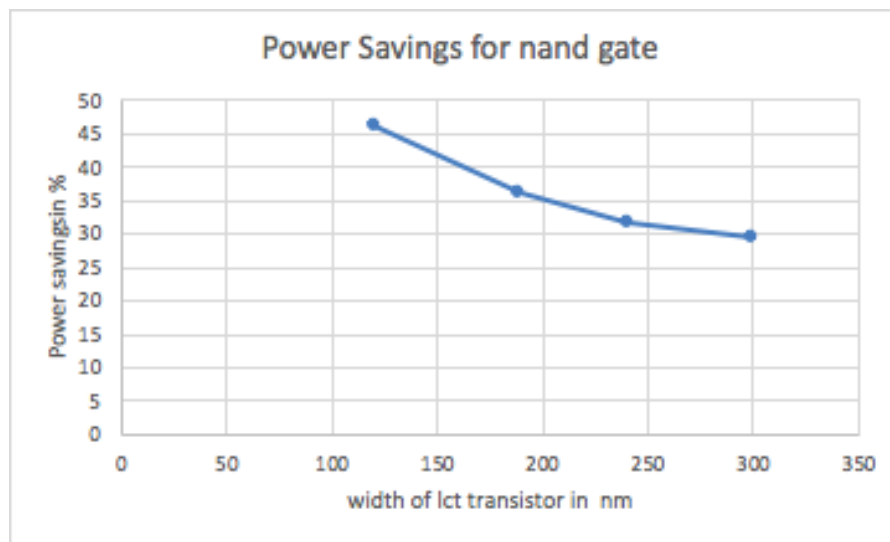
Figure 17: Multiplier Truth Table

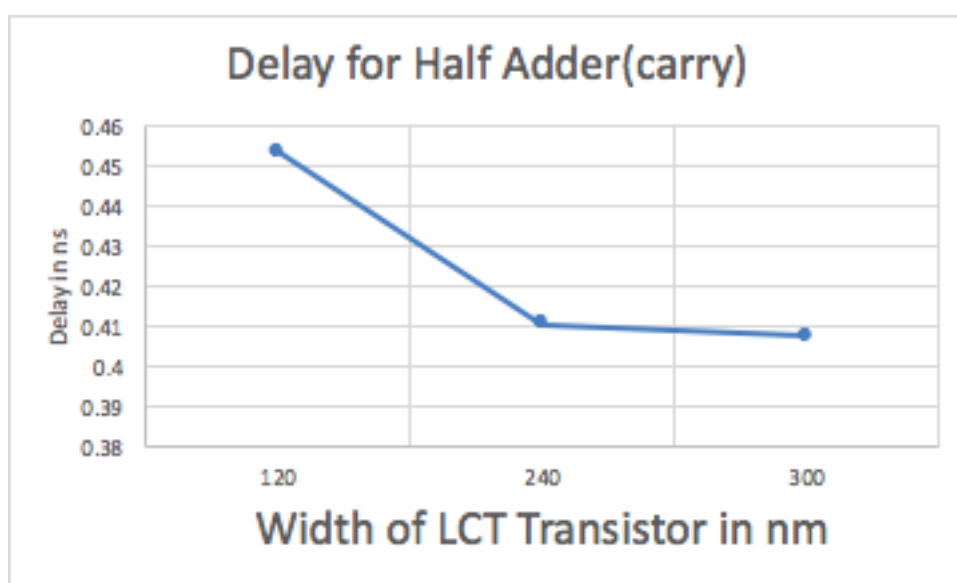
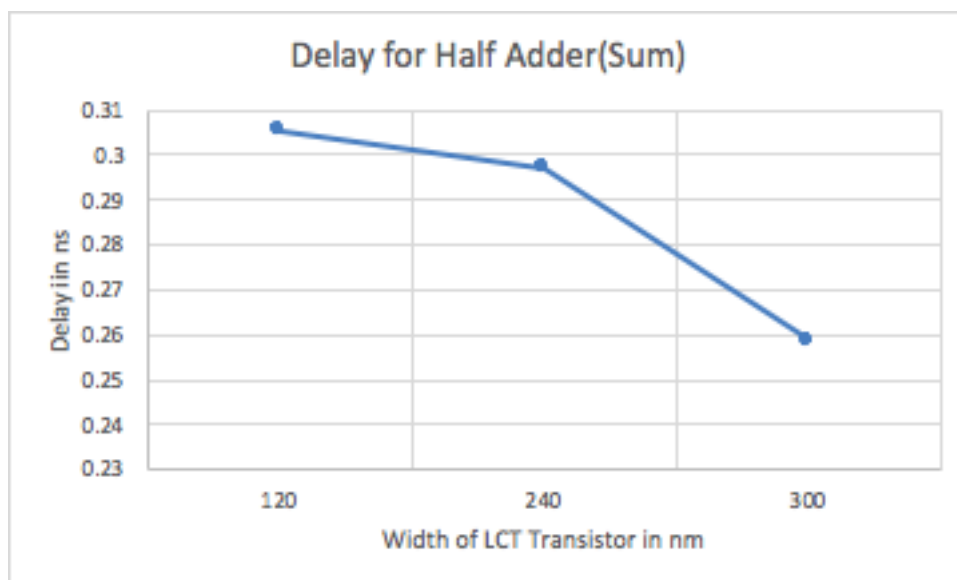
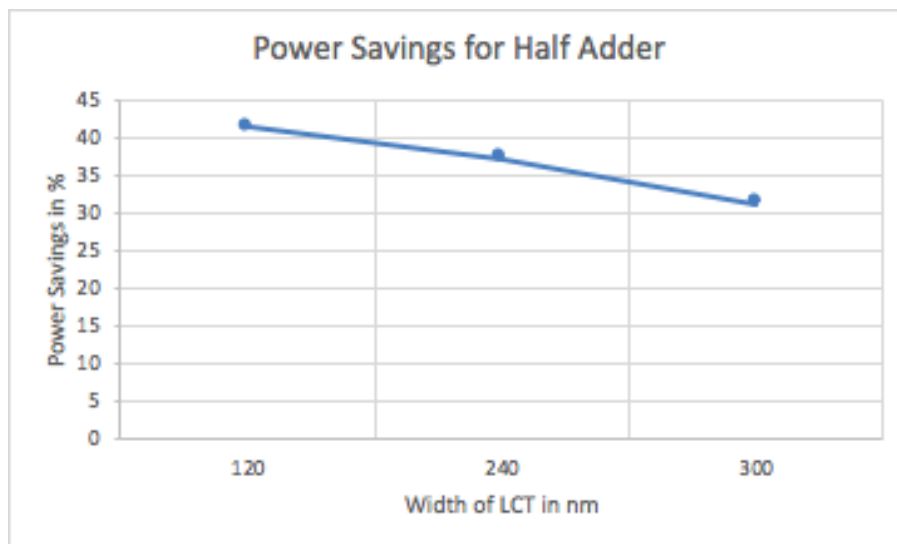
We use Vpulse with Voltage 1=0V ; Voltage 2=1V; DC Voltage=1V						
			Multiplier	Delay (ns)		
	Power Dissipation(nW)	% Saving	C0	C1	C2	C3
Conventional	92.2585		0.503092	0.574564	0.632817	0.578122
LCT	56.2128	39.07032956	0.681552	1.10175	2.13838	1.1295
2-LCT	60.8723	34.01984641	0.750161	1.10147	1.85926	1.1268
2.5-LCT	67.4502	26.88998846	0.785058	1.1346	1.83943	1.15798

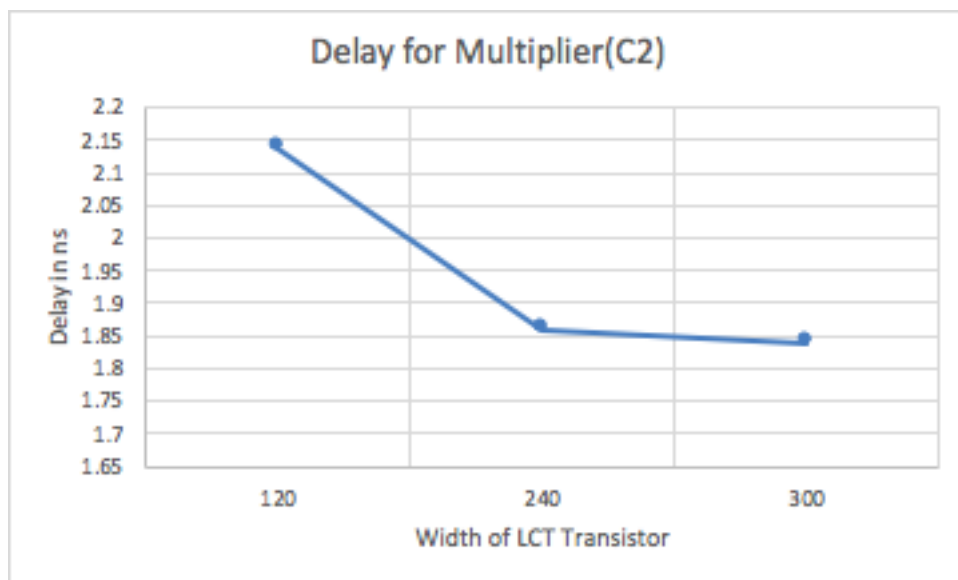
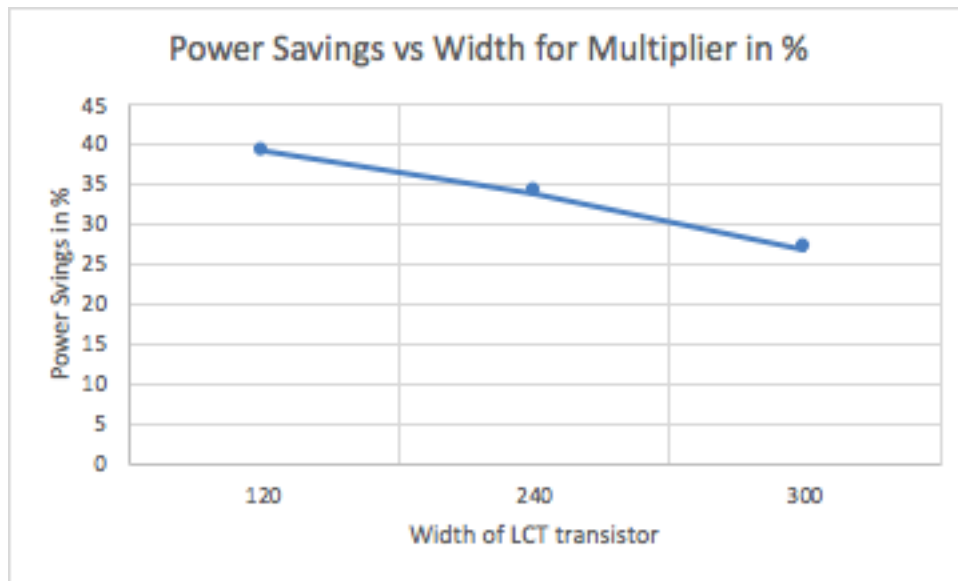
Figure 18: MULTIPLIER ANALYSIS

- We can see that the power dissipated increases from LCT to 2.5LCT implying that power savings in % decrease with decrease in delay.
- We also notice that C2 has the worst case delay in this case.

Graphs/Trends:
(0,0) Case







Observations:

- All the analysis are done by considering the threshold voltage $V_{TO} = 0.39V$ and by using 45nm technology.
- We observe that introduction of LCT's increases the resistance of the path from V_{dd} to ground leading to significant decrease in leakage currents. This also increases the propagation delay of the gate. To reduce this hostile effect, the transistors of LCT gate are sized such that the propagation delay is equal to its conventional counterpart.
- By varying the combination of input vectors of the NAND gate the delay and power dissipation have been calculated. For NAND Gate : When all the inputs are low (all NMOS transistors are OFF) the power dissipation is minimum and when all the inputs are high (all NMOS transistors are ON) the power dissipation is maximum. If the number of low input increases, the power dissipation decreases because the sub threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off.

- The LECTOR technique has been applied to the half adder and multiplier circuit and the performance results were compared to that of conventional technology.
- On increasing the width of the LCT transistors in comparison to the normal transistors, the power savings decrease along with slight decrease in delay.

Conclusion/Inferences:

- Scaling down of device dimensions, supply voltage, and threshold voltage for achieving high-performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. LECTOR requires exactly two additional transistors for every path from supply voltage to ground irrespective of the logic function realized by the gate. Leakage current is especially important in portable systems where battery life is important.
- LECTOR is an efficient design methodology made for reducing the leakage power in CMOS circuits. The leakage savings obtained is without any significant sacrifice in dynamic power.
- The required series and parallel combinations of transistors are generated by analysing the relevant Karnaugh map for both n- and p- logic structures and using De-Morgan's theorems. As these gates are built on static CMOS technology, they are called Static CMOS Complex Gates.
- Static Cmos gates have exactly one common node which connects the pull-up and pull-down circuits of the gate. This node is the appropriate place for inserting LCTs as all the paths from the supply voltage to ground would pass through this node. The limitation with gates is that if the number of transistors in series exceeds an upper limit in any path of pull-up or pull-down logic then there is a hostile effect on the propagation delay of the gate which can be seen from our analysis concluding that LECTOR performs better in terms of power dissipation than conventional technology but at the same time there is an increase in propagation delay.
- Y-LCT gates are obtained by sizing the widths of only the leakage control transistors, and to Y-times the width of other PMOS and NMOS transistors of the gate respectively.
- Varying the input vector combination, we can reduce the power dissipation.
- There is a tradeoff between power and delay. To have minimum delay and power dissipation without degrading the performance or maximum power saving, the tradeoff requires optimized device dimensions and supply voltage for getting the best results.
- Further, ISO -LCT case could be calculated where delay of the LCT based circuit is same as that of conventional one but power dissipated is less.
- Experimental results show that LCT technique offers a leakage reduction for the same critical path delay relative to the unmodified circuit for MCNC '91 benchmarks also.

References

[1]. A New Technique for Leakage Reduction in CMOS Circuits using Self-Controlled Stacked Transistors
Narender Hanchate and N. Ranganathan Nanomaterials and Nanomanufacturing Research Center Department of Computer Science and Engineering University of South Florida, Tampa, FL 33620.

[2]. Implementation of Transistor Stacking Technique in Combinational Circuits
IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 5, Ver. I (Sep-Oct.
2014), PP 01-05 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197

[3]. Study and Analysis of Universal Gates Using Stacking Low Power Technique Neha
Goyal^{#1}, Renu Singla^{*2}, Puneet Goyal^{#3} ^{#1, *2} Department of Computer Science And
Engineering, Shri Ram College Of Engg. & Mgmt, Palwal, India ^{#3} Directorate General of Civil
Aviation, New Delhi, India