4’bit Counter using Verilog and DE 10lite FPGA board

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DE-10 LITE

Table of contents:

1. Introduction
2. Objective
3. Methodology
4. Components used
- FPGA board
- Software Quartus prime
- Seven segments

1. Logic
2. PIN assignments
3. Output
4. Conclusion
5. References

Introduction

The field of digital design and programmable logic has opened up exciting possibilities for creating versatile and efficient systems. In this mini project, we present an implementation of a digital counter using the DE10-Lite FPGA board. The FPGA serves as a powerful platform to design and deploy custom digital circuits, allowing us to create a precise and flexible counter capable of measuring time intervals ranging from 10s of seconds up to 59 minutes.

Objective

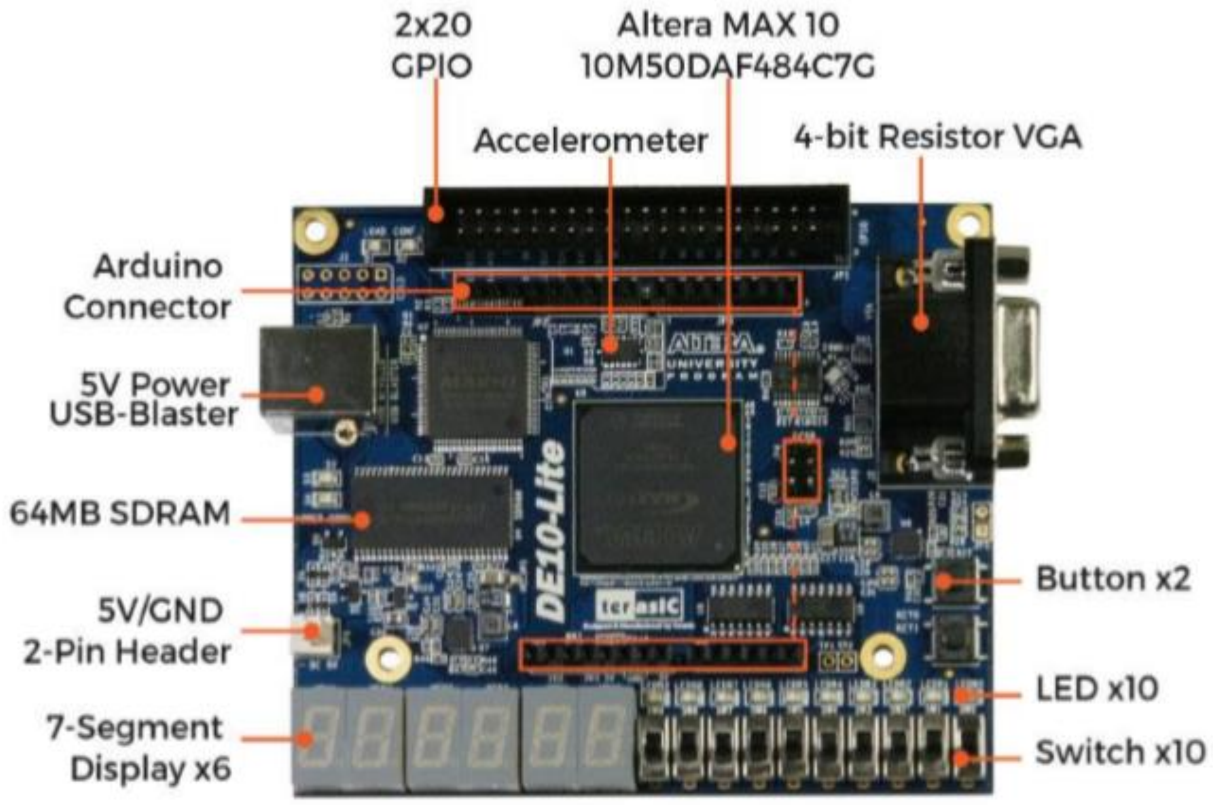
The main objective of this project is to demonstrate the capabilities of the DE10-Lite FPGA board by designing a time counter with high accuracy and flexibility. By utilizing the FPGA's programmable logic resources, we can create a customizable and efficient counter for various applications such as time measurement, event timing, or system synchronization.

Methodology

The digital counter is implemented using a combination of synchronous digital design techniques and FPGA programming. The DE10-Lite board offers a range of resources, including programmable logic elements, clock resources, and input/output interfaces, which are leveraged to build the counter circuit.

Components used

FPGA (DE-10 LITE)



The DE10-Lite FPGA board is a popular and versatile development platform designed by Terasic. It is built around the Intel Cyclone® V FPGA, offering a range of features and capabilities for various digital design and prototyping projects.

FPGA (DE-10 LITE)

FPGA Chip: The DE10-Lite board utilizes the Intel Cyclone V FPGA, which provides a large number of programmable logic elements, dedicated memory blocks, and other resources for implementing custom digital circuits.

Processing Power: The FPGA chip on the DE10-Lite board is equipped with an embedded dual-core ARM Cortex-A9 processor, enabling both hardware and software co-design possibilities.

On-Board Memory: The board includes 1GB DDR3 memory, which can be used for storing data or program instructions during FPGA operation.

I/O Interfaces: The DE10-Lite board offers a range of input and output interfaces, including push-buttons, switches, LEDs, seven-segment displays, VGA output, audio output, and USB connectivity. These interfaces allow for user interaction, data display, and connection with external devices.

Educational Resources: Terasic provides comprehensive documentation, tutorials, and example projects to support users in getting started with the DE10-Lite board. These resources help beginners and experienced designers alike to learn and explore FPGA development.

Applications: The DE10-Lite FPGA board is suitable for a wide range of applications, including digital logic design, embedded systems development, algorithm prototyping, robotics, image and signal processing, and more

Software Quartus prime lite edition

Quartus Prime is a software suite developed by Intel (formerly Altera) for designing and programming FPGA (Field-Programmable Gate Array) devices. Quartus Prime provides a comprehensive set of tools for designing, simulating, synthesizing, and programming FPGAs. The Lite Edition of Quartus Prime is a free version of the software that offers a subset of features compared to the full version

Design Entry: Quartus Prime Lite Edition supports schematic, HDL (VHDL/Verilog), and Block Diagram/Simulation design entry methods.

Simulation: ModelSim-Intel FPGA Starter Edition allows design simulation and verification.Synthesis and Optimization: Translates RTL code into gate-level representation and optimizes design for better performance.

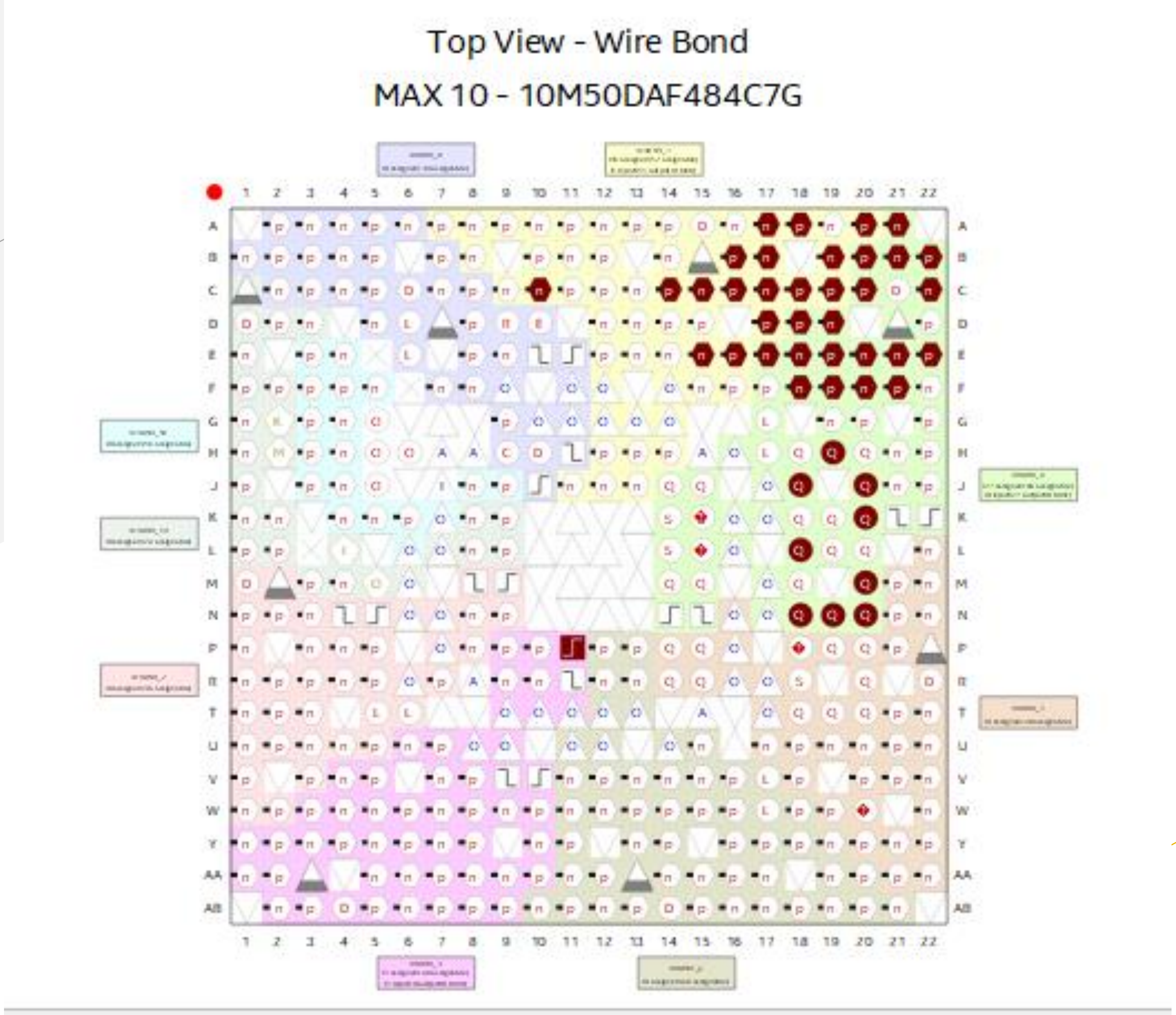
Place and Route: Automatically determines physical placement and route interconnections for FPGA implementation.

Seven Segment displays

A common anode seven-segment display is a type of electronic display that consists of seven individual segments (labeled A to G) arranged in the shape of a digit "8". Each segment can be individually controlled to display different numbers and characters. In a common anode configuration, the anodes of all the LED segments are connected together and connected to a positive voltage supply, while the cathodes of each segment are connected to the ground through current-limiting resistors.

To illuminate a specific segment, a low logic level or ground is applied to the corresponding cathode pin, allowing current to flow through the segment and light it up. By selectively activating different combinations of segments, various numbers, letters, and symbols can be displayed on the seven-segment display.

PIN Assignments



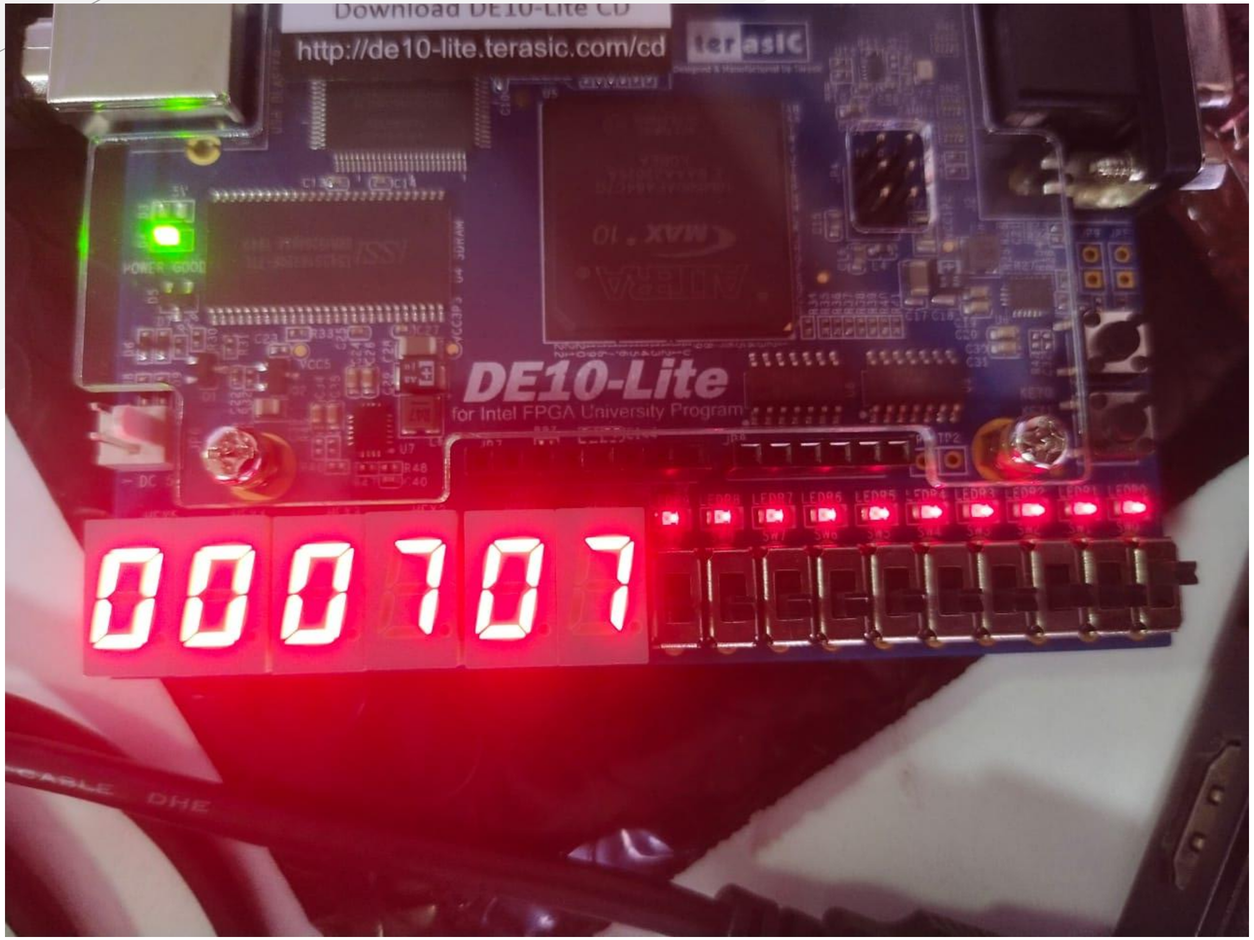
Top View - Wire Bond

MAX 10 - 10M50DAF484C7G

Logic

- Declare a register to store the current count value. For example, reg [N-1:0] count;, where N represents the number of bits required to represent the count value.
- Create a sensitivity list or use an always block with a clock edge condition (posedge or negedge) to trigger the counter update. For example: always @(posedge clk).
- Inside the always block, use an if statement or a case statement to control the counter behavior. For an up-counter, increment the count value when the desired condition is met. For example: if (condition) count <= count + 1;.
- Assign the counter value to an output signal if necessary. For example, assign counter_out = count;.
- Repeat the process for subsequent bits if you need a multi-bit counter

Output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Conclusion:

Conclusion: This mini project showcases the potential of the DE10-Lite FPGA board for digital design applications. The implemented digital counter, capable of measuring time intervals from 10s of a second to 59 minutes, highlights the flexibility, accuracy, and versatility of FPGA-based systems. By exploring the design and functionality of this counter, we gain insights into the power of programmable logic and its role in creating innovative solutions for time measurement and related applications.

References:

1.Altera DE10-Lite User Manual: This manual provides detailed information about the DE10-Lite development board, including the FPGA features, pin assignments, and programming steps. It can be found on the Terasic website or in the documentation section of the DE10-Lite board.

2.Quartus Prime Software User Guides: Quartus Prime is the software tool used for designing and programming the DE10-Lite FPGA. The user guides provide step-by-step instructions on how to use Quartus Prime for creating and compiling Verilog designs, configuring the FPGA, and generating programming files.

3.Verilog Tutorial: If you're new to Verilog or need a refresher, a Verilog tutorial can be helpful. There are many online resources available that provide a comprehensive introduction to Verilog syntax, design concepts, and coding techniques. One popular tutorial is the "Verilog HDL Quick Reference Guide" by Stuart Sutherland.

4.FPGA Counter Examples: To gain a better understanding of counter implementations in Verilog, it can be helpful to study example codes. Look for FPGA counter examples online or in Verilog reference books. These examples can provide insights into different counter designs, including up-counters, down-counters, binary counters, and more.

5.FPGA Forum and Communities: Engaging in FPGA forums and online communities can be beneficial for getting guidance, troubleshooting, and learning from experienced FPGA designers. The Altera/Intel FPGA Forum, Xilinx Community Forums, and FPGA-related subreddits are good places to start.

6.Terasic Forum and Resources: Terasic, the manufacturer of the DE10-Lite board, provides a forum and resources section on their website. This platform allows users to share their projects, ask questions, and access additional reference materials specific to Terasic development boards.

Remember to cite and credit any references you use in your project to acknowledge the sources properly. Good luck with your project!