This page should be stapled together with the rest of the report. After the grading, this page will be taken and kept by the TAs for the record.

A. (This section to be completed by student)

Student logic number: _____

Student name: (Last) _____, (first) _____

Experiment number: 1

Date/time: _____/_____/ _____, _____a.m./p.m.

B. Preliminary checking

1. Is the report written on 8½" x 11" paper and stapled at left margin?
2. Is a cover page included?
3. Is the report written using the given template?
4. Is the correct assignment used in design?

Report will not be accepted if the answer is "NO" to any of the above questions.

C. Grade

1.	Step 1: (a) Is circuit correct?		(20) _____
	(b) Gate minimization		(05) _____
2.	Step 2		(20) _____
3.	Step 3		(20) _____
4.	Step 4		(15) _____
5.	Step 5		(20) _____
		Gross grade	(100) _____

D. Adjustment to gross grade

1.	Grade sheet, cover page	(−5) _____
2.	Title box of schematic diagram	(−5) _____
3.	Schematic diagram in correct format	(−10) _____
4.	Misrepresentation of test (simulation) results	(−30) _____
5.	Neatness and legibility	(−10) _____
6.	Templates	(−20) _____
	Final grade	(100) _____

Comments: _____

_____

Grader: _____ Date: ____/____/_____

16.265 Logic Design	
Student Logic Number	
Name	
E-mail address (print)	
Experiment Number	1
Date	

For grader use	
Schematic diagram submitted is different from the one in the report. (Need to re-submit the schematic diagram in the report or will be graded based on a maximum of 50 points.)	5 points deduction
Cannot open file	
File is not readable	
Date student is notified to re-submit a schematic file by e-mail	
Date schematic file received	

Report will be graded based on a maximum of 50 (out of 100 points) if a schematic diagram is not received within three calendar days of notification or the re-submitted schematic file still cannot be opened or is not readable.

Grade: _____

Experiment 1 Analysis of Digital Circuits

1. (a) Attach a complete schematic diagram including the original circuit, the title box, and your circuit at the end of the report.

(b) List of gates

Type of gates	Number of given gates	Number of unused gates
Inverter	4	0
2-input AND	4	
3-input AND	4	
2-input OR	4	
3-input OR	4	

(c) Record the simulation results in the following table.

Inputs	Simulation results					
A B C D	EQ1	EQ2	EQ3	EQ4	EQ5	EQ6
0 0 0 0						
0 0 0 1						
0 0 1 0						
0 0 1 1						
0 1 0 0						
0 1 0 1						
0 1 1 0						
0 1 1 1						
1 0 0 0						
1 0 0 1						
1 0 1 0						
1 0 1 1						
1 1 0 0						
1 1 0 1						
1 1 1 0						
1 1 1 1						

2. List the simplest POS expressions for G_1 and G_2 and the simplest SOP expressions for G_3 and G_4 obtained from the circuit in step 1 in the following table.

   Use A', B', C', and D' for your expressions. Do not use /A, /B, /A. and /D.

Simplest POS for G_1	
Simplest POS for G_2	
Simplest SOP for G_3	
Simplest SOP for G_4	

   Show how to get the simplest SOP for G_4 below.
   (Hint: Use the Sandwich algorithm to convert POS to SOP)

3. Obtain the maxterm lists of G_1 and G_2 and the minterm lists of G_3 and G_4 obtained from step 2 in the following table.

Maxterm list of G_1	π M (
Maxterm list of G_2	π M (
Minterm list of G_3	Σ m (
Minterm list of G_4	Σ m (

   Show the detailed work of Step 3 below or no credits.

4. List the minterm lists of G_1, G_2, G_5 and G_6 obtained from step 3 in the following table.

Minterm list of G_1	Σ m (
Minterm list of G_2	Σ m (
Minterm list of G_5	Σ m (
Minterm list of G_6	Σ m (

5. List the minterm and maxterm lists of G_1 to G_6 in the following table if AB = 01 (A = 0 ***AND*** B = 1) never occurs.

G_1	Σ m (
	π M (
G_2	Σ m (
	π M (
G_3	Σ m (
	π M (
G_4	Σ m (
	π M (
G_5	Σ m (
	π M (
G_6	Σ m (
	π M (