Combating the Memory Walls: Optimization Pathways for Long-Context Agentic LLM Inference

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Abstract

LLMs now form the backbone of AI agents for a diverse array of applications, including tool use, command-line agents, and web or computer use agents. These agentic LLM inference tasks are fundamentally different from chatbot-focused inference — they often have much larger context lengths to capture complex, prolonged inputs, such as entire webpage DOMs or complicated tool call trajectories. This, in turn, generates significant off-chip memory traffic for the underlying hardware at the inference stage and causes the workload to be constrained by two memory walls, namely the *bandwidth* and *capacity* memory walls, preventing the on-chip compute units from achieving high utilization.

In this paper, we introduce PLENA, a hardware-software co-designed system that applies three core optimization pathways to tackle these challenges. PLENA includes an efficient hardware implementation of compute and memory units supporting an asymmetric quantization scheme. PLENA also features a novel flattened systolic array architecture that has native support for FlashAttention to tackle these memory walls in the scenario of inference serving for long-context LLMs. Additionally, PLENA is developed with a complete stack, including a custom ISA, a compiler, a cycle-emulated simulator, and an automated design space exploration flow. The simulated results show that PLENA achieves up to 8.5× higher utilization than existing accelerators, and delivers 2.24× higher throughput than the A100 GPU and 3.85× higher throughput than the TPU v6e, under the same multiplier count and memory settings. The full PLENA system will also be open-sourced.

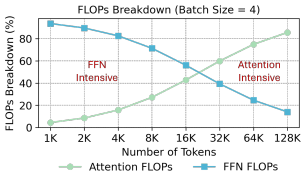
1 Introduction

Transformer models have revolutionised AI across numerous fields, including language, vision, and science [34, 65, 69]. Decoder-only transformer-based autoregressive large language models (LLMs), like GPT [50] and LLaMA [63], are now widely deployed in many applications, such as real-time chatbots [49], code generation [32] and agentic tool-use and computer-use workflows [48].

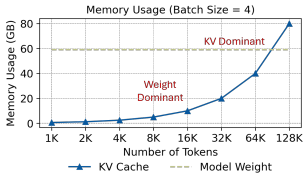
The rapid rise of agentic LLM capabilities, e.g. computer use [41], tool use [27, 46], and command-line agents [1], relies heavily on their ability to process and reason over very long contexts. For instance, command-line agents need to both comprehend and generate large-scale codebases [30, 55, 71], while tool- and computer-use agentic workflows must keep track of multiple pieces of information across prolonged inputs—such as an entire web page DOM—which typically require very long contexts [12, 20, 35]. Figure 1(a) shows that, compared with chatbot workloads, agentic workloads consume 100× more tokens per inference on average and up to 1,000× at the maximum case. In response, modern LLMs have expanded their context windows: the original GPT-3 [11] supports roughly 2K tokens, whereas GPT-4 [50] reaches up to 32K tokens, and LLaMA4-Maverick [2] extends the context window to 1M tokens.

To clarify the computational impact of agentic workloads, Figure 1(b) analyzes a LLaMA 3.3 70B model with long-context capability and shows that, when the number of generated tokens is low, the Feed-Forward Networks (FFNs) account for most of the total inference FLOPs, whereas the attention layers become dominant as the number of tokens generated grows. Notice these two phases can happen in a single inference run since we are performing autoregressive decoding. For instance, in the Longwriter [8] workload, the

(a) Compared with standard chatbot workloads, the selected agentic web and code tasks generally consume over 100× more tokens.



(b) Compute shifts from FFN to Attention with increasing context length.



(c) KV cache scales with context length, eventually dominating memory usage.

Figure 1: An illustration of agentic inference workloads shows how they typically generate many more tokens per inference run (Figure 1(a)), contain both FFN-compute-intensive and attention-compute-intensive phases (Figure 1(b)), and include weight memory-capacity-dominant and KV-dominant phases (Figure 1(c)) within a single inference run.

prefilling phase finishes at 5K tokens, and the decoding phase starts from there and continues to expand the context to up to 85K tokens, causing the workload to shift from the FFN-intensive to Attention-intensive region in terms of FLOPs in a single inference run as shown in Figure 1(b). Furthermore, with such large context lengths, the KV cache becomes the primary consumer of HBM resources.

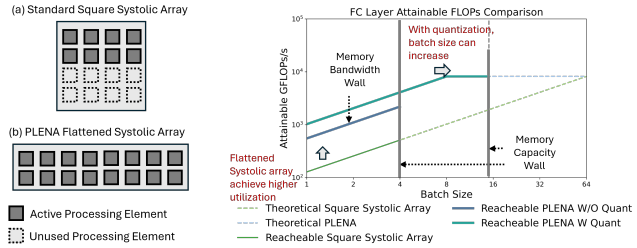
Figure 1(c) also identifies two major limiting factors on the memory side. The large number of KV values and weights that must be read, together with the portion of KV values written back, impose very substantial memory bandwidth demands. In addition, as context length increases, the KV-cache requirement grows linearly, quickly increasing memory usage and often surpassing the size of the model weights, making HBM capacity a primary limiting factor. For example, in LLaMA-3.3-70B, at a 128k context [45], the FP16 KV cache for a single batch is approximately 39 GB, which limits how many batches can be kept on the chip [23]. Building on this observation, we suggest that the two main challenges on the off-chip memory side, namely, (i) the limited memory bandwidth and (ii) the restricted memory capacity. We collectively term these *memory walls*. Together, they prevent devices from reaching peak performance at inference time, consistent with observations in prior work [18, 23, 74].

The memory wall phenomenon leads to underutilization of computing resources on modern hardware, including TPUs and GPUs. This effect is particularly evident in compute units dedicated to General Matrix-Matrix Multiplication (GEMM) operations ($\mathbb{R}^{M\times K} \times \mathbb{R}^{K\times N} \rightarrow \mathbb{R}^{M\times N}$), denoted as $(M, K) \times (K, N)$, which constitute the core computational workload during LLM inference [26]. At the microarchitectural level, most hardware is built with square-shaped systolic arrays or matrix multiplication units, typically designed so that the M and N dimensions are close in size to K. For example, TPU v3 [24] features a 128×128 systolic array, supporting $M = K = N = 128$ GEMM operations. The NVIDIA Blackwell B200 architecture [15] introduces a minimal computation granularity of $64 \times 8 \times 16$. However, in long-context models, as demonstrated in Figure 1(c), memory often constrains the inference batch size. This results in a *fat GEMM*, where the batch-related dimension (typically M in $(M, K) \times (K, N)$) is much smaller than the others, producing an uneven matrix shape. This imbalance hinders systolic arrays and Tensor Cores from achieving high utilization rate, resulting in significant underuse of computational resources [28].

To this end, we propose the **P**rogrammable **L**ong-context **E**fficient **N**eural **A**ccelerator (PLENA), an efficient transformer model accelerator system designed to maintain high utilization of GEMM units across all inference stages (prefilling and decoding), particularly for agnetic LLM inference tasks with large contexts. PLENA achieves high efficiency for long-context inference by exploring three optimization pathways across both hardware and software design spaces: i) a flattened systolic array architecture tailored to *fat GEMM* (large inner dimension K); ii) a set of quantization methods with mixed data types and precisions to address both memory wall challenges; and iii) a set of custom instructions (the PLENA_ISA) that contain native FlashAttention support [16].

Figure 2 shows how these three pathways together can **increase the utilization** compared to the conventional square-shaped GEMM hardware without any optimization. First, our novel flattened systolic-array optimization (*Pathway 1*) achieves a higher attainable compute utilisation. The (M, K, N) matrix multiplication typically has $N \ll K$ because of the memory capacity wall.[2] Our flattened systolic array thus brings a more effective utilization of the multiplication resources, as illustrated in Figure 2(a) and Figure 2(b). Second, we apply an *asymmetric quantization strategy* (*Pathway 2*), where Weights(W)/Activations(A)/KV Cache(KV) can be set to different arithmetic widths and precisions to

[1] 64×64 square-shaped systolic array and 8×512 flattened systolic array. Data derived from 144 GB HBM capacity and 512 GB/s memory bandwidth.
[2] All KVs must be stored, so the batch size (the N dimension) is kept lower than the hidden size (K). While various offloading techniques are available [4], they complicate system-level trade-offs and tend to make the system more memory I/O–bound.



(a) PLENA achieves higher utilization than the standard square systolic array(same resources).

(b) PLENA's optimization pathways—(1) a flattened systolic array and (2) asymmetric quantization—together achieve improved effective memory bandwidth utilization and help reduce memory capacity limitations.

Figure 2: A comparison of attainable FLOPs between a square-shaped systolic array (e.g. TPUs) and PLENA's when using the same number of multipliers for running LLaMA3.3 (70B, 128K context)[1]. PLENA's optimization pathways yield higher attainable FLOPS.

address both memory bandwidth and capacity limitations. With more aggressive W and KV cache quantization such as $W_{mxint4}, A_{mxint8}, KV_{mxint4}$, we free up more space in HBM for data scaling (e.g., larger batch sizes). We strategically integrate and enhance state-of-the-art (SOTA) optimization schemes for quantization, incorporating techniques such as micro-scaling [56], output-norm-guided Hessian-based iterative optimization [22], and selective rotation [6]. Our final quantization results demonstrate SOTA performance, effectively reducing limitations related to both memory bandwidth and capacity. Finally, we design and implement PLENA with a custom ISA to have native support for FlashAttention (*Pathway 3*), since Figure 1(b) shows that attention dominates at longer context lengths. We present a novel approach for effectively supporting FlashAttention on systolic-array-based architectures that avoids excessive off-chip memory I/O during attention. Together, these three optimizations yield significantly higher utilization than conventional square-shaped systolic-array accelerators. The main contributions of our work are as follows:

- We analytically characterize the bandwidth and capacity memory walls in agentic LLM inference and show that existing systolic-array accelerators are normally under-utilized when running this workload.
- We introduce three optimization pathways that jointly address the under-utilization caused by memory walls: (i) a flattened systolic array architecture; (ii) an asymmetric quantization scheme with mixed data types and precisions; and (iii) native support for FlashAttention.
- We present PLENA, a complete hardware–software system that realizes the above optimizations. It comprises (i) a custom instruction set (PLENA_ISA) for large Transformer inference; (ii) a PyTorch-to-PLENA_ISA compiler; (iii) an HBM-enabled transaction-level simulator; (iv) an automated, accuracy aware design space exploration (DSE) flow; and (v) a full RTL implementation. We demonstrate that PLENA supports different SOTA transformer model variants (e.g., GQA, MHA and MLA [43], Dense and MoE [5]). We also show that PLENA achieves SOTA energy efficiency for agentic LLM inference tasks – it achieves *2.24*× higher throughput than A100 GPUs on *3.85*× higher throughput than v6e TPU. The overall PLENA system is illustrated in Figure 10, and the entire system will be fully open-sourced upon acceptance.

2 Background

2.1 Model Quantization

Quantization compresses LLMs by mapping high-precision floating-point parameters $\mathbf{X}$ into lower-bit representations. Following the standard integer quantization definition [47], we formalize the process over the arbitrary target data format under a single-level scaling scheme using three elements: the *data format* (τ), the *scale factor* (s) and the *zero point* (z).

A data format is defined as a tuple $\tau = (d, b)$, where d denotes the numerical datatype and b is the bit-width specifying its precision. For a datatype τ the values it can represent are restricted to a finite interval. We denote this interval as the representable set:

$$\Omega(\tau) = \{\, x \in \mathbb{R} \mid \min_{\tau} \le x \le \max_{\tau} \,\}, \tag{1}$$

with $\min_\tau$ and $\max_\tau$ as the representable bounds. The scale factor s maps the dynamic range of $\mathbf{X}$ into $\Omega(\tau)$, typically defined as:

$$s = \frac{\max(\mathbf{X})}{\max_{\tau}}, \tag{2}$$

while the zero-point z shifts the range for alignment (with $z = 0$ in symmetric quantization). Quantization then maps $\mathbf{X}$ into the target format as:

$$X_\tau = \mathrm{clip}\left(\mathrm{RTN}\left(\frac{\mathrm{X}}{s}\right) + z, \min_{\tau}, \max_{\tau}\right), \tag{3}$$

where $\mathrm{RTN}(\cdot)$ denotes round-to-nearest. To approximate the original tensor, the quant–dequant operator is:

$$Q(\mathbf{X}; s, \tau) = s(X_\tau - z). \tag{4}$$

In Equation 3, values exceeding the representable range are clipped, introducing the clipping error. In this work, we address this with a novel adaptive clipping search, described in Section 4.2.

As the tensor size grows, the probability of having these outliers increases, widening the dynamic range and amplifying clipping error. Prior work mitigates this by varying the granularity at which scale and zero-point parameters are shared: from per-tensor, to per-channel, and to vector-wise schemes. In this work, we adopt block-wise micro-scaling datatypes (MXINT and MXFP), with both software and hardware implementation to support our dataformat-aware co-design, which we defer in Section 4.2.

Table 1: A Comparison of LLM accelerators: most lack cycle-accurate simulators for RTL-level timing, omit accurate HBM simulation in evaluation, are constrained by a lack of an ISA with compiler support, and accelerate only a subset of kernels — resulting in restricted flexibility, the need to offload to GPUs/CPUs and frequent host-device transfers and significant data-movement overheads.

	PLENA	PICACHU [53]	MicroScopiQ [54]	FlightLLM [73]	Tender [36]	FIGNA [31]	SystolicAttention [38]	Olive [25]
Simulator	L3	L1	L2	L1	L1	L1	L1	L1
Custom ISA & Auto Code Gen	✓	✓	✗	✓	✗	✗	✗	✗
DSE	✓	✗	✗	✗	✗	✗	✗	✗
FlashAttention support	✓	✗	✗	✗	✗	✓	✗	✗
Full inference coverage*	✓	✗	✗	✓	✓	✗	✗	✗
Open source	✓	✗	–	✗	–	✗	✗	✗

L1: functional simulator; L2: cycle-accurate simulator; L3: cycle-accurate simulator with HBM enabled.
–: partial or planned open-source. Full inference coverage*: all Transformer computations executed on-accelerator.

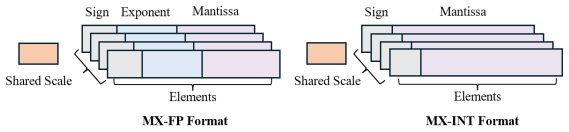


Figure 3: A typical setting of the MX data formats in this design. A scale is shared by a group of elements. Scale is in power of two quantization and elements can be quantized to integer or minifloat.

Additionally, quantization approaches generally fall into two categories: *quantization-aware training* (QAT), which integrates quantization during fine-tuning, and *post-training quantization* (PTQ), which applies quantization directly to a pretrained model. Our PTQ method achieves accuracy competitive with full-precision baselines, even under aggressive low-bit, full-system quantization, as demonstrated in Table 3.

Microscaling. Microscaling (MX) data formats, proposed in prior work [56], define a standardized format that enables block-wise scaling sharing. These formats support multi-level scaling schemes. We adopt only the level-1 scaling strategy, as illustrated in Figure 3. The scaling factor in the MX format can be computed similarly to Equation (2), after which it is quantized using power-of-two (PoT) quantization. The data elements in MX formats can be represented either as integers or as minifloats. In our design, we include both representations in the search space to evaluate software performance.

Quantization Comparison. In long-context scenarios, KV cache size is a key challenge [76], but hardware support for efficient quantization of KV cache remains limited [25, 54]. Existing frameworks often treat quantization in isolation rather than as part of full-system design, leaving gaps in non-GEMM operations and causing a mismatch between algorithmic advances and practical deployment on hardware.

2.2 FlashAttention

FlashAttention optimizes memory I/O in the standard attention layer [16]. In a standard attention layer, computing $QK^\top$ produces a prohibitively large square matrix, often thousands by thousands in size. Because on-chip memory cannot hold this intermediate result, it must be written to off-chip memory and later reloaded for the subsequent softmax and PV steps, which significantly degrades performance. FlashAttention avoids this round trip by tiling and fusing the attention computation (GEMM–Softmax–GEMM) so that all intermediate results fit on-chip.

3 PLENA Hardware System

The overall configuration of PLENA is shown in Figure 4. It is designed to support instruction-level pipelining and mainly consists of three compute units: the Matrix Unit, the Vector Unit, and the Scalar Unit. All units are highly configurable, supporting multiple data types and precisions, enabling the application of different quantization methods to the accelerator. PLENA also includes two main on-chip SRAM blocks. The Vector SRAM acts as a scratchpad for computation, storing frequently used data such as activations, which do not need to be written back to HBM, thereby reducing memory access overhead. The custom Matrix SRAM is dedicated to loading weights and KV tensors and supports reading data in either transposed or untransposed layouts with no additional overhead.

3.1 Hardware Support for Asymmetric Arithmetic Types

To support asymmetric quantization strategies (Section 4.1), PLENA natively offers multiple numeric formats—covering different data types and precisions—across its compute and memory units (Table 14). This innovative *asymmetric* data-handling configuration has the following characteristics:

(i) Activations are stored in a high-precision floating-point (FP) format on-chip in the Vector SRAM, as they are more sensitive to quantization errors than KV or weights. (ii) KV and weights, being less accuracy-sensitive, can be more aggressively quantized and staged in the Matrix SRAM using lower-precision MX formats (MX-FP or MX-INT). (iii) An optional on-chip rotation step can suppress outliers before quantization to preserve accuracy.

Figure 5 illustrates the precision formats used by each unit and the dataflow between them. When appending newly computed K and V to the KV cache, we optionally apply a

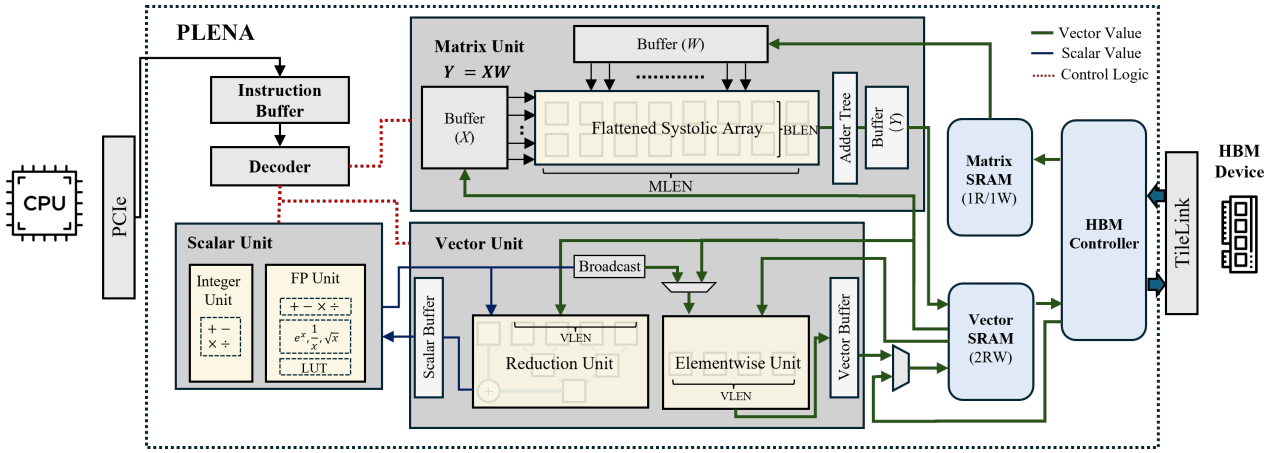


Figure 4: PLENA architecture overview. Execution is controlled by the decoder's system-pipeline controller, which derives control signals from decoded instructions and monitors memory dependencies. For example, if the current instruction needs to read from a Vector SRAM row that is still being updated by the vector or matrix unit, the controller inserts a stall to ensure correctness. Vector SRAM acts as the on-chip scratchpad, providing data to the matrix and vector units and accepting their results.

selective rotation (Hadamard transform) to suppress outliers before quantizing to MX-INT. Because K and V are consumed only by the attention layer's GEMM, they are loaded exclusively into the Matrix SRAM. Before use, the matrix unit applies the inverse Hadamard transform to de-rotate K and V. These rotation/de-rotation stages can be selectively applied per tensor; for example, weights loaded into the matrix unit bypass the inverse transform.

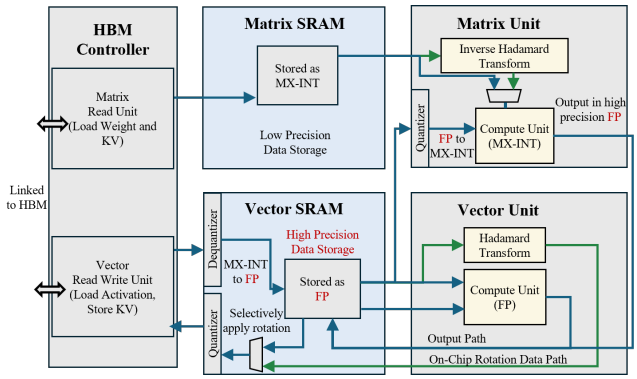


Figure 5: Asymmetric-precision datapath example. Vector SRAM stores FP4 values, whereas Matrix SRAM stores MX-INT4 values. Green paths denote the selective rotational quantization flow: a fast Walsh–Hadamard transform is applied, with its inverse used to map back [51]. Blue paths indicate the data flow for the remaining computation.

3.2 Computational Units

All compute units are optimized for feed-forward (FFN) and attention computations in transformer inference, with particular emphasis on long-context workloads. As shown in Figure 2(b), long-context workloads frequently involve *fat GEMMs*, where the batch-related dimension (typically M in $(M, K) \times (K, N)$) is much smaller than the others, resulting in uneven matrix shapes (Figure 6). The reduction dimensions K tend to be very long. For example, the weight–activation GEMM reduces over the model's hidden size (e.g., 4,096 for LLaMA-8B and 8,192 for LLaMA-70B). In addition, a variety of arithmetic operations—such as elementwise addition, summation, and special functions like the exponential—are required across long-dimension tensors.

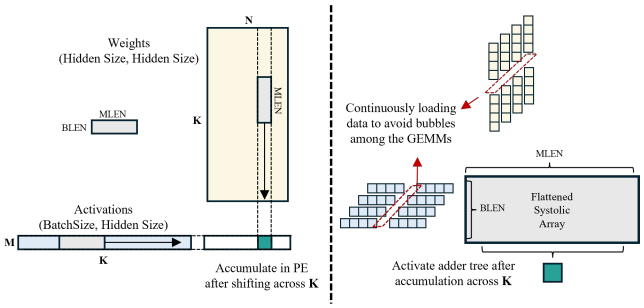


Figure 6: Processing flow for the weight–activation GEMM. Because memory capacity constrains batch size, the M dimension remains small. Setting BLEN = M on the flattened systolic array yields near-100% utilization.

Matrix Unit. To optimize GEMM in long-context workloads involving *fat GEMMs*, we propose flattened systolic arrays, enabling higher utilization across the entire *fat GEMM* computation flow. The unit computes a (BLEN, MLEN)×(MLEN, BLEN) GEMM and produces results of shape (BLEN, BLEN), and normally BLEN is set to be much smaller than MLEN to match the workload characteristics of long-context LLM inference.

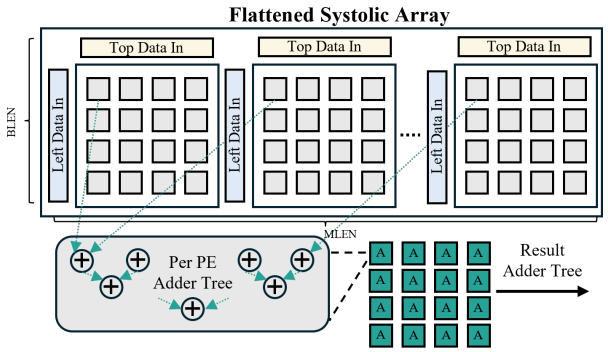


Figure 7: The flattened systolic array is composed of a series of smaller square-shaped systolic arrays arranged in a row to form the desired *fat GEMM* shape. Each receives inputs distributed from the MLEN vector buffers W and X, as shown in Figure 4.

This flattened systolic array is designed for output-stationary dataflow in order to maintain high utilization and avoid frequent reads/writes of partial sums—and the bubbles associated with streaming operands into the systolic array. As shown in Figure 6, operands stream along the large reduction dimension K while partial sums remain resident in the PEs. The array is fully pipelined, eliminating bubbles between consecutive GEMM tiles.

The microarchitecture of the flattened systolic array is shown in Figure 7. It is built from a series of small square-shaped systolic arrays (*sub-arrs*), each consisting of a grid of processing elements (PEs). Each PE repeatedly performs multiply–accumulate operations and passes data to its neighboring PEs below and to the right across the array. As described in Section 3.1, the systolic array is designed to natively accept data in the MX format. The detailed PE configuration is provided in the Figure 13.

On each cycle, the flattened systolic array fetches two MLEN-wide inputs, one from the Matrix SRAM (top) and one from the Vector SRAM (left). These inputs are buffered and reordered, then partitioned into MLEN/BLEN vectors (assuming MLEN is divisible by BLEN), each of length BLEN. Each vector is then fed to a corresponding *sub-arrs* from the top and left direction.

However, a matrix unit composed solely of *sub-arrs* is insufficient to complete a $(\texttt{BLEN}, \texttt{MLEN}) \times (\texttt{MLEN}, \texttt{BLEN})$ GEMM. Each array accumulates only partial sums for a fragment of the final result; producing a complete $(\texttt{BLEN}, \texttt{BLEN})$ output requires a cross-array reduction that sums the partial sums held in the PEs across the tiled row. To address this, we integrate an output adder tree (see Figure 7) that performs the cross-array summation efficiently. This unit is invoked via a dedicated instruction, as only one cross-array summation is required when computing GEMM along the large reduction dimension. This could prevent bubbles and improve computational efficiency.

Vector Unit. This unit supports all vector operations required during LLM inference, including elementwise computations (e.g., addition, multiplication, and exponential) and reduction operations (e.g., summation, maximum). The vector dimension is parameterised by VLEN. A complete list of vector-unit instructions is provided in Table 12.

Scalar Unit. The scalar unit has two separate ALU units supporting the two data types of computations: Integer (INT) and Floating Point (FP). Both the INT and FP units are connected to their respective SRAMs and register files and operate independently.

INT operations are used primarily for on-chip address generation and indexing, and run on a control path decoupled from the FP datapath. In contrast, the FP unit implements basic arithmetics and the non-linear functions required by transformer workloads (e.g., exponential, reciprocal, and reciprocal square root (rsqrt)). To accommodate future models that may require additional special functions, we also include a look-up table (LUT) unit so new functions can be realized via table lookups without introducing additional logic.

3.3 Memory System

Our memory system is characterized by two key properties:

- Support for asymmetric precisions, variable-length memory transfers, and strided loads/stores to HBM.
- Latency hiding for HBM accesses via a hardware prefetcher, enabling high bandwidth utilization.

To make more effective use of HBM capacity, as discussed in Section 3.1, all data stored in HBM is kept in MX format. However, due to address alignment constraints, it is impractical to concatenate each data block with its associated per-block scales. This is because the resulting combined size seldom matches a (2^n) multiple, making it inefficient for the memory system.

To address this problem, we store the blocks and their scales separately – laying out all blocks contiguously, followed by the corresponding scales at the end of the block region. With this technique, the memory address alignment is preserved while locality is maintained. The resulting layout is shown in Figure 8.

To support variable-length transfers, the HBM controller integrates two data-packing units. MX-format blocks fetched via TileLink [62] (the on-chip interconnect used to access the HBM controller) are repacked into (i) MLEN-wide vectors for the Matrix SRAM and (ii) VLEN-wide vectors for the Vector SRAM. The controller automatically locates and fetches the corresponding per-block scales based on the active precision and the requested transfer size. On the write path, dedicated units accept vectors from the Matrix and Vector SRAMs, partition them into MX blocks, attach the appropriate per-block scales, and commit the aligned layout back to HBM.

The loading logic is critical to help us fully utilize the HBM memory bandwidth. The hardware load unit resides in both

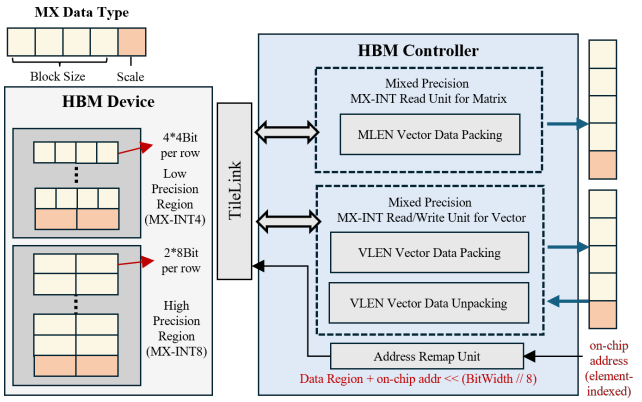


Figure 8: Data layout and interaction in HBM. Data of different precisions can be stored simultaneously according to the defined storage pattern in HBM. Strided load and store operations are managed by the address remap unit, which generates and passes strided addresses to the TileLink channel.

the Matrix and Vector SRAMs and is connected directly to the HBM controller. This enables background fetching and streaming into each SRAM while the rest of PLENA executes other instructions, sustaining full utilization of the matrix unit and avoiding stalls on HBM accesses. The two load units are controlled directly by instructions, with the amount of data to be load encoded in each instruction. For example, during weight–activation GEMMs, where GEMM operations are invoked repeatedly while streaming data across the hidden dimension, the loaded amount is set to this dimension, so the load instruction only needs to be issued once.

3.4 PLENA ISA

Our customized ISA is designed to cover all operations required for transformer inference. The instructions are structured to balance efficiency with flexibility and are built to support multiple transformer-based models and computation optimizations. In addition to FlashAttention, the ISA also supports different transformer variants, such as MHA, MLA [43], and MoE [5]. A brief summary is provided in Table 11, with the detailed specification given in Table 12.

To achieve the efficiency and flexibility balance, the ISA is designed to minimize overhead while maximizing utilization of compute and memory resources. This is achieved through features such as tile-level scheduling, which enables fine-grained control of computation and memory instructions at the tile granularity. Furthermore, the ISA defines dedicated instruction classes (Matrix, Vector, Scalar, Memory, and Control) that decouple responsibilities, simplify scheduling, and allow flexible mixing across different computation types.

The instructions (32bits per instr) are dynamically passed from the CPU to the instruction buffer via PCIe. The scalar unit contains an integer register file storing on-chip addresses. Vector- or matrix-related instructions control reads and writes to the matrix and vector SRAMs using the specified integer registers. Simple arithmetic operations in the scalar unit are used for address manipulation.

3.5 Flash Attention

Most current accelerators cannot execute FlashAttention natively because (i) they expose only GEMM primitives and lack in-line, row-wise reductions and nonlinear operations (`max/sum`, `exp`, `div`) required for the online softmax; (ii) they lack memory-layout support such as transpose-on-read and efficient strided/blocked streaming; and (iii) they rely on rigid ISAs with fixed scheduling and coarse-grained kernel boundaries, preventing tile-by-tile flexible execution.

In PLENA, we address (i) with tightly coupled vector and scalar units that implement the required reductions and elementwise operations; the vector unit's width is configurable to match the tile dimensions used by FlashAttention. For (ii), we introduce a *Matrix SRAM* that can be read in either standard or transposed order without extra data movement. In the $QK^\top$ step, explicitly transposing large tiles on the fly is costly in area, energy, and latency, and storing $K^\top$ in HBM is impractical because it complicates appending new K vectors to the existing K cache during decoding. The Matrix SRAM avoids both issues by banking the storage across multiple sub-SRAMs and using lightweight address remapping to present a transposed view at read time (implementation details in Figure 12). For (iii), our custom ISA offers composable, fine-grained control that enables persistent, tile-by-tile scheduling of the fused attention pipeline. This allows each operation in FlashAttention to be controlled individually at the tile level. Combined with the above capabilities, this allows PLENA to support FlashAttention natively.

4 Quantization

4.1 Asymmetric Quantization

The proposed quantization framework supports a wide range of datatypes and precisions. As shown in Figure 9, to accurately reflect hardware behavior in LLM architectures, the framework must satisfy two key requirements: 1) different operands within the same operation can be quantized to different datatypes and precisions, and 2) all operations in the model must be quantized. Table 2 summarizes existing quantization methods. Most of these approaches focus on GEMMs only, several support mixed precision, while none of them support mixed data types. In contrast, our quantization flow allows both mixed precision and mixed data types in GEMMs, with all intermediate data between GEMM operations quantized.

For GEMM operations (e.g., linear layers and matrix multiplications between activations), the two operands can have two different precisions; e.g., INT4 activations multiplied

Table 2: Comparison of post-training quantization methods for LLMs across key features. (QW, QACT, QKV) denote quantization of weights, activations, and key–value cache, respectively. Each decoder layer in LLaMA contains nine matrix multiplications, as outlined in Algorithm 2. **PLENA** introduces the first accuracy evaluator supporting mixed MX datatypes, providing software emulation for MXINT, MXFP, and MiniFloat formats. Unlike prior approaches, it fully simulates hardware-precision behavior in software, extending quantization beyond matrix multiplications to also include RMSNorm, embedding layers, LM output heads, and nonlinear operations such as RMSNorm, softmax, and SiLU (see Algorithm 2).

	PLENA	MicroScopiQ* [54]	GPTQ[22]	QuaRot[6]	OmniQuant[60]	SmoothQuant[70]	Atom[75]	KiVi[76]	M-ANT[29]
(QW, QACT, QKV)	(✓,✓,✓)	(✓,✓,✓)	(✓,✗,✗)	(✓,✓,✓)	(✓,✓,✓)	(✓,✓,✓)	(✓,✓,✓)	(✗,✗,✓)	(✓,✓,✓)
No. GEMMs	9/9	9/9	7/9	7/9	9/9	7/9	9/9	0/9	9/9
Nonlinear_FN	✓	✗	✗	✗	✓*	✗	✗	✗	✗
Embeddin & lm_head	✓	✗	✗	✗	✗	✗	✗	✗	✗
RMSNorm	✓	✗	✗	✗	✗	✗	✗	✗	✗
ROPE	✓	✗	✗	✗	✗	✗	✗	✗	✗
Supported datatypes	MXFP, MXINT, MiniFloat	MXFP, MXINT	INT	INT	INT	INT	INT, FP	INT	MANT
Mixed-precision	✓	✓	✗	✓	✓	✓	✓	✗	✓

✓* denotes partial quantization support ; * At the time of writing, MicroScopiQ has not yet released its code; the comparison is based on information obtained directly from the authors.

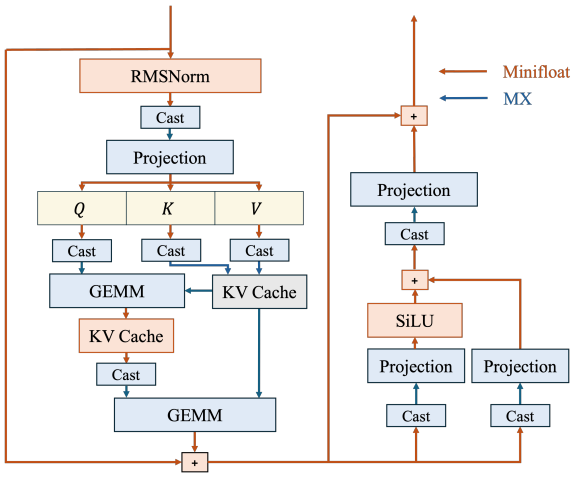


Figure 9: A dataflow graph of LLM workloads in PLEANA. The blue lines indicate data represented in MX datatypes, and the orange lines indicate minifloat datatypes. The GEMM and projection layers are executed on the PLENA matrix unit, which takes inputs in MX and produces outputs in minifloats. All other operations are executed on the vector unit in minifloats.

with INT8 weights. The operands may also use two different datatypes, e.g., MXFP activations multiplied with MXInt weights. Besides, the GEMM operation also models the behaviour that the output will be casting to minifloat. For non-GEMM operations, which are executed on the vector machine in hardware, the data is stored as minifloats. When data flows from a non-GEMM operation to a GEMM, a cast module is required to convert minifloats to the corresponding target formats, and this is also modelled in the quantization framework. Beyond this basic setup, we adopt and refine advanced quantization tactics for a more aggressive quantization scheme than plain casting, including Hessian-based quantization optimization (GPTQ) and selective online activation rotation (QuaRot).

4.2 Fusing Output-Guided Blockwise Clipping into GPTQ

GPTQ was initially designed for integer quantization. When adapting GPTQ for MXFP/MXINT, we observe that the clipping range within each microscaling block significantly affects overall model performance. To address this problem, we propose a blockwise clipping range search method that minimizes the quantization error of each output block.

Algorithm 1 outlines the quantization process of PLENA. PLENA uses per-microscaling-block quantization error to guide the search of the clipping range, and fuses this clipping range optimization into GPTQ's iterative error propagation. This also mitigates the outlier problem of weights, which later on affects the value of the shared exponents in MX format, and eventually enables a better end-to-end model performance.

Formally, let $\mathbf{X} \in \mathbb{R}^{M\times K}$ be the inputs for calibration, and $\mathbf{W} \in \mathbb{R}^{N\times K}$ the layer weights. Given a linear layer $\mathbf{Y} = \mathbf{X}\mathbf{W}^\top$, slice the weights across the K dimension with the block size B (i.e., MLEN in Figure 6) defined in our MX data format τ, yielding $\mathbf{W}_b \in \mathbb{R}^{N\times B}$ to be quantized. We also slice activations across the K dimension with the same block size, giving $\mathbf{X}_b \in \mathbb{R}^{M\times B}$. Let $\textsc{Quantize}(\cdot; p, \tau)$ denote per-row quantization in data format τ with clipping percentile p. For each row $i = 1, \ldots, N$, we search for the percentile by

$$p_i^\star = \arg\min_{p\in\mathcal{P}} \left\| \mathbf{X}_b \left(\mathbf{W}_{i,\,b:b+B-1} - \textsc{Quantize}(\mathbf{W}_{i,\,b:b+B-1}; p, \tau) \right)^\top \right\|_2^2 \quad (5)$$

and get the quantized weight block:

$$\mathbf{Q}_{i,\,b:b+B-1} = \textsc{Quantize}\left(\mathbf{W}_{i,\,b:b+B-1}; p_i^\star, \tau\right). \quad (6)$$

We now detail the per-block clipping search, following the quantization definitions in Section 2.1, consider a block of weights w_τ in data format τ, with representable range $[\min_\tau, \max_\tau]$ and empirical weight range $[x_{\min}, x_{\max}]$. Directly mapping the full weight range usually wastes precision due to extreme outliers. To mitigate this, we introduce a *clipping parameter* $p \in \mathcal{P} \subset [0.5, 0.99]$, which shrinks the

Algorithm 1 PLENA L2-Norm-Guided Hessian-Based Weights Quantization

Require: full-precision weight matrix $\mathbf{W} \in \mathbb{R}^{N\times K}$
Require: calibration activations $\mathbf{X} \in \mathbb{R}^{M\times K}$
Require: block size B (i.e., MLEN) defined in our MX data format τ
Require: percentile set $\mathcal{P}$, target format τ
Ensure: quantized weight matrix $\mathbf{Q}$; block quantisation errors $\mathbf{E}$

Initialize quantized weights $\mathbf{Q} \leftarrow \mathbf{0} \in \mathbb{R}^{N\times K}$
Initialize quantisation errors $\mathbf{E} \leftarrow \mathbf{0} \in \mathbb{R}^{N\times B}$
$\mathbf{H}^{-1} = (2\mathbf{X}\mathbf{X}^\top + \lambda\mathbf{I})^{-1}$
$\mathbf{H}^{-1} \leftarrow \text{Cholesky}(\mathbf{H}^{-1})^\top$
for each block $b = 0, B, 2B, \ldots, K-1$ **do**
  $b_2 \leftarrow \min(b{+}B,\ K)$
  $\mathbf{W}_b \leftarrow \mathbf{W}_{:,b:b_2}$ ▷ Extract weight block
  $\mathbf{X}_b \leftarrow \mathbf{X}_{:,:,b:b_2}$ ▷ Extract activation block
  Initialize $\mathbf{Q}_b^{\text{best}} \leftarrow \mathbf{0}$, $\boldsymbol{\epsilon}^{\text{best}} \leftarrow \infty$
  for each candidate percentile $p \in \mathcal{P}$ **do**
    $\widetilde{\mathbf{W}}_b \leftarrow \textsc{Quantize}(\mathbf{W}_b, p, \tau)$; $\boldsymbol{\epsilon} \leftarrow \left\|\mathbf{X}_b\mathbf{W}_b^\top - \mathbf{X}_b\widetilde{\mathbf{W}}_b^\top\right\|_2^2$
    $\mathbf{mask} \leftarrow \boldsymbol{\epsilon} < \boldsymbol{\epsilon}^{\text{best}}$
    $\mathbf{Q}_b^{\text{best}}[\mathbf{mask}, :] \leftarrow \widetilde{\mathbf{W}}_b[\mathbf{mask}, :]$; $\boldsymbol{\epsilon}^{\text{best}}[\mathbf{mask}] \leftarrow \boldsymbol{\epsilon}[\mathbf{mask}]$
  $\mathbf{Q}_{:,b:b_2} \leftarrow \mathbf{Q}_b^{\text{best}}$; $\boldsymbol{\Delta}_b \leftarrow \mathbf{W}_b - \mathbf{Q}_b^{\text{best}}$; $\mathbf{d}_{bb} \leftarrow \text{diag}(\mathbf{H}^{-1}_{b:b_2,\,b:b_2})$
  $\mathbf{E}_b \leftarrow \boldsymbol{\Delta}_b\,\text{diag}(\mathbf{d}_{bb})^{-1}$; $\mathbf{W}_{:,\,b_2:} \leftarrow \mathbf{W}_{:,\,b_2:} - \mathbf{E}_b \cdot \mathbf{H}^{-1}_{b:b_2,\,b_2:}$

effective range to $[p\,x_{\min},\ p\,x_{\max}]$. We then adopt the symmetric quantization setting with zero-point fixed at $z = 0$, the corresponding scale factor is

$$s(p) = \frac{p x_{\max}}{\max_\tau}. \tag{7}$$

The blockwise quant–dequant operator then becomes

$$\widehat{w}(p) = s(p)\ \text{clip}\Big(\text{RTN}\Big(\tfrac{w}{s(p)}\Big),\ \min_\tau,\ \max_\tau\Big). \tag{8}$$

where RTN denotes round-to-nearest MX numbers.

By sweeping over a discrete candidate set $\mathcal{P}$ of clipping parameters, we evaluate multiple effective ranges and select the p per block that minimizes the output reconstruction loss defined in Equation (5).

4.3 Selective Online Activation Rotation

As shown in prior work, activations in LLMs typically contain more outliers than weights [37], therefore more sensitive to quantization. QuaRoT [6] recently demonstrated that applying a rotation matrix to LLMs can effectively suppress outliers. However, we observe that rotating all tensors suggested by QuaRoT may not yield the best performance for MX formats. When a tensor (e.g., the weight matrix) does not exhibit significant outliers, the benefit of rotation diminishes. Equation (9) is a simplified rotation mechanism in QuaRot [6], where a Hadamard matrix $\mathbf{H}$ smooths out the activation distributions, and its inverse is fused into weights. We performed experiments to empirically identify the activation tensors with extreme outliers and propose a selective online rotation scheme.

We notice that applying the rotation to finer-grained weight quantization (e.g., MXInt with smaller block sizes) may increase perplexity. Intuitively, weights have smaller dynamic ranges compared to activations. The rotation may be unnecessary since most weight outliers are effectively captured by the shared exponents, while permuting the weights with $\mathbf{H}$ leads to different quantized values, which may impact the model performance.

$$\mathbf{Y} = \text{Quantize}(\mathbf{X}\mathbf{H}) \cdot \text{Quantize}(\mathbf{H}^{-1}\mathbf{W}) \tag{9}$$

To address the issue that weight with fine-grained blocking does not need rotation, we propose an *activation-only rotation* strategy. As shown in Equation (10), the inverse rotation matrix H^{-1} is decoupled from weight quantization and is instead applied directly to the quantized rotated activation at runtime.

$$\mathbf{Y} = \text{Quantize}(\mathbf{X}\mathbf{H}) \cdot \mathbf{H}^{-1} \cdot \text{Quantize}(\mathbf{W}) \tag{10}$$

The activation distribution varies significantly across layers. Consequently, the effect of rotation also differs from layer to layer. Rather than rotating all activations, we apply the rotation matrix *selectively*. A search is performed to identify the layers where rotation yields the greatest benefit. This selective activation rotation is performed on-the-fly (the green paths in Figure 5). The ablation of the above quantization modifications is shown in Table 8.

5 PLENA Software Tooling

As discussed in Table 1, existing works lack several key components necessary to achieve complete end-to-end LLM inference. Some of these missing elements include a compiler, a simulator, and design-space exploration tools. In contrast, PLENA features a complete design and verification framework that allows it to rapidly adapt to new models or even new hardware accelerators and optimize for them. We also anticipate that future accelerators in the field could reuse certain components of this comprehensive framework to establish end-to-end performance comparisons.

5.1 Compiler

To efficiently deploy decoder-style LLMs, we design a compiler stack targeting only LLM models on our PLENA hardware. The models are first exported from the PyTorch framework into the ONNX format [7], where standard graph optimizations such as constant folding are applied. The optimized graph is then parsed into our custom IR through pattern matching, this essentially lowers high-level operators into primitives such as GEMM, quantization, dequantization, and FlashAttention.

The critical challenge lies in searching for an optimal scheduling strategy tailored to PLENA. Our scheduling policies include operator fusion, tiling configurations, memory

placement, and loop transformations, which jointly determine data reuse, memory traffic, and compute unit utilization. To accelerate the search, we systematically traverse candidate configurations and validate them by checking memory footprint constraints and transaction requirements. Feasible candidates are further evaluated by a lightweight roofline-based performance model, and finally, the top-K schedules are selected to generate the assembly code for execution on PLENA.

5.2 Cycle-accurate Simulator

Our Rust-based cycle-accurate simulator offers significant advantages over the functional-level simulators used in most published accelerators:

- Supports full cycle-accurate emulation.
- Event-driven simulation that directly executes the generated machine code from the compiler.
- HBM-enabled simulation, incorporating realistic HBM timing and bandwidth characteristics (via Ramulator [42]).

This simulator supports the same data types and precisions as the PLENA accelerator, and we verified that it could generate closely matching results as the RTL simulation for the accelerator.

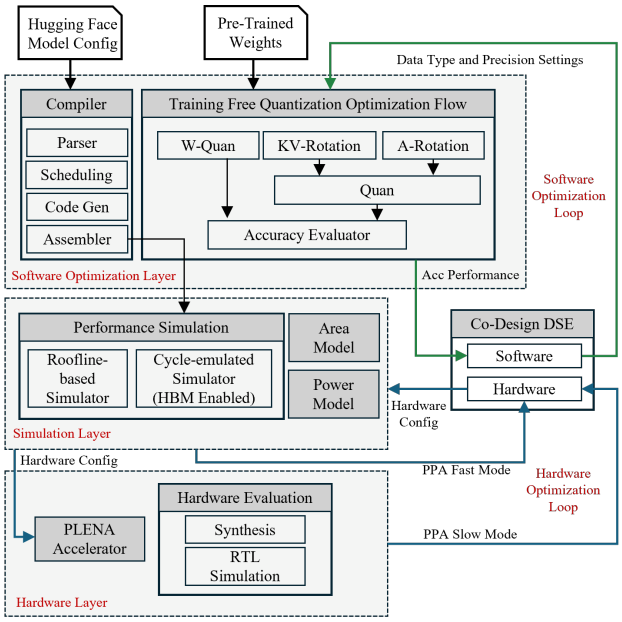


Figure 10: An overview of the open-source PLENA system.

5.3 Hardware-Software Co-Design

To automate finding optimal hardware design and quantization parameters, we propose to employ active learning for design space exploration (DSE). We also provide capability for investigating the trade-offs between optimizing different objectives, such as maximizing accuracy, while minimizing latency and area. For this, we employ multi-objective Bayesian optimization (BO), which allows exploring the Pareto frontier in an active manner.

BO is a framework for optimising non-differentiable functions [59]. Multi-objective BO searches for optimal points in the design space that minimize a multi-objective function $\mathbf{f}$, i.e. $\mathbf{f}(\mathbf{x}_*) = \min_{\mathbf{x}} \mathbf{f}(\mathbf{x})$. In our case, the objective function has three components: perplexity, latency, and chip area: $\mathbf{f} = \left[f_p(\cdot), f_l(\cdot), f_a(\cdot)\right]$. $\mathbf{f}$ is modelled with a multi-output Gaussian Process, which keeps track of the predictive mean and uncertainty for all points $\mathbf{x}$ in the design space. BO selects which candidate to evaluate next, such that uncertainty is reduced globally, but also comes back to regions with high predictive mean to further improve upon the previous points with favorable outcomes. BO scales to high-dimensional spaces [40, 66], supports both discrete and continuous search variables [9, 17, 19], and doesn't impose limiting restrictions on the properties of the objective $\mathbf{f}$. Its model of the global posterior also facilitates interpretable analysis of the search results. Hence, this setup yields a flexible and informative framework for automating DSE.

We base our DSE implementation on the Optuna package [3] and conduct experiments with a BOTorch sampler and a tree-search sampler. With BOTorch [9] sampler we treat the design space as continuous during posterior modelling, but discretize the points proposed by BO for evaluating concrete design choices. We also test an alternative of using the Tree-Structured Parzen Estimator [68], often used for discrete spaces.

In our co-design setup, we incorporate post-training quantization directly into the optimization loop. This allows us to evaluate candidate hardware and quantization configurations jointly, using pre-trained model weights while searching over quantization parameters such as datatype and precision settings for activations and KV cache. The joint search space is defined in Table 14. For each candidate design, we assess *accuracy*, *latency*, and *area*:

- Accuracy is measured in terms of language modeling quality, where we evaluate perplexity on Wikitext2 using our accuracy evaluator.
- Latency and area utilization are obtained from our Roofline-based simulators, as illustrated in Figure 10.

To ensure efficient exploration, we impose input constraints over the design space (Table 15) and apply rejection sampling to discard invalid or infeasible candidates. This avoids unnecessary costly objective evaluations and accelerates convergence of the search. We first conduct experiments on LLAMA3.2-1B to enable rapid iteration, and then extend our evaluation to LLAMA-3-8B. The results are described in Section 5.3.

6 Evaluation

6.1 Experiment Setup

Models and Datasets. We evaluate our quantization framework on mainly two families of LLMs, namely LLaMA-2 [64] and LLaMA-3 [45]. We also demonstrate our system on MoE (eg. GPT-OSS) and MLA-based (QWen-MLA) models. Quantization performance is measured in terms of perplexity on the WikiText-2 dataset [44]. The entire quantization process requires approximately 2–20 GPU hours on NVIDIA H100 GPUs, depending on the model size and configuration.

Quantization Baselines. We compare against several state-of-the-art quantization methods, including software-based approaches such as GPTQ [22], OmniQuant [61], and QuaRoT [6], as well as hardware-accelerated approaches such as Atom [75] and MicroscopiQ [54].

Accelerator Implementation. PLENA is implemented in SystemVerilog RTL. We perform synthesis using Synopsys Design Compiler with the 7 nm OpenROAD predictive process design kit [13] to generate area and power estimates under a 1 GHz clock frequency.

Accelerator Baselines. Since the works we selected for comparison, MicroscopiQ [54], FIGNA [31], and Olive [25], are not open-source and were not evaluated using the same technology node or toolchain, we re-implemented their core components and integrated them into the PLENA system for a fair inference performance comparison. Additionally, DeepScale [58] is used for overall system performance estimation, scaling all designs to the 7 nm process. Their detailed area and power of the core units are evaluated using our own implementations.

Inference Process. Instead of comparing only with SOTA accelerators, we also evaluate against the latest high performance commercial compute units, including GPUs (A100 80G) and TPUs (v6e-8). The GPU experiments are conducted in an environment with Ubuntu 22.04, CUDA 12.8, Python 3.11, PyTorch 2.8.0, and vLLM 0.10 V1. The TPU experiments are conducted in an environment with v2-alpha-tpuv6e software and vllm\vllm_tpu docker image.

6.2 Quantization

Quantization Comparison. We evaluate our quantization method against related work; results are summarized in Table 3. For a fair comparison, we first match prior settings by quantizing only the nine GEMMs in the Llama decoder. We then report full-system experiments that also quantize nonlinear functions, RoPE, and embeddings in table 4. In the W4A4KV16 setting, our results outperform all related work. For Llama-3-8B, compared with prior approaches, our method achieves at least a 1.24 reduction in perplexity. The key contributions to this performance improvement come from three aspects: 1). **MXInt operation**: While previous work [29] adopts a group size of 32, our design keeps the group size small while still maintaining high hardware efficiency. 2). **Selective rotation**: Our approach searches for the best layer-wise rotation combination for each model. Unlike QuaRoT [6], which merges rotation into weights, we apply online rotation only to specific layers. This provides an additional design space for finding optimal solutions in the PTQ setting. 3). **Clipping strategy:** By integrating *output-guided*, blockwise clipping into iterative weight quantization, we validate that output reconstruction error correlates strongly with end-task performance; consequently, our approach substantially reduces perplexity degradation.

Full System Design. We performed a brute-force sweep to select the vector-core precision. where we find quantizing the remaining operators to a MiniFloat E6M5 format is effectively lossless in perplexity while reducing precision

Table 3: WikiText-2 perplexity (lower is better) under GEMM-only emulation (nonlinear ops left in full precision) for Llama. Results for GPTQ, AWQ, OmniQuant, and Atom are taken from MicroScopiQ; QuaRot numbers are from the paper or reproduced when not reported. W/A/KV denote bit widths for weights, activations, and KV cache.

		LLaMA-2 [64]			**LLaMA-3** [45]	
Method	**W/A/KV**	**7B**	**13B**	**70B**	**8B**	**70B**
Baseline	16/16/16	5.47	4.83	3.31	6.13	2.85
GPTQ [22]	4/16/16	6.23	5.58	4.28	8.12	3.75
AWQ [39]	4/16/16	5.82	5.19	4.08	7.96	3.58
OmniQuant [61]	4/16/16	5.74	5.02	3.47	7.09	3.46
MicroScopiQ [54]	4/16/16	5.65	5.02	3.42	6.89	**3.25**
QuaRot [6]	4/16/16	**5.60**	5.00	3.41	6.52*	3.53*
Ours	4/16/16	5.61	**4.97**	**3.41**	**6.45**	3.59
OmniQuant [61]	4/4/16	11.47	8.32	5.41	10.21	5.30
SmoothQuant [70]	4/4/16	20.47	15.63	17.62	29.54	19.32
Atom [75]	4/4/16	6.16	6.12	5.20	8.12	4.69
MicroScopiQ [54]	4/4/16	6.11	5.57	4.48	8.12	4.65
QuaRot [6]	4/4/16	6.02*	5.36*	3.78	8.00*	6.33*
M-ANT [29]	4/4/16	5.92	5.24	-	-	-
Ours	4/4/16	**5.69**	**5.03**	**3.59**	**6.76**	**4.51**
QuaRot [6]	4/4/4	6.10	5.40	3.79	8.16	6.66
QuaRot-128G [6]	4/4/4	5.93	5.26	**3.61**	7.36	5.51
Ours	4/4/4	**5.89**	**5.18**	3.62	**7.22**	**4.77**

*Note: Results marked with * are reproduced from the authors' released code. Specifically, for the QuaRot 4/4/16 configuration, we follow the experimental setup described in their paper, where activations are per-token symmetric-quantized with a clipping ratio of 0.9.*

Table 4: Quantization results for Llama comparing GEMM-only qunatization with full-system quantization (including GEMM, nonlinear ops, input embeddings, and LM head). Nonlinear operators are simulated in MiniFloat E6M5.

		LLaMA-2 [64]			**LLaMA-3** [45]	
Method	**W/A/KV**	**7B**	**13B**	**70B**	**8B**	**70B**
Baseline	16/16/16	5.47	4.83	3.31	6.13	2.85
Ours	4/4/4	5.89	5.18	3.62	7.22	4.77
Ours-Full System	4/4/4	5.91	5.19	3.63	7.23	4.82

Table 5: System-level comparison across standard (Prompt = 1k, Gen = 128) and agentic (Prompt = 5.6k, Gen = 85k) workloads. For fairness, we use four A100 GPUs with a total HBM capacity of 320 GB as the reference. PLENA and MicroScopiQ are both assumed to have four cores and identical HBM configurations, including capacity and bandwidth. The selected configurations are listed in Table 17. Since the GPU's silicon area includes significant overhead for non-compute functionality, we ensure that the multiplier count is matched across systems for a balanced comparison.

System	LLaMA-3.1-8B				LLaMA-3.3-70B			
	Standard		Agentic		Standard		Agentic	
	TTFT (s)	TPS (×A100)	TTFT (s)	TPS (×A100)	TTFT (s)	TPS (×A100)	TTFT (s)	TPS (×A100)
A100 80G	6.20	1.00×	0.22	1.00×	1.12	1.00×	1.05	1.00×
A100 80G (With Q)*	5.13	1.66×	0.19	1.39×	3.41	1.23×	2.46	1.32×
TPU v6e	5.63	0.90×	4.58	0.39×	50.07	0.31×	7.98	0.84×
MicroScopiQ [54]	16.43	0.35×	3.27	0.57×	61.63	0.16×	19.23	0.09×
PLENA	4.19	**2.24×**	0.21	**1.58×**	5.65	1.19×	1.27	**1.49×**

Note: MicroScopiQ [54] was developed by us, and we deploy its replicated compute unit on the PLENA platform to do the testing. The version of LLaMA-3.1-8B used is `LLaMA-3.1-8B-Instruct-quantized.w8a8`. *With Q* means QuaRot quantization [6].*

Table 6: System-level comparison on GPT-OSS 20B (MoE) [5] and QWen with MLA [43], showing that PLENA can be adapted to new models with both MLA and MoE configurations and achieve higher TPS than A100 80G under the same experimental settings as Table 5.

System	GPT-OSS 20B (MoE)				qwen2.5-7B*			
	Standard		Agentic		Standard		Agentic	
	TTFT (s)	TPS (×A100)	TTFT (s)	TPS (×A100)	TTFT (s)	TPS (×A100)	TTFT (s)	TPS (×A100)
A100 80G	9.39	1.00×	1.87	1.00×	8.21	1.00×	1.17	1.00×
PLENA	6.13	**1.36×**	1.41	**1.21×**	5.71	**1.42×**	1.52	**1.30×**

Note: The remaining accelerators and TPUs are not included since they do not support these configurations.

by 25% relative to FP16. As shown in table 4, the maximum perplexity increase under full-system quantization is ≤ 0.05.

6.3 Co-design

This subsection shows the results of our design space exploration experiments. Figure 11 shows the Empirical Attainment Surfaces (EAS) for the Pareto fronts found when optimizing with LLAMA3.2-1B and LLAMA-3-8B. EAS is a visualization approach well-suited for conveying the uncertainty of the Pareto fronts from multiple runs with different random seeds [21, 33]. Existing tools support visual analysis for two objectives [67], hence we plot EAS for accuracy and latency first. Then, in Table 16 we analyze the relationship between all objectives. Figure 11 shows that active learning with BOTorch sampler achieves a significantly better trade-off between latency and perplexity than naive randomized sampling. Tree-Structured Parzen Estimator (TPE) shows more modest gains when optimizing with LLAMA3.2-1B compared to using BOTorch sampler, thus we focus on the latter for experiments with LLAMA-3-8B.

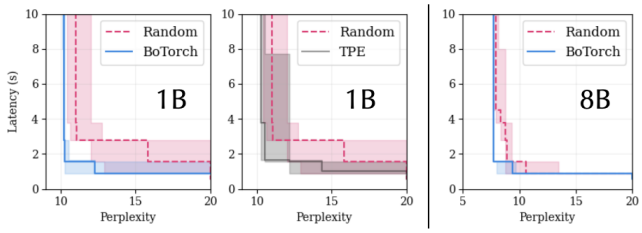


Figure 11: Empirical Attainment Surfaces for latency (↓) and perplexity (↓) objectives across multiple seeds, evaluated with LLAMA3.2-1B and LLAMA-3-8B over the co-design space shown in Table 14. For the 1B model, we run 9 seeds with 50 trials, comparing BoTorch and TPE methods against Random sampling. For the 8B model, we run 5 seeds with 50 trials, comparing BoTorch against Random. Shaded regions show the 25% and 75% attainment bands across seeds.

6.4 Compute Performance

The system-level performance comparison is shown in Table 5, evaluating both small and large GQA-based LLaMA models as well as the recently published MoE-based GPT-OSS model, all implemented in 7 nm technology and supporting long-context inputs. This experiment investigates peak TPS by scaling the batch size to the maximum capacity that HBM can accommodate. As shown, PLENA achieves consistently higher TPS than both the A100 and TPU v6e under identical HBM settings and multiplier counts, with peak performance reaching up to 2.24× that of the A100 and 3.85× that of the TPU v6e. The higher TTFT observed in PLENA is

explained by its ability to store more batches within the same HBM capacity using our quantization scheme. As batch size increases, the prefill stage grows longer due to additional memory accesses and computation.

Table 7: Compute area, utilization, and attainable FLOPs of systolic arrays under W4A4KV4 bitwidth for LLaMA-3.3-70B. Baselines use 64×64 arrays, while PLENA employs a flattened $(4, 512)$ array. Results are shown for Standard (Prompt = 1k, Gen = 128) and Agentic (Prompt = 5.6k, Gen = 8k) workloads.

Metric	Micro [54]	Olive [25]	FIGNA [31]	**PLENA**
Comp Area (mm^2)	0.1378	0.319	0.471	0.237
TOPs/mm^2	59.45	25.66	17.39	34.49
S. A FLOPs/mm^{2*}	28.76	11.59	7.51	**32.80**
A. A FLOPs/mm^{2*}	1.08	0.44	0.31	**5.31**

**Attainable FLOPs are computed from utilization and peak design throughput. Micro = MicroscopiQ. S. A FLOPs = Standard workload attainable FLOPs. A. A FLOPs = Agentic workload attainable FLOPs.*

As shown in Table 7, PLENA achieves significantly higher utilization than prior designs in both short- and long-context workloads, with up to 8.5× improvement in attainable utilization.

7 Conclusion

This paper introduces **PLENA**, a hardware–software co-designed system that features a flattened systolic array, an asymmetric quantization scheme, and native architectural support for FlashAttention, addressing the underutilization challenges posed by memory bandwidth and capacity walls. Beyond the hardware, PLENA is supported by a full toolchain—including a compiler, cycle-accurate simulator, and design space exploration framework—that enables rapid adaptation and optimization for emerging transformer models. Future work will focus on further optimizing GEMM utilization in FlashAttention and extending PLENA with a multi-core flattened systolic array to better exploit parallelism. In addition, the compiler can be enhanced to provide finer-grained control over execution scheduling. Finally, we plan to integrate PLENA with GPUs to form a heterogeneous LLM acceleration system.

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A Appendix

A.1 Ablation Study on Quantization Methods

Table 8: Ablation study on quantization techniques. Covering all 9 GEMMs in the LLAMA-3-8B model. Quantization configured with W_MXINT4, A_MXINT4, KV_MXINT4 with block size 16.

Method	Metric (e.g., PPL↓)
Baseline FP16	6.14
RTN	8.2763(2.3793 ↑)
RTN + Err_w Clip	8.1948(0.0815 ↓)
GPTQ + Err_w Clip	8.5193 (0.3245 ↑)
GPTQ + Err_y Clip	7.6026 (0.9167 ↓)
GPTQ + Err_y Clip + Selective Rotation	7.2218(0.3808 ↓)

A.2 A/KV Datatype Search

Table 9: Perplexity on WikiText2 (lower is better) for various quantization settings applied to LLaMA-3 8B. We kept MXINT4 for weights.

Quant Method	A/KV Datatype Search		
	e1m2 (MXFP4)	e2m1 (MXFP4)	MXINT4
Baseline FP16	6.14		
Ours	8.7205	23.1579	7.22

A.3 Selective Rotation

Table 10: This table investigates the effect of online rotation on activations in the linear layers. For the LLaMA2-7B model, applying rotation to the `down_proj` layer results in worse performance compared to not rotating it, whereas this effect is not observed in the LLaMA3-8B model. Moreover, rotating the `o_proj` layer severely degrades the performance of LLaMA3-8B. These results suggest that the effectiveness of rotation is highly model-dependent.

Rotated Layer	LLaMA2-7B	LLaMA3-8B
Attn Only	5.9367	7.3933
Attn + Down_proj	5.9405	7.2721
Attn + Up_proj	5.9263	7.3529
Attn + Gate_proj	5.9241	7.3875
Attn + Q_proj	5.9183	7.3616
Attn + K_proj	5.9182	7.3555
Attn + V_proj	5.9322	7.3788
Attn + O_proj	5.9238	nan

A.4 Computation Flow of LLaMA Decoder-only Transformer

Algorithm 2 Computation flow of a LLaMA decoder-only Transformer with embedding, lm_head, and with L layers: each decoder layer performs **[MatMul1–9]** interleaved with RMSNorm, RoPE , and nonlinear activations (SOFTMAX, SILU).

Require: $t \in [V]^T$ ▷ token ids
Require: $B, T, d, L, H, H_{\text{kv}}$ ▷ batch, seq, hidden_dim, #layers, #Q heads, #KV heads
Require: $(\cos\theta, \sin\theta)$ ▷ RoPE parameters
$X^{(1)} \leftarrow \text{EMBED}(t)$ ▷ $X^{(1)} \in \mathbb{R}^{B\times T\times d}$
for $\ell = 1$ **to** L **do**
  Layer input: $X^{(\ell)} \in \mathbb{R}^{B\times T\times d}$
  $X_n \leftarrow \text{RMSNorm}(X^{(\ell)})$
  $Q \leftarrow X_n W_Q$ **[MatMul1]**
  $K \leftarrow X_n W_K$ **[MatMul2]**
  $V \leftarrow X_n W_V$ **[MatMul3]**
  $(Q, K) \leftarrow \text{RoPE}(Q, K; \cos\theta, \sin\theta)$
  $(K, V) \leftarrow \text{RepeatGroups}(K, V, H/H_{\text{kv}})$ ▷ GQA
  $A_w \leftarrow \text{SOFTMAX}\left(\frac{QK^\top}{\sqrt{d_h}}\right)$ **[MatMul4]**
  $A_w \leftarrow A_w V$ **[MatMul5]**
  $A_o \leftarrow A_w W_O$ **[MatMul6]**
  $X' \leftarrow X^{(\ell)} + A_o$ ▷ residual add
  $X'_n \leftarrow \text{RMSNorm}(X')$
  $X_{\text{act}} \leftarrow \text{SiLU}(X'_n W_{\text{up}})$ **[MatMul7]**
  $X_{\text{gate}} \leftarrow X'_n W_{\text{gate}}$ **[MatMul8]**
  $X_{\text{mlp}} \leftarrow (X_{\text{act}} \odot X_{\text{gate}}) W_{\text{down}}$ **[MatMul9]**
  $X^{(\ell+1)} \leftarrow X' + X_{\text{mlp}}$ ▷ residual add
logits $\leftarrow X^{(L+1)} W_{\text{LM}}$
$\hat{p} \leftarrow \text{SOFTMAX}(\text{logits})$
return $\hat{p}$

A.5 Matrix SRAM

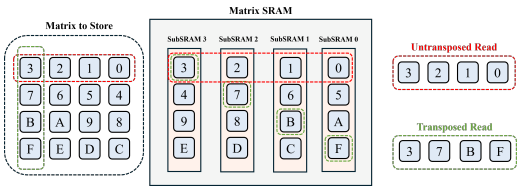

Figure 12: This matrix SRAM supports both transposed and untransposed reads without additional cost. The key idea is to store each row of data separately across a set of sub-SRAMs, where the number of sub-SRAMs equals the vector dimension being stored. The row index assigned to each element differs across the sub-SRAMs, ensuring that elements from the same matrix column (green dotted line) are distributed across different sub-SRAMs. With this organization, when reading from the SRAM—whether in transposed or untransposed mode—each requested element resides in a different sub-SRAM. As a result, only one read port per sub-SRAM is required.

A.6 PE Array

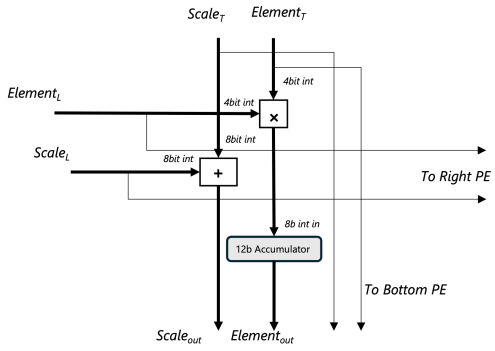

Figure 13: In the hardware implementation of the PE array, element and scale will flow from top to bottom, left to right. All computations are performed using integer arithmetic.

A.7 Custom ISA

Table 11: A summary of the PLEANA customized ISA for the accelerator

Instruction Type	Description	Instruction No.
Matrix	Controls GEMM and GEMV operations, with or without matrix transposition	6
Vector	Performs elementwise, reduction operations, and rotation for quantization	13
Scalar	Performs scalar INT and FP arithmetic	17
HBM	Handles data transfers between HBM and matrix/vector SRAMs	3
Control	Defines operation settings, including the HBM physical address	4

A.8 Custom Instructions

Table 12: Summary of Custom ISA Instructions.

Type	Instruction (Format)	Description
Matrix (M)	M_MM (opcode, rd, rs1, rs2)	Multiply Matrix[rs2] and Vector[rs1]; accumulate in systolic array.
	M_TMM (opcode, rd, rs1, rs2)	Same as M_MM but with matrix transpose.
	M_MV (opcode, rd, rs1)	Multiply Matrix[rs2] and Vector[rs1]; store in first row of systolic array.
	M_TMV (opcode, rd, rs1)	Same as M_MV but with matrix transpose.
	M_MV_WO (opcode, rd, imm)	Write out first row of systolic array to Vector SRAM[rd+imm].
	M_MM_WO (opcode, rd, imm)	Write out systolic array results to Vector SRAM[rd+imm].
Vector (V)	V_ADD_VV (opcode, rd, rs1, rs2)	Elementwise vector addition.
	V_ADD_VF (opcode, rd, rs1, rs2)	Vector plus broadcasted FP register.
	V_SUB_VV (opcode, rd, rs1, rs2)	Elementwise vector subtraction.
	V_SUB_VF (opcode, rd, rs1, fp2)	Vector minus broadcasted FP register.
	V_MUL_VV (opcode, rd, rs1, rs2)	Elementwise vector multiplication.
	V_MUL_VF (opcode, rd, rs1, fp2)	Vector times broadcasted FP register.
	V_EXP_V (opcode, rd, rs1)	Elementwise exponentiation.
	V_REC_V (opcode, rd, rs1)	Elementwise reciprocal.
	V_LD_F (opcode, rd, rs1)	Broadcast FP register value to vector.
	V_RED_SUM (opcode, rd, rs1)	Reduction sum of vector into FP register.
	V_RED_MAX (opcode, rd, rs1)	Reduction max of vector into FP register.
	V_ROTATION_EN (opcode, rd, rs1)	Selectively apply Hadamard rotation
	V_INV_ROTATION_EN (opcode, rd, rs1)	Selectively apply inverse Hadamard rotation
Scalar (S)	S_ADD_INT (opcode, rd, rs1, rs2)	Integer addition.
	S_ADDI_INT (opcode, rd, rs1, imm)	Integer add immediate.
	S_SUB_INT (opcode, rd, rs1, rs2)	Integer subtraction.
	S_LUI_INT (opcode, rd, imm)	Load upper immediate.
	S_MUL_INT (opcode, rd, rs1, rs2)	Integer multiplication.
	S_DIV_INT (opcode, rd, rs1, rs2)	Integer division.
	S_LD_INT (opcode, rd, rs1, imm)	Load from FIX_MEM into integer register.
	S_ST_INT (opcode, rd, rs1, imm)	Store integer register to FIX_MEM.
	S_ADD_FP (opcode, rd, rs1, rs2)	FP addition.
	S_SUB_FP (opcode, rd, rs1, rs2)	FP subtraction.
	S_MUL_FP (opcode, rd, rs1, rs2)	FP multiplication.
	S_EXP_FP (opcode, rd, rs1)	FP exponentiation.
	S_MAX_FP (opcode, rd, rs1, rs2)	FP maximum.
	S_LD/ST_FP (opcode, rd, rs1, imm)	Load/store FP register from/to FP_MEM.
Memory (H)	H_PREFETCH_M (opcode, rd, rs1, rs2, rstride, prec)	Prefetch specified rows from HBM to Matrix SRAM.
	H_PREFETCH_V (opcode, rd, rs1, rs2)	Prefetch specified amount of rows from HBM to Vector SRAM.
	H_STORE_V (opcode, rd, rs1, rs2, stride, prec)	Store VLEN rows from Vector SRAM to HBM.
Control (C)	C_SET_ADDR_REG (opcode, rd, rs1, rs2)	Set HBM address register from two FIX regs.
	C_SET_SCALE_REG (rd, opcode)	Set MX scale offset for quantized data.
	C_SET_LUT_REG (rd, opcode)	Set MX scale offset for quantized data.
	C_BREAK (opcode)	Trigger breakpoint exception.

A.9 Downstream Tasks

Table 13: Zero-shot accuracy of LLAMA-3 and LLAMA-2 models with 4 bits (A4W4KV4) only comparing with QuaRot on PIQA (PQ), WinoGrande (WG), HellaSwag (HS), Arc-Easy (A-e), Arc-Challenge (A-c), and LAMBADA (LA). Baseline and quarot results taken from QuaRot Table2 and Table 12.

Model	Method	PQ [10]	WG [57]	HS [72]	A-e [14]	A-c [14]	LA [52]	Avg.
LLAMA-3-8B	FP16	80.74	72.77	79.06	77.82	53.33	75.63	73.22
	QuaRot [6]	75.14	65.82	72.94	68.01	43.34	65.81	65.18
	Ours	79.11	71.35	76.97	74.07	50.51	74.07	71.01
LLAMA-2-7B	FP16	79.11	69.06	75.99	74.58	46.25	73.90	69.82
	QuaRot [6]	76.77	63.77	72.16	69.87	40.87	70.39	65.64
	Ours	78.73	68.19	74.24	72.52	43.69	73.30	68.45

A.10 Co-Design Space and Analysis

Table 14: Hardware and quantisation parameters co-design search space. Categorical parameters are one-hot encoded, integer parameters are expressed as a power of 2.

Parameter	Description	Search range
BLEN	Tile size of block unit	[2, 4, 8, 16, 32]
MLEN	Tile size of matrix unit	[2, 4, 8, 16, 32, 64, 128, 256, 512]
VLEN	Tile size of vector unit	[2, 4, 8, 16, 32, 64, 128, 256, 512, 1024]
HBM_M_Prefetch	Prefetch amount for matrix data from HBM	[2, 4, 8, 16, 32, 64, 128, 256]
HBM_V_Prefetch	Prefetch amount for vector data from HBM	[2, 4, 8, 16, 32, 64, 128, 256]
HBM_V_Writeback	Writeback amount for vector data to HBM	[2, 4, 8, 16, 32, 64, 128, 256]
ACT_WIDTH	Activation precision	MXINT_{2,3,4,8}, MXFP_{E1M2, E2M1, E3M4, E4M3, E5M2}
KV_WIDTH	Key/Value precision	MXINT_{2,3,4,8}, MXFP_{E1M2, E2M1, E3M4, E4M3, E5M2}
FP_SETTING	Floating-point precision setting	FP_{E3M2, E2M3, E6M5, E5M6, E4M7, E8M5}
INT_DATA_WIDTH	Integer data width	[16, 32, 64]

Table 15: Constraints applied to the hardware and quantisation co-design search space.

Constraint	Description
$\text{MLEN} \geq \text{BLEN}$	Matrix tile size must be at least the block tile size
$\text{MLEN} \bmod \text{BLEN} = 0$	Matrix tile size must be divisible by the block tile size
$\text{MATRIX_SRAM_DEPTH} \geq 2\times \text{MLEN}$	Matrix SRAM depth must accommodate 2× MLEN
$\text{VECTOR_SRAM_DEPTH} \geq 2\times \text{HEAD_DIM} + \frac{\text{HIDDEN_DIM}}{\text{VLEN}}$	Vector SRAM depth must store heads and hidden slices
$\text{INT_SRAM_DEPTH} \geq 16$	Minimum integer SRAM depth
$\text{FP_SRAM_DEPTH} \geq 3\times \text{MLEN} + \text{FP_CONSTANT_NUM}$	Floating-point SRAM depth constraint
$(\text{MLEN} \times \text{ACT_WIDTH} + (\text{MLEN} / \text{BLEN}) \times \text{ACT_SCALE_WIDTH}) < 1510$	Bandwidth constraint at 1 GHz, 1 TB/s
$(\text{VLEN} \times \text{ACT_WIDTH} + (\text{VLEN} / \text{BLEN}) \times \text{ACT_SCALE_WIDTH}) < 1510$	Bandwidth constraint at 1 GHz, 1 TB/s
$(\text{MLEN} \times \text{ACT_WIDTH} + (\text{MLEN} / \text{BLEN}) \times \text{ACT_SCALE_WIDTH}) < 1510$	Bandwidth constraint at 1 GHz, 1.5 TB/s
$(\text{VLEN} \times \text{ACT_WIDTH} + (\text{VLEN} / \text{BLEN}) \times \text{ACT_SCALE_WIDTH}) < 1510$	Bandwidth constraint at 1 GHz, 1.5 TB/s

Table 16: Design space exploration on LLAMA-3-8B: multi-objective results for five configurations from a BoTorch run. We report perplexity (↓) from the accuracy evaluator, end-to-end latency (seconds ↓), and area (micrometer^2 ↓) from the respective cost models. Perplexity is computed with GEMM-only emulation (nonlinear ops omitted) for faster iteration, therefore the FP setting affects latency and area but not the accuracy metric. We load weights pre-quantized to MXINT4 via our PTQ method and quantize activations and the KV cache on-the-fly during inference.

Parameters										Metrics		
BLEN	**MLEN**	**VLEN**	**HBM_M Prefetch**	**HBM_V Prefetch**	**HBM_V Writeback**	**ACT WIDTH**	**KV WIDTH**	**FP SETTING**	**INT_DATA WIDTH**	**Perplexity ↓**	**Lat (s) ↓**	**Area (mm^2) ↓**
32	128	32	16	8	256	MXFP_E4M3	MXFP_E3M4	FP_E4M7	64	6.70	0.24	49615017.52
32	128	64	4	8	256	MXINT_8	MXINT_4	FP_E3M2	32	6.76	0.24	51639793.20
32	256	128	256	64	128	MXFP_E1M2	MXINT_8	FP_E6M5	16	12.14	0.15	99425984.56
8	128	32	128	8	256	MXFP_E3M4	MXFP_E3M4	FP_E5M6	16	6.54	1.47	26456937.52
16	128	16	4	16	64	MXINT_8	MXFP_E4M3	FP_E3M2	64	6.60	0.49	31983011.76

A.11 Compute Performance Experiment Settings

Table 17: Configuration settings for compute performance experiments, chosen to match the multiplier count of the A100 GPU. For MicroscopiQ, MLEN and BLEN are set to the same value to form a square shape.

System	Freq (GHz)	MLEN	BLEN	VLEN	SRAM (MB)	W. Width	A. Width	KV Width	FP Setting
PLENA	1	2048	32	2048	128	MXINT4	MXINT4	MXINT4	FP E4M3
MicroscopiQ	1	256	256	2048	128	MXINT4	MXINT4	MXINT4	FP E4M3