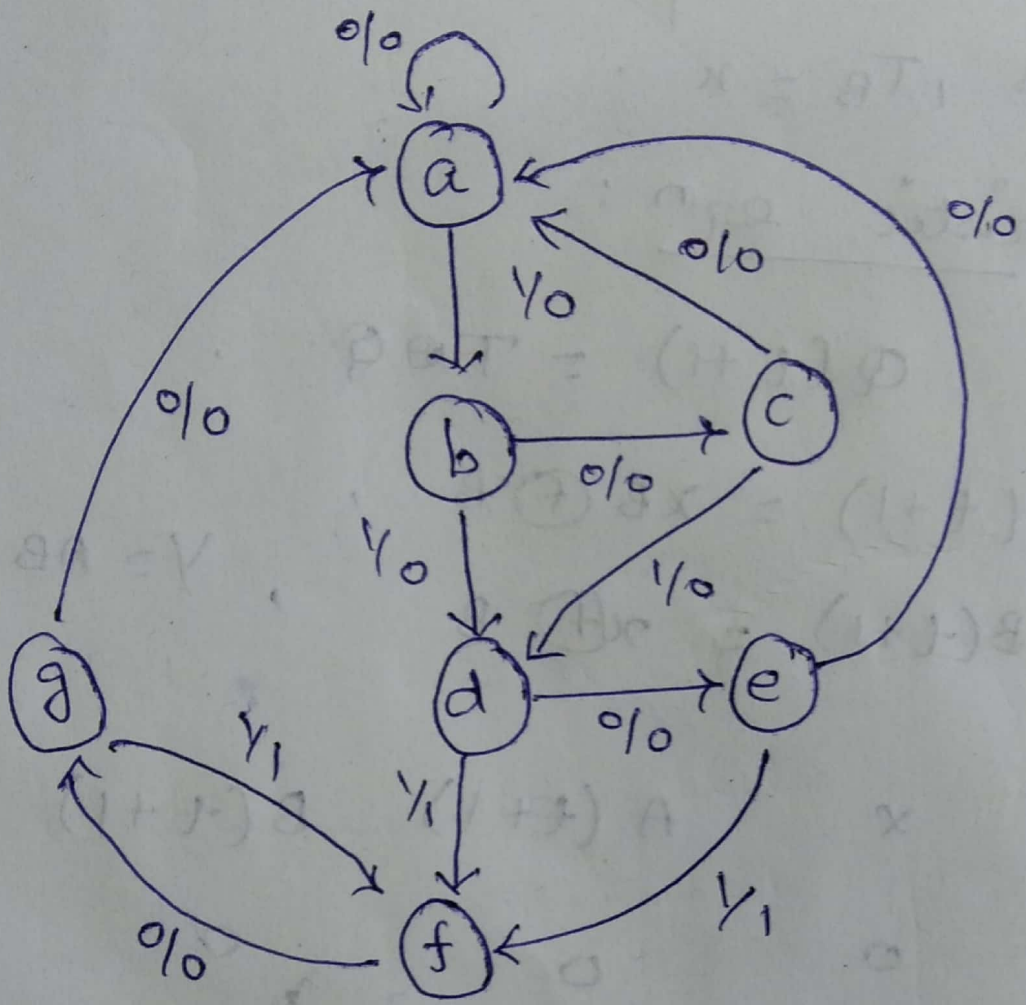
# State reduction & assignment



| Present state | Next state x=0 | Next state x=1 | o/p x=0 | o/p x=1 |
|---|---|---|---|---|
| a | a | b | 0 | 0 |
| b | c | d | 0 | 0 |
| c | a | d | 0 | 0 |
| d | e | f | 0 | 1 |
| e | a | f | 0 | 1 |
| f | g | g | 0 | 1 |
| g | a | f | 0 | 1 |

similar

Then we have to see similar term then we have to replace it.

Here g and e are similar.

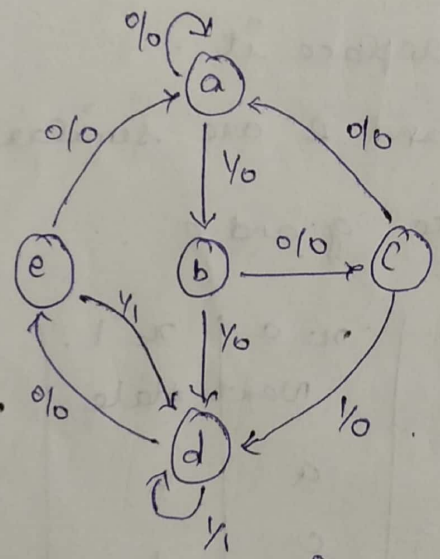
∴ Replace g and e.

| Present state | Next state x=0 | Next state x=1 | o/p x=0 | o/p x=1 |
|---|---|---|---|---|
| a | a | b | 0 | 0 |
| b | c | d | 0 | 0 |
| c | a | d | 0 | 0 |
| d | e | f | 0 | 1 |
| e | a | f | 0 | 1 |
| f | e | f | 0 | 1 |
| ~~g~~ | | | | |

d and f are similar replace by d.

| Present state | Next state x=0 | Next state x=1 | O/P x=0 | O/P x=1 |
|---|---|---|---|---|
| a | a | b | 0 | 0 |
| b | c | d | 0 | 0 |
| c | a | d | 0 | 0 |
| d | e | d | 0 | 1 |
| e | a | d | 0 | 1 |

Reduced state diagram:




Reduced state table with binary assignment:

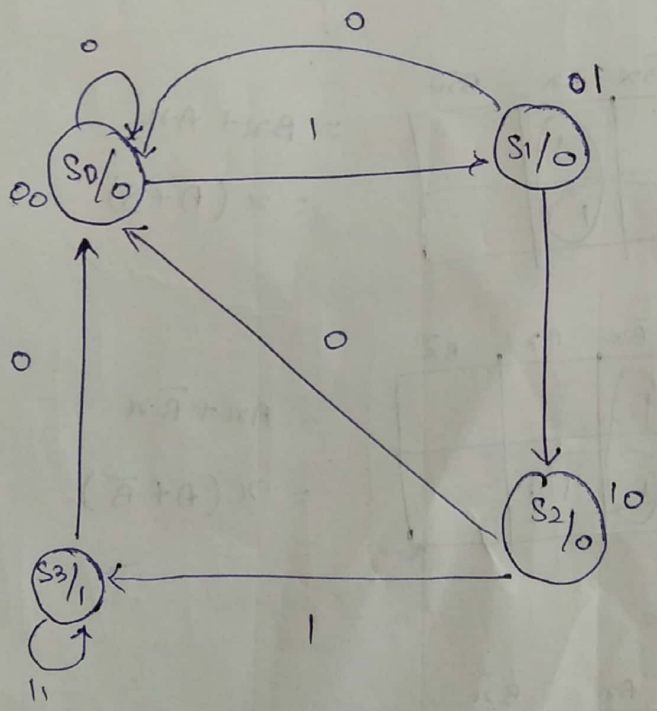
| Present state | Next state x=0 | Next state x=1 | O/P x=0 | O/P x=1 |
|---|---|---|---|---|
| 0 0 0 | 0 0 0 | 0 0 1 | 0 | 0 |
| 0 0 1 | 0 1 0 | 0 1 1 | 0 | 0 |
| 0 1 0 | 0 0 0 | 0 1 1 | 0 | 0 |
| 0 1 1 | 1 0 0 | 0 1 1 | 0 | 1 |
| 1 0 0 | 0 0 0 | 0 1 1 | 0 | 1 |

## Design procedure :

1. From the word description and specification of the desired operation, derive a state diagram for the circuit.
2. Reduce the no. of states if necessary
3. Assign binary value to the state.
4. Obtain the binary coded state table.
5. Choose the type of flip flop to be used.
6. Derive the simplified flip flop input and output eqn.
7. Draw the logic diagram.

Problem:

1.



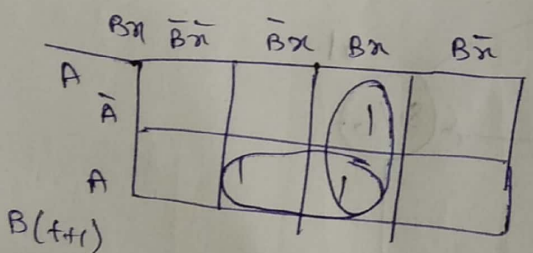
| present state | | i/p | next state | | o/p |
|---|---|---|---|---|---|
| A | B | x | A(t+1) | B(t+1) | y |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | (1) | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | (1) | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | (1) | 1 | 1 |

$A(t+1) = \Sigma_m(3,5,7)$

$B(t+1) = \Sigma_m(1,5,7)$

$y = \Sigma_m(6,7)$

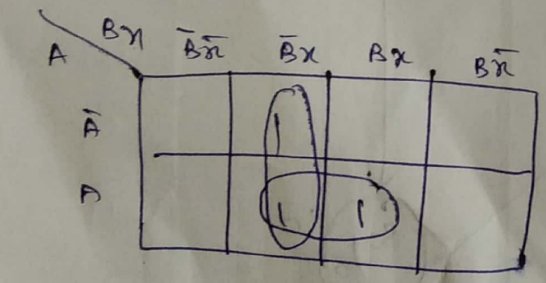
A(t+1)




$= Bx + A\bar{x}$

$= x(A+B)$

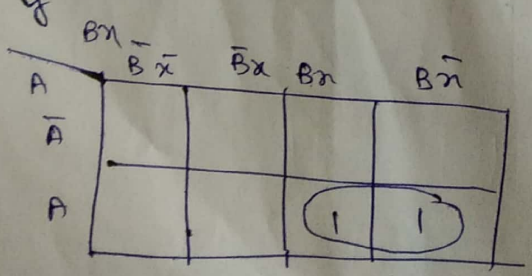
B(t+1)



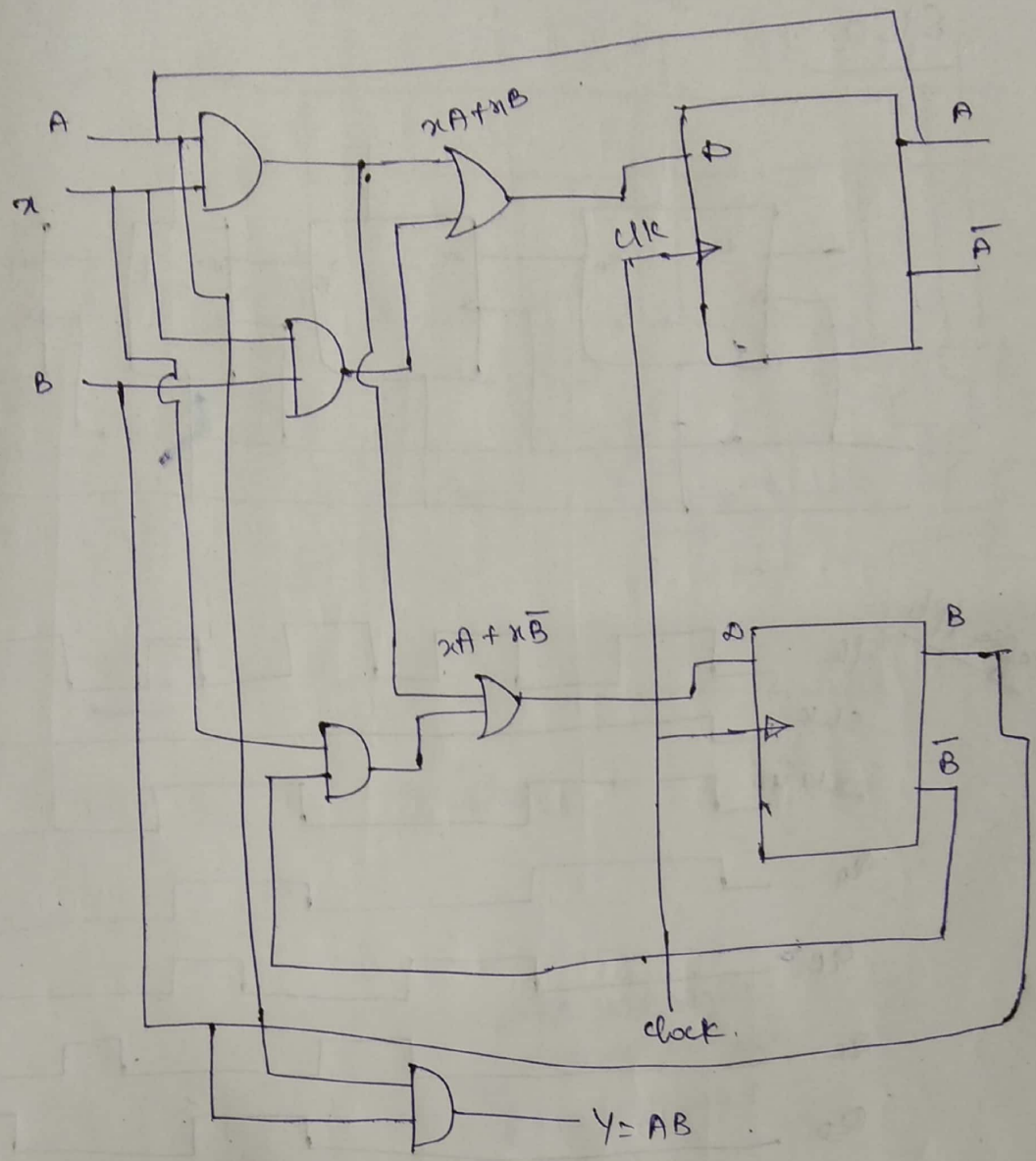

$= Ax + \bar{B}x$

$= x(A+\bar{B})$

y




$y = AB$

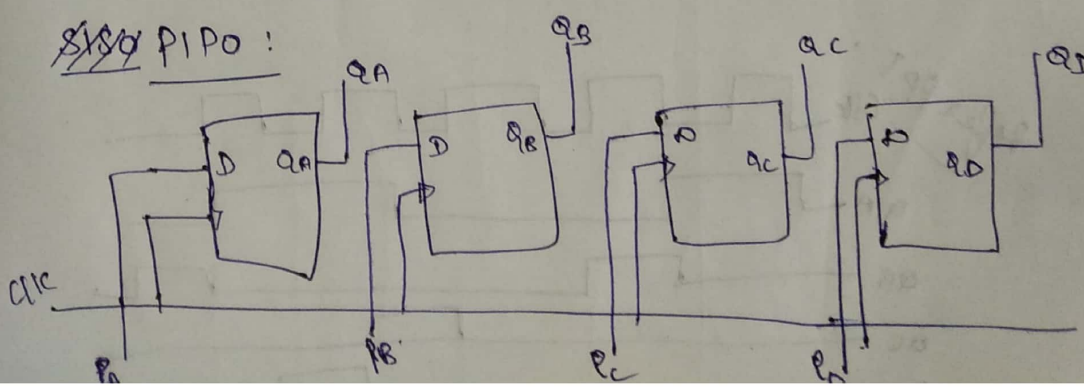



25/9/18.

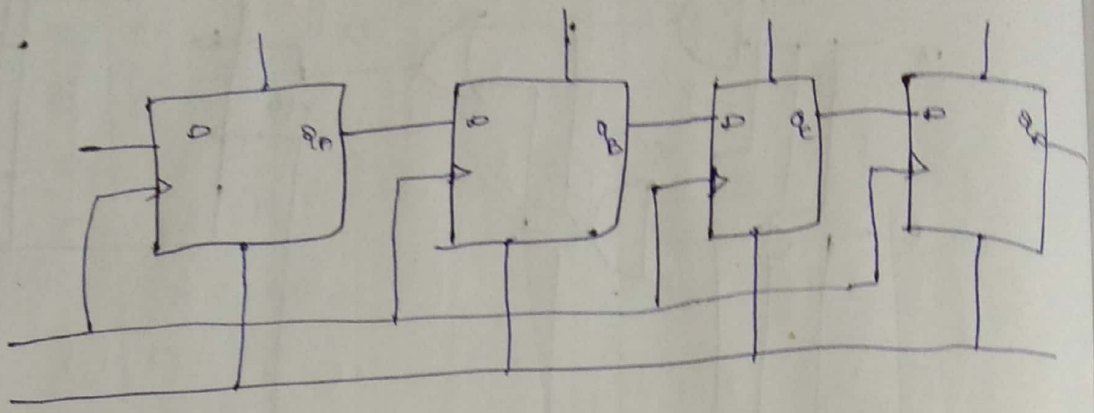
## Shift registers.

- Serial in - serial out. (SISO)
- Serial in - parallel out. (SIPO)
- parallel in - series out (PISO)
- parallel in - parallel out. (PIPO)

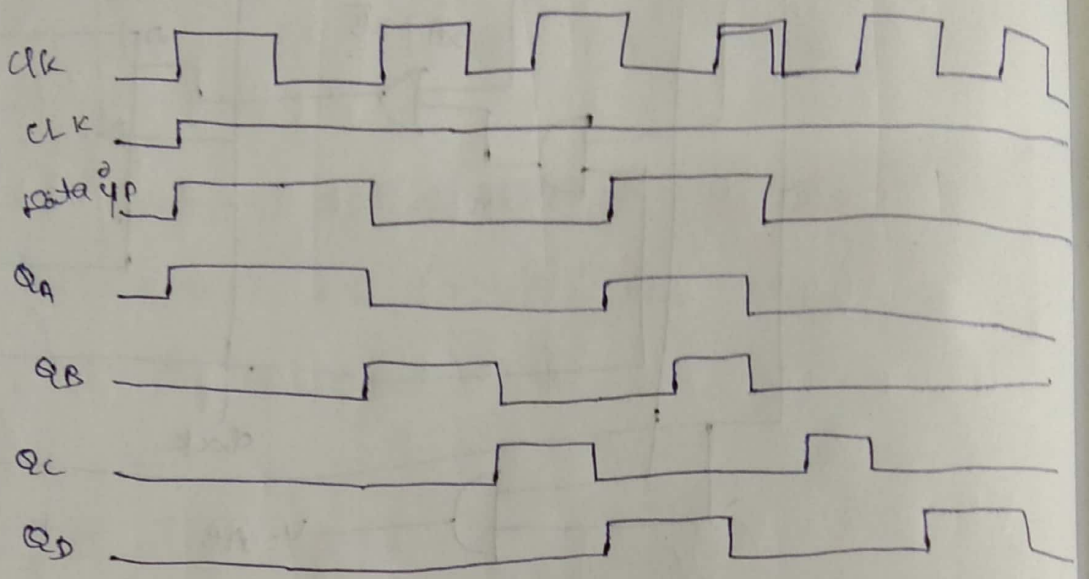
~~SISO~~ PIPO :



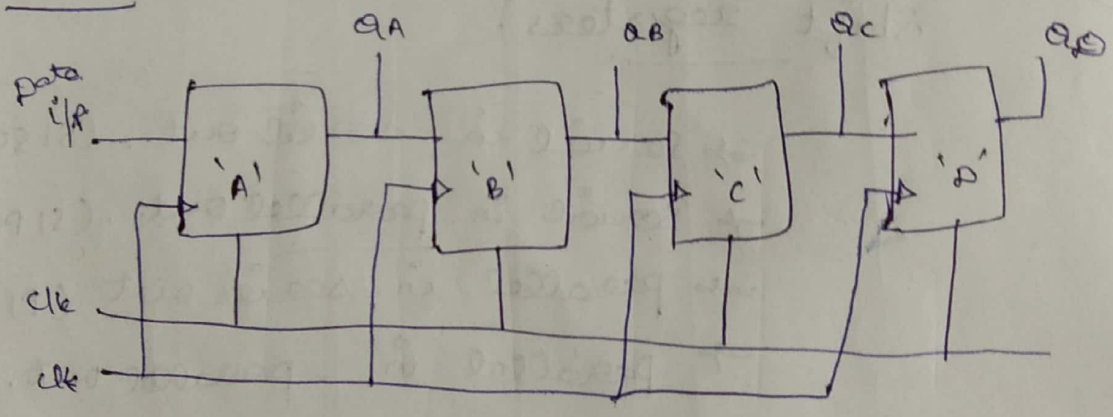
## SISO :



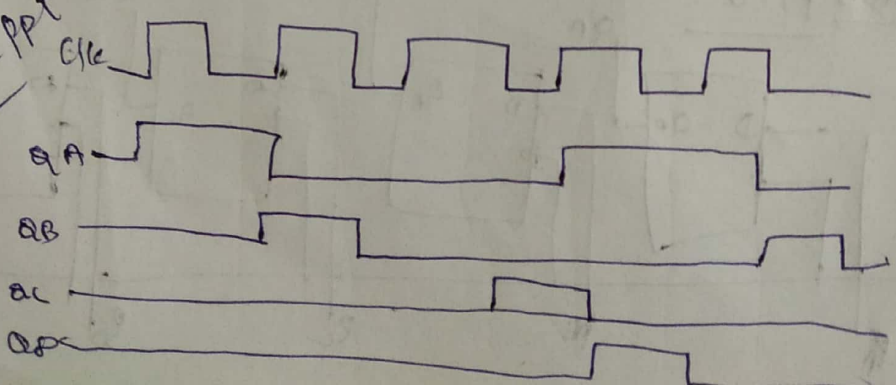
Refer PPt.



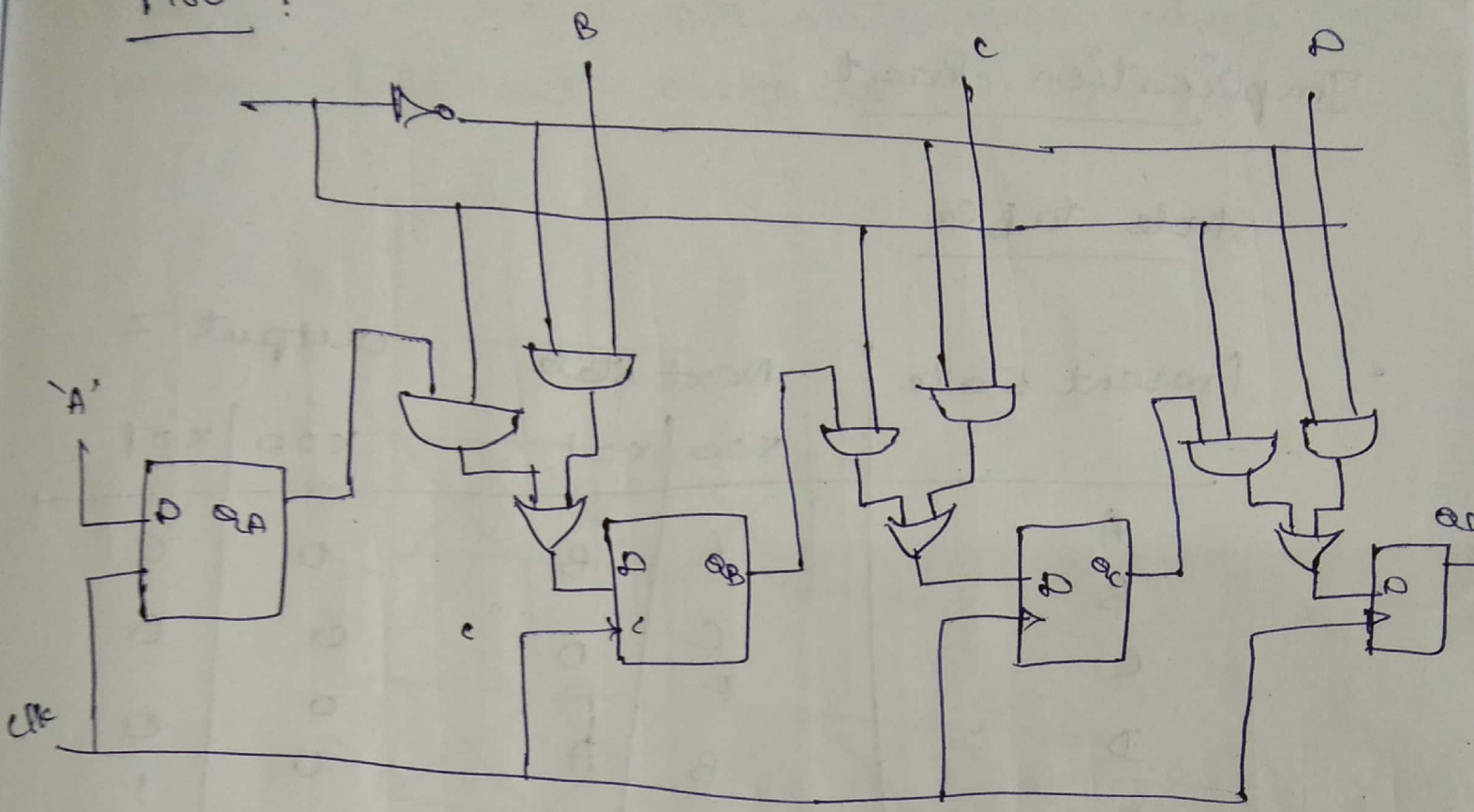

## SIPO :




Refer PPt.



PISO :




Universal shift register :

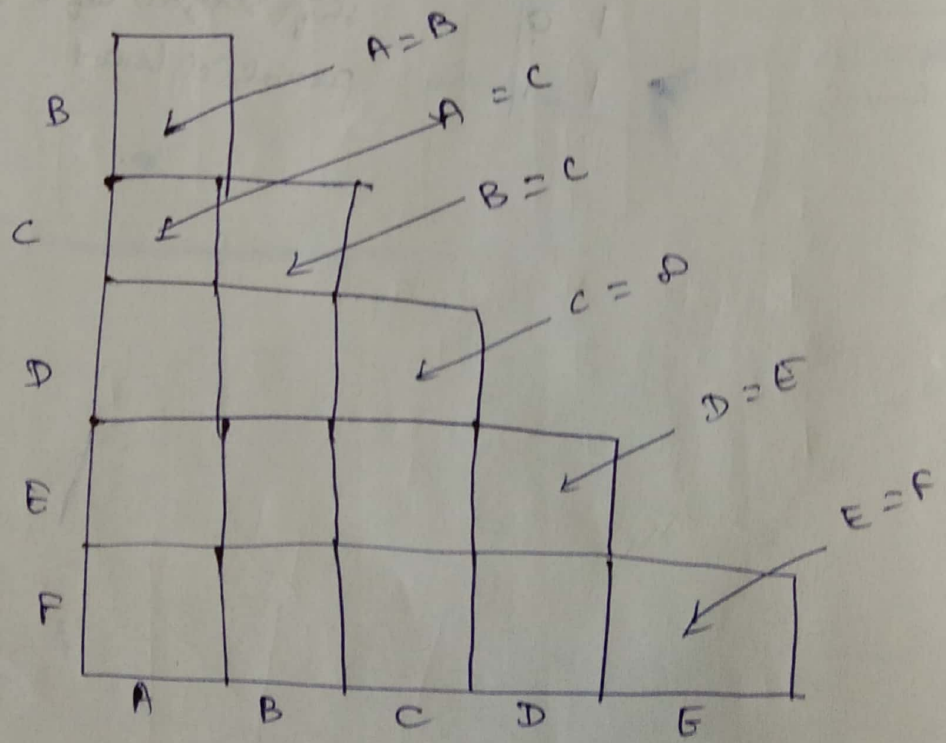
| $S_1$ | $S_2$ | |
|---|---|---|
| 0 | 0 | No change |
| 0 | 1 | shift right |
| 1 | 0 | shift left |
| 1 | 1 | parallel load |

## Implication chart :

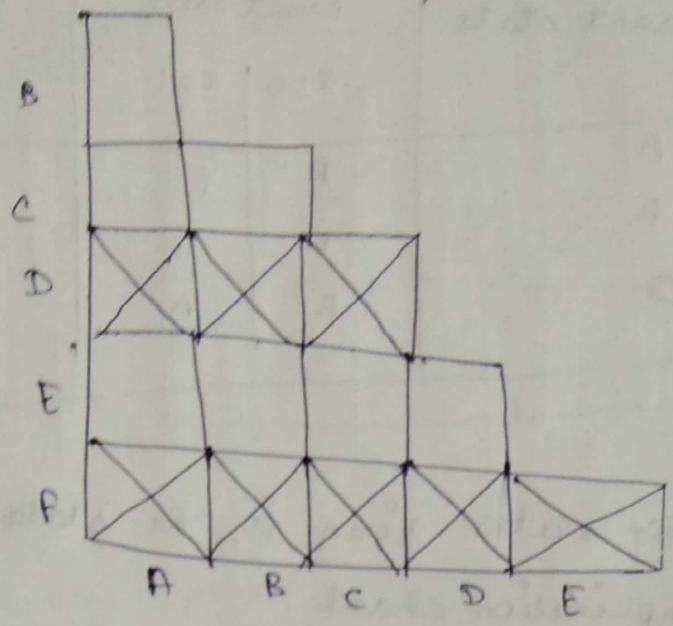
### State table :

| Present state | Next state | | output Z | |
|---|---|---|---|---|
| | x=0 | x=1 | x=0 | x=1 |
| A | A | B | 0 | 0 |
| B | C | D | 0 | 0 |
| C | E | F | 0 | 0 |
| D | B | A | 0 | 1 |
| E | C | D | 0 | 0 |
| F | B | A | 0 | 1 |

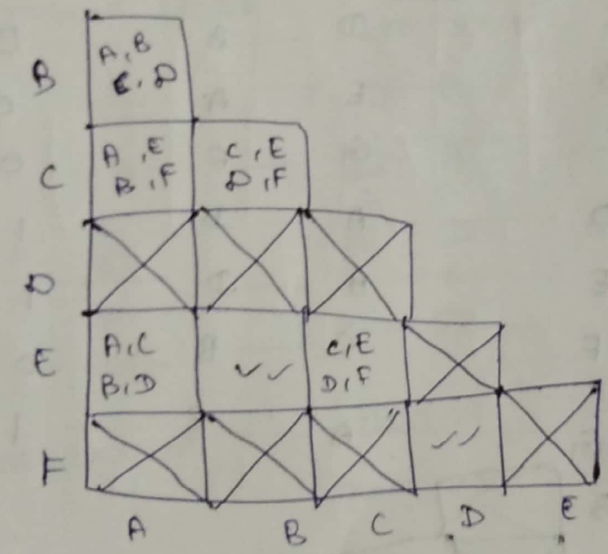
Set up implication chart.



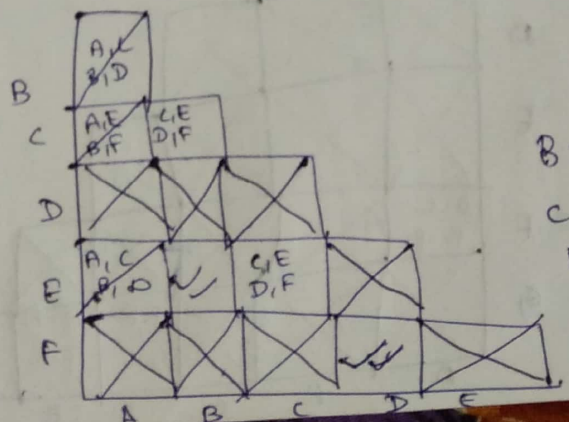
Fill the squares for state pairs which have different outputs.




Fill the squares for state pairs which may have same outputs.




Apply equivalency test on each square.




B = C = E

C = E

D = F.

Reduced state table :

| Present state | Next state | | Output Z | |
|---|---|---|---|---|
| | x=0 | x=1 | x=0 | x=1 |
| A | A | B | 0 | 0 |
| B | B | D | 0 | 0 |
| D | B | A | 0 | 1 |

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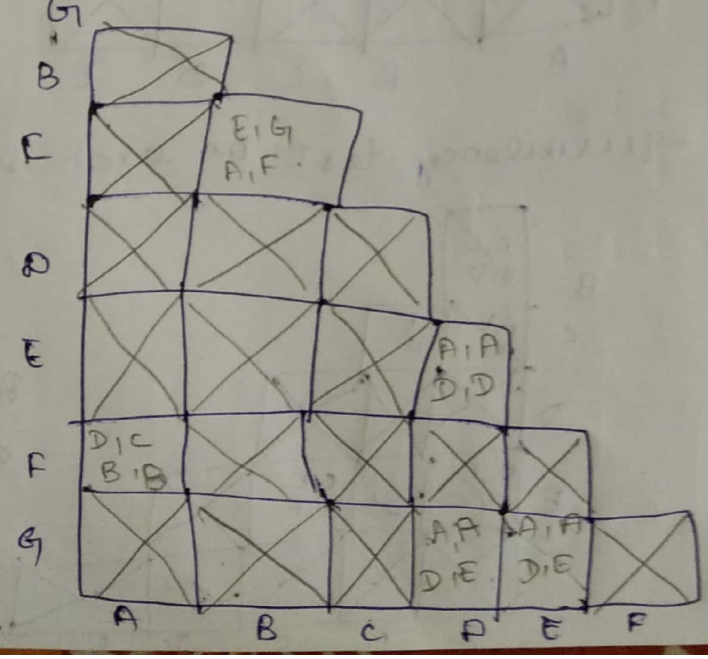
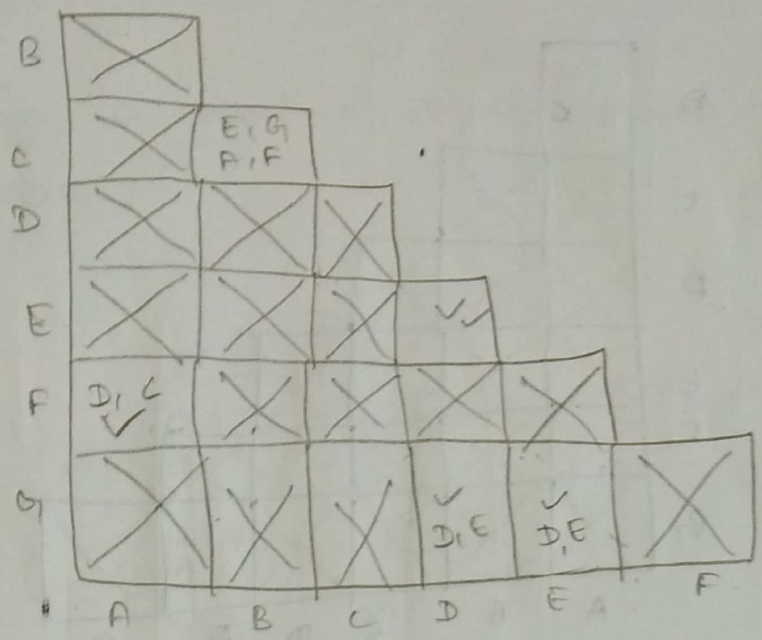
2. Reduce the states given in the state table using implication chart.

| Present state | Next state | | o/p | |
|---|---|---|---|---|
| | x=0 | x=1 | x=0 | x=1 |
| A | D | B | 0 | 0 |
| B | E | A | 0 | 1 |
| C | G | F | 0 | 1 |
| D | A | D | 1 | 0 |
| E | A | D | 1 | 0 |
| F | C | B | 0 | 0 |
| G | A | E | 1 | 0 |






B = E, G, A, F.

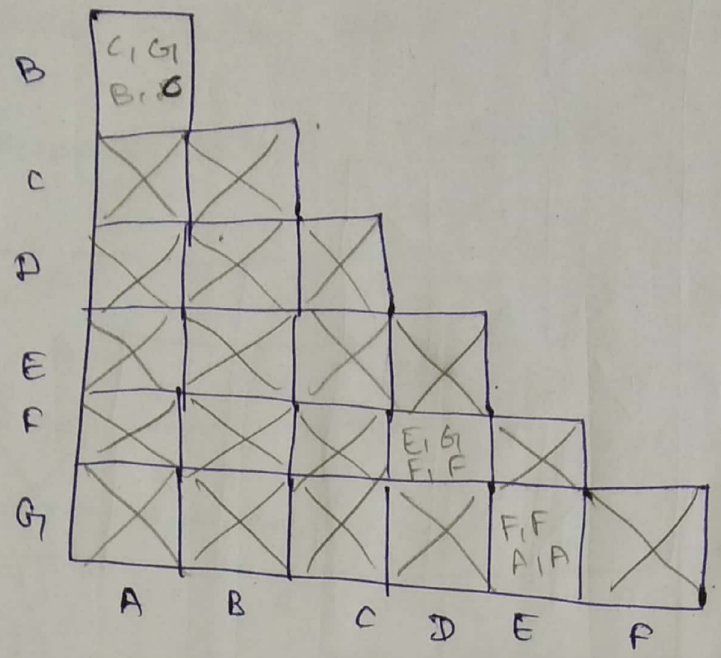
01 = 10, 10, 00, 00

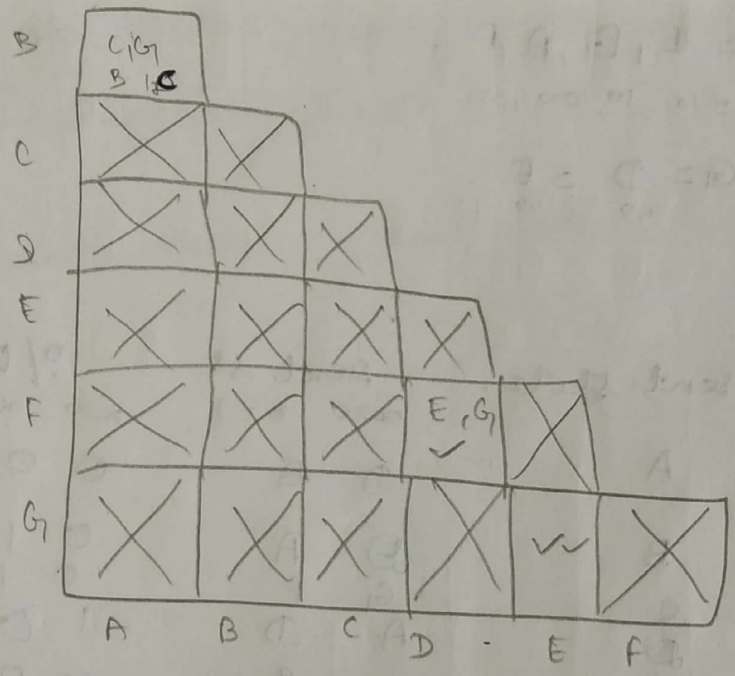
G = D = E.
1,0 1,0

| Present state | Next st x=0 | Next st x=1 | o/p x=0 | o/p x=1 |
|---|---|---|---|---|
| A | D | B | 0 | 0 |
| B | E | A | 0 | 1 |
| C | G | F | 0 | 1 |
| D | A | D | 1 | 0 |
| E | C | B | 0 | 0 |
| F | ~~A~~ | ~~E~~ | ~~1~~ | ~~0~~ |
| ~~G~~ | | | | |

(5).

| Present st | Next st x=0 | Next st x=1 | o/p x=0 | o/p x=1 |
|---|---|---|---|---|
| A | C | B | 0 | 0 |
| B | D | C | 0 | 0 |
| C | G | D | 1 | 1 |
| D | E | F | 1 | 0 |
| E | F | A | 0 | 1 |
| F | G | F | 1 | 0 |
| G | F | A | 0 | 1 |




~~A = B~~

~~D = F~~

$A = C, G, B, \overline{E}$

0,0 0,1 1,0 0,1 1,0

$D = E, G, F$

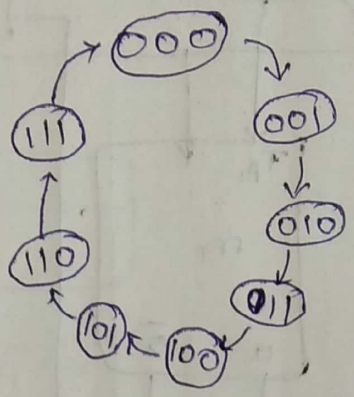
1,0 1,0 . 1,0 . 0,0

~~D ≠ E ≠ G~~

Nothing is reduced.

Counter :

1. Design a Mod-8 synchronous up counter.



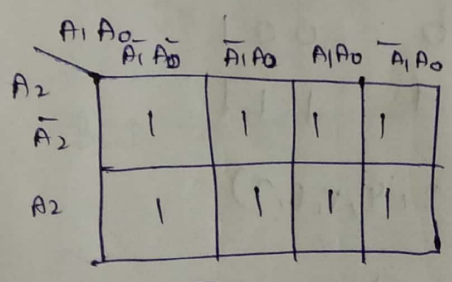

By (Toggle flip flop)

| Pulse | Present st. $A_2$ $A_1$ $A_0$ | Next st. $A_2$ $A_1$ $A_0$ | o/p $T_{A_2}$ $T_{A_1}$ $T_{A_0}$ |
|---|---|---|---|
| 0 | 0 0 0 | 0 0 1 | 0 0 1 |
| 1 | 0 0 1 | 0 1 0 | 0 1 1 |
| 2 | 0 1 0 | 0 1 1 | 0 0 1 |
| 3 | 0 1 1 | 1 0 0 | 0 1 1 |
| 4 | 1 0 0 | 1 0 1 | 1 0 1 |
| 5 | 1 0 1 | 1 1 0 | 0 1 1 |
| 6 | 1 1 0 | 1 1 1 | 0 0 1 |
| 7 | 1 1 1 | 0 0 0 | 1 1 1 |

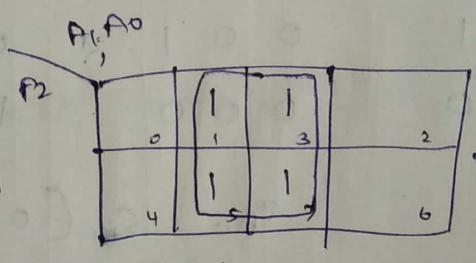
$T_{A_0} = \Sigma_m(0,1,2,3,4,5,6,7)$

$T_{A_1} = \Sigma_m(1,3,5,7)$

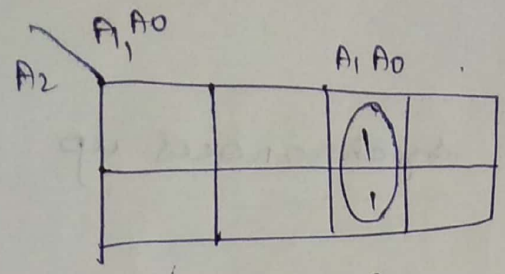
$T_{A_2} = \Sigma_m(4,7)$.

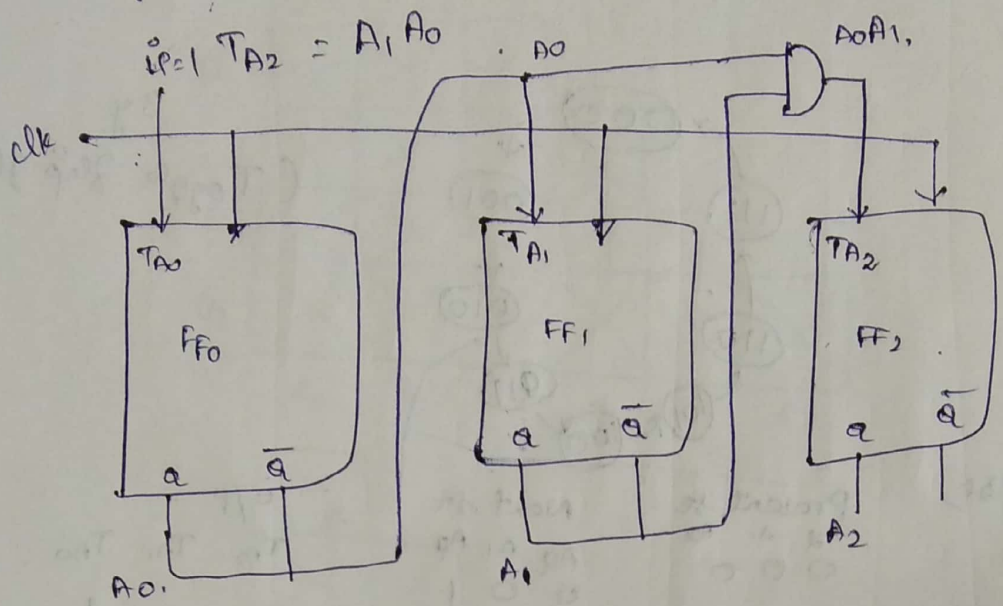



$T_{A_0} = 1$




$T_{A_1} = A_0$



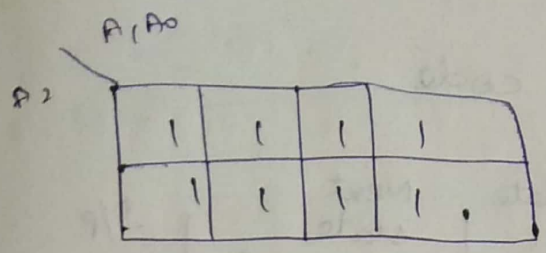

Q. Design MOD-8 synchronous down counter.

| Pulse | Present state $A_2 A_1 A_0$ | Next state $A_2 A_1 A_0$ | o/p $A_2 A_1 A_0$ |
|---|---|---|---|
| 7 | 1 1 1 | 0 1 0 | 0 0 1 |
| 6 | 1 1 0 | 1 0 1 | 0 1 1 |
| 5 | 1 0 1 | 1 0 0 | 0 0 1 |
| 4 | 1 0 0 | 0 1 1 | 1 1 1 |
| 3 | 0 1 1 | 0 1 0 | 0 0 1 |
| 2 | 0 1 0 | 0 0 1 | 0 1 1 |
| 1 | 0 0 1 | 0 0 0 | 0 0 1 |
| 0 | 0 0 0 | 1 1 1 | 1 1 1 |

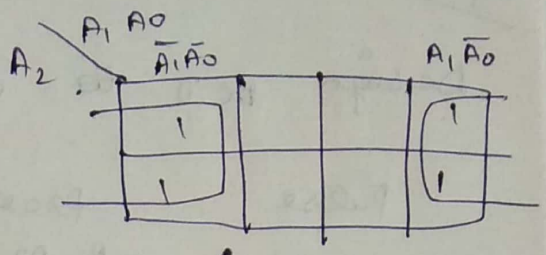
$T_{A0} = \Sigma m(0,1,2,3,4,5,6,7)$

$T_{A1} = \Sigma m(6,4,2,0)$

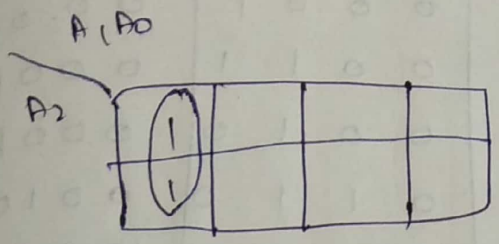
$T_{A2} = \Sigma m(4,0)$



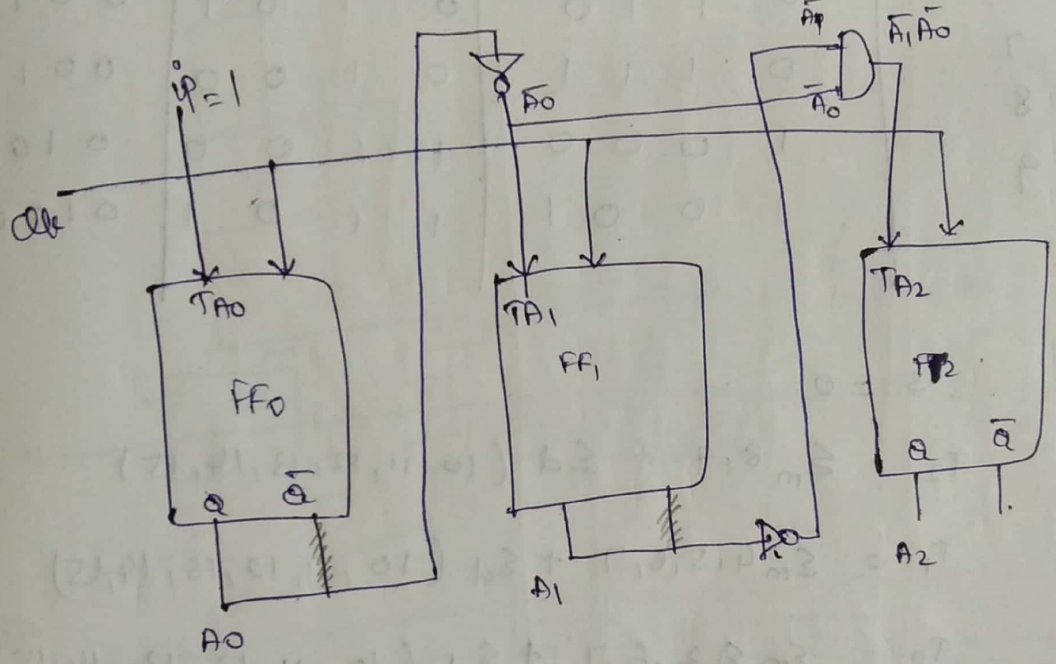

$T_{A0} = 1$




$T_{A_1} = \bar{A}_0$ .




$T_{A_2} = \bar{A}_1 \bar{A}_0$




H/W

1. Design MOD 3 up synchronous counter using JK flip flop
2. BCD to graycode with T-flip flop.

5/10/18

Design BCD to gray code :

| Pulse | Present state $A_3$ $A_2$ $A_1$ $A_0$ | Next state $g_3$ $g_2$ $g_1$ $g_0$ | O/P $T_3$ $T_2$ $T_1$ |
|---|---|---|---|
| 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 |
| 1 | 0 0 0 1 | 0 0 0 1 | 0 0 0 |
| 2 | 0 0 1 0 | 0 0 1 1 | 0 0 0 |
| 3 | 0 0 1 1 | 0 0 1 0 | 0 0 0 |
| 4 | 0 1 0 0 | 0 1 1 0 | 0 0 1 |
| 5 | 0 1 0 1 | 0 1 1 1 | 0 0 1 |
| 6 | 0 1 1 0 | 0 1 0 1 | 0 0 1 |
| 7 | 0 1 1 1 | 0 1 0 0 | 0 0 1 |
| 8 | 1 0 0 0 | 1 1 0 0 | 0 1 0 |
| 9 | 1 0 0 1 | 1 1 0 1 | 0 1 0 |

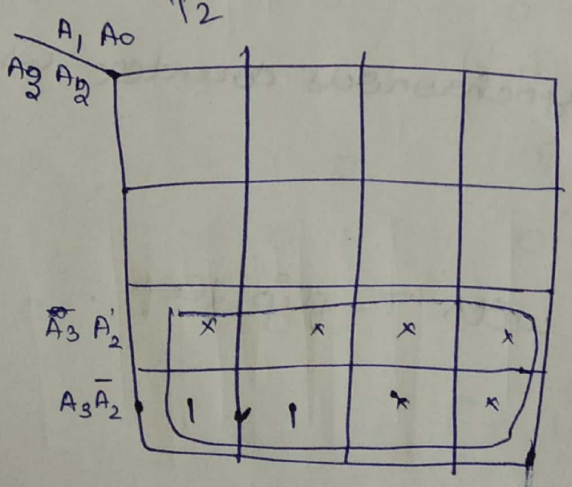
$T_3 = 0$

$T_2 = \Sigma_m 8,9 + \Sigma_d (10,11,12,13,14,15)$

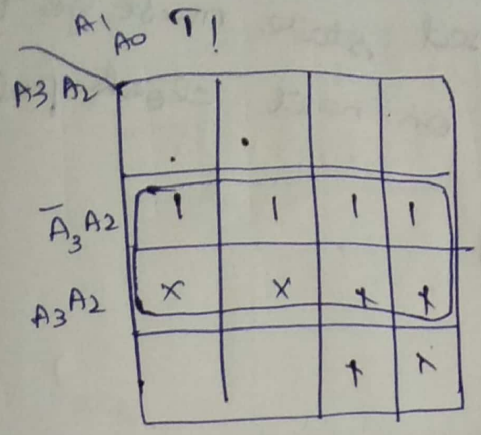
$T_1 = \Sigma_m 4,5,6,7 + \Sigma_d (10,11,12,13,14,15)$

$T_0 = \Sigma_m 2,3,6,7 + \Sigma_d (10,11,12,13,14,15)$

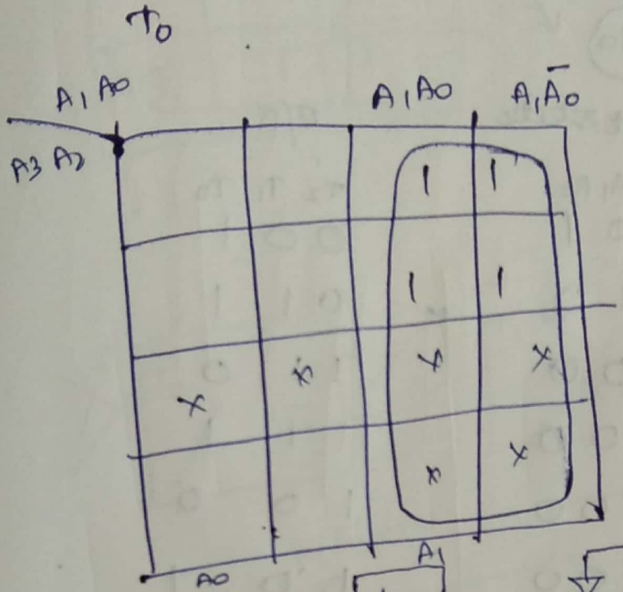
$T_2$



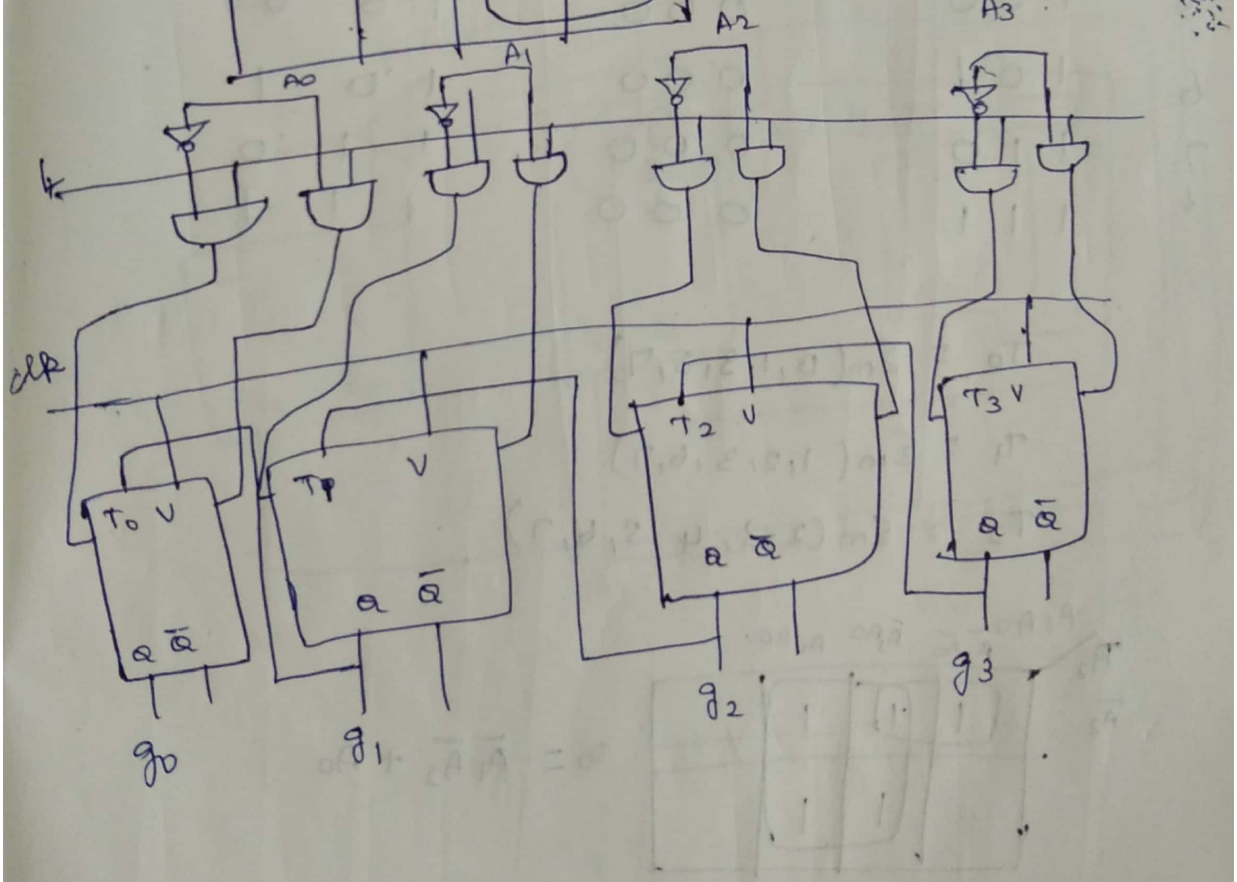

$T_2 = A_3$.



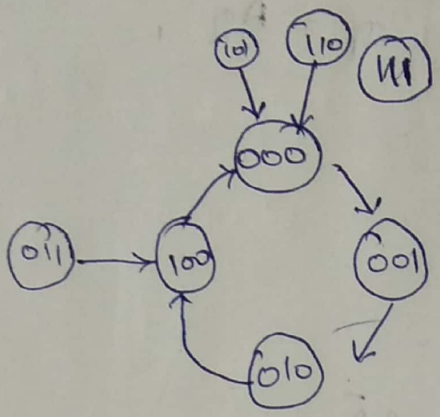

$T_1 = A_2$ .




$T_0 = A_1$ .



Design a synchronous counter that goes through 0, 1, 2, 4, 0. unused state must go to zero or to next state on next clock pulse.

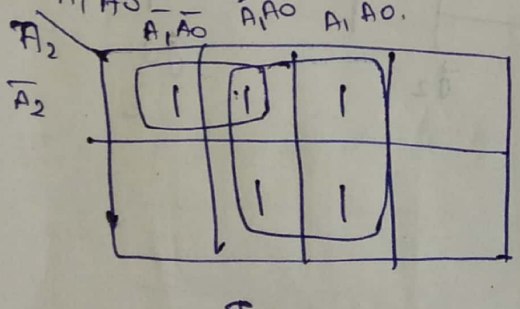



| | Present st $A_2$ $A_1$ $A_0$ | Next state $A_2$ $A_1$ $A_0$ | O/P $T_2$ $T_1$ $T_0$ |
|---|---|---|---|
| 0 | 0 0 0 | 0 0 1 | 0 0 1 |
| 1 | 0 0 1 | 0 1 0 | 0 1 1 |
| 2 | 0 1 0 | 1 0 0 | 1 1 0 |
| 3 | 0 1 1 | 1 0 0 | 1 1 1 |
| 4 | 1 0 0 | 0 0 0 | 1 0 0 |
| 5 | 1 0 1 | 0 0 0 | 1 0 1 |
| 6 | 1 1 0 | 0 0 0 | 1 1 0 |
| 7 | 1 1 1 | 0 0 0 | 1 1 1 |

$T_0 = \Sigma m(0,1,3,5,7)$

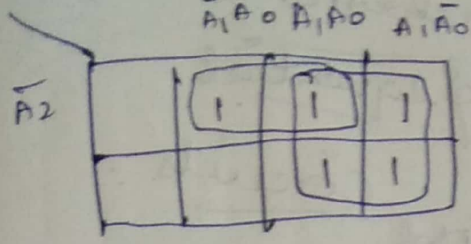
$T_1 = \Sigma m(1,2,3,6,7)$

$T_2 = \Sigma m(2,3,4,5,6,7)$



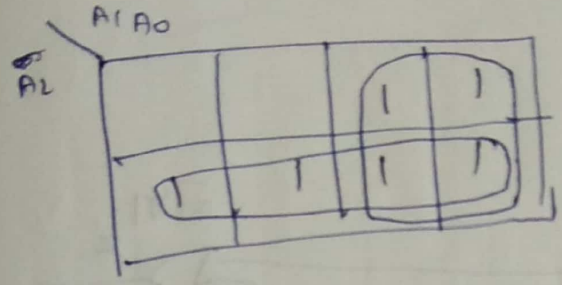

$T_0 = \bar{A}_1\bar{A}_2 + A_0$

$T_0$

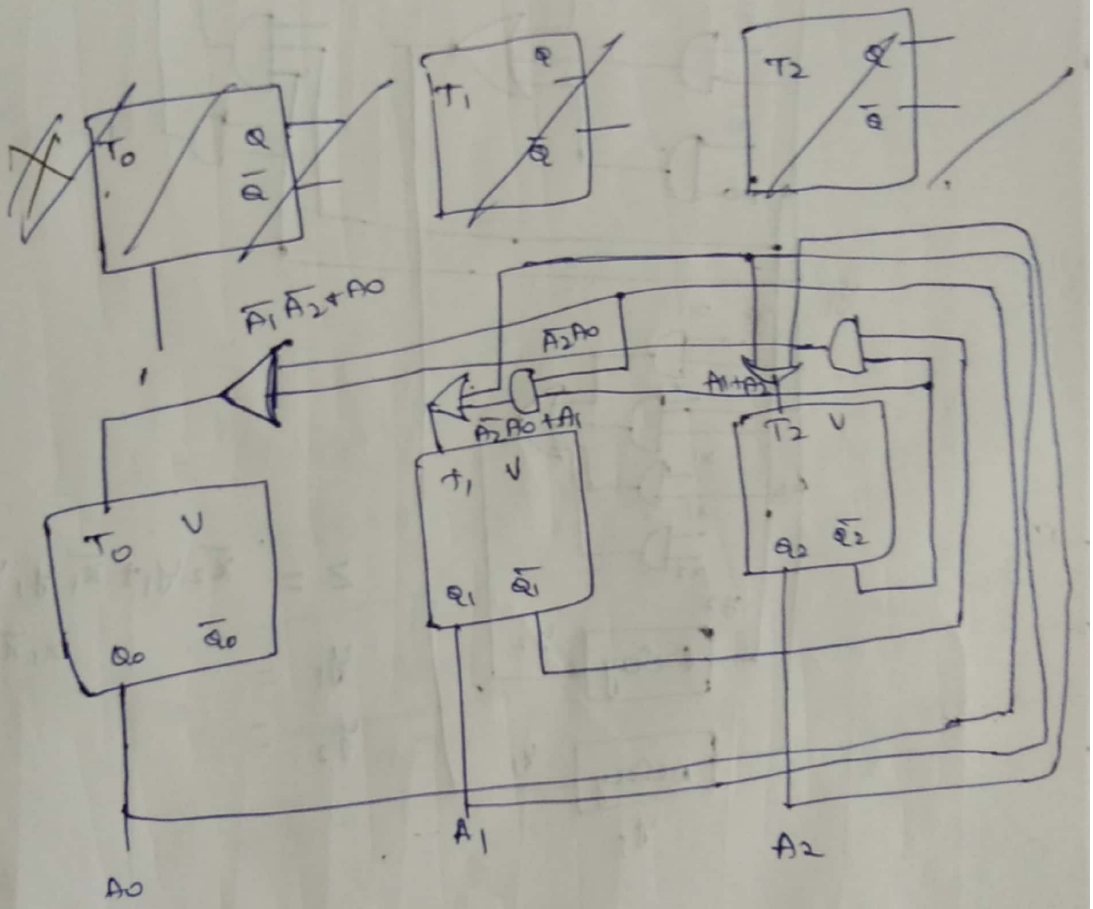



$T_1 = \bar{A}_2 A_0 + A_1$.

$T_2$ $T_1$.




$T_2 = A_1 + A_2$




— X —