DESIGN PROCEDURE FOR **ASYNCHRONOUS** SEQUENTIAL **CIRCUIT**

- There are 2 inputs x1 and x2 and a single output z

 The input x1 and x2 never changes simultaneously

 The output is always to be 0 when x1=0, independent of x2

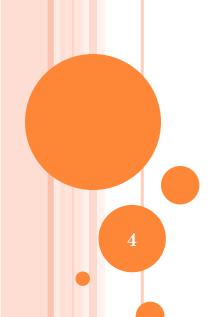
 The value of x2
 - and is to remain 1 until x1 becomes 0 again

EXAMPLE 9.3

Design a fundamental-mode asynchronous sequential network meeting the following requirements:

- 1. There are two inputs x_1 and x_2 and a single output z.
- 2. The inputs x_1 and x_2 never change simultaneously.
- 3. The output is always to be 0 when $x_1 = 0$, independent of the value of x_2 .
- 4. The output is to become 1 if x_2 changes while $x_1 = 1$ and is to remain 1 until x_1 becomes 0 again.

THE PRIMITIVE FLOW TABLE



OBTAINING PRIMITIVE FLOW TABLE

9/5/2018

Present state		Next	state			Outp	ut (z)	
	00	Input sta	ate (x_1x_2) 10	11	00	Input sta 01	ate (x_1x_2) 10	11
A	(A)				0			-

Present state Next state			Output (z)					
	00	Input sta	te (x_1x_2) 10	11	00	Input sta 01	te (x_1x_2) 10	11
A	A	В	C	_	0			
В		(B)			_	0	_	
C			0			_	0	
			(b)					
ARENA MI	\$ 11 mm & 1		h one, and				Co. H. Bial	

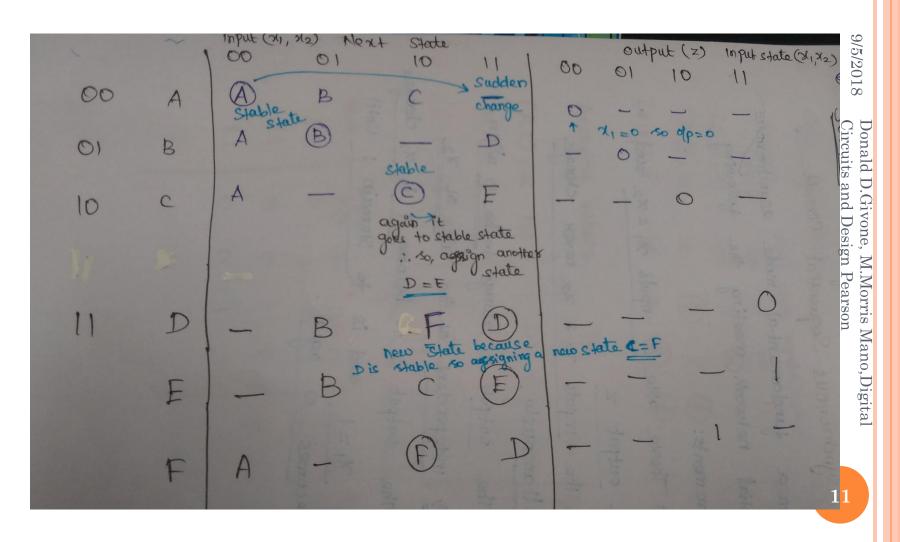
Present state Next state			Output (z)					
	00	Input sta 01	te (x_1x_2) 10	11	00	nput sta 01	te (x ₁ x ₂) 10	11
A	A	В	C	-	0	-	-	405
В	A	B	Yol-in	D	30+	0	-	460
C			0		11411	-	0	-
D				(D)	-	-	1004.00	0
			(c)					

Present state		Next state				Output (z)			
	00	Input sta	ate (x_1x_2) 10	11	00	nput sta 01	te (x_1x_2)	11	
A	A	В	C	-	0	-	-	-	
В	A	\bigcirc	0 = 2 0	D	-	0	-	111	
C	A	-	0	E	- 1	-	0		
D				(D)	10.77	-		1	
E				E		-	-		
			(d)						

Present state	nt state Next state				Output (z)			
	00	Input sta 01	ate (x_1x_2) 10	11	00	nput sta 01	te (x_1x_2) 10	11
A	A	В	C		0	_	_	-
В	A	B	_	D	_	0	_	_
C	A		0	E		-	0	_
D	_	В	F	(D)	- 5	_	_	0
E				E	-			1
F			F			_	1	
			(e)					

Present state		Next state			Output (z)			
	00	Input sta 01	te (x_1x_2) 10	11	00	nput sta 01	te (x_1x_2) 10	11
A	A	В	C	_	0	_	_	_
В	A	(B)	3973	D	11929	0		-
C	A	MANUAL MAN	(C)	E	S HOLD	MAN - 2 2.22	0	-
D	11110000	В	\widetilde{F}	(D)	21213	1-1-1200	in une	0
E	MARTHO	В	F	(E)	30304	SPATA)	4 12 14	1
F	A	111-111	(F)	E	16-1	-	1	-
			(f))				

SOLUTION



CONSTRUCTING THE MINIMUM ROW FLOW TABLE

Present state		Output (z)						
	00	Input sta 01	te (x_1x_2) 10	11 -	00 I	nput sta 01	te (x_1x_2) 10	11
$\{A,C\}:\alpha$	α	β	α	γ	0	-	0	-
$\{A,C\}$: α $\{B,D\}$: β	α	B	γ	B	-	0	-	0
$\{E,F\}$: γ	α	β	0	0	-	-	1	1

9/5/201

STATE REDUCTION

Palesent	Next S	01	10	11	00 00	ut (z) ilp 01 10 - 0	Donald D.Givone Circuits and Des
(A,c); \(\alpha\) (B,D); \(\beta\) (E,F); \(\gamma\)		B B B		(A)	O V	0 -	e, M.Morris Mano, Digital sign Pearson

Assigning values.	Circu
000	01 10 11 00 01 10 13
	OI OO II
(B,D); B 01 00	M.Morris n Pearson
(E,F); y 11 00	
71 D ₁ D	2 D1 D2 D1 D2 D1 D2

۵, ۹,	2,22	D1 10	"	OO OI 10 11 and
00	0	0 0	1	Givone, Mad Design
01	0	0 1	0	Non Pears
11	0	0 1	1	o 1 1 Mano, Digit

01 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Qox1, 7/2 + 2/9, + 2/12 = 90
D2 3172 01 00 01 11 10 01 0 1 1 1 0 11 0 1 1 1 0	Qox, + x2

CIRCUIT DIAGRAM

