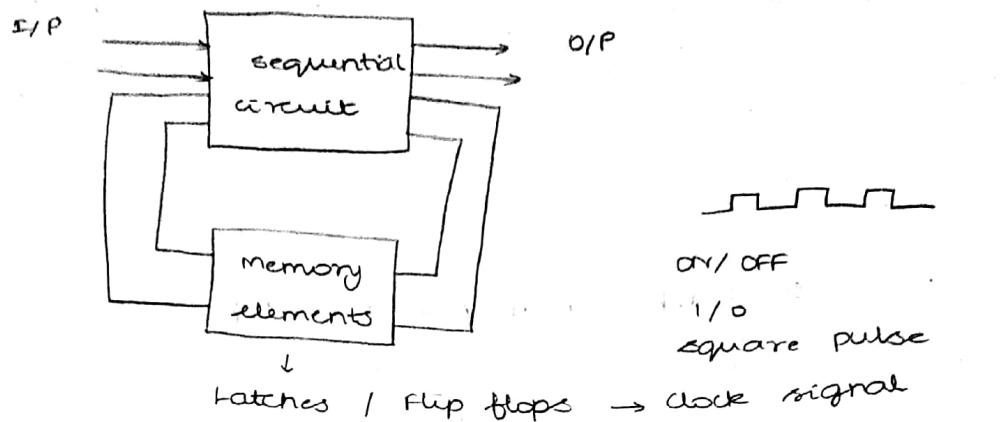
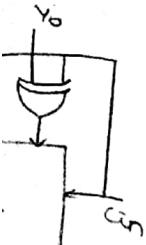


Synchronous Sequential circuits



latches :

level triggered
signals

flip flops :

edge triggered signals

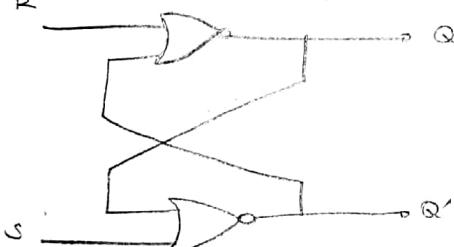


SR latch :

NOR NOR

implementation

reset



set

value retained on

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

0/0 combination

Q Q'

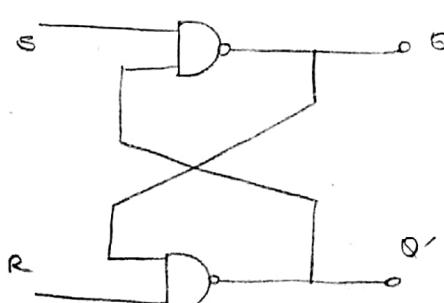
R	S	Q	Q'
0	0	1	0
0	1	1	0
1	0	0	1
0	0	0	1

Invalid

NAND

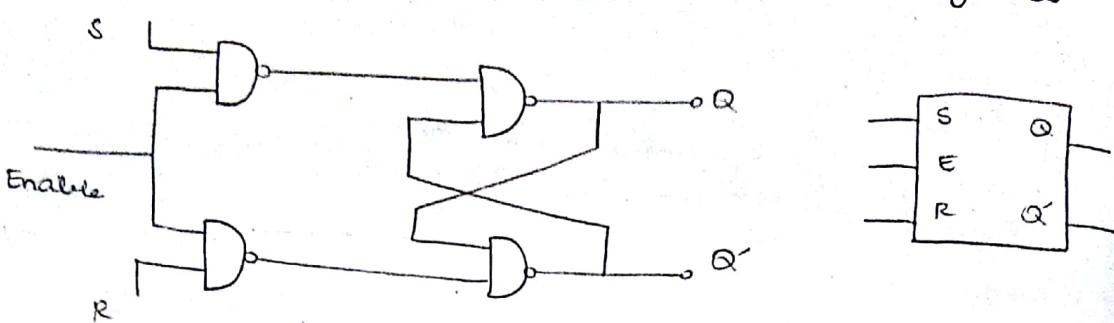
S	R	Q	Q'
0	1	1	0
0	1	1	0
0	0	0	1
1	1	0	1

Invalid

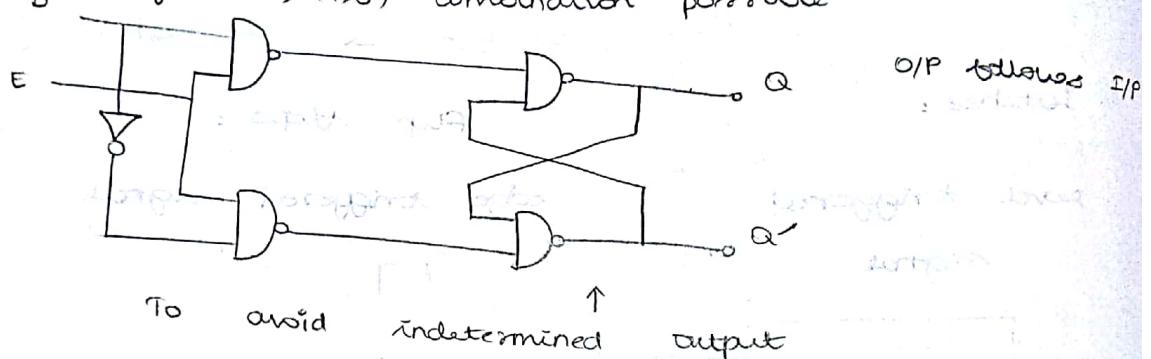


value retained on (1,1) combination

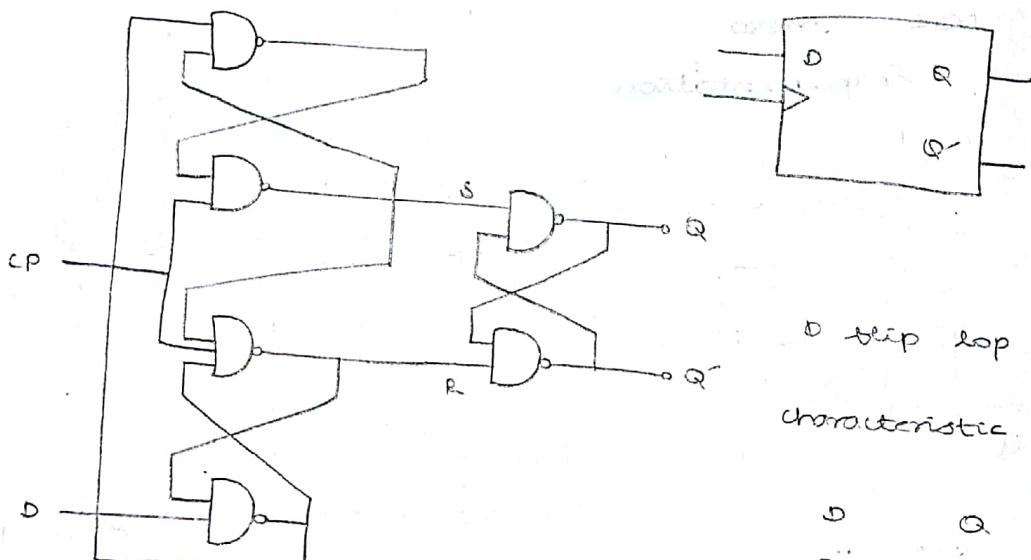
S-R latch with control input



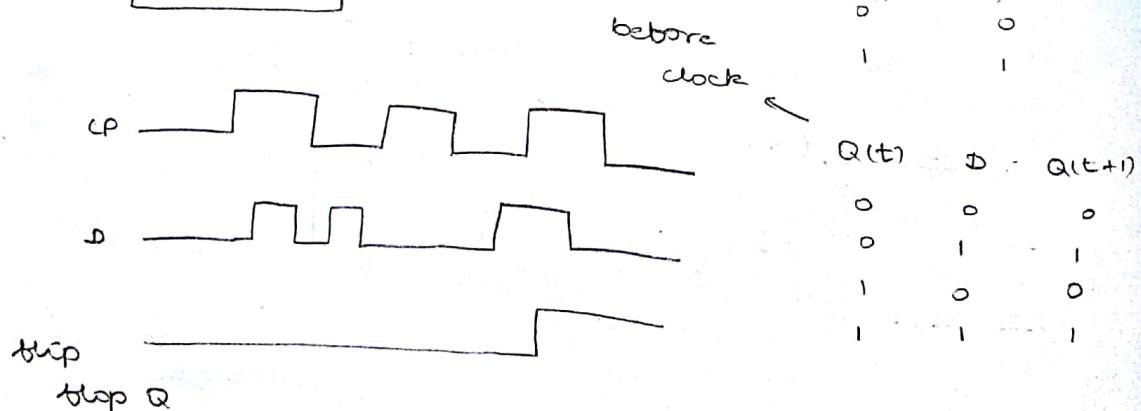
D-latch (transparent latch)
only (0,1), (1,0) combination possible



Positive edge triggered D-flip flop



D flip flop
characteristic table



S-R flip flop

$Q \quad S \quad R \quad Q(t+1)$

0 0 0 0

0 0 1 0

0 1 0 1

0 1 1 invalid

1 0 0 1 retained

1 0 1 0 previous output

1 1 0 1

1 1 1 invalid

$s \quad r \quad Q(t+1)$

0 0 Q(t)

0 1 0 → reset

1 0 1 → set

1 1 1 Invalid

characteristic table

$J-K$ flip flop

$Q \quad J \quad K \quad Q(t+1)$

0 0 0 0

0 0 1 0

0 1 0 1

0 1 1 toggle $\rightarrow T$ -flip flop

1 0 0 1

1 0 1 0

1 1 0 1

1 1 1 0

$J \quad K \quad Q(t+1)$

0 0 Q(t)

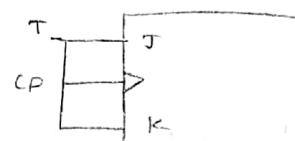
0 1 0

1 0 1

1 1 $\overline{Q(t)}$

$\rightarrow T$ -flip flop

(0,0) (1,1)



		JK				$Q(t+1)$
		00	01	11	10	
Q	0	0	1	1	1	2
	1	1	0	0	0	4 5 7 6

$$Y = Q\bar{K} + \bar{Q}J$$

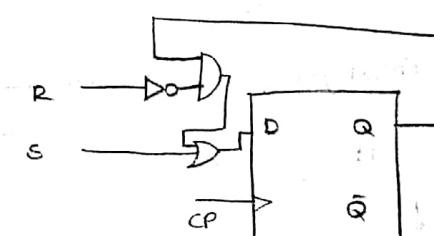
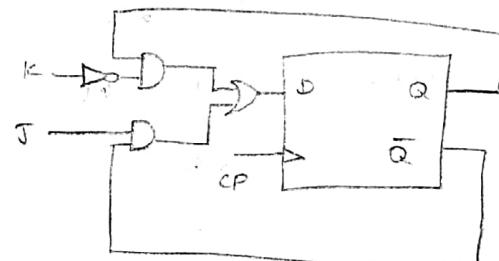
↓ characteristic eqn of

J-K flip flop

$$Y = Q\bar{K} + \bar{Q}J$$

T-K flip flop from D

flip flop



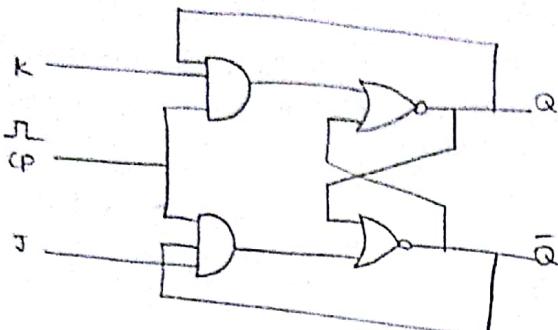
S-R flip flop from D flip

flop

		SR				$Q(t+1)$
		00	01	11	10	
Q	0	0	1	X	1	2
	1	1	0	S	R	4 5 7 6

$$Y = S + QR$$

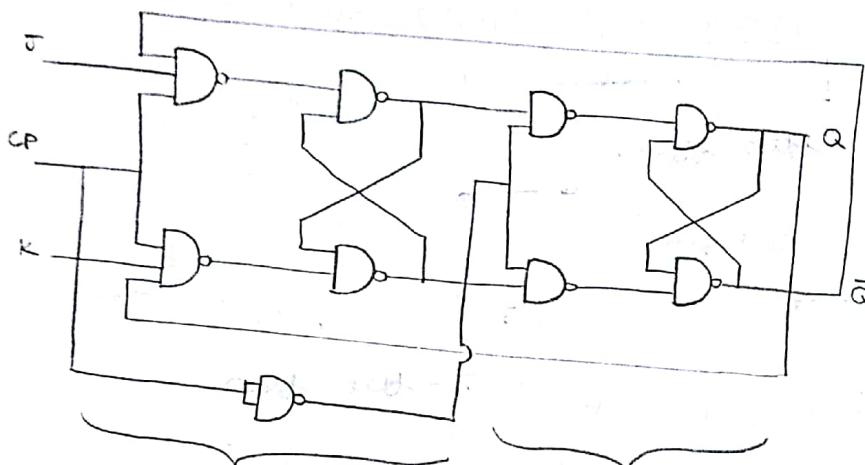
J-K flip flop



characteristic table

T	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

Master slave J-K FF



Q	J	K	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$$Q(t+1) = \bar{J}\bar{Q} + \bar{K}Q$$

D : characteristic equation
 $Q(t+1) = D$

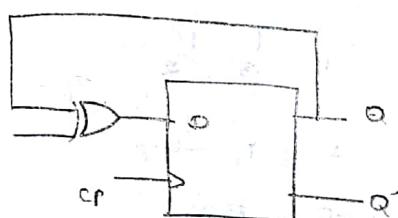
S-R : $Q(t+1) = S + \bar{R}Q$

J-K : $Q(t+1) = \bar{J}\bar{Q} + \bar{K}Q$

T : $Q(t+1) = \bar{Q}T + Q\bar{T}$
 $= Q \oplus T$

T	$Q(t+1)$
0	$Q(t)$
1	$\overline{Q(t)}$

Q	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0



Synchronous sequential T flip flop from
circuit

→ flip flop

Analysis Design

circuit, eqn

↓
eqn

↓
state table

↓
state diagram

Problem specification

↓
state table

↓
transition

↓
flip flop table

↓
equations

↓
logic diagram

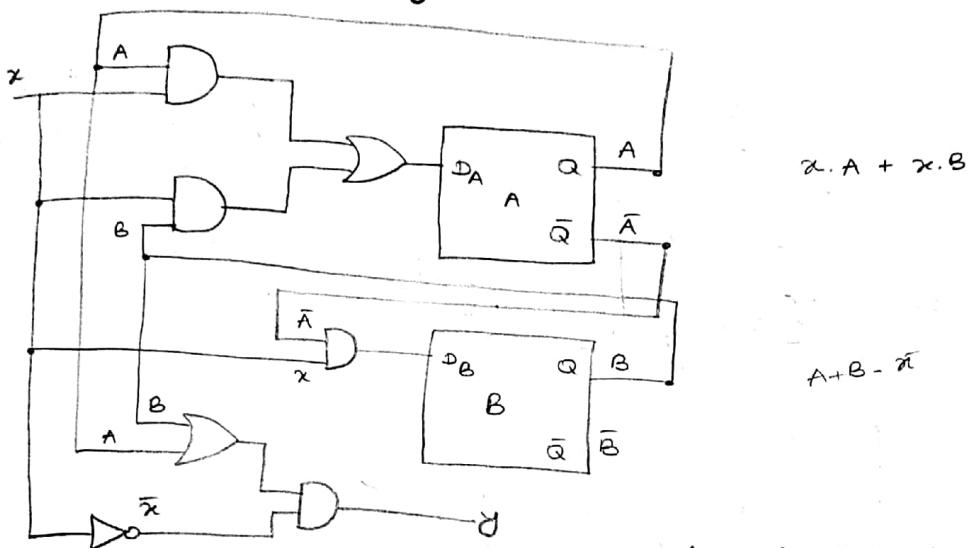
state table : present, next I/P, O/P

Excitation table : $Q(t) \rightarrow Q(t+1)$ for FF I/P
P.S N.S

Transition table : P.S, N.S, FF I/P

Characteristic table : I/P, sometimes previous I/P, bünd
next I/P

Analyses



characteristic eqn

Equations

$$Q(t+1) = D$$

D - flip flop

State equations, $A(t+1) = D_A = xA + xB = x(A+B)$

$$B(t+1) = D_B = x\bar{A}$$

$$\text{output equations} = A+B * \bar{x} = \bar{x}(A+B)$$

State table

P.S x	N.S	Output
A B 0 0 0	A(t+1) B(t+1) 0 0	Y 0
0 0 1	0 1	0
0 1 0	0 0	1
0 1 1	1 1	0
1 0 0	0 0	1
1 0 1	1 0	0
1 1 0	0 0	1
1 1 1	1 0	0

- 00 → a
- 01 → b
- 10 → c
- 11 → d

		Excitation table	
P.S	N.S	output y	
x=0	x=1	x=0	x=1
a	a	b	0
b	a	d	0
c	a	c	0
d	a	c	0

State diagram

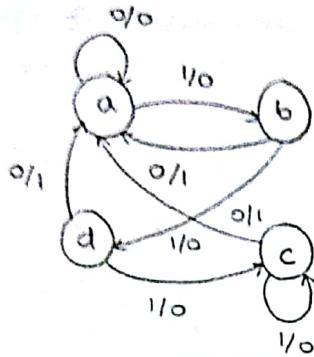
dependance of output

Mealy

P.S., I/P

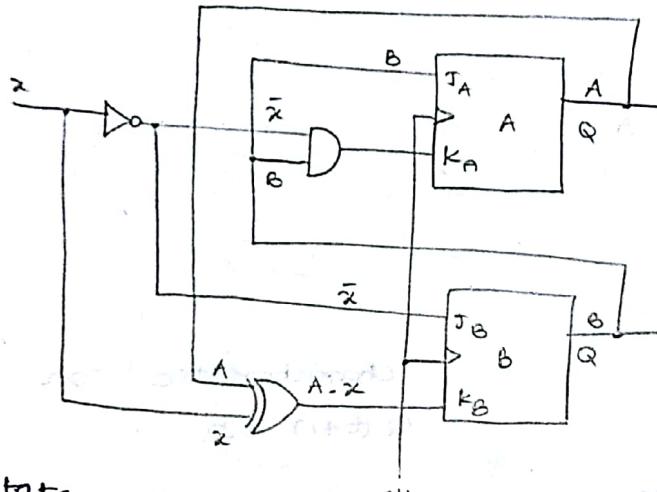
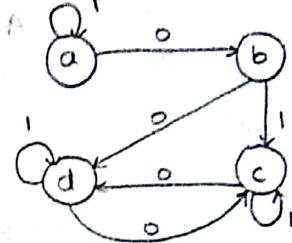
Moore

P.S.



State diagram

outputs



state eqns :

clk

characteristic equation $\Rightarrow Q(t+1) = J\bar{Q} + \bar{K}Q$

$$J_A = B$$

$$J_B = \bar{x}$$

$$K_A = \bar{x} \cdot B$$

$$K_B = A \oplus x$$

$$A(t+1) = B\bar{A} + \bar{x} \cdot B \cdot A = B\bar{A} + (\bar{x} + B)A$$

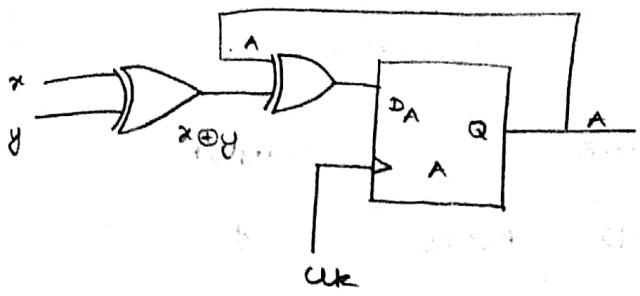
$$B(t+1) = \bar{x}\bar{B} + A \oplus x \cdot B = \bar{x}\bar{B} + (\bar{x} + \bar{x})B$$

State table

P.S

N.S

A	B	x	J_A	K_A	J_B	K_B	$A(t+1)$	$B(t+1)$
0	0	0	0	0	1	0	0	1
1	0	1	0	0	0	1	0	0
2	0	1	1	1	1	0	1	1
3	0	1	1	0	0	1	1	0
4	1	0	0	0	1	1	1	1
5	1	0	0	0	0	0	1	0
6	1	1	0	0	1	1	1	0
7	1	1	1	0	0	0	1	1



state eqns:

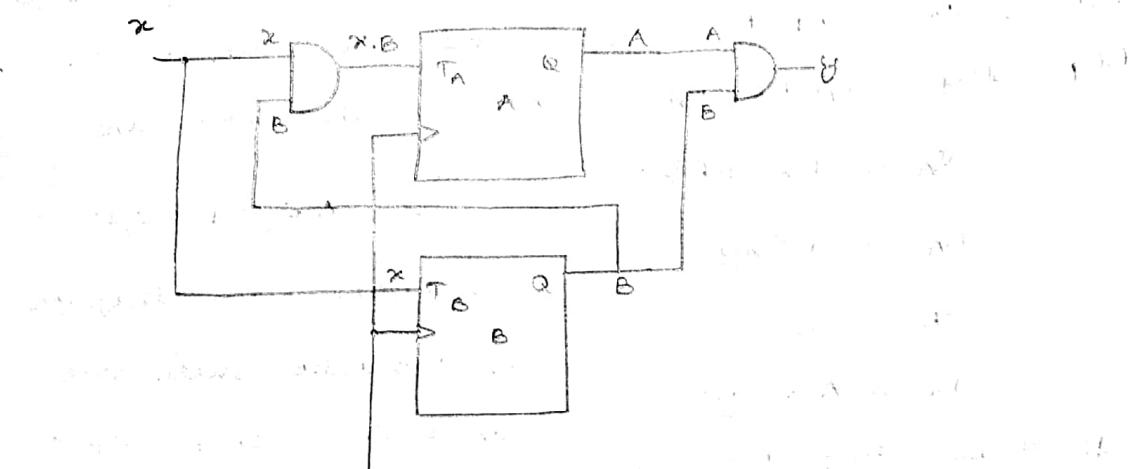
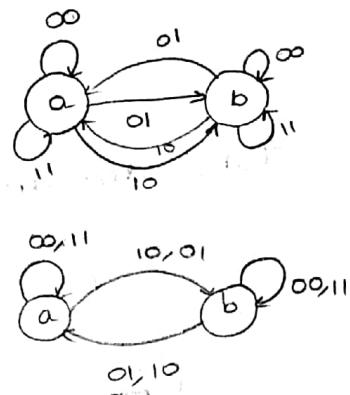
$$\text{characteristic eqn: } Q(t+1) = D$$

$$A(t+1) = D_A = (X \oplus Y) \oplus A$$

state diagram

state table:

P.S			N.C	
A	X	Y	$X \oplus Y$	$A(t+1)$
0	0	0	0	0
1	0	1	1	1
2	1	0	1	1
3	0	1	0	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1



State eqns:

$$\text{characteristic eqn: } Q(t+1) = Q \oplus T$$

$$A(t+1) = A \oplus T_A = A \oplus X \cdot B$$

$$B(t+1) = B \oplus T_B = B \oplus X$$

$$Y = A \cdot B$$

state eqn

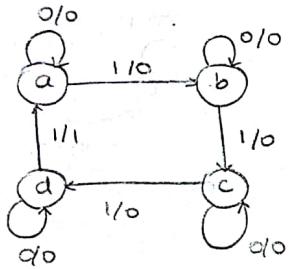
charac

 $A(t+1)$ $B(t+1)$ $Z =$

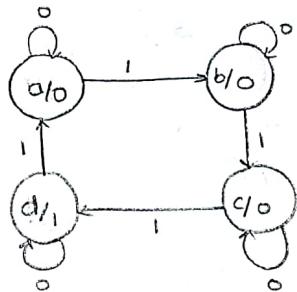
P.S

	P.S			N.S		output $A \cdot B$ Y
	A	B	X	$A \oplus X \cdot B$ $A(t+1)$	$B \oplus X$ $B(t+1)$	
a	0	0	0	0	0	0
	0	0	1	0	1	0
b	0	1	0	0	1	0
	0	1	1	1	0	0
c	1	0	0	1	0	0
	1	0	1	1	1	0
d	1	1	0	1	1	1
	1	1	1	0	0	1

State diagram: Mealy



Moore state



A sequential circuit has two J-K flip-flops A, B , two inputs x, Y and one output Z .

Flip flop input eqns and output eqns are

$$J_A = Bx + B'Y'$$

$$Z = Ax'Y' + Bx'Y$$

$$K_A = B'xy$$

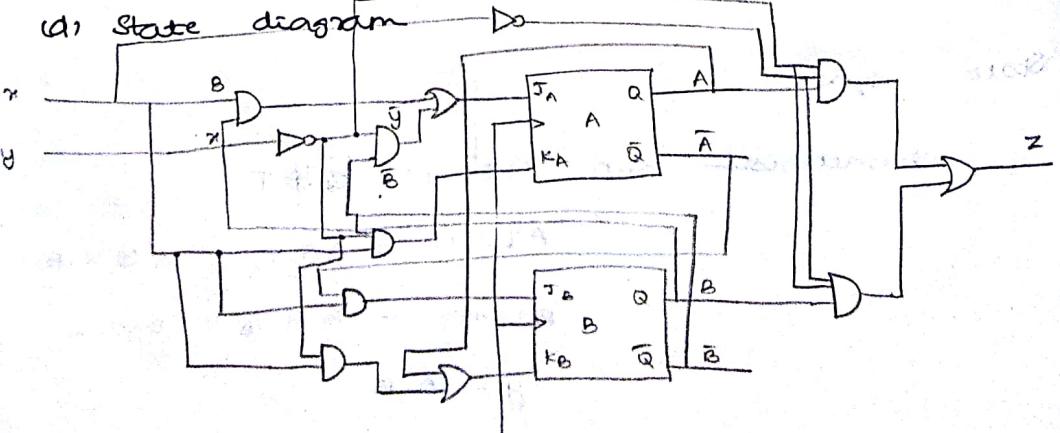
(a) draw logic diagram

$$J_B = A'x$$

(b) Tabulate state table

$$K_B = A + xy$$

(c) Derive state eqns



State

diagram

state eqns :

characteristic eqn : $Q(t+1) = J\bar{Q} + EQ$

$$A(t+1) = (Bx + B'y')\bar{A} + \overline{Bxy'} A$$

$$B(t+1) = Ax\bar{B} + \overline{A+xy'} B$$

$$Z = Ax'y' + Bx'y' \text{ depends on } x, y \rightarrow \text{Mealy}$$

P. &

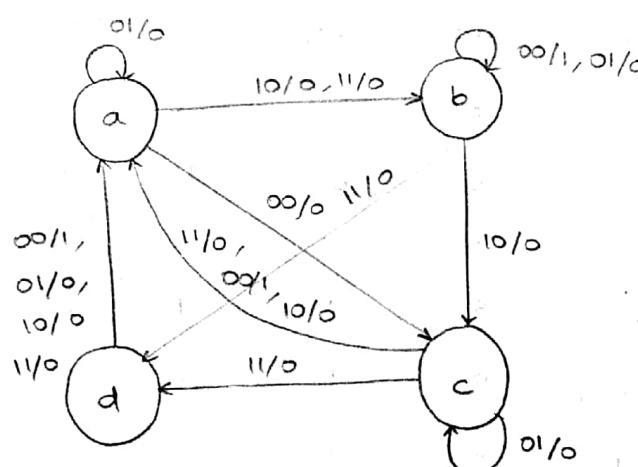
n. s

output

A a	B b	x	y	J _B	A(t+1)	B(t+1)	K _B	Z	J _A	K _A
0 0	0	0	0	0	1	0	0	0	1	0
1 0	0	0	1	0	0	0	0	0	0	0
2 0	0	1	0	1	0	1	1	0	0	1
3 0	0	1	1	1	0	1	0	0	0	0
4 0	1	0	0	0	0	1	0	1	0	0
5 0	1	0	1	0	0	0	0	0	0	0
6 0	1	1	0	1	1	0	1	0	0	0
7 0	1	1	1	1	1	1	0	0	1	0
8 1	0	0	0	0	0	0	0	1	1	0
9 1	0	0	1	0	0	0	1	1	1	0
10 1	0	1	0	0	0	0	1	0	0	0
11 1	0	1	1	0	0	0	1	0	1	1
12 1	1	0	0	0	0	0	1	0	0	0
13 1	1	0	1	0	0	0	1	1	0	0
14 1	1	1	0	0	0	0	1	0	0	0
15 1	1	1	1	0	0	0	1	0	0	0

state

diagram :



Design of clocked sequential logic circuits

Problem statement

Implication /

now ← Reduce the states
elimination

Method

state table

Logical diagram

All state lines → Binary coded state table

Binary ↘

gray

one hot

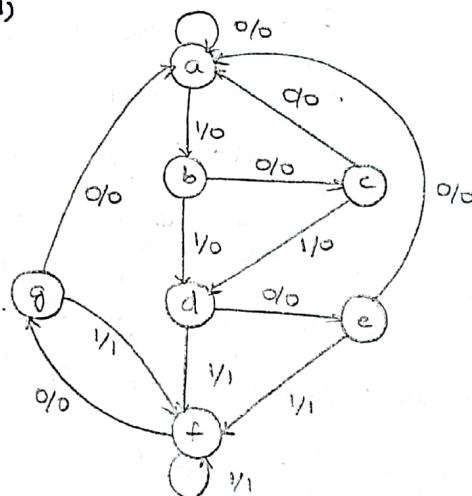
flip flop I/P & O/P
seq. ckt O/P & I/P

✓ FF I/P, O/P of SC

Excitation table

State reduction by now elimination method

1)



1st

States a b d e f f f f f f f f

x 1 1 0 1 1 1 1 0 1 1 0

2nd

States a b d e d d d d d d d e

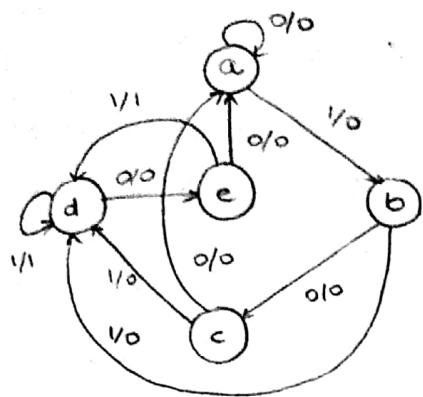
x 1 1 0 1 1 1 1 0 1 1 0

y 0 0 0 1 1 1 1 0 1 1 0

Reduced state table

P.S	N.S	State table		Reduced state table	
		O/P Y		O/P Y	
		X=0 X=1		X=0 X=1	
a	a	b	0	0	a
b	c	d	0	0	b
c	a	d	0	0	c
d	e	f	0	1	d
e	a	f	0	1	e
f	g	*	0	1	a
g	a	*	0	1	b

reduced state diagram



States $a + b + c + d + g + h + a' + b' + c' + d' + g' + h' = f$
 $a = 0 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 1 \ 0$
 $b = 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0$

States $a + b + c + b' + d + g + g' + d' + a + b + a' + f$
 $a = 0 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 1 \ 0$
 $b = 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0$

2) State table

P.S	N.S	O/P Y
x=0	x=1	x=0
a	f	b
v b	d	xa
x c	f	xb
v d	θ	a
x e	d	c
f	f	b
g	θ	kd
x h	g	a

Reduced state table

P.S	N.S	O/P Y
x=0	x=1	x=0
a	oo	f
b	01	d
c	00	a
d	10	θ
e	11	f
f	11	b
g	0	d
h	1	0

5 states $\Rightarrow 2^n - 2^2 = 4$
 \downarrow

$n \rightarrow$ bits not sufficient

so $n = 3$

A B C n = 3 : FF

Binary Assignment

Binary	Gray	Onehot
000	000	00001
001	001	00010
010	011	00100
011	010	01000
100	110	10000

} FF representation

excitation table

S-R flip flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S-K flip flop

Q(t)	Q(t+1)	S	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D - flip flop

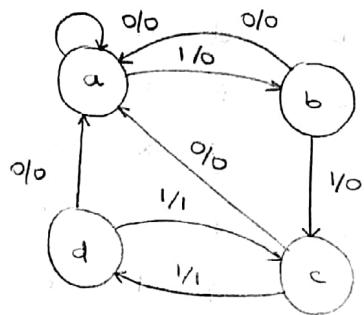
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

T - flip flop

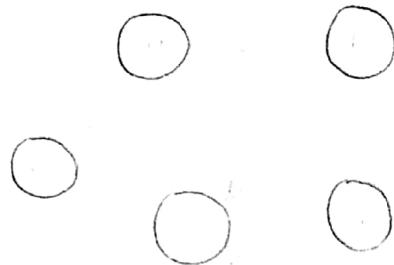
$Q(t)$	$Q(t+1)$	T
0	0	1
0	1	0
1	0	1
1	1	0

Design a sequential logic circuit to detect the sequence of 3 consecutive 1's or more. Use D-flip flop

Mealy state M/c



Moore state M/c



State table

P.S	$x = 0$		$x = 1$		O/P z
	N.S	I/P	N.S	I/P	
a	a	b	0	0	
b	a	c	0	0	
c	a	d	0	1	
d	a	c	0	1	

Transition table using D - flip flop

P.S	I/P	x	N.S		O/P z	D_A	D_B
			A(t+1)	B(t+1)			
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1
1	1	0	0	0	0	0	0
1	1	1	1	0	1	1	0

	B(t)x			
A(t)	00	01	11	10
0	0	0	0	0
1	4	5	7	6

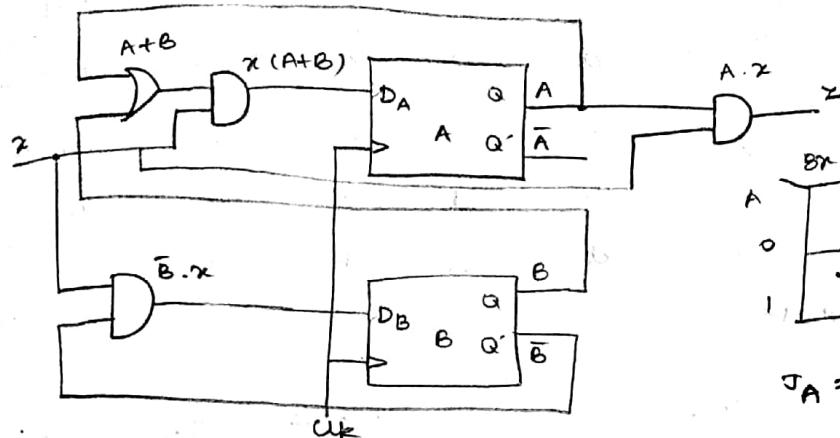
	Bx			
A	00	01	11	10
0	0	0	1	0
1	0	1	1	0

	Bx			
A	00	01	11	10
0	0	1	0	2
1	0	1	5	7

$$z = A(t)x$$

$$D_A = Ax + Bx$$

$$D_B = \bar{B}x$$



	Bx			
A	00	01	11	10
0	0	0	1	0
1	x ₄	x ₅	x ₇	x ₆

$$J_A = Bx$$

Transition table using S-K flip flop

P.S	I/P	N.S	O/P	S _A	K _A	S _B	K _B
A	B	x	A(t+1)	B(t+1)			
0	0	0	0	0	0	x	0
0	0	1	0	1	0	x	1
0	1	0	0	0	0	x	x
0	1	1	1	0	1	x	1
1	0	0	0	0	x	1	0
1	0	1	1	1	x	0	1
1	1	0	1	0	x	1	x
1	1	1	1	0	x	0	x

	Bx			
A	00	01	11	10
0	x ₀	x ₁	x ₃	x ₂
1	1	D ₅	D ₇	D ₆

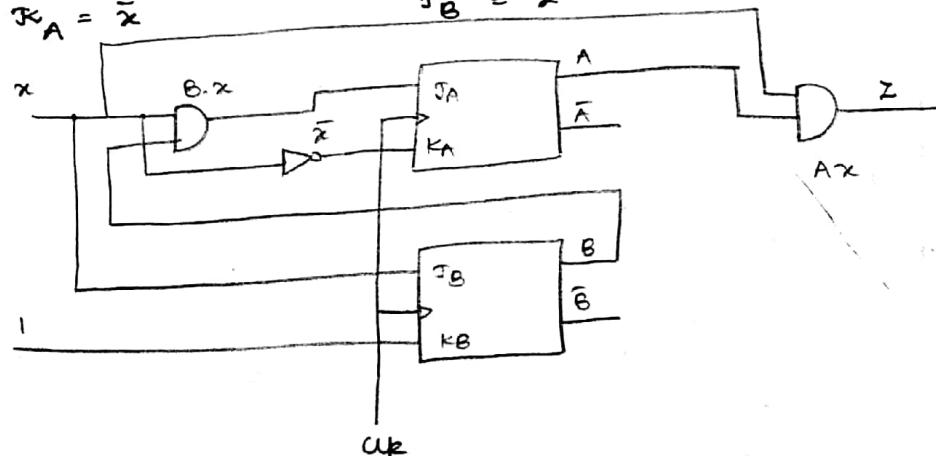
	Bx			
A	00	01	11	10
0	0	1	x ₃	x ₂
1	0	1	x ₅	x ₇

	Bx			
A	00	01	11	10
0	x ₀	x ₁	1	1
1	x ₄	x ₅	1	1

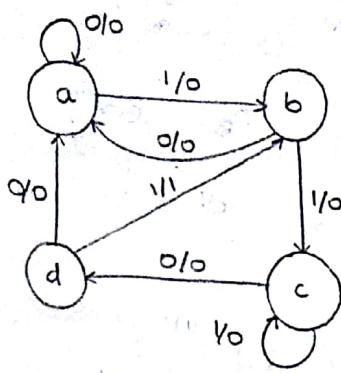
$$K_A = \bar{x}$$

$$S_B = x$$

$$K_B = 1$$



Design a sequential logic circuit to detect the sequence 00101. Using T flip flop



State table

P.S	N.S	O/P Z	
x=0	x=1	x=0	x=1
a	a	b	0
b	a	c	0
c	d	c	0
d	a	b	1

Transition table

P.S	N.S	A	B	x	A(t+1)	B(t+1)	O/P Z
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	1	0	0	0	0	0	1
0	1	1	0	1	0	0	1
1	0	0	0	1	1	0	0
1	0	0	1	1	0	0	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	1	0

A	Ex	00	01	11	10
0	0	0	0	0	0
1	0	4	5	1	6

A	Ex	00	01	11	10
0	0	1	1	0	1
1	0	4	5	1	6

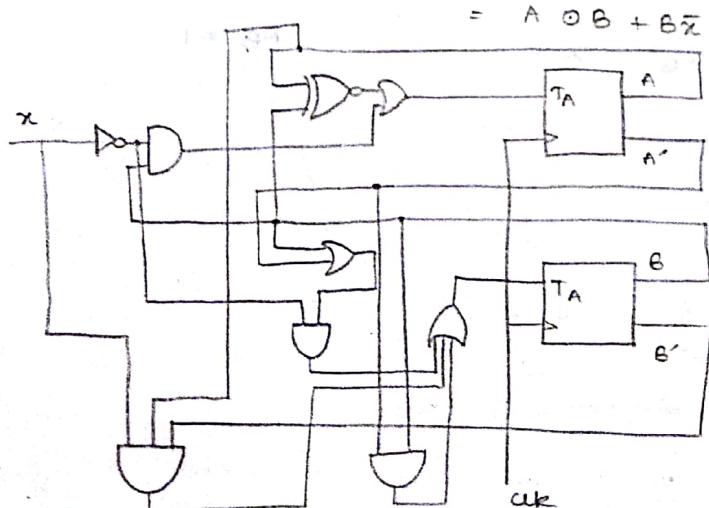
A	Ex	00	01	11	10
0	0	1	0	1	2
1	0	4	1	5	6

$$Z = ABx$$

$$T_A = \bar{A}\bar{B} + B\bar{x} + AB \\ = A \oplus B + B\bar{x}$$

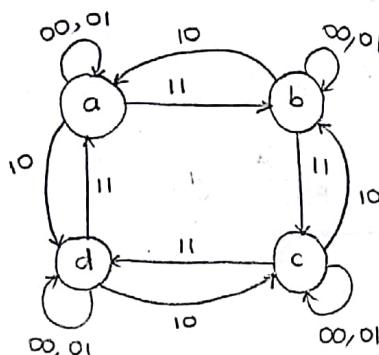
$$T_B = \bar{A}\bar{x} + \bar{A}B + A\bar{B}x$$

$$= \bar{x}(\bar{A} + B) + A\bar{B}x \\ AB$$



Design a sequential logic circuit that has two JK

- flip flops A, B and two I/P E, F. If E=0, circuit remains in same state regardless of value of F. When E=1, F=1, circuit goes through state transitions from 00 to 01, to 10, to 11, back to 00 and repeats. When E=1, F=0, circuit goes through state transitions from 00 to 11, to 10, to 01, back to 00 and repeats.



State table

P.S	N.S	O/P Z
	x y	x y
	00 01 10 11	0 1 0 1

EF	00	01	11	10
AB	00	0	0	1
	01	0	1	0
	11	X	X	X
	10	X	X	X

$$\begin{aligned}
 J_A &= \bar{B}EF + B\bar{E}F \\
 &= E(\bar{B}F + BF) \\
 &= E(B \oplus F)
 \end{aligned}$$

EF	00	01	11	10
AB	X	X	X	X
	X	X	X	X
	0	0	0	0
	1	1	1	1
	2	0	0	0
	3	0	0	0
	4	1	0	0
	5	0	1	0
	6	0	1	0
	7	0	1	1
	8	1	0	0
	9	1	0	1
	10	1	0	0
	11	1	1	0
	12	1	0	0
	13	1	0	1
	14	1	1	0
	15	1	1	1

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	1
0	0	X	0
1	0	X	0
0	1	X	0
1	1	X	0

Transition table

P.S	N.S	J _A	K _A	J _B	K _B
A B	E F	A(t+1)	B(t+1)		
0 0	0 0	0	0	0	X
1 0	0 1	0	0	0	X
2 0	1 0	1	1	1	X
3 0	0 1	0	0	0	0
4 b	0 1	0	1	0	X
5 0	1 0	0	0	0	1
6 0	1 1	0	0	1	X
7 0	1 1	1	0	0	X
8 1	0 0	0	0	0	0
9 1	0 1	0	1	1	X
10 1	1 0	0	1	0	1
11 1	1 1	1	1	0	0
12 1	0 0	1	0	0	X
13 1	1 0	0	0	1	X
14 1	1 1	0	1	0	1
15 1	1 1	1	1	1	1

AB	00	01	11	10
EF	0	0	1	1
AB	00	X	X	X
EF	0	1	3	2
AB	01	X	X	X
EF	4	5	7	6
AB	11	X	X	X
EF	12	13	15	14
AB	10	8	9	11
EF	10	11	14	10

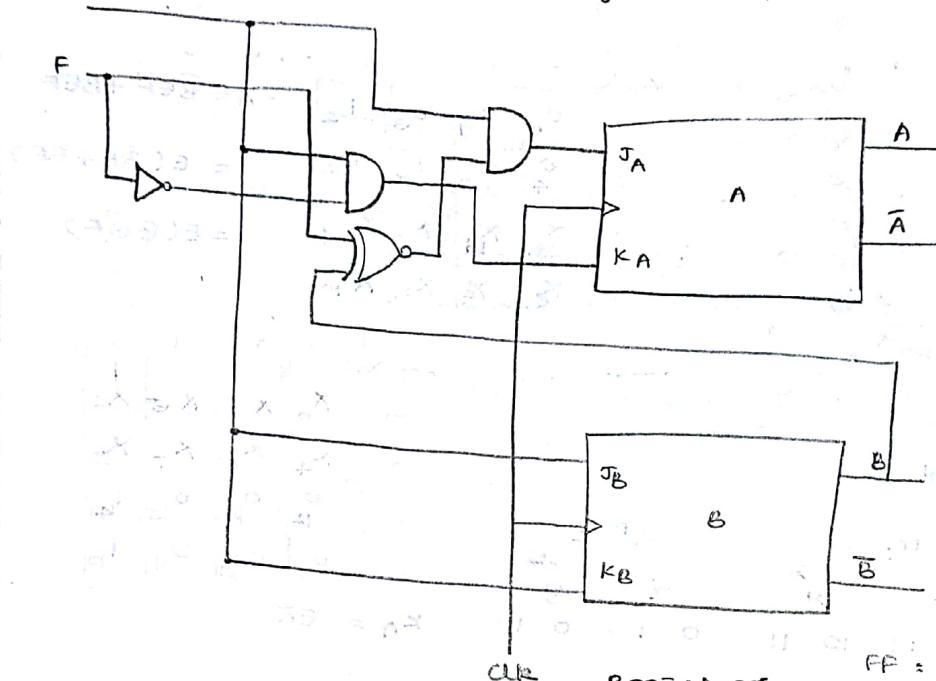
$$\sigma_B = E$$

AB	00	01	11	10
EF	X	0	K ₃	K ₂
AB	00	0	1	1
EF	4	5	7	6
AB	11	X	X	X
EF	12	13	15	14
AB	10	X ₈	X ₉	X ₁₁
EF	X ₈	X ₉	X ₁₁	X ₁₀

$$K_B = E$$

E

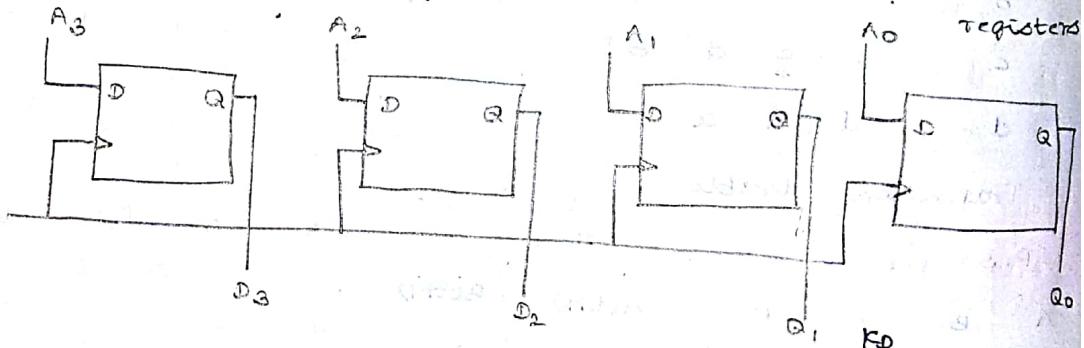
logic diagram



FF : Stores 1 bit information

4-bit Registers

D, FF are used in



Shift register: < left shift
right shift

SISO

SIPO

PISO

common clock

PIPO (since synchronous

sequential circuits)

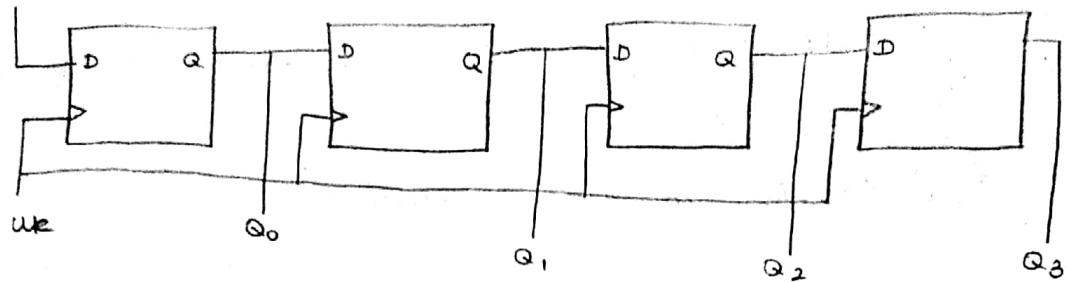
AB	00	01	11	10
EF	0	1	3	2
AB	01	X	5	X
EF	4	5	7	6
AB	11	X	X	X
EF	12	13	15	14
AB	10	X ₈	X ₉	X ₁₁
EF	X ₈	X ₉	X ₁₁	X ₁₀

n-bit \rightarrow n-number of flip flops

For each clock signal, a single unit gets shifted

SISO shift registers # FF = # clock cycles

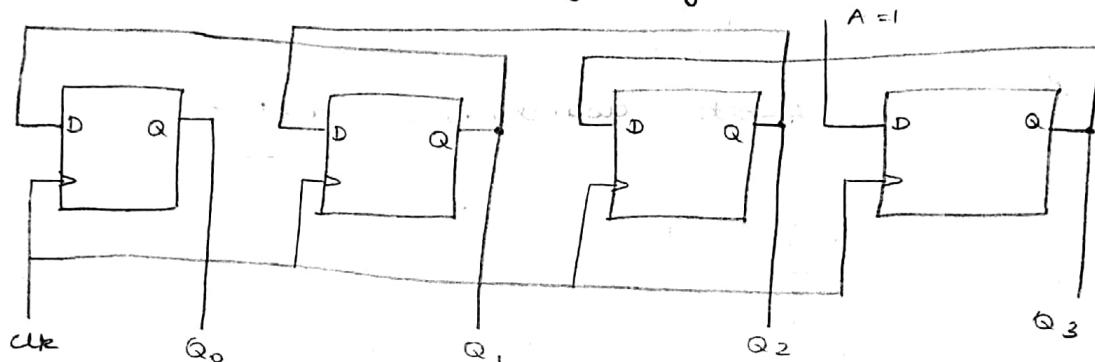
A = 1



4.

div left reg
mul right reg

SISO PISO shift registers



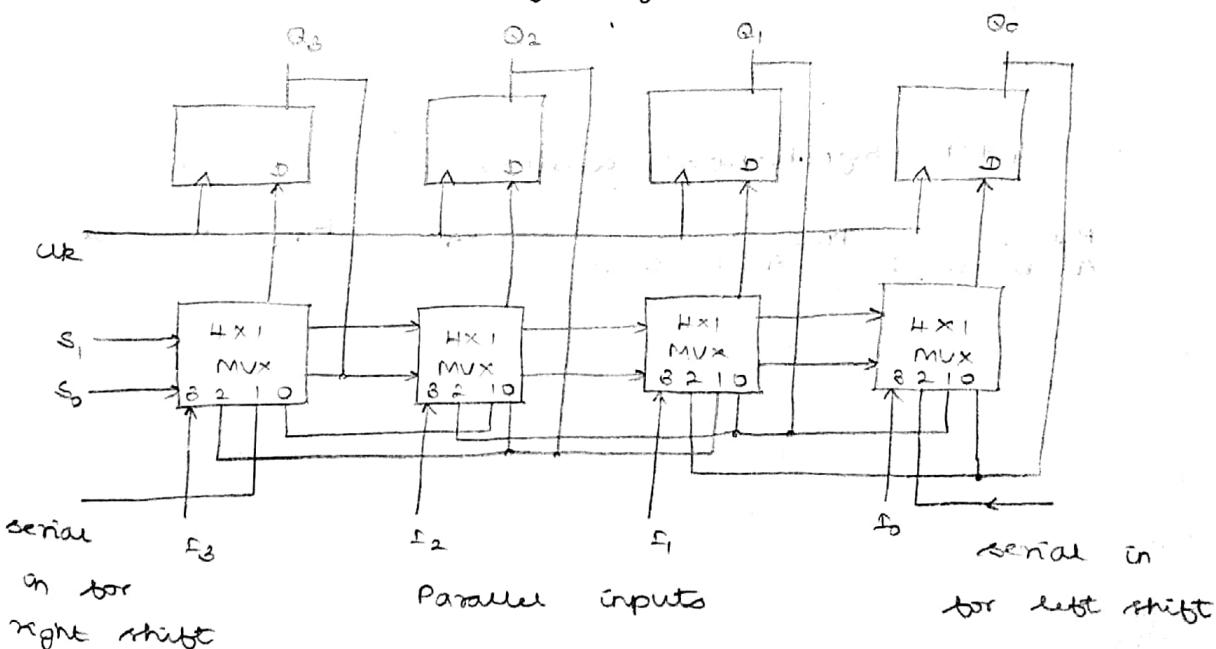
SISO

clk	Q ₀	Q ₁	Q ₂	Q ₃
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0

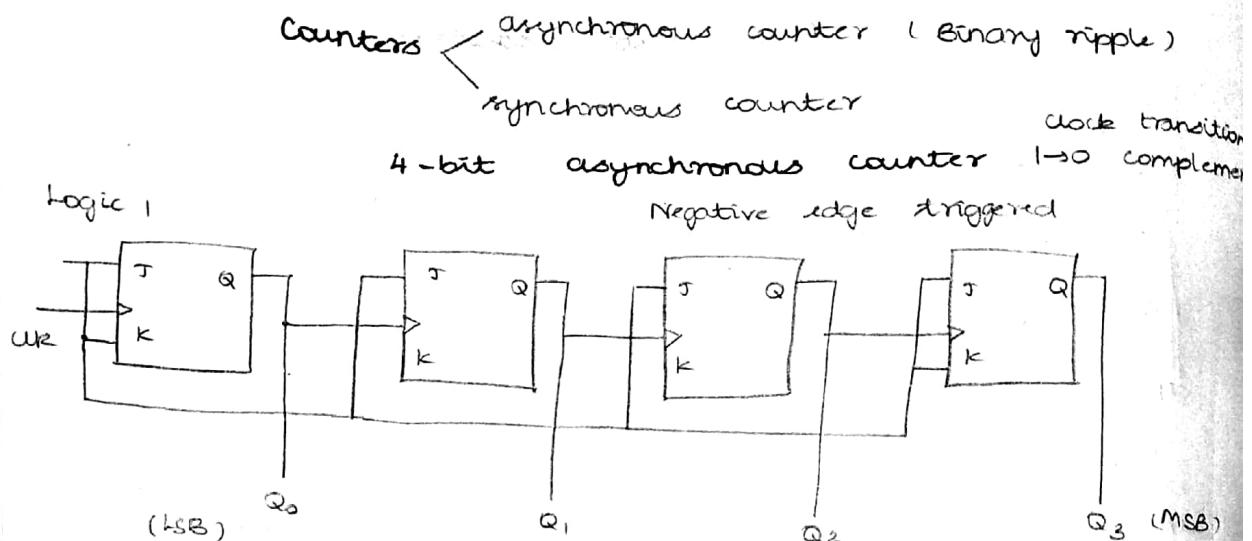
SIPO

clk	Q ₀	Q ₁	Q ₂	Q ₃
1	1	1	0	0
2	1	1	0	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1

Universal shift registers



S . S
 0 0 No change
 0 1 right shift \rightarrow output: Q_0
 1 0 left shift \rightarrow output: Q_3
 1 1 Parallel in 01, 10 combo can be loaded in
 this and respective observations
 can be made



$Q_3 \quad Q_2 \quad Q_1 \quad Q_0$

1st FF - accepts original

clk signal

0 0 0 1
 0 0 1 0

Remaining FF accepts clk

0 0 1 1
 0 1 0 0

from output of 3rd before FF

0 1 0 1
 1 1 x 0

00 0x
 01 1x
 10 x1
 11 x0

4, 6, 8, 10, 11, 12, 13, 14

Dont care

4-bit Synchronous counter

P.S	A	B	C	D	N.S	A	B	C	D	J _A	K _A	J _B	K _B
0	0	0	0	0	0	0	0	0	1	0	x	0	x
1	0	0	0	1	0	0	0	1	0	0	x	0	x
2	0	0	1	0	0	0	1	0	1	0	x	1	x
5	0	1	0	1	0	0	0	1	1	0	x	x	1
3	0	0	1	1	0	0	1	1	1	0	x	1	x
7	0	1	1	1	1	0	0	1	1	1	x	0	x
9	1	0	0	1	1	0	0	1	1	x	1	x	1
15	1	1	1	1	0	0	0	1	1	x	1	x	1

J_C	K_C	T_D	K_D
0	x	1	x
1	x	x	1
x	1	1	x
1	x	x	0
x	0	x	0
1	x	x	0
x	1	x	0
0	x	x	0
x	1	x	0

J_A	00	01	11	10
AB	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{15}	x_{14}
10	x_8	9	x_{11}	x_{10}

K_A	00	01	11	10
CD	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{15}	x_{14}
10	x_8	9	x_{11}	x_{10}

J_B	00	01	11	10
CD	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{14}	x_{15}
10	x_8	9	x_{11}	x_{10}

P_B	00	01	11	10
AB	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{15}	x_{14}
10	x_8	9	x_{11}	x_{10}

J_C	00	01	11	10
PB	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{15}	x_{14}
10	x_8	9	x_{11}	x_{10}

K_C	00	01	11	10
CD	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{15}	x_{14}
10	x_8	9	x_{11}	x_{10}

T_D	00	01	11	10
AB	00	01	11	10
00	0	1	3	2
01	x_4	5	7	x_6
11	x_{12}	x_{13}	x_{15}	x_{14}
10	x_8	9	x_{11}	x_{10}