Design of Asynchronous seq. circuit

↓

prob statement

↓

Primitive flow table

↓

reduced flow table → Implication table

↓

Transition table

↓

eqns using kmap.
(state eqns & o/p eqns)

↓

logic diagram

State table

1. Row elim
2. Implication table.

Implication table ↓

compatible pair

↓

maximal compatibles (using merger graph diagram)

& closed covering condition

↓

reduced flow table

if it has
3 values (states)
use 0, 1

1 a
0 b

4-state (2 bit)
more than 4 (3 bit)

State table reduced from Implication table.

1.Q)

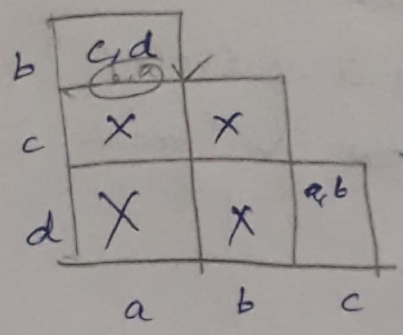
Q)

P.S	N.S x=0	N.S x=1	o/p x=0	o/p x=1
a	c	b	0	1
b	d	a	0	1
c	a	d	1	0
d	b	d	1	0

i/p o/p are equal, check the next state

→ equal check n.s

soln (a,b) imply (c,d)



Vertical & horizontal (states)
from 2nd
from 1 elim last.

(for comparison purpose)

when o/p are unequal put X

* once ad is checked, no need to check d and c

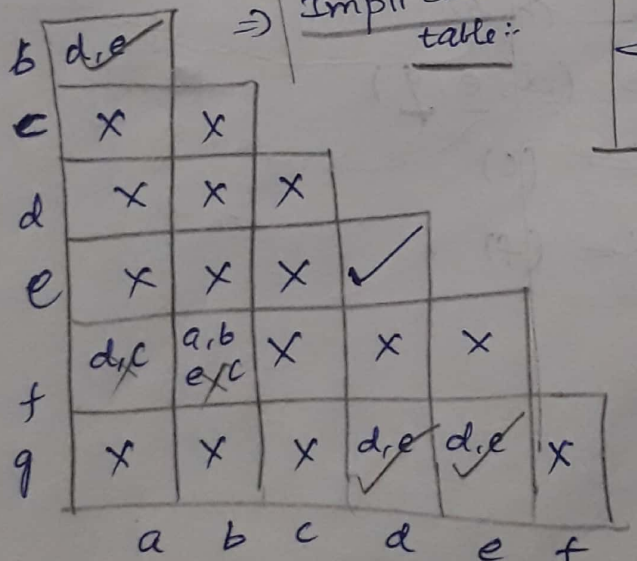
Q.2)

2)a)

State table

P.S	N.S x=0	N.S x=1	o/p x=0	o/p x=1
a a	d	b	0	0
a b	e	a	0	0
c c	g	f	0	1
d d	a	d	1	0
d e	a	d	1	0
f f	c	b	0	0
d g	a	e	1	0

soln ⇒ Implication table:



both are same	✓
both are x same	X

Then find '✓', combination of (d,e) check for implied state.

Where ever (d,e) → it is equivalent
⇒ (a,b) = (d,e) ⇒ put '✓' mark

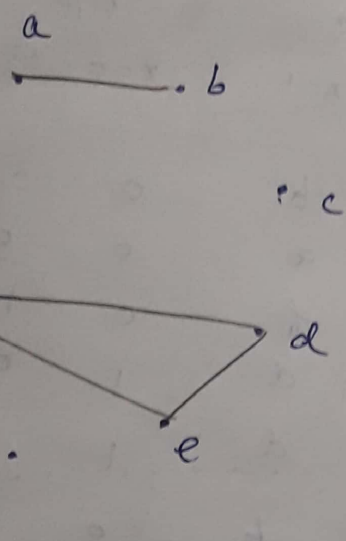
'✓' ⇒ compatible pairs.

(a,b) (d,e) (d,g)(e,g)

write '✓' as compatible pairs.

Merger diagram:

join corresponding compatible pairs with lines

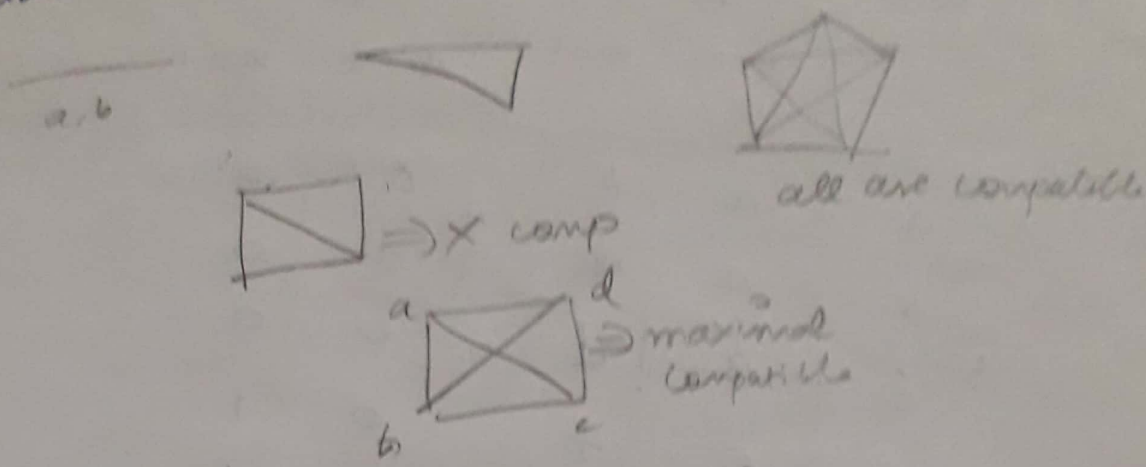


If they are not connected → take as individual states.

maximal compatible pairs.

take
- a ⇐ (a,b) → replace by a
- d ⇐ (d, e, g) → replace by d
- c ⇐ (c)
- f ⇐ (f)

1 state connected to each & every state, all states are compatible



(applicable for all polygons)

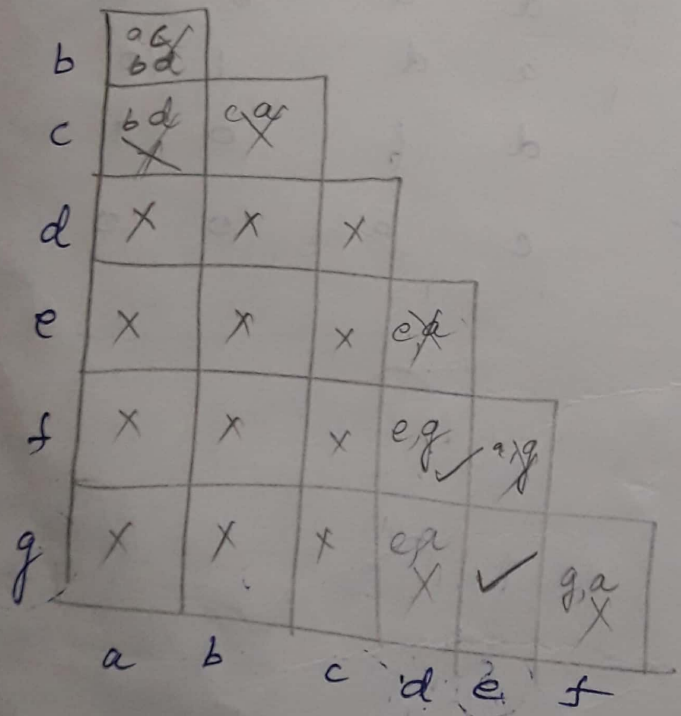
Reduced ~~state~~ table, from given ~~table~~ state table:

P.S	N.S		O/P	
	x=0	x=1	x=0	x=1
a	d	a	0	0
d	a	d	1	0
c	d	f	0	1
f	c	a	0	0

B(Q)

P.S	N S		o/p	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f d	0	1
e	a	f d	0	1
f	g e	f d	0	1
g	a	f d	0	1

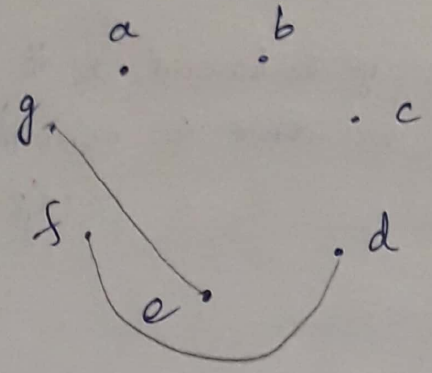
soln: implication table



compatible pairs:-

(g,e) (d,f) (a) (b) (c).

Merger diagram

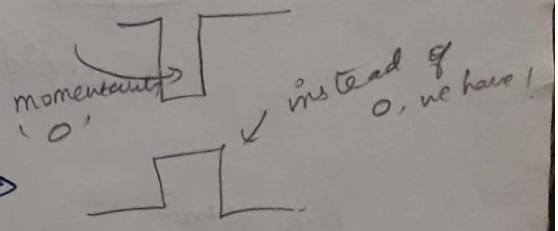


Reduced state table

P.S	N.S		O/P	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
e	e	d	0	1
d	a	d	0	1

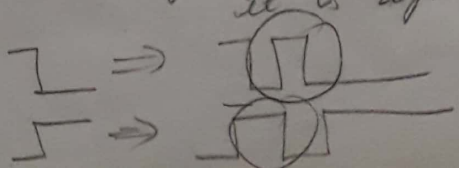
Hazards

(If any unwanted switching transience, it may change the o/p temporarily as false) It is called static-1-hazard.



static 0 hazard →

static 1 hazard → from 1 to 0 (or) 0 to 1 it is dynamic hazard.

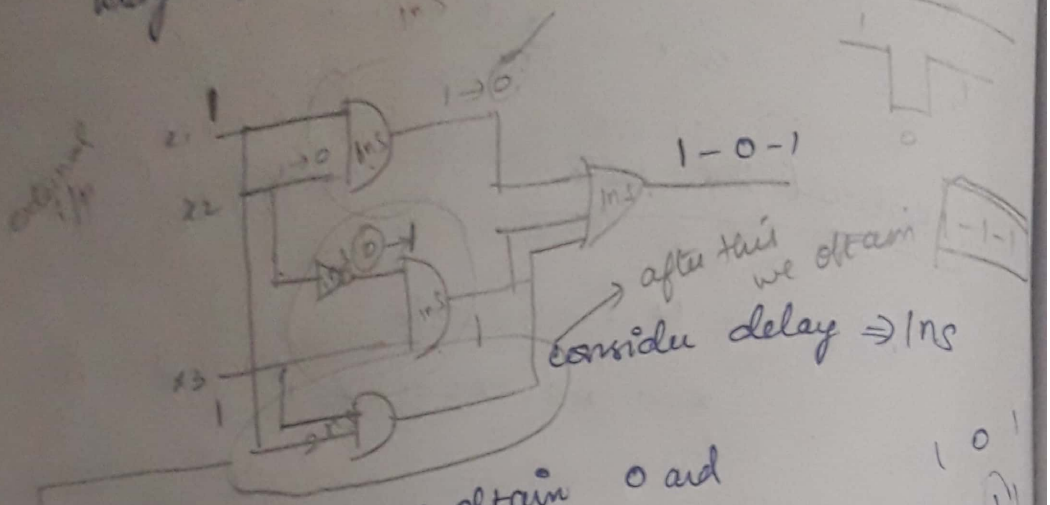


Essential hazard

[(To elim) insert latch to feed back ckt.]

Because of the hazard, if it goes to wrong ref. circuit, we have to eliminate hazard

(i/p ⇒ 1)



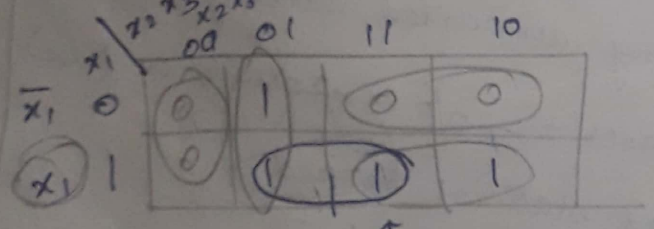
after 1ns → we obtain 0 and 0

after 2ns → we obtain 0, 1

→ Static-1

eqn $Y = x_1x_2 + \bar{x}_2x_3$

Draw the K map:-



x1 and where ever x2 → make

0 → a

0 → ā

To avoid static hazard, include redundant case (unwanted loop)

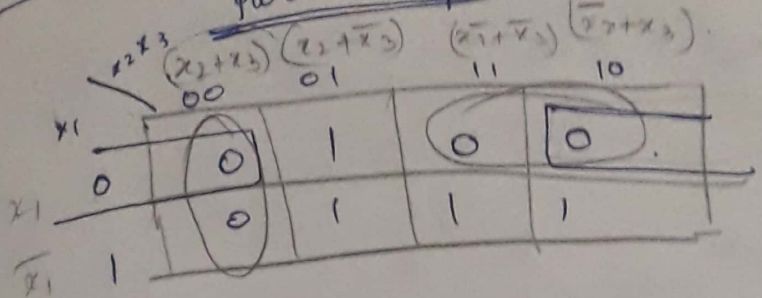
we obtain

$x_1x_2 + \bar{x}_2x_3 + x_1x_3$

always 1 1 → o/p = 1

using product of sum

plot k map



$$Y = (x_2 + x_3)(x_1 + \bar{x}_2)$$

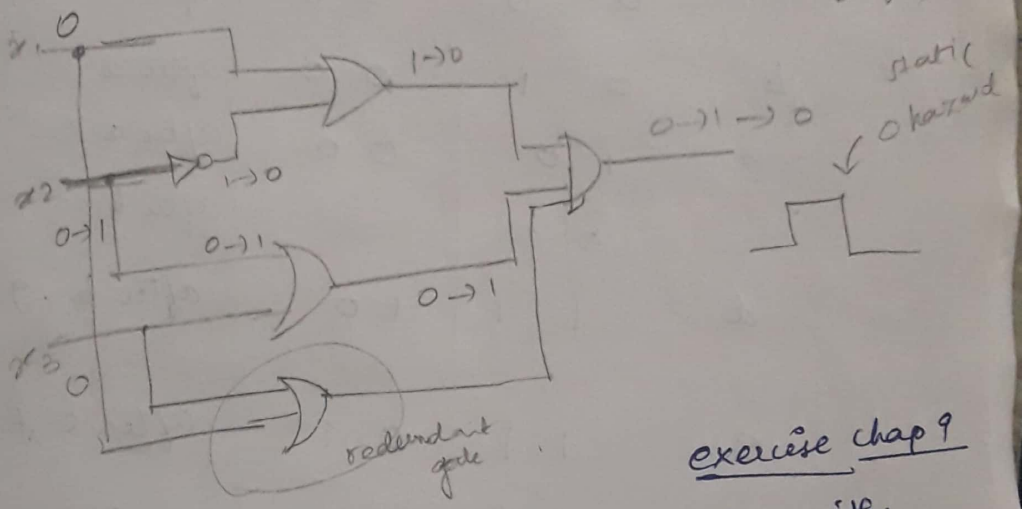
after using redundat

$$Y = (x_2 + x_3)(x_1 + \bar{x}_2)\cancel{(x_1 + x_3)(x_2 + x_3)}$$

⇒ To check static 0 hazard

(take pdt of sums & put i/p ⇒ 0)

(longest path → apply signal change)



exercise chap 9

Q) obtain a primitive flow table for ckt with 2 i/p x_1 and x_2 and 2 o/p z_1 and z_2, that satisfy the following 4 conditions when (i) $x_1, x_2 = 0, 0$ the o/p is $z_1, z_2 = 0, 0$

(ii) when $x_1 = 1$, x_2 changes from 0 to 1 } the o/p is $z_1\ z_2 = 0, 1$

(iii) when $x_2 = 1$, and x_1 changes from 0→1 } the o/p is $z_1\ z_2 = 1, 0$

(iv) otherwise the o/p does not change

Solⁿ:-

	x_1	x_2	z_1 z_2.
1.	0	0	0 0
2.	!	0→1	0 1
3.	0→1	1	1 0
4.	Autre		Blocage

~~state~~ ~~x_1 x_2~~

state	x_1	x_2	z_1	z_2	comments.
a	0	0	0	0	after b, c, f, g, h, i
b	0	1	0	0	after a
00 11 > c	1	0	0	0	after a. (mettre dash)
	0	0	0	0	after b.
10 01 > d	1	1	1	0	after b, g, i
	0	0	0	0	after c
10 01 > e	1	1	0	1	after c, f, h
00 11 > f	1	0	1	0	after d.
> g	0	1	1	0	after d.
11 00 > h	1	0	0	1	after e.
i	0	1	0	1	after e.
~~g~~	~~0~~	~~0~~	~~1~~	~~0~~	~~after f~~
g	0	1	1	0	after d
h	1	0	0	1	after e
i	0	1	0	1	after e

Primitive Flow Table :-

PS \ x_1x_2	00	01	11	10
a	(a), 00	b, –	–, –	c, –
b	a, –	(b), 00	d, –	–, –
c	a, –	–, –	e, –	(c), 00
d	–, –	g, –	(d), 10	f, –
e	–, –	i, –	(e), 01	h, –
f	a, –	–, –	e, –	(f), 10
g	a, –	(g), 10	d, –	–, –
h	a, –	–, –	e, –	(h), 01
i	a, –	(i), 01	d, –	–, –

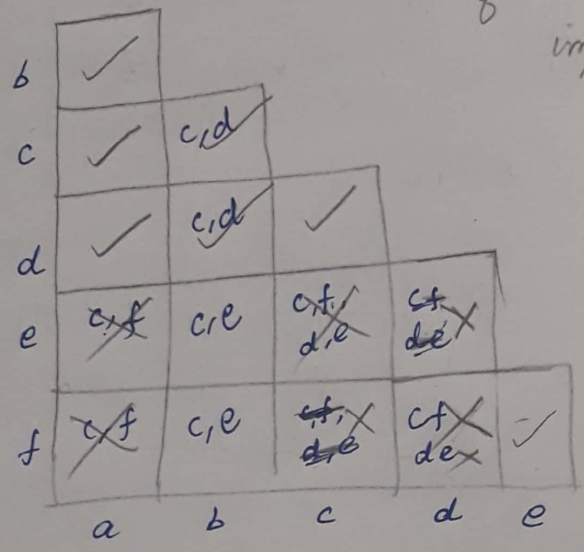
each row contains 1 stable state

1) mark stable state
2) mark unpossible i/p changes
3) mark remaining from table

23.10.18

Reduction of PFT using implication table Method.

	00	01	11	10
a	c,-	(a),0	b,-	-,-
b	-,-	a,-	(b),1	c,-
c	(c),0	a,-	-,-	d,-
d	c,-	-,-	b,-	(d),0
e	f,-	-,-	b,-	(e),1
f	(f),1	a,-	-,-	e,-

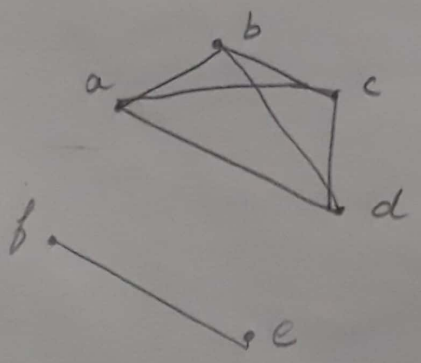


if one of the implied state not equal, that box ☒

compatible pairs:

(a,b) (a,c) (a,d) (b,c) (b,d) (c,d) (e,f)

Merger diagram:



Maximal compatible pairs:

Maximal compatibilities:

(a, b, c, d) (e, f)

closed covering condition

1. all the states should be included. (covering condn)
2. closure condn:-

If no implied states

(or)

all implied states.

stable state with o/p

	00	01	11	10
a b c d	ⓒ, 0	ⓐ, 0	ⓑ, 1	ⓓ, 0
e f	ⓕ, 1	a, –	b, –	ⓔ, 1

replace b c d ⇒ a

f ⇒ e.

	00	01	11	10
a	ⓐ, 0	ⓐ, 0	ⓐ, 1	ⓐ, 0
e	ⓔ, 1	a, –	a, –	ⓔ, 1

state Y: (i/p)

y \ x_1x_2	00	01	11	10
0 = a	0	0	0	0
1 = e	1	0	0	1

$Y = y\bar{x}_2$

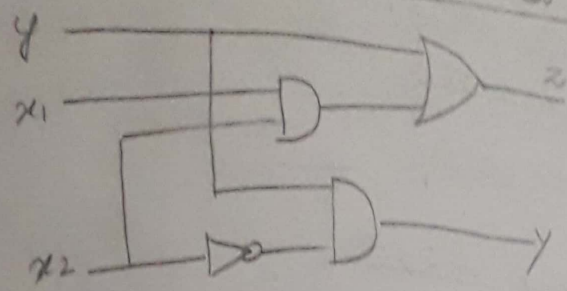
state z: o/p

	00	01	11	10
0	0	0	1	0
1	1	X	1	1

From stable to unstable state, take the value from stable state

$Z = x_1x_2 + y$

Without latch



With latch (RS latch)

excitation table of SR flip flop:

Q	q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

From the transition table Y

P.S y	x1x2 = 00	01	11	10
0	N.S 0	0	0	0
1	1	0	0	1

For both SR.

From the excitation table

y	00	01	11	10
0	SR 0X	SR 0X	0X	0X
1	X0	01	01	X0

Separating s and R.

For S

y \ x1x2	00	01	11	10
0	0	0	0	0
1	X	0	0	X

S=0

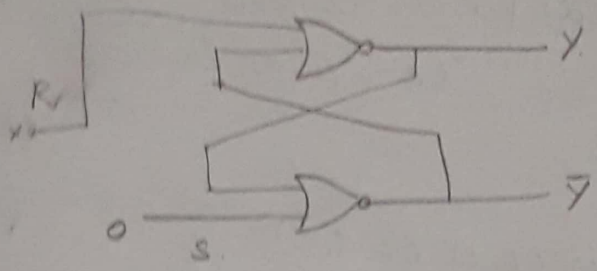
For R

y \ x1x2	00	01	11	10
0	X	X	X	X
1	0	1	1	0

R = x2

Note: For nand table complimented values of s and R (ie) $\bar{S}$ and $\bar{R}$

With NOR latch:-



example: 1

	a	b	c	d
b	b,c			
c	X	d,e		
d	b,c	X	a,d	
e	X	X	✓	b,c

Compatible pairs:

(a,b) (a,d) (b,c) (d,e)
(c,d) (c,e)

From the merger diagram;

Max comp. pairs

(a,b) (a,d) (b,c) (c,d,e)

(as per 1st condition)

X (a,b) (c,d,e)

within the pair check the implied state (From the Q)

a,d
b,c.

b,c

(5) states are reduced to (4) states.

As per condn I.

(a,b)	(a,d)	(b,c)	(c,d,e)
b,c	b,c	d,e	(a,d) (b,c)

Final set

(a,d) (b,c) (c,d,e)

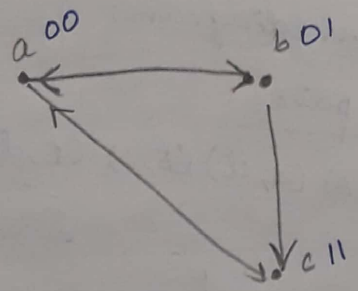
(5) → (3)

Race free state assignment

PS \ i/p	00	01	11	10
a	(a)	b	c	a
b	a	(b)	(b)	c
c	a	(c)	(c)	(c)

If stable state has adjacent unstable state, there is transition

Transition diagram



No transition from c to b.

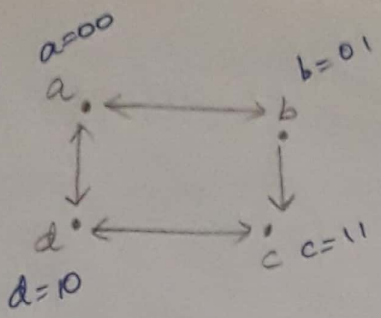
Assign binary values randomly (say: 1 bit variable change)

⇐ Due to critical race (assign new state)

so the diagram is modified as.

(From a c)

[since we have a → c and c → a]



From the new diagram,

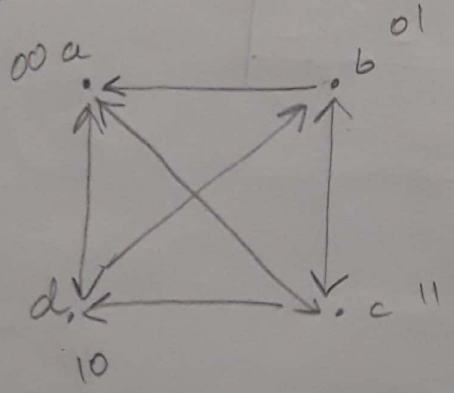
00	(a)	b	c/d	(a)
01	a	(b)	(b)	c
11	a/d	(c)	(c)	(c)
10	a	—	c	—

From table (a) to (c)
↓
(a) to d and goes to (10 to 11) c and settles at (c) [1 bit variable change]

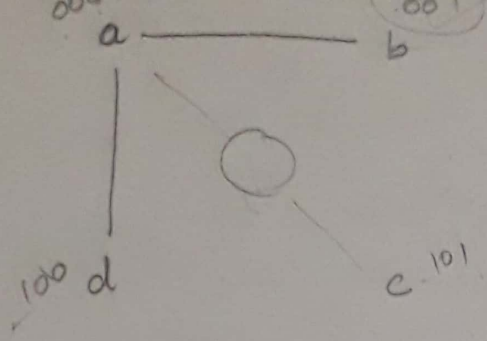
2 (a)

	00	01	11	10
a	(a)	c	(a)	d
b	a	(b)	c	(b)
c	(c)	(c)	(c)	d
d	(d)	b	a	(d)

Transition diagram



* From a to c there is a possibility of critical race since (more than 1 bit variation)
also d to b since 2 bit variation



* Draw general table to avoid confusion:

	00	01	11	10
0	a	b	c	f
1	d e	f d	g	

Introduce 1 more variable to avoid confusion

(Write the transition to the adjacent boxes)

Introduce 3 more states:-

a	ⓐ	f	ⓐ	d
b	a	ⓑ	c	ⓑ
c	e	ⓒ	ⓒ	d g
d	ⓓ	b	e	ⓓ
e	-	-	a	d
f	-	c	-	-
g	-	-	-	d

a → (f, g) → c

b → e → d

Q) Design a negative edge triggered T flip flop which has 2 i/p T & C (clock) and 1 o/p Q. → the o/p state is complemented if T=1 and C changes from 1 to 0 otherwise under any i/p condn the o/p remains unchanged.

Procedure
Design
Reduced
Assigning Race free
+ Latch (design)