Digital assignment - 2

(1) A PRN flipflop has four operations, no change, clear to 0, set 1 and complement, when inputs P and RN are 00, 01, 10 and 11, respectively.

a) Tabulate the characteristic table.

b) Derive the characteristic eqn.

c) Tabulate the excitation table

d) Show how the PRN flipflop can be converted to a D flipflop.

(2) A sequential circuit with two D flipflops A and B, two inputs x and y and one output z is specified by the following next state and o/p eqns

$$A(t+1) = x'y + xB$$

$$B(t+1) = x'A + xB$$

$$z = A$$

a) Draw the logic diagram of the circuit

b) List the state table for the sequential circuit.

c) Draw the corresponding state diagram.

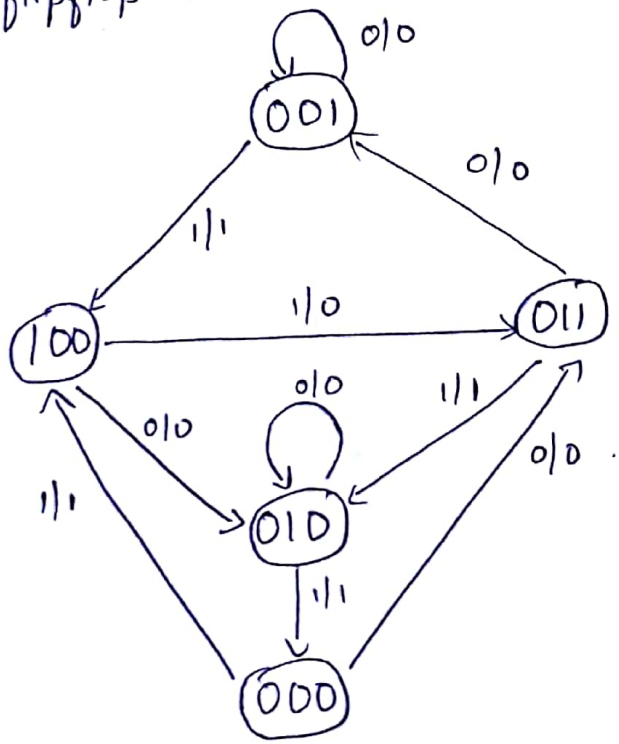
(3) Design a sequential ckt with two JK flipflops A and B and two inputs E and F. If E = 0, the circuit remains in the same state regardless of the value of F. When E = 1 and F = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11 back to

00 and repeats. When E=1 and F=0, the circuit goes through the state transitions from 00 to 11, to 10, to 01 back to 00 and repeats. What is the role of F input?

(4) A sequential ckt has three flipflops A, B and C; one input x and one output y. The state diagram is shown. The circuit is to be designed by treating the unused states as don't care conditions. Analyse the circuit obtained from the design to determine the effect of the unused states

a) Use D flipflop in the design

b) Use JK flipflop in the design.



(5) What is the difference between serial and parallel transfer? Which transfer is a faster one? Explain how to convert serial data to parallel data and parallel to serial What type of register is needed.

(6) Design a four bit shift register with a parallel load using D flipflops. There are two control i/ps shift and load. When shift = 1, the contents of the register one shifted by one position. New data are transferred into the register when load = 1 and shift = 0. If both control i/p's are equal to 0, the contents of the register do not change. Provide highest priority to load.

(7) Draw the logic diagram of a four bit register with four D flipflops and four 4 x 1 multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table.

S_1	S_0	Register operation.
0	0	No change
0	1	Complement the four i/p's
1	0	Clean registers to 0 (synchronous with clk)
1	1	Load parallel data.

(8) A binary ripple counter uses flipflops that trigger on the positive edge of the clock. What will be the ~~content~~ count if.

a) the normal o/p's of the flipflops are connected to the clock and

b) the complements outputs of the flipflops are connected to the clock?

c) What happens if negative edge of clock is used to trigger counter flipflops?

(9) How many flipflops will be complemented in a 10-bit binary ripple counter to reach the next counter after the following counts?

a) 1001101111

b) 0111111111

c) 1111111110