1. A PN flip-flops has four operations, no change, clear to 0, set 1 and complement. when inputs P and N are 00, 01, 10 and 11, respectively.

a) Tabulate the characteristic table.

b) Derive the chaaracteristic equations

c) Tabulate the excitation table.

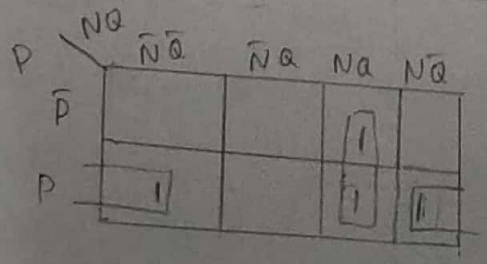
d) show how the PN flipflop can be converted to a D-flipflop.

a.

P	N	Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
1	1	1

b.

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



$Q(t+1) = PQ' + NQ$.

c.

Q(t)	Q(t+1)	P	N
0	0	0	x
0	1	1	x
1	0	x	0
1	1	x	1

d. connect p and N together.

2. A sequential circuit with two D flipflops A and B two inputs x and y and one output z is specified by the following next state and output equations

$$A(t+1) = \bar{x}y + xB$$

$$B(t+1) = \bar{x}A + xB$$

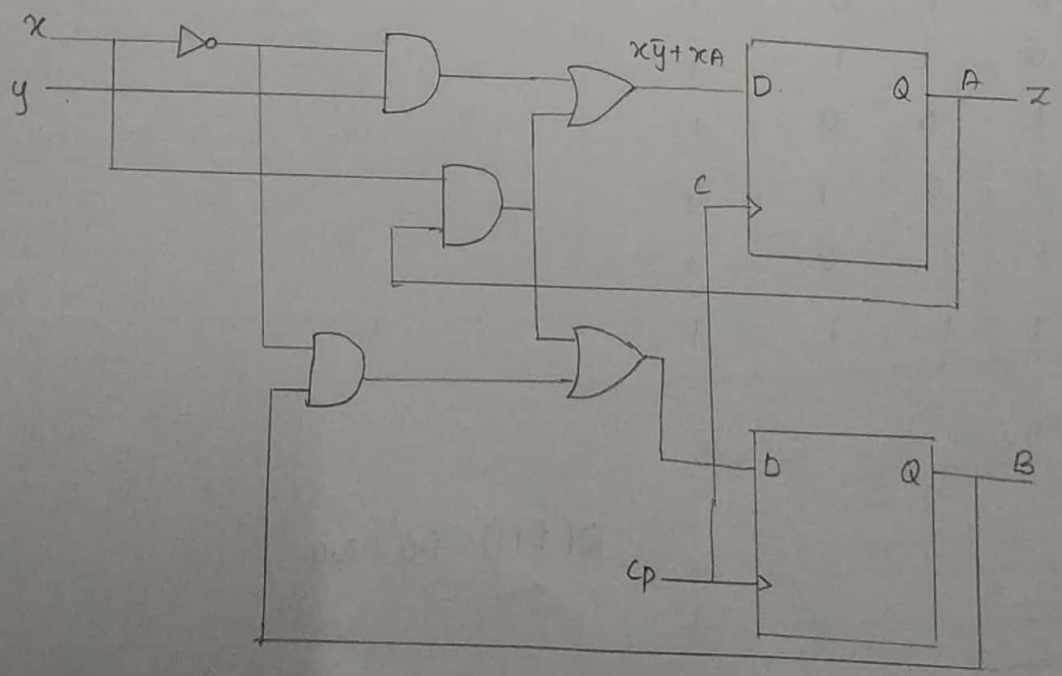
$$z = A$$

a) Draw the logic diagram of the circuit

b) List the state table for the sequential circuit.

c) Draw the corresponding state diagram.

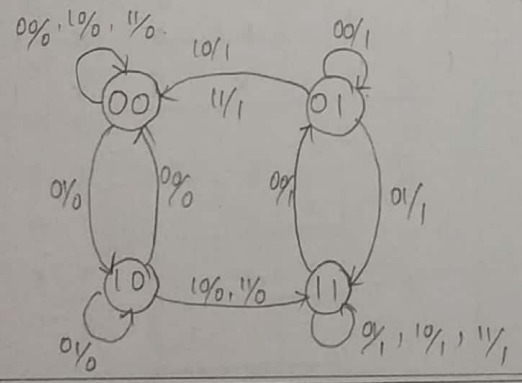
a.



b.

A	B	x	y	A	B	Z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

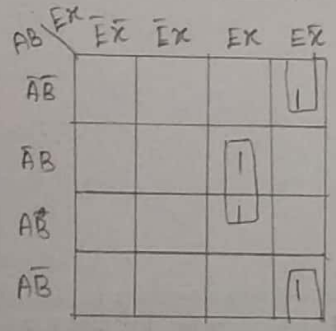
c.



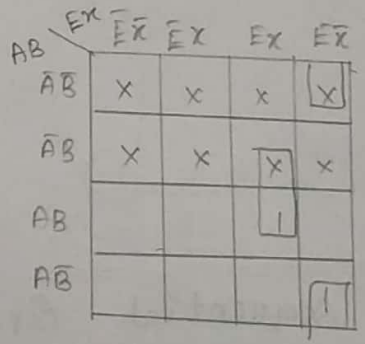
3. Design a sequential circuit with two JK flip flops A and B and two inputs E and F. If E=0 the circuit remains in the same state regardless of the value of F. when E=1 and F=1 the circuit goes through the state transitions from 00 to 01, to 10 to 11, back to 00 and repeats. when E=1 and F=0 the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and

repeats what is the role of F input?

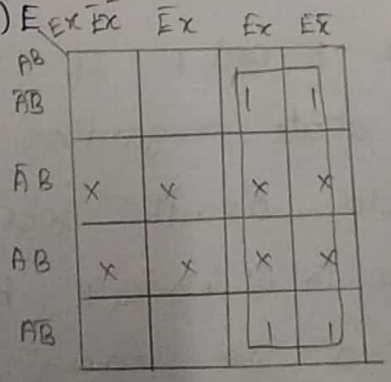
present state A	B	Input x		Next state A(t+1)	B(t+1)	flip flop inputs J_A	K_A	J_B	K_B
0	0	0	1	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	1	0	X	X	1
0	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	1	0
1	0	0	1	1	0	X	0	1	0
1	0	1	0	0	1	X	1	X	1
1	0	1	1	1	1	X	0	X	1
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	1	1	0	X	1
1	1	1	1	1	1	X	1	X	1



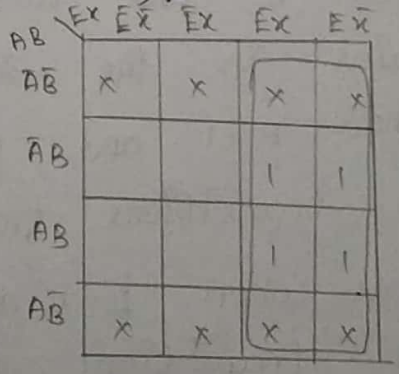
$J_A = (Bx + \bar{B}\bar{x})E$



$K_A = (Bx + \bar{B}\bar{x})E$



$J_B = E$



$K_B = E$

The F is up/down control

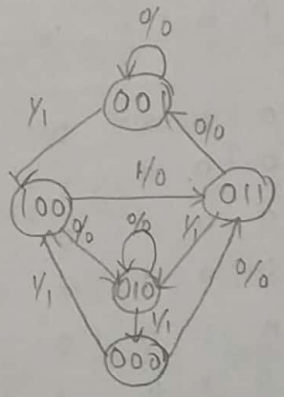
F = 0 up counting

F = 1 down counting.

4. A sequential circuit has three flipflops A, B and C one input x_in; and one output y_out. The state diagram is given. The circuit is to be designed by treating the unused state as don't care conditions Analyze the circuit obtained from the design to determine the effect of the unused states.

a) use D flipflops in the design

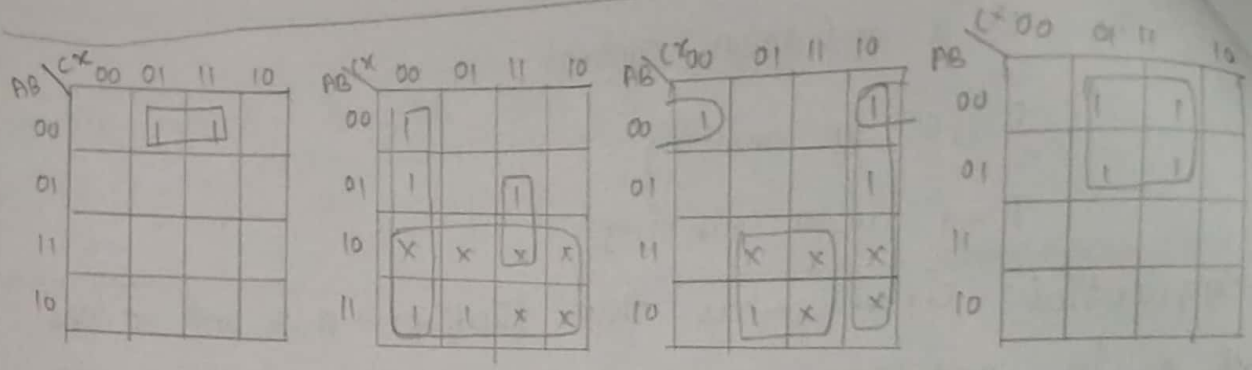
b) use JK flipflops in the design



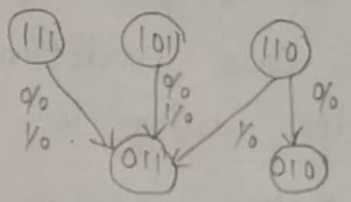
a) unused states : 101, 110, 111

Present state			Input	Next state			output
A	B	C	x	A	B	C	Y
0	0	0	0	0	1	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	1

$d(A, B, C, x) = \Sigma (10, 11, 12, 13, 14, 15)$

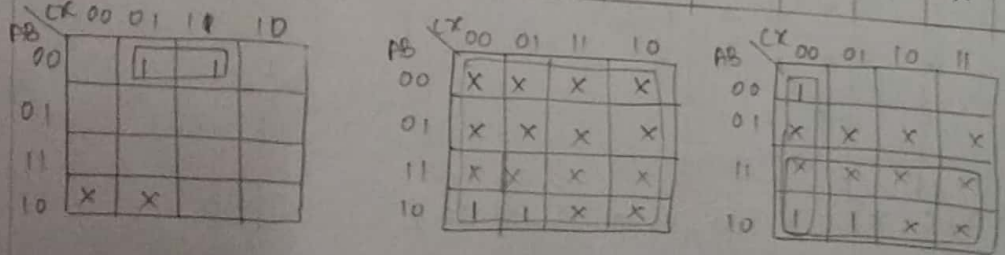


$D_A = A'B'x$ $D_B = A + C'x' + BCx$ $D_C = C\bar{x} + Ax + \bar{A}\bar{B}\bar{x}$ $y = \bar{A}x$

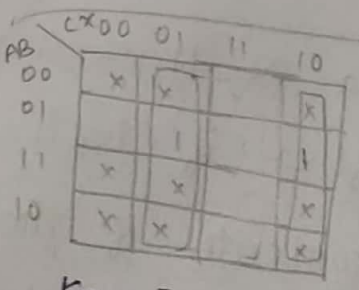


b) with JK flip flops,

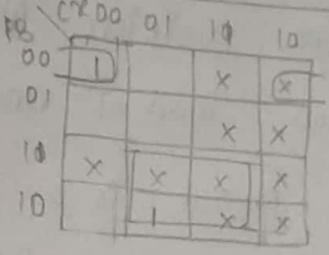
A	B	C	x	A	B	C	y	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	0	0	x	1	x	1	x
0	0	0	1	1	0	0	1	1	x	0	x	0	x
0	0	1	0	0	0	1	0	0	x	0	x	x	0
0	0	1	1	1	0	0	1	1	x	0	x	x	1
0	1	0	0	0	1	0	0	0	x	x	0	0	x
0	1	0	1	0	0	0	1	0	x	x	1	0	x
0	1	1	0	0	0	1	0	0	x	x	1	x	0
0	1	1	1	0	1	0	1	0	x	x	0	x	1
1	0	0	0	0	1	0	0	x	1	1	x	0	x
1	0	0	1	0	1	1	1	x	1	1	x	1	x



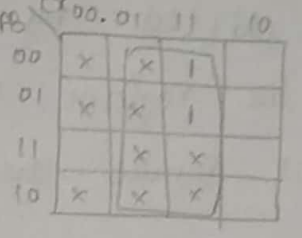
$J_A = Bx$ $K_A = 1$ $J_B = A + \bar{C}\bar{x}$



$K_B = \bar{C}x + C\bar{x}$



$J_C = Ax + \bar{A}\bar{B}\bar{x}$



$K_C = x$

$J_A = \bar{B}x \quad K_A = 1$

$J_B = A + \bar{C}\bar{x} \quad K_B = \bar{C}x + C\bar{x}$

$J_C = Ax + \bar{A}\bar{B}\bar{x} \quad K_C = x$

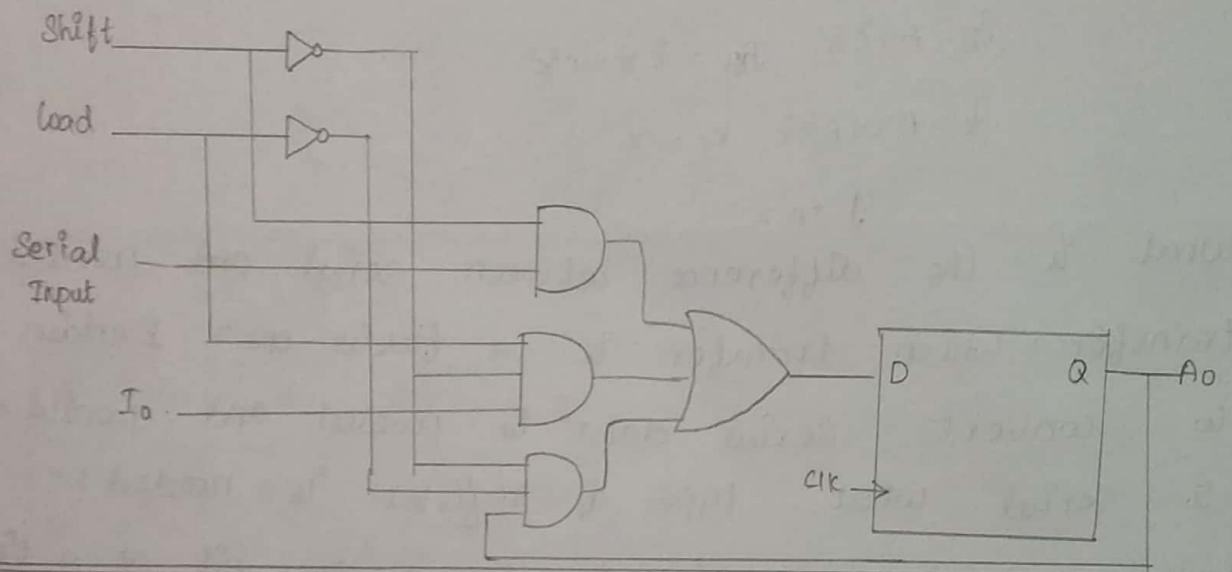
$y = A'x$

5. What is the difference between serial and parallel transfer? Which transfer is a faster one? Explain how to convert serial data to parallel and parallel data to serial. what type of register is needed?

Serial data is transferred one bit at a time. parallel data is transferred n bits at a time ($n > 1$). A shift register can convert serial data into parallel data by first shifting one bit a time into the register and then taking the parallel data from the register outputs A shift register with parallel load can convert parallel data to a serial format by first loading the data in parallel and shifting the bits one at a time.

6. Design a four-bit shift register with a parallel load, using D flipflops. There are two control inputs. shift and load. when shift = 1, the contents of the regist

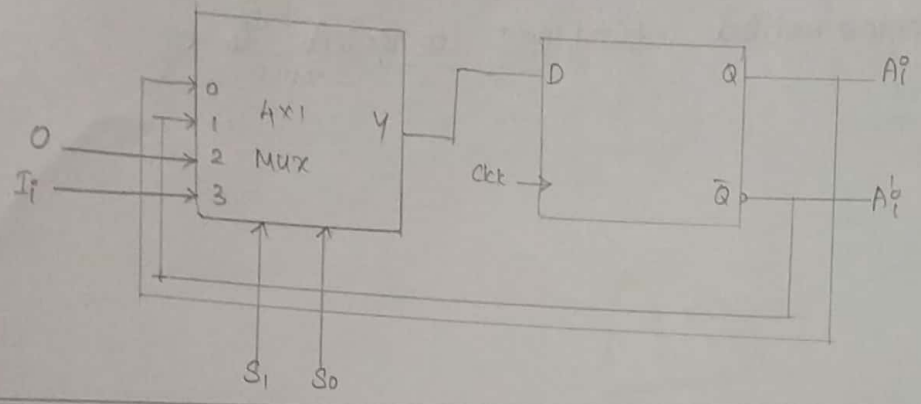
are shifted by one position Now data are transferred into the register when load =1 and shift =0 if both control inputs are equal to 0 the contents of the register do not change. provide highest priority to load.



7. Draw the logic diagram of a four-bit register with four D flipflops and four 4×1 mux with mode selection inputs S_1 and S_0. the register operates according to the following function table:

S_1	S_0	Register operation
0	0	No change
0	1	complement the four outputs
1	0	clear register to 0
1	1	Load parallel data.

stage of register:



CS

8 How many flipflops will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts?

a) 1001101111

b) 0111111111

c) 1111111110

a) 1001101111 – 5 flip flops

b) 0111111111 – 10 flip flops

c) 1111111110 – 10 flip flops.

JA

9. A binary ripple counter was flipflop that trigger on the positive edge of the clock. what will be the count if

a) the normal o/p's of the flipflop are connected to the clock and

4004

b) the complements outputs of the flipflops are connected to the clock?

a) with the bubbles in c removed

b) with complemented flipflops connected to c