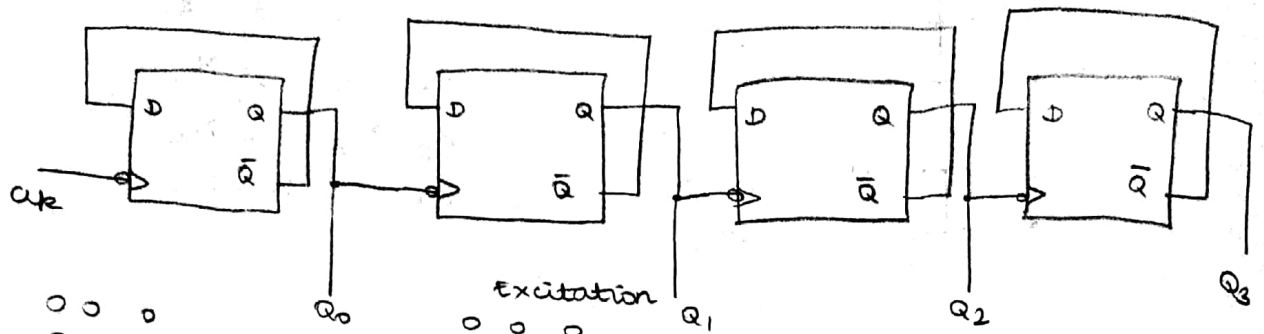


Asynchronous binary ripple counter using D-flip flop



0	0	0
0	1	1
1	0	1
1	1	0

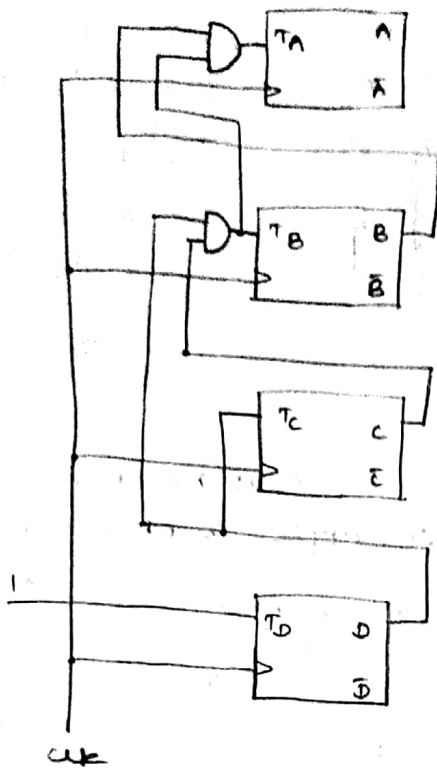
Synchronous binary ripple counter using T-flip flop

N.S				N.S				T _A	T _B	T _C	T _D
A	B	C	D								
0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0	0	1	1
2	0	0	1	0	0	0	1	0	0	0	1
3	0	0	1	0	0	1	0	0	1	1	1
4	0	1	0	0	0	1	0	0	0	0	1
5	0	1	0	1	0	1	1	0	0	1	1
6	0	1	1	0	0	1	1	0	0	0	1
7	0	1	1	1	1	0	0	0	1	1	1
8	1	0	0	0	1	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0	0	1	1
10	1	0	1	0	1	0	1	0	0	0	1
11	1	0	1	1	1	1	0	0	1	1	1
12	1	1	0	0	1	1	0	1	0	0	1
13	1	1	0	1	1	1	1	0	0	1	1
14	1	1	1	0	1	1	1	1	0	0	1
15	1	1	1	1	0	0	0	0	1	1	1

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10



Up counter

for n-bit counter

$v \ w \ x \ y \ z$

$T_x = yz \quad T_y = z \quad T_z = 1$

$T_w = xyz \quad T_v = wxyz$

Synchronous 8-bit up/down counter using

Z	P.S			N.S			T-flip flop		
	A	B	C				T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	0	1	1	0	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	0	1	1	0	1	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	0	1	0	0	0	0	0	1
1	0	0	0	1	1	1	1	1	1

BC	00	01	11	10
XA				
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

BC	00	01	11	10
XA				
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

BC	00	01	11	10
XA				
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$$T_A = BC\bar{D}\bar{A} +$$

$$T_B = \bar{D}C \oplus X$$

$$T_C = 1$$

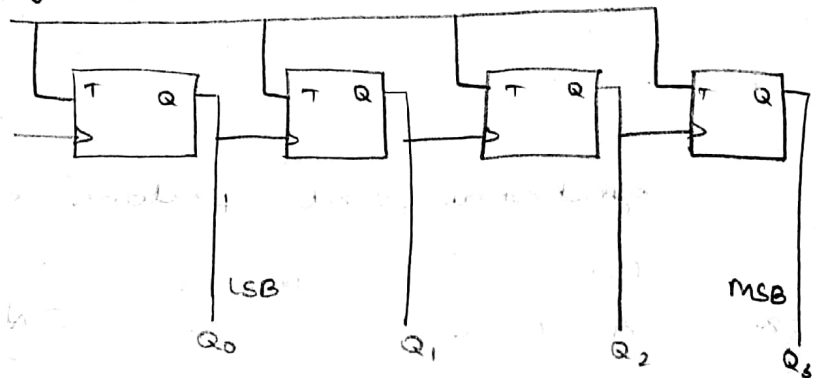
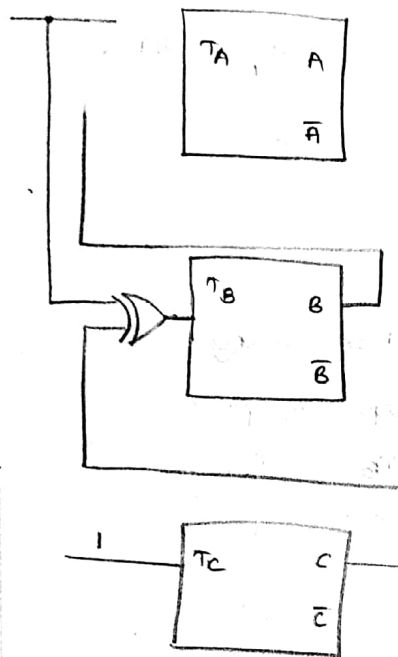
$$X\bar{B}\bar{C} + \bar{X}A + \bar{A}X$$

$$X \oplus A \quad X \oplus B \oplus C$$

Asynchronous

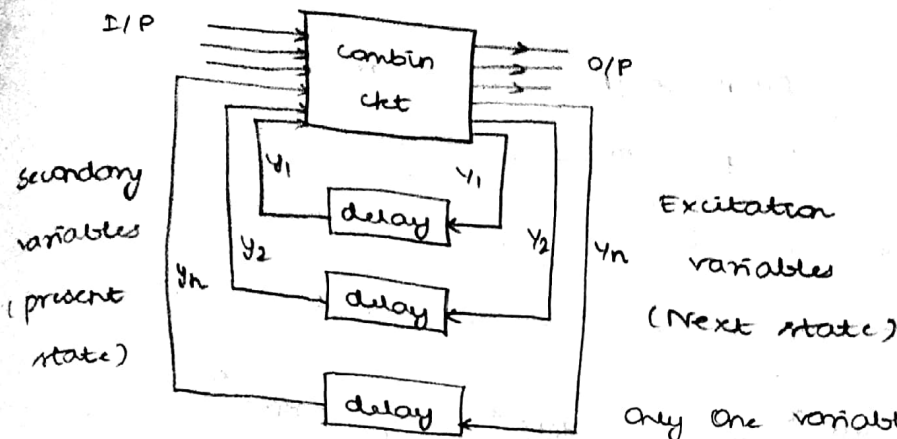
BCD ripple counter (Decade counter)

logic 1 Mod-10 counter



counts = $0 \rightarrow n-1$ = Mod-n counter

4. Asynchronous sequential circuits



Two modes of operation =

- * Fundamental mode
- * Pulse mode

At steady state, $Y_i = y_i$

After achieving steady state only, the input is allowed to change

Stable state

Unstable state

Transition table

Flow table

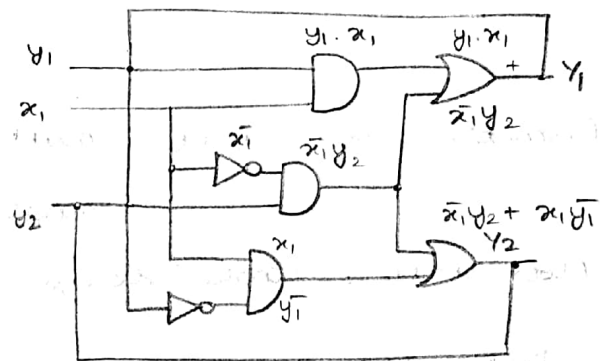
Race Noncritical
critical

Hazards Static
Dynamic
Essential

P.S $y_1 y_2$	I/P x	N.S, O/P $y_1 y_2$
00	0	00
01	0	01
11	0	11
10	0	10
00	1	01
01	1	11
11	1	10
10	1	00

transition table

change of transition to unstable state then settles down to stable state = race



$$Y_1 = xY_1 + xY_2$$

$$Y_2 = xY_2 + xY_1$$

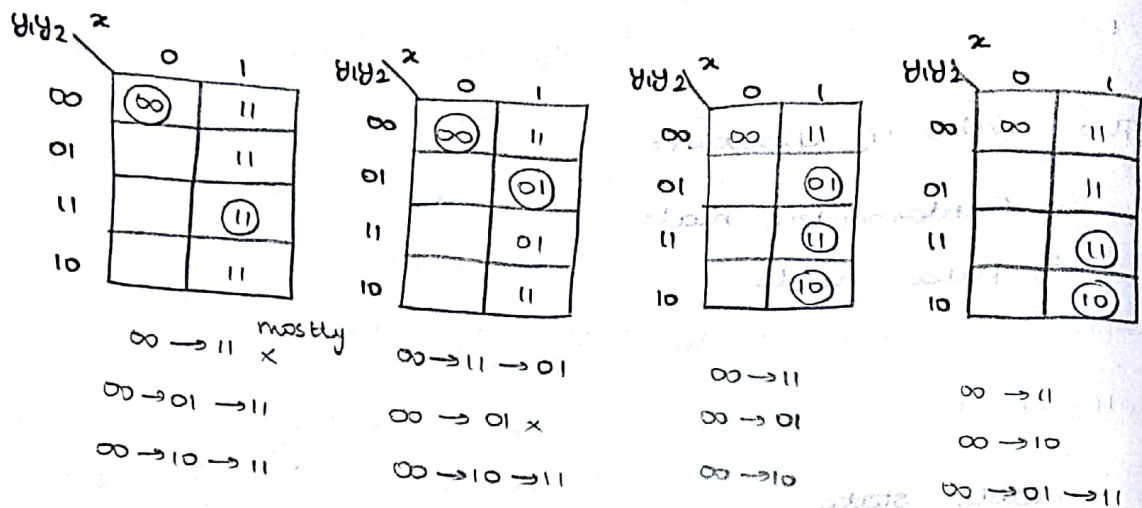
$y_1 y_2$	x	0	1
00	0	00	01
01	0	11	01
11	0	11	10
10	0	00	10
00	1	a	b
01	1	d	b
11	1	d	c
10	1	a	c

When input (x) changes, any one of the P.S changes faster than the other

Non critical race : (One steady state) - Final stable state doesn't depend on the state variable change

critical race : Final stable state depend on the state variable change. (multiple stable state)

Cycle : Changes to unstable state starting from stable state but doesn't settle down to stable state.



Primitive flow table : multiple steady states in a single row

Flow table : Single steady state in a row

Implication table → Merger diagram

Design a gated latch with two I/P G (gate), D (data) and one O/P Q . Binary information present at the D is transferred to Q when G is equal to 1.

The Q O/P will follow the I/P D as long as $G=1$

When $G=0$, O/P Q is retained

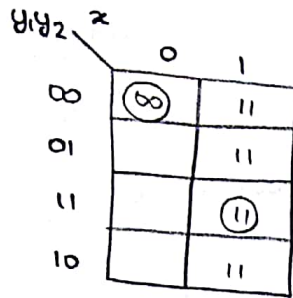
$G=1 : Q=D$
 $G=0 : Q = \text{retained}$

State	Input		Output	Comments
	D	G		
a	0	0	0	after b, c
b	0	1	0	after a, d, f
c	1	0	0	after a, d
d	1	1	1	after b, c, e
e	1	0	1	after d, f
f	0	0	1	after a, d

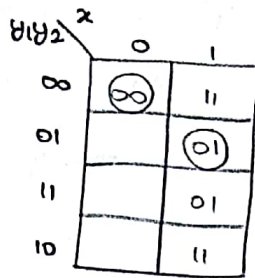
Non critical race : (One steady state) : Final stable state doesn't depend on the state variable change

Critical race : Final stable state depend on the state variable change. (multiple stable state)

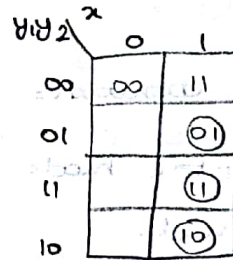
Cycle : Changes to unstable state starting from stable state but doesn't settle down to stable state.



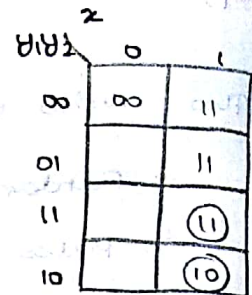
$00 \rightarrow 11$ mostly x
 $00 \rightarrow 01 \rightarrow 11$
 $00 \rightarrow 10 \rightarrow 11$



$00 \rightarrow 11 \rightarrow 01$
 $00 \rightarrow 01$ x
 $00 \rightarrow 10 \rightarrow 11$



$00 \rightarrow 11$
 $00 \rightarrow 01$
 $00 \rightarrow 10$



$00 \rightarrow 11$
 $00 \rightarrow 10$
 $00 \rightarrow 01 \rightarrow 11$

Primitive flow table : multiple steady states in a single row

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Design a gated latch with two I/P G (gate), D (data) and one O/P Q. Binary information present at the D is transferred to Q when G is equal to 1.

The Q O/P will follow the I/P D as long as $G=1$

When $G=0$, O/P Q is retained

$G=1 : Q=D$
 \downarrow
 $G=0 : Q = \text{retained}$

State	Input		Output	Comments
	D	G		
a	0	0	0	after b, c
b	0	1	0	after a, d, f
c	1	0	0	after a, d
d	1	1	1	after b, c, e
e	1	0	1	after d, f
f	0	0	1	after a

	ΣQ	00	01	11	10
a		(a)0	b, $\bar{0}$	-,-	c,-
b		a,-	(b)0	d,-	-,-
c		a,-	-,-	d,-	(c)0
d		-,-	b,-	(d)1	e,-
e		f,-	-,-	d,-	(e)1
f		(f)1	b,-	-,-	e,-

	ΣQ	00	01	11	10
a,b,c		(a)0	(b)0	d,-	(c)0
d,e,f		(b)1	b,-	(d)1	(e)1

	ΣQ	00	01	11	10
a		(a)0	(a)0	d,-	(a)0
d		(d)1	a,-	(d)1	(d)1

	ΣQ	00	01	11	10
0		0,0	0,0	1,-	0,0
1		1,1	0,-	1,1	1,1

	ΣQ	00	01	11	10
0		0	0	1	0
1		1	0	1	1

$$Y = \Sigma Q + Y\bar{A}$$

	ΣQ	00	01	11	10
0		0	0	1	0
1		1	0	1	1

$$Z = \Sigma Q + Y\bar{A}$$

