



Development of the MIPI Camera Interface Prototype Adapter Board

Intern: Haruka Kido

Bachelor of Science in Electrical Engineering
University of North Dakota

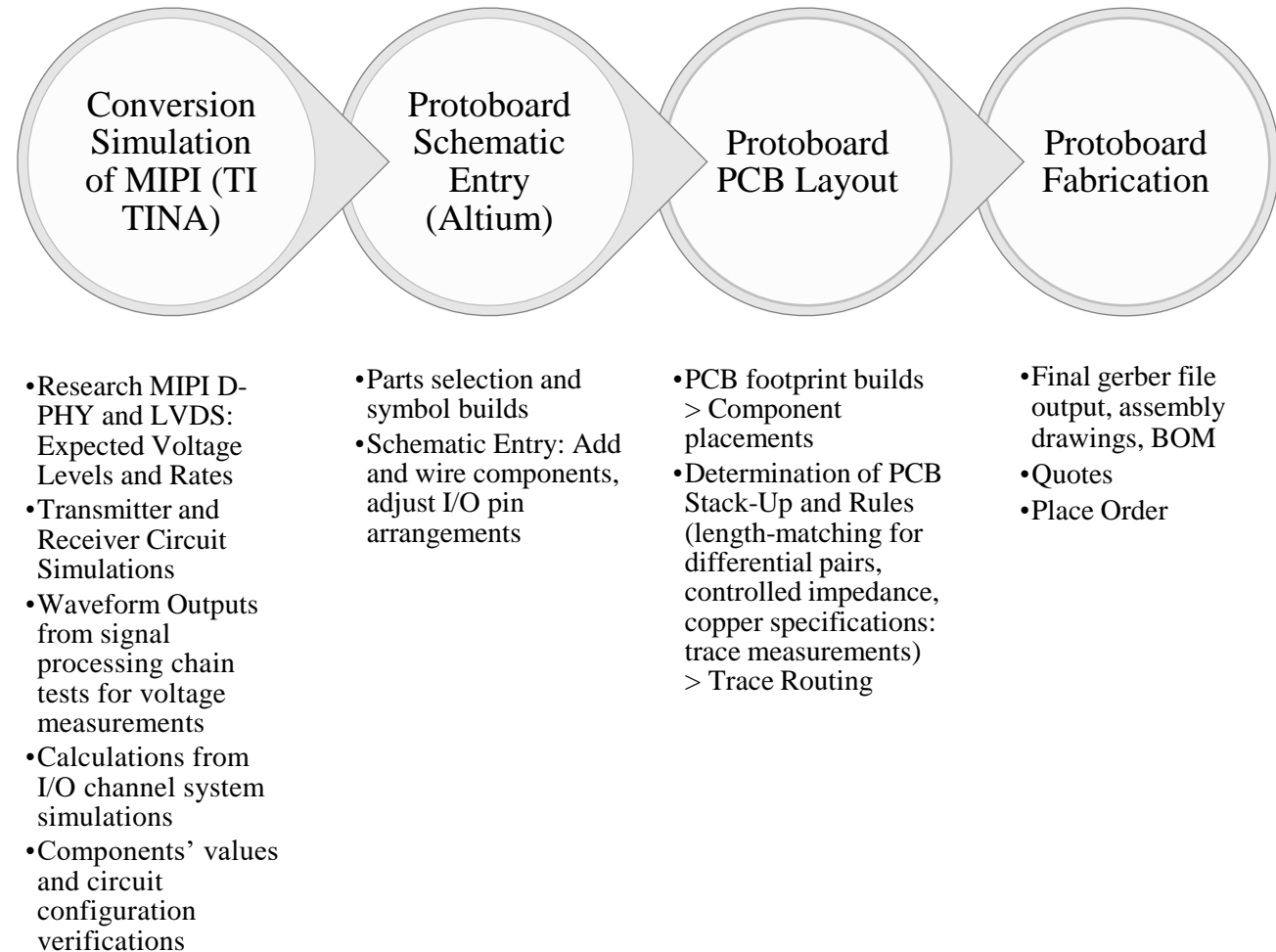
Mentor: Alessandro Geist. **Co-mentor:** Cody Brewer

*Embedded Processing Group, Code 587. Data Processing Branch, Software Engineering Division,
Space Technology Mission Directorate, GSFC, NASA*

FPGA-Compatible MIPI CSI-2 D-PHY Adapter Board Development Methodology

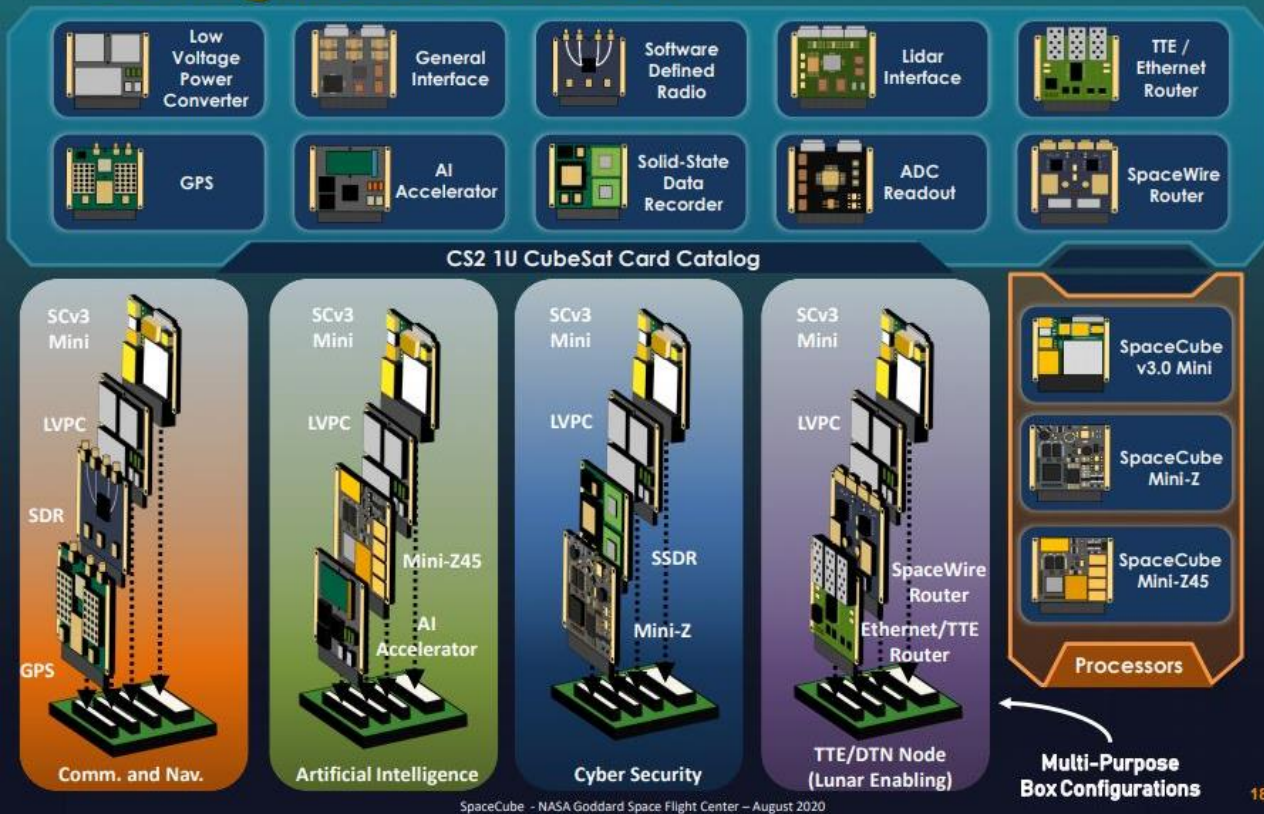
Project Description

This project is the development of the **prototype FPGA-Compatible MIPI CSI-2 (Camera Serial Interface) D-PHY adapter board**. The FPGA used on the SpaceCube processor card does not have I/O that natively supports the D-PHY standard, and thus requires additional external components to adapt the interface to the FPGAs I/O. The goal of this project is to develop a prototype board with this external circuitry. The project tasks include **1)** preliminary research and analysis of the adapter circuit requirements involving waveform comparisons, **2)** signal processing chain tests for voltage measurements, **3)** calculations from I/O channel system simulations in TI-TINA, **4)** components' values and circuit configuration verifications, **5)** protoboard schematic entry, **6)** both PCB footprint builds and PCB layout in Altium Designer, and lastly, **7)** PCB manufacturing. This adapter board is useful in data conversion and transmission from the MIPI camera module to the FPGA, a D-PHY circuit arrangement used in NASA's SpaceCube Mini's VADIR (Versatile Analog/Digital Interface) between the MIPI Camera module and the Backplane Connector.



Engineering Contextualization: SpaceCube Configurable Slices

Configurable Slices

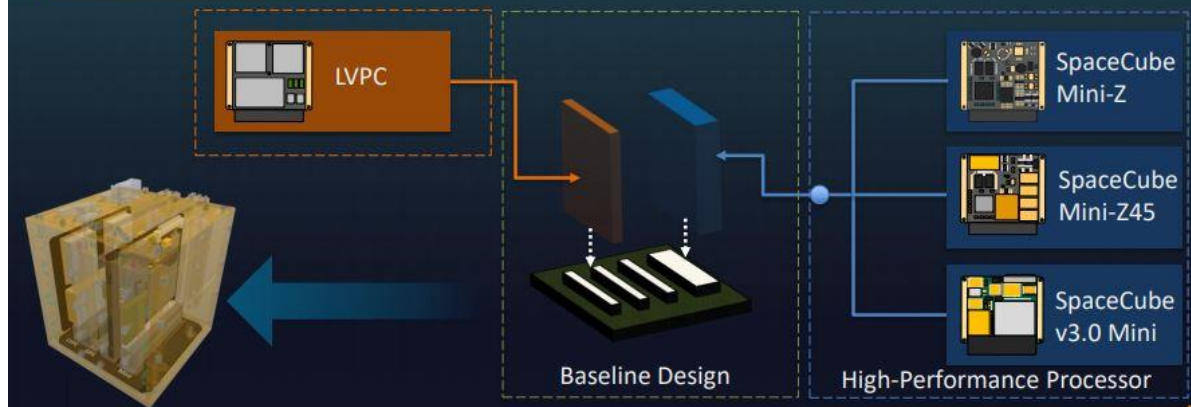


IMPS Concept Overview

Diverse set of payloads can be realized with **same baseline infrastructure** of key reused cards and **simple addition** of one or two cards for mission-specific needs

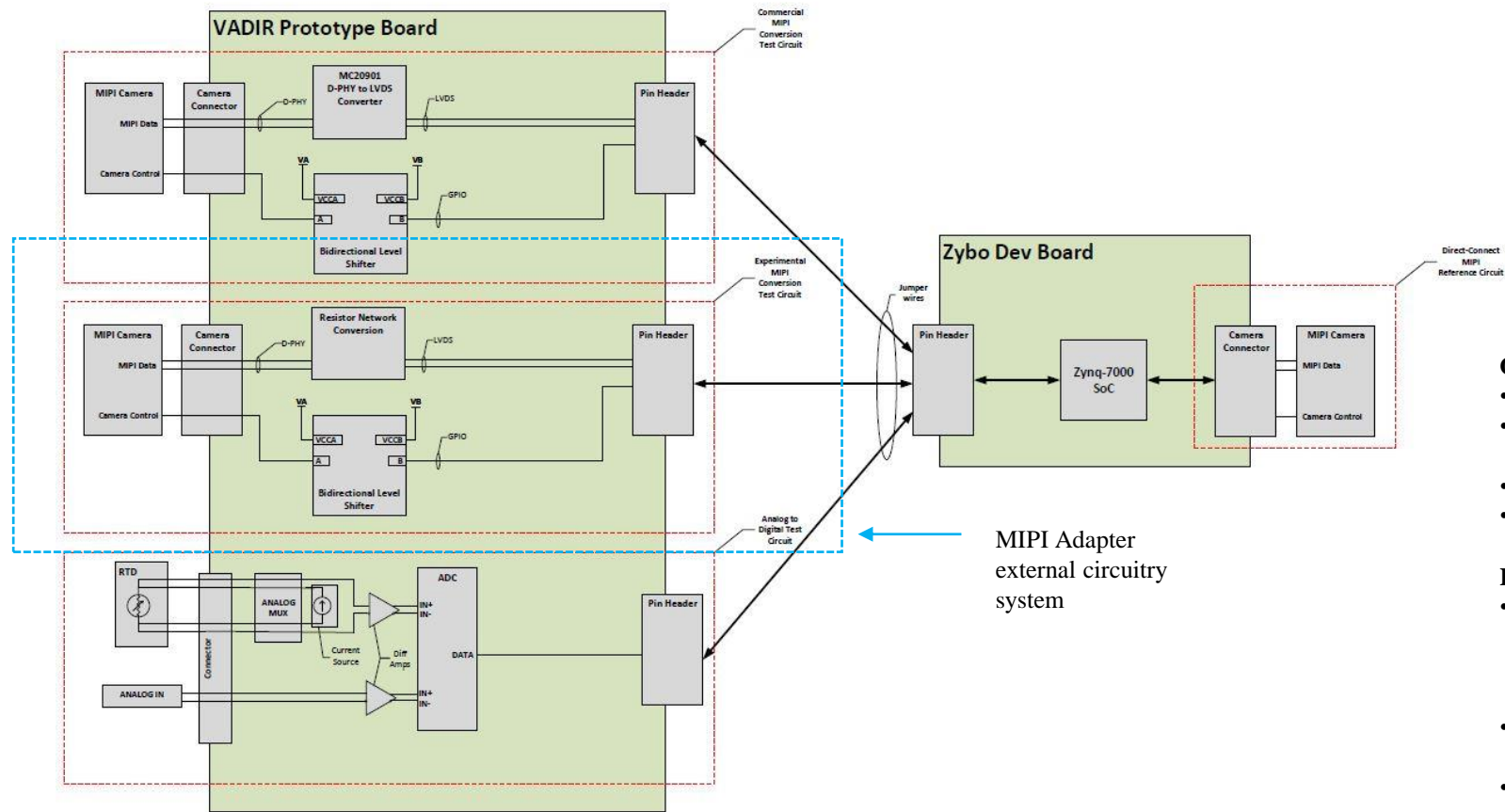
SpaceCube provides **high-performance computing** designs to be combined with added features from catalog of supporting cards

Designs are reusable and can be reconfigured for **multiple mission classes** (or varying orbits/environments) and science objectives



SpaceCube - NASA Goddard Space Flight Center - August 2020

Engineering Contextualization: MIPI Adapter in SpaceCube's Versatile Analog-Digital Interface (VADIR) Card



Overview:

- Multiple configurable analog inputs in CubeSat form-factor
- Selective population enables SWAP-C savings depending on mission needs
- On-board level shifter allows for multiple control voltages
- Conforms to CubeSat Card Standard (CS²)

[CS]²

High-Level Specifications:

- 24-bit Science & Telemetry ADC
 - 2 independent ADCs, up to 52ksps each
 - 16x 4-wire RTD up to 45k Ω resistance
 - 15x Single-Ended or Differential Analog Inputs
- 12-bit Housekeeping ADC
 - 8x 0-5V Single-Ended Analog Inputs
- Bias Supplies
 - 2x LDO supplies, <1.5A, 1.2-3.3V
- Requires $\pm 12V$, +5V, and +3.3V
- Requires 16x I/O lines (1.8V or 3.3V)

Preliminary Research and Analysis: Schematics of Resistor Networks and System Integration Mapping of MIPI CSI-2 Transceiver Unit

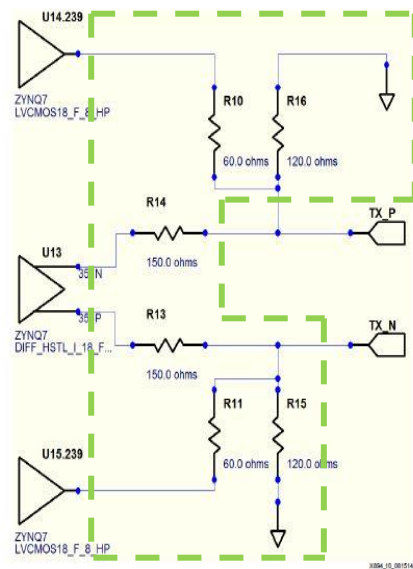


Figure 10: FPGA Compatible D-PHY Transmitter

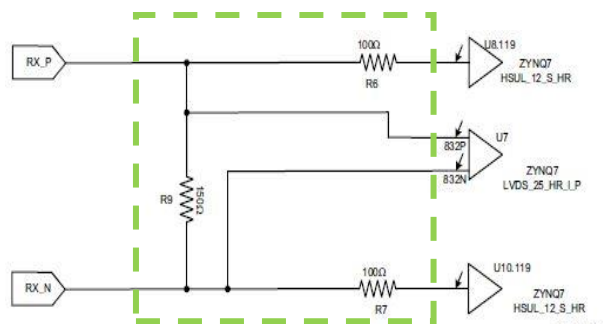
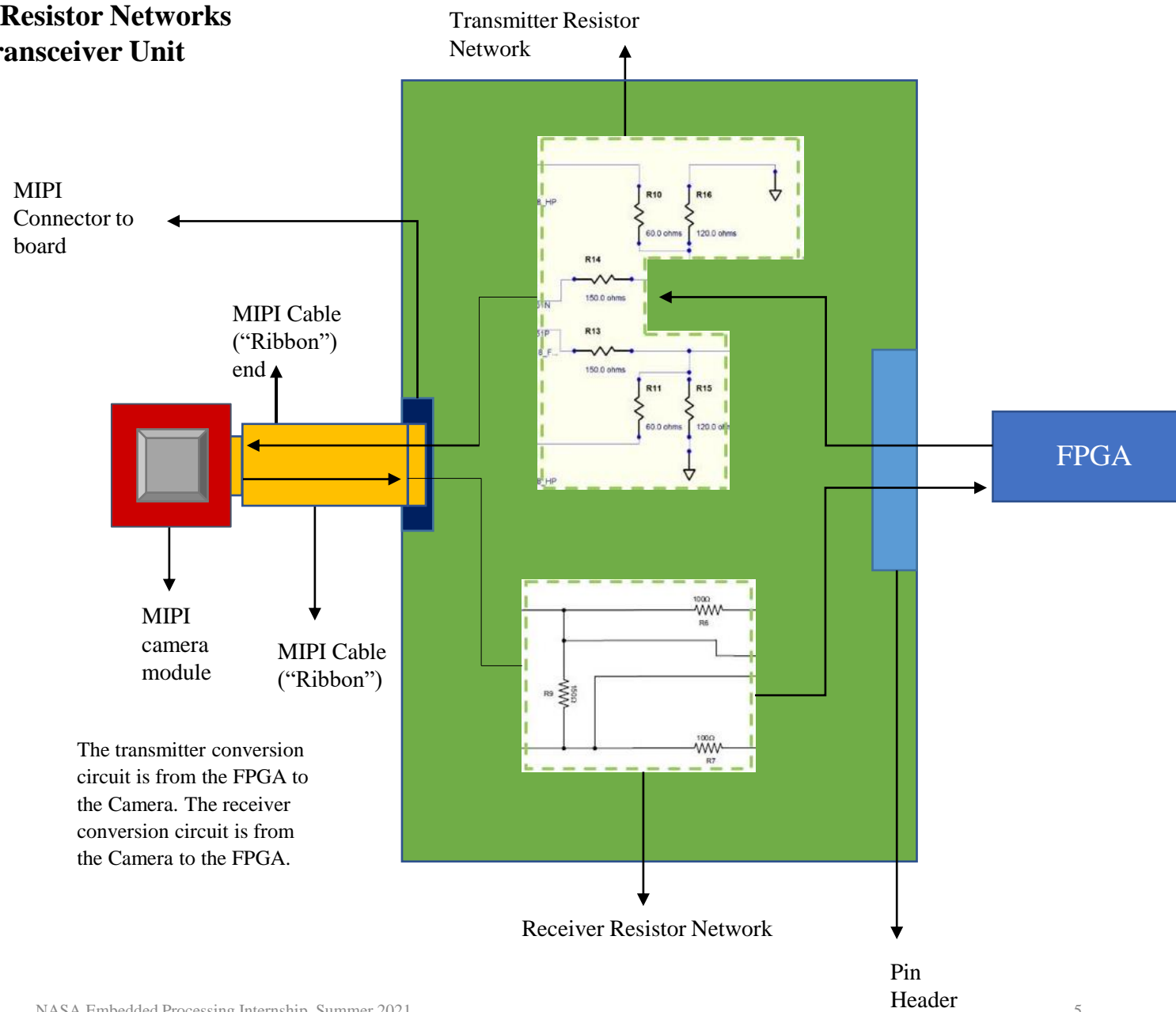


Figure 11: FPGA Compatible D-PHY Receiver



TI TINA Simulations for Receiver Network:

Signal-Processing Chain Tests, Waveform Analyses, Voltage Measurements and Calculations

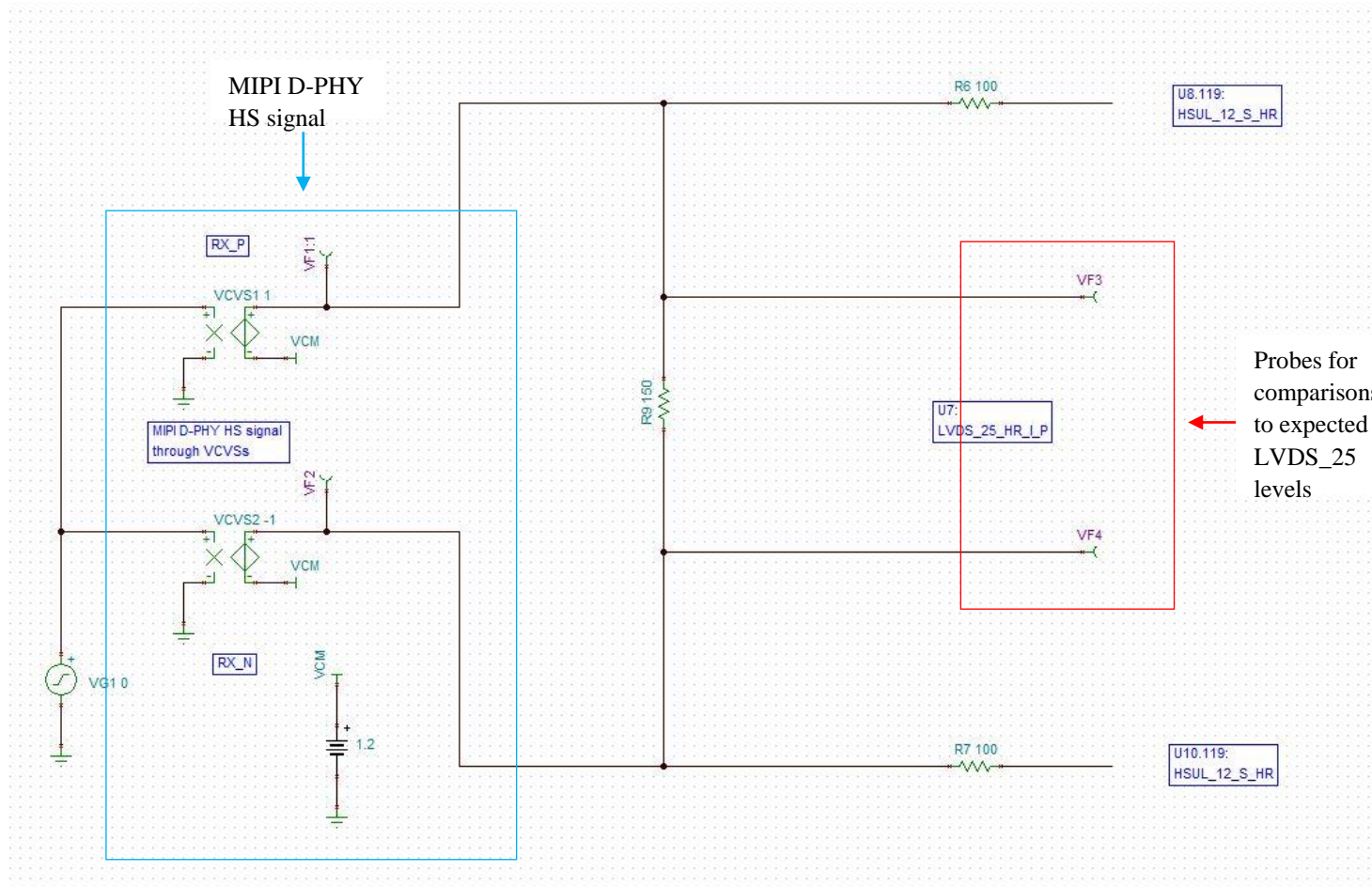
U7 (LVDS_25) + U8/10 (HSUL)

FPGA-Compatible D-PHY Receiver

Baseline Circuit Simulations and Waveform Analyses:

- The FPGA inputs do not need to be simulated in attempting to verify that given a MIPI D-PHY input.
- The resistor network will output a signal that is compatible with the LVDS (for HS) or HSUL (for LP) I/O standard.
- The baseline simulation will be an attempt to see what is present at the resistor network output.
- U8 and U10 are assumed to be high impedance inputs (effectively open) and U7 is assumed to have an internal 100Ω differential termination.
- The **HS (LVDS_25)** and **LP (HSUL_12)** cases are analyzed separately.

U7; HS, (LVDS_25) Baseline Circuit Simulation



U7; HS, (LVDS_25_HR_I_P (Low-Voltage Differential Signaling)) Specifications:

- LVDS is a dedicated differential buffer, which runs at a higher speed compared to 2 single-ended differential buffers.
- The *HS receiver* has a *switchable parallel termination* (as differential signaling).

U7; HS, (LVDS_25) Waveform Analysis

Xilinx Specifications (Expected Values):

$$V_{CCO} = 2.5V$$

$$2.375V < V_{CCO} \text{ (supply voltage)} < 2.625V$$

$$R_T = 100\Omega$$

$$V_{OH, MAX} = 1.675V$$

$$V_{OL, MIN} = 0.700V$$

$$1V < V_{OCM} \text{ (output common-mode voltage)} < 1.425V$$

$$.3V < V_{ICM} < 1.5V$$

Waveform Values (VF3 and VF4):

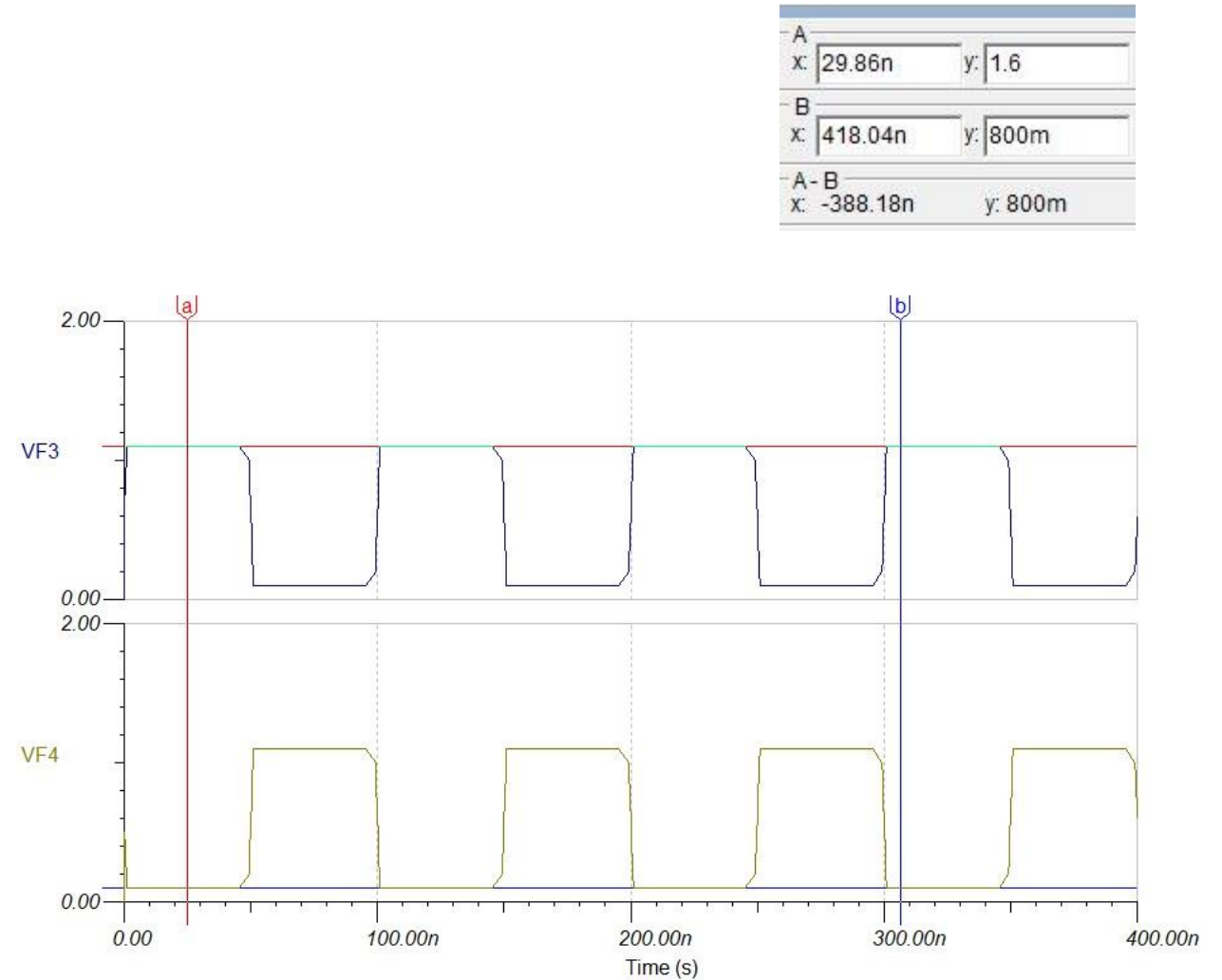
$$VG1 = 0V$$

$$\text{Amplitude: } 0.4V$$

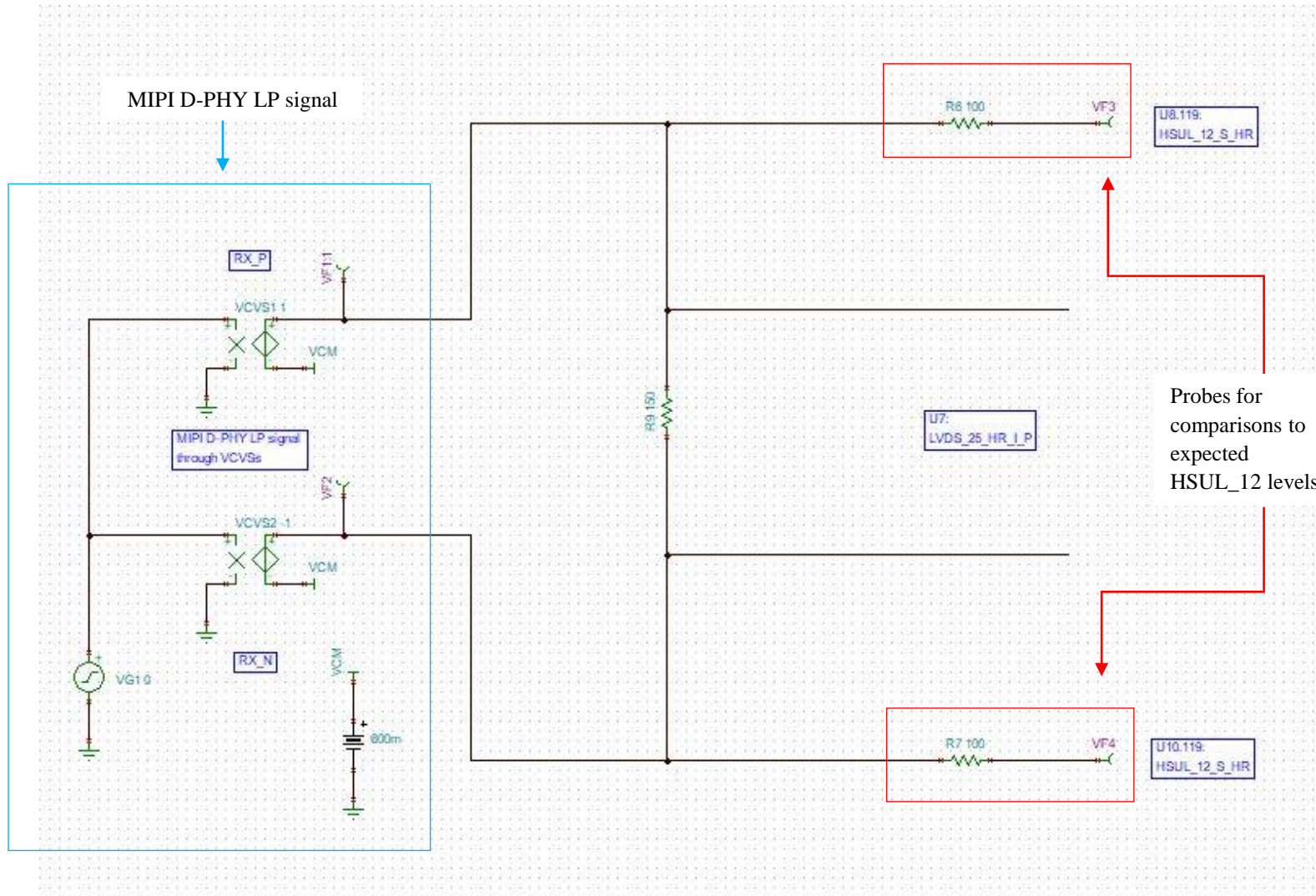
$$V_{CM} = 1.2V$$

$$V_{OL} = 0.8V$$

$$V_{OH} = 1.6V$$



U8/U10; LP, (HSUL_12) Baseline Circuit Simulation



U8/U10; LP, (HSUL_12_S_HR (High Speed Unterminated Logic))

Specifications:

- FPGAs support the HSUL_12 standard for single-ended signaling and differential signaling.”
- The *LP receiver* function as a *low power signaling mechanism*.

Probes for comparisons to expected HSUL_12 levels

U8/U10; LP, (HSUL_12) Waveform Analysis

Xilinx Specifications (Expected Values):

$$V_{\text{REF}} (\text{Input}) = 0.6\text{V}$$

$$V_{\text{CCO}} (\text{Output}) = 1.2\text{ V}$$

$$V_{\text{CCO}} (\text{Input}) = \text{Any}$$

$$-0.300\text{V} < V_{\text{IL}} < V_{\text{REF}} - 0.130\text{V}$$

$$V_{\text{REF}} + 0.130\text{V} < V_{\text{IH}} < V_{\text{CCO}} + 0.300\text{V}$$

$$V_{\text{OL, MAX}} = 20\% (V_{\text{CCO}})$$

$$V_{\text{OH, MIN}} = 80\% (V_{\text{CCO}})$$

Calculations:

$$V_{\text{OL, MAX}} = 20\% (V_{\text{CCO}})$$

$$V_{\text{OL, MAX}} = 20\% (1.2\text{V})$$

$$V_{\text{OL, MAX}} = .24\text{V}$$

$$V_{\text{OH, MIN}} = 80\% (V_{\text{CCO}})$$

$$V_{\text{OH, MIN}} = 80\% (1.2\text{V})$$

$$V_{\text{OH, MIN}} = .96\text{V}$$

Waveform Values (VF3 and VF4):

$$V_{\text{G1}} = 0\text{V}$$

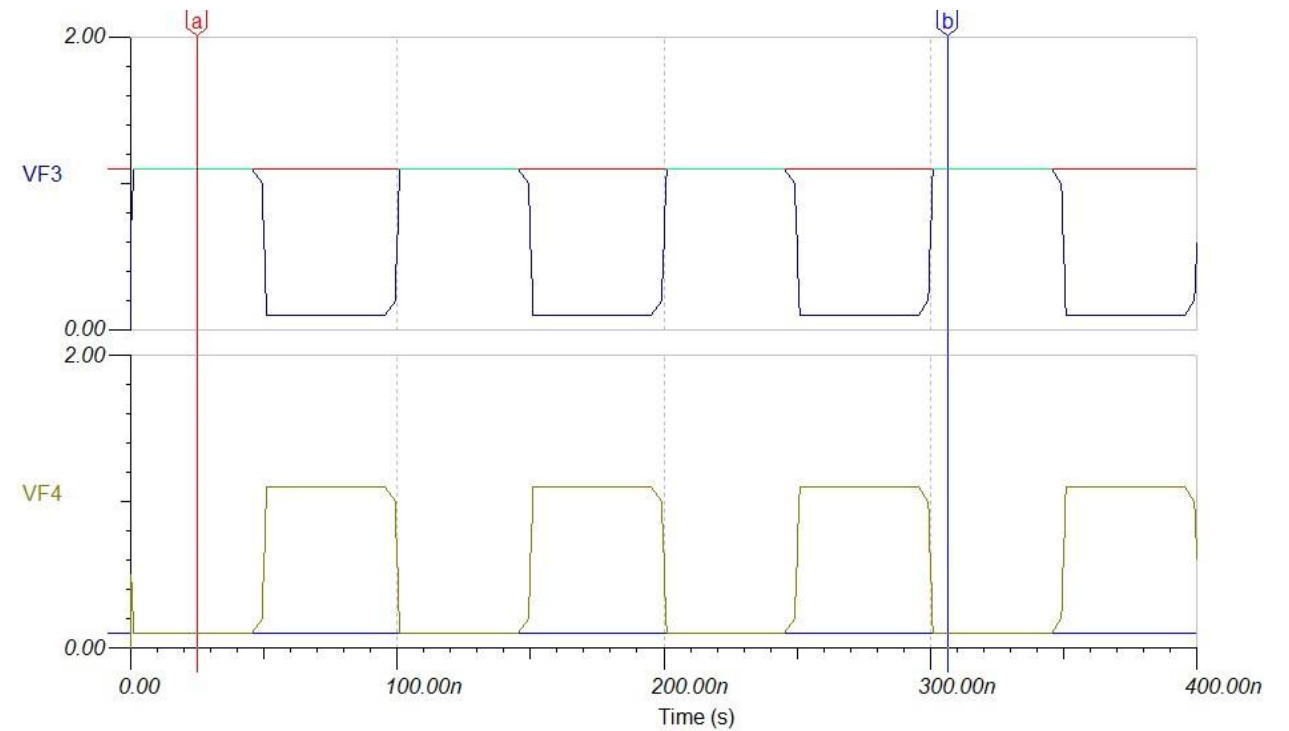
$$\text{Amplitude} = 0.5\text{V}$$

$$V_{\text{CM}} = 0.6\text{V}$$

$$V_{\text{OL}} = 0.1\text{V}$$

$$V_{\text{OH}} = 1.1\text{V}$$

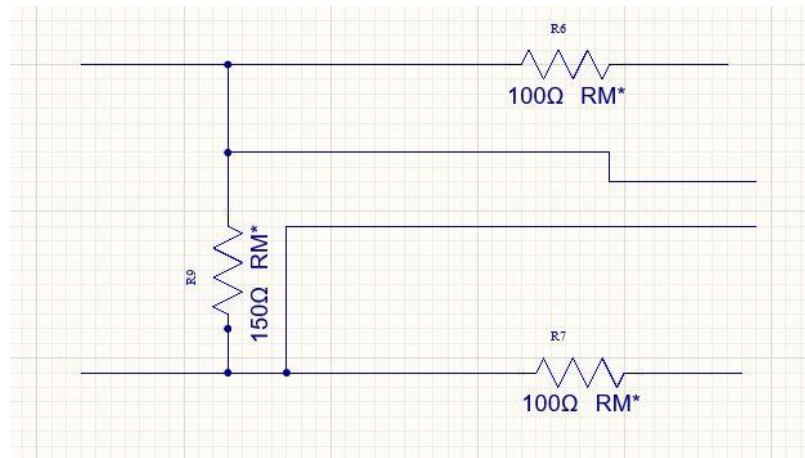
A	x: 24.94n	y: 1.1
B	x: 306.47n	y: 100m
A-B	x: -281.53n	y: 1



Circuit Schematic (.SchDoc):

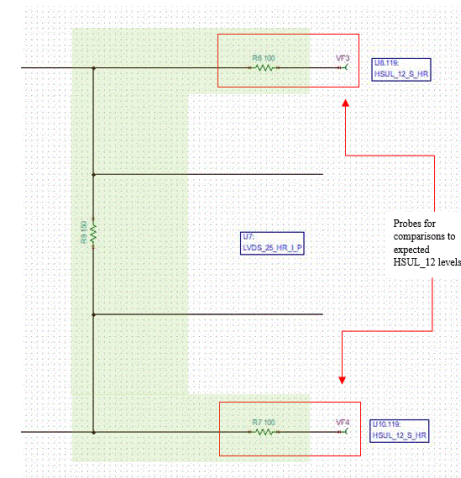
Pin Configuration Requirements:

- Connect 3 copies of the receiver between the FMC connector and the MIPI connector.
 - For the MIPI connector side, follow the pinout in the camera module datasheet (Table 3).
 - For the FMC side:
 - Use pins labelled LA##
 - Keep differential pairs together. For example, if MIPI_D1_P goes to LA03_P, then MIPI_D1_N should go to LA03_N.
 - Have the clock (MIPI_CLK) go to a clock-capable (_CC) LA pin.
- Connect the CSI pins directly between the MIPI connector and FMC connector.
 - For the MIPI connector side, follow the pinout in the camera module datasheet (Table 3).
 - For the FMC side:
 - Use pins labelled LA##
 - Use pins labelled _P

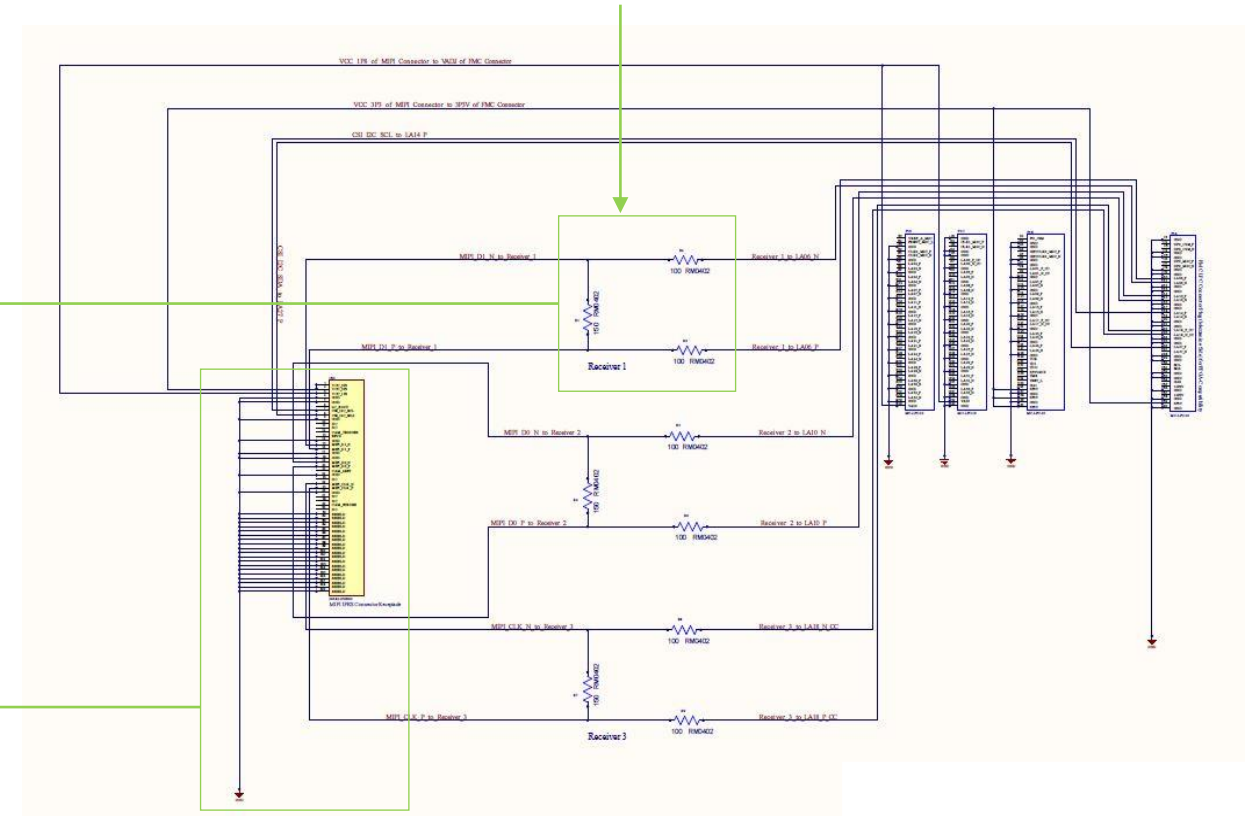


1 Receiver Network with verified resistor values

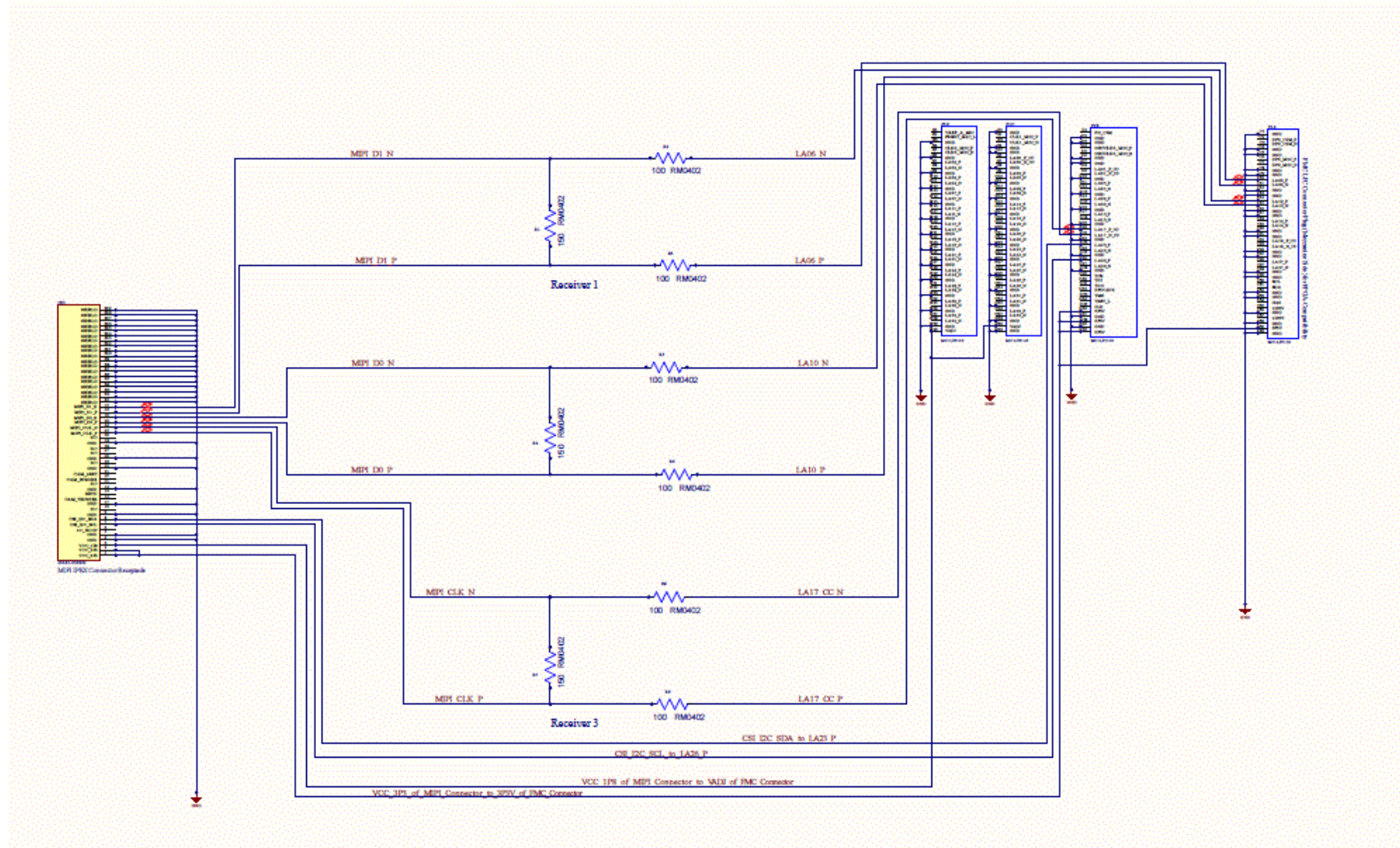
The MIPI IPEX Connector requires spatial reconfiguration during iterative design process. Its I/O pins are rearranged to meet trace routing requirements.



1 D-PHY Receiver network

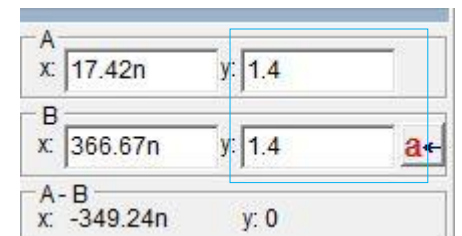
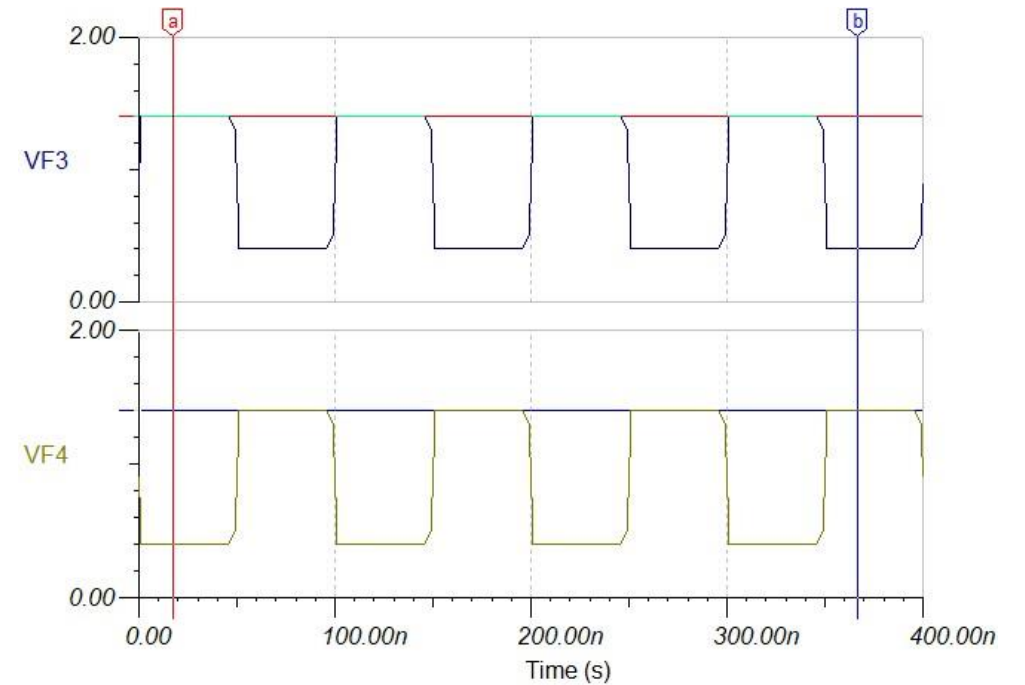
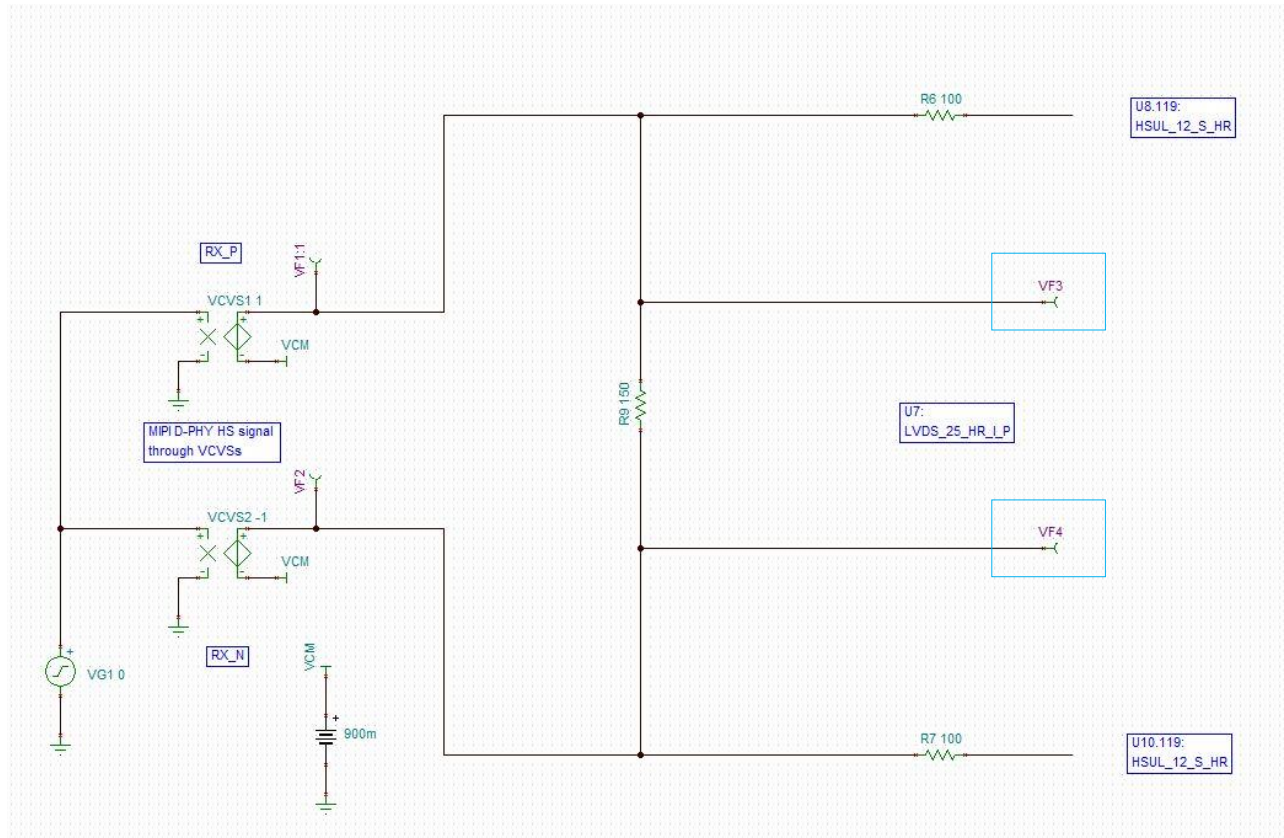


Final Circuit Schematic in Altium



FPGA-Compatible MIPI CSI-2 D-PHY Adapter Board Circuit Schematic

Using the TI-TINA Simulation's Receiver Voltage Probe Results for verification of the 150 Ω resistor package type



Calculations of current and allowable dissipated power for verification of the 150 Ω resistor package type (Using *NEP: Power Dissipation Ratings for Resistors (after 2007)*):

MIL-PRF-55342 Slash Sheet	Chip Size	Old Ratings (Before Oct. 2007)		New Ratings (After Oct. 2007)	
		Power (mW)		Power (mW)	Volt
		Thick Film	Thin Film	Thin & Thick Film	Thin & Thick Film
13	0302	40	40	15	40
11	0402	40	40	25	50
1	0502	20	10	40	50
2	0505	50	25	40	125
12	0603	70	70	50	100
6	0705	100	50	50	150
3	1005	100	50	40	200
10	1010 (FR4)	400	250	75	500
	1010 (Ceramic)	500	250		
7	1206	250	125	100	250
4	1505	150	100	40	150
8	2010 (FR4)	600	400	150	800
	2010 (Ceramic)	800	400		
5	2208	225	200	40	225
9	2512 (FR4)	750	500	200	1000
	2512 (Ceramic)	1000	500		

On calculating for the appropriate power rating for the **150 Ω** resistor:

From the circuit simulation, **V = 1.4 V**.

$$V = IR$$

$$1.4 \text{ V} = (I)(150 \Omega)$$

$$1.4 \text{ V}/(150 \Omega) = 0.00933 \text{ A} = I$$

$$P_{\text{dissipated}} = I^2 R$$

$$P_{\text{dissipated}} = (0.009333333 \text{ A})^2 (150 \Omega)$$

$$P_{\text{dissipated}} = (0.00008711111111)(150) = \mathbf{0.013066667 \text{ W}}$$

$$\text{or simply from } P = V^2/R = (1.4)^2/(150) = 1.96/150 = \mathbf{0.013066667 \text{ W}}$$

If the **calculated dissipated power** does not exceed the power rating of the resistor for a particular package type, then there is no resistor degradation. Since **0.013066667 W** does not exceed the **0402 package type power rating of 50 mW** (or 0.05 W), the **0402 package type** is sufficient to use.

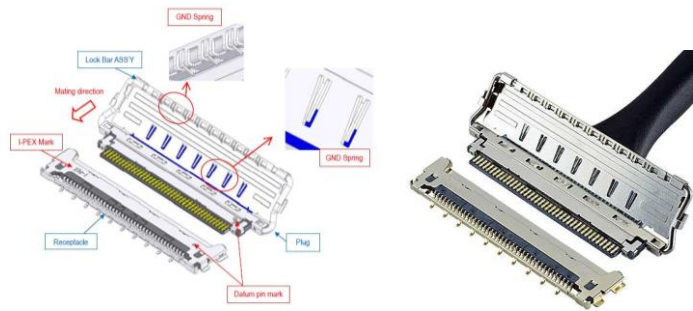
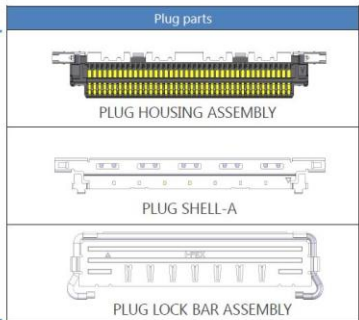
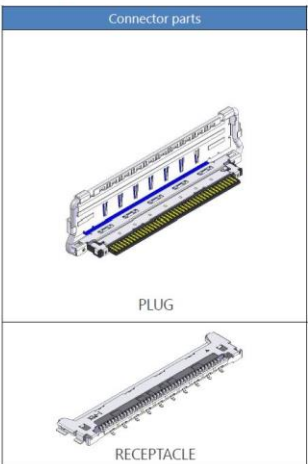
The power rating specifies the maximum steady state power the package allows to dissipate under given conditions (at the rated ambient temperature).

The **voltage rating** is typically for the resistor series and specifies the **maximum peak voltage** that can be continuously applied to a resistor at a rated ambient temperature without resistor degradation.

MIPI I-PEX Connector Receptacle

for high-speed signal transmission between the co-axial camera cable and a circuit board

Component Parts:



5 Pin Description

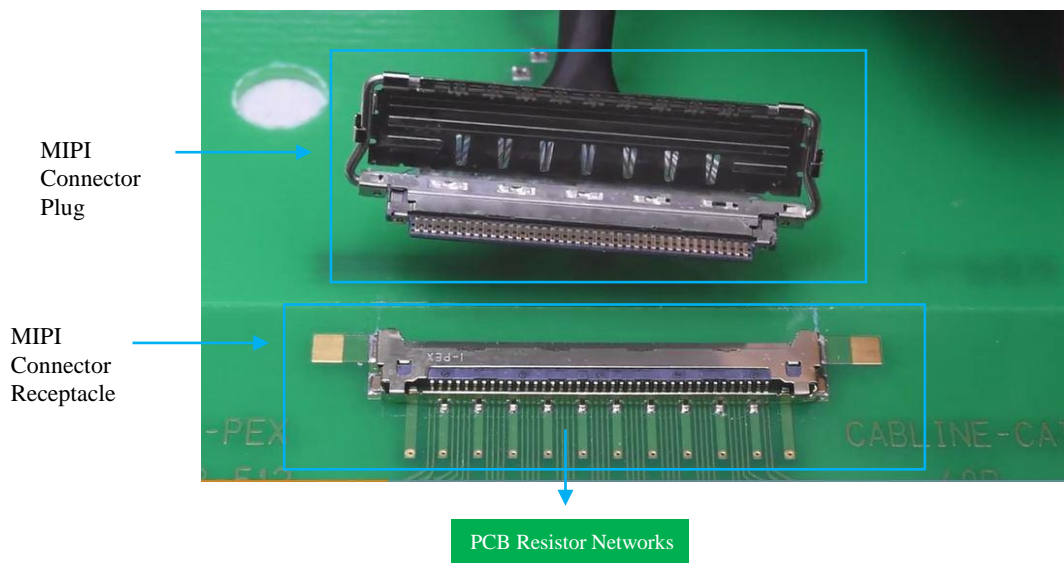
e-CAM222_CUMI2311_MOD has a I-PEX connector (CN1). The pin types are described from sensor perspective. The signal names and pin numbers are given below.

CN1 Pin No	Signal Name	Pin Type	Description
1	VCC_3P3	POWER	3.3V Power supply for camera and adaptor boards
2	VCC_3P3	POWER	3.3V Power supply for camera and adaptor boards
3	VCC_1P8	POWER	1.8V Power supply for camera and adaptor boards
4	GND	POWER	Ground signal for digital and analog
5	GND	POWER	Ground signal for digital and analog
6	uC_BOOT	INPUT	Camera Power down signal
7	CSI_I2C_SCL	INPUT	I2C Clock signal 1.8V I/O. Internal Pull ups are disabled
8	CSI_I2C_SDA	I/O	I2C Data Signal 1.8V I/O. Internal Pull ups are disabled
9	GND	POWER	Ground signal for digital and analog
10	NC	-	NC
11	NC	-	NC
12	CAM_TRIGGER	INPUT	Camera trigger signal 1.8V I/O. Internal PD to 1MΩ
13	RSVD	-	Reserved
14	GND	POWER	Ground signal for digital and analog
15	MIPI_D1_N	OUTPUT	MIPI Data Lane 1 Differential Pair -
16	MIPI_D1_P	OUTPUT	MIPI Data Lane 1 Differential Pair +
17	GND	POWER	Ground signal for digital and analog
18	GND	POWER	Ground signal for digital and analog
19	MIPI_D0_N	OUTPUT	MIPI Data Lane 0 Differential Pair -
20	MIPI_D0_P	OUTPUT	MIPI Data Lane 0 Differential Pair +
21	CAM_nRST	INPUT	Camera reset signal (Active low) 1.8V I/O
22	GND	POWER	Ground signal for digital and analog
23	NC	-	NC
24	MIPI_CLK_N	OUTPUT	MIPI Clock Lane Differential Pair -
25	MIPI_CLK_P	OUTPUT	MIPI Clock Lane Differential Pair +
26	GND	POWER	Ground signal for digital and analog
27	NC	-	NC
28	NC	-	NC
29	CAM_STROBE	OUTPUT	Camera Strobe signal 1.8V I/O
30	NC	-	NC

Table 3: CN1 Pin Descriptions

1	VCC_3P3
2	VCC_3P3
3	VCC_1P8
4	GND
5	GND
6	uC_BOOT
7	CSI_I2C_SCL
8	CSI_I2C_SDA
9	GND
10	NC
11	NC
12	CAM_TRIGGER
13	RSVD
14	GND
15	MIPI_D1_N
16	MIPI_D1_P
17	GND
18	GND
19	MIPI_D0_N
20	MIPI_D0_P
21	CAM_nRST
22	GND
23	NC
24	MIPI_CLK_N
25	MIPI_CLK_P
26	GND
27	NC
28	NC
29	CAM_STROBE
30	NC
S1	SHIELD
S2	SHIELD
S3	SHIELD
S4	SHIELD
S5	SHIELD
S6	SHIELD
S7	SHIELD
S8	SHIELD
S9	SHIELD
S10	SHIELD
S11	SHIELD
S12	SHIELD
S13	SHIELD
S14	SHIELD
S15	SHIELD
S16	SHIELD
S17	SHIELD
S18	SHIELD
S19	SHIELD

Schematic Symbol built to represent the MIPI IPEX Connector Receptacle (in Altium)



MIPI I-PEX Connector Receptacle (CN1 on the e-CAM222_CUMI2311_MOD module)

Specifications

- **Description:** CONN Micro Coaxial CABLINE-CA II P-0.40mm 30Pos with Shield Cover Right Angle SMT
- **Manufacturer:** I-PEX
- **Part Number:** 20682-030E-02
- **Part Name:** Receptacle, 30 pins

CABLINE®-CA II

Fully-shielded with mechanical lock, high-data-rate transfer (20+ Gbps/lane), 0.4 mm pitch, horizontal mating type micro-coaxial connector

Building the MIPI I-PEX Connector Receptacle

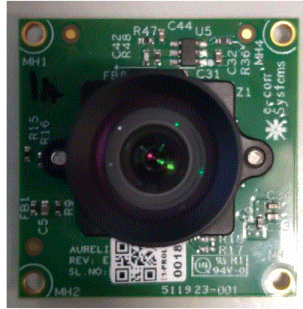


Figure 1: Front View of e-CAM222_CUMI2311_MOD Camera Module



Figure 2: Rear View of e-CAM222_CUMI2311_MOD Camera Module



Part Number: 20682-030E-02
Part Name: Receptacle, 30 pins

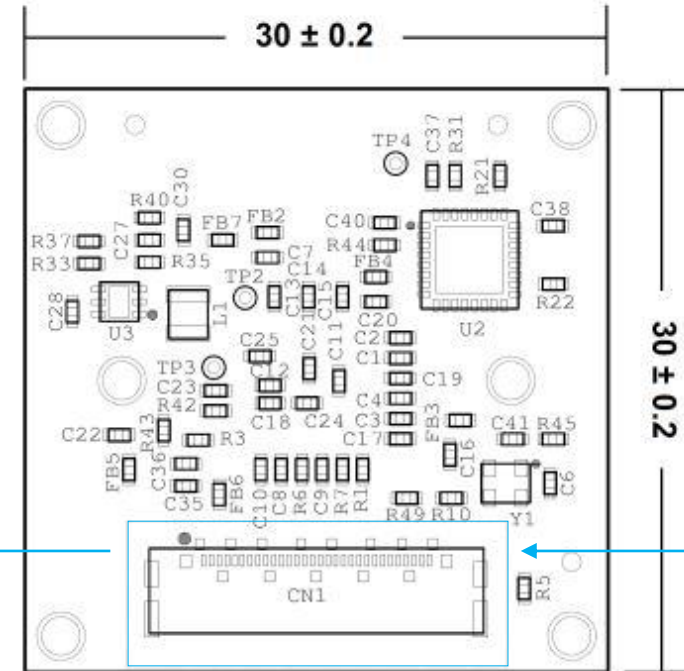


Figure 5: Bottom View of e-CAM222_CUMI2311_MOD

Building a corresponding Altium PCB footprint for the MIPI I-PEX Connector Receptacle (CN1 on the e-CAM222_CUMI2311_MOD module) **to be added to NASA's "SC-Connector-Mech.PcbLib" in Altium:**

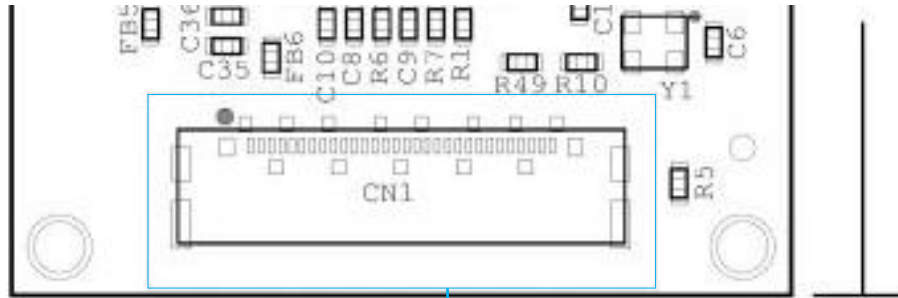
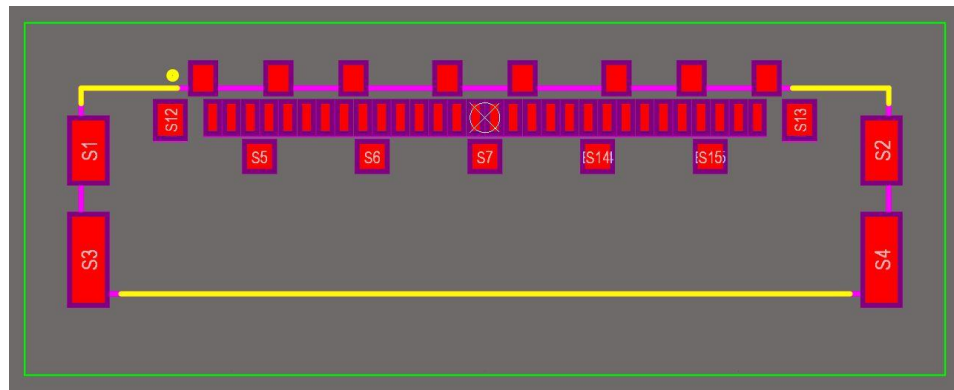


Figure 5: Bottom View of e-CAM222_CUMI2311_MOD



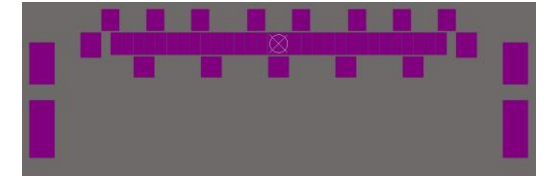
PCB footprint of IPEX MIPI Connector Receptacle built and linked to its schematic symbol (in Altium)

Top and Mechanical Layers

Top Overlay:
silkscreen overlay



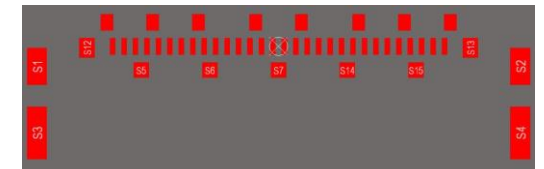
Top Solder: exposed surface mount pads; needs to be coated with solder paste before welding.



Top Paste:



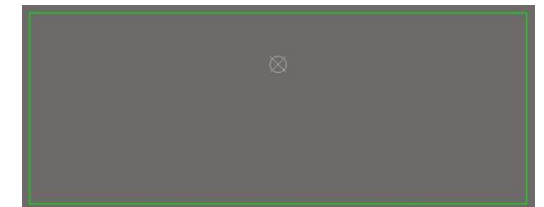
Top Layer:
(Signal Layer); component layer, is mainly used to place components (electrical connections, aka the actual copper layers)



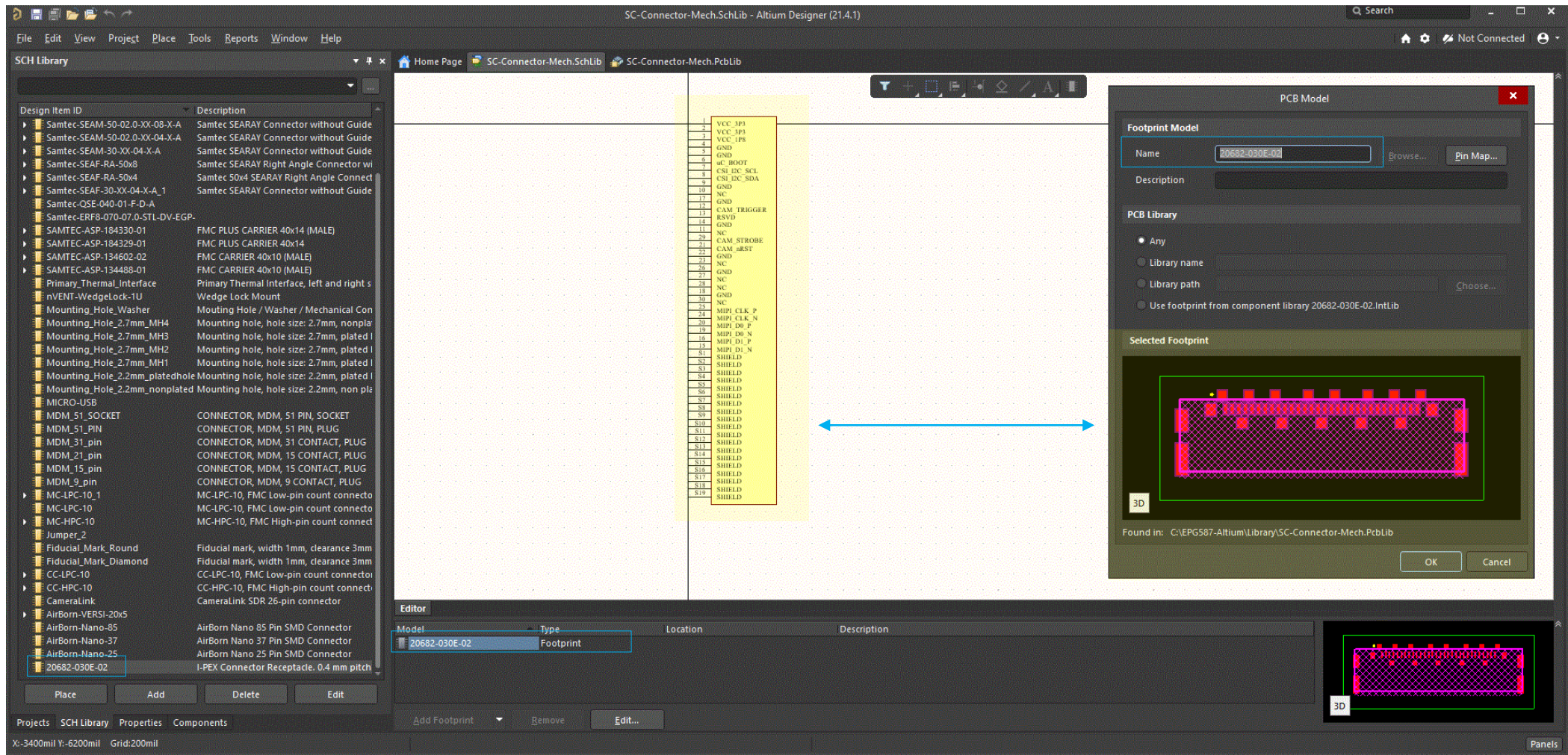
Mechanical 1:



Mechanical 2:



Linking the schematic symbol to the PCB footprint and 3D model between NASA’s “SC-Connector-Mech.SchLib” and “SC-Connector-Mech.PcbLib” in Altium:

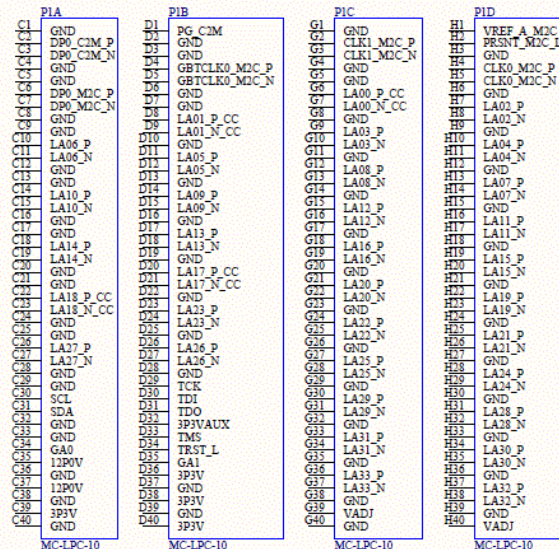


for high-speed signal transmission between the PCB and FPGA

MC-LPC-10, Part A, FMC Low-pin count connector, lead free, 160 I/O pins, male, 10 mm mated stack height. **ASP-134604-01.**

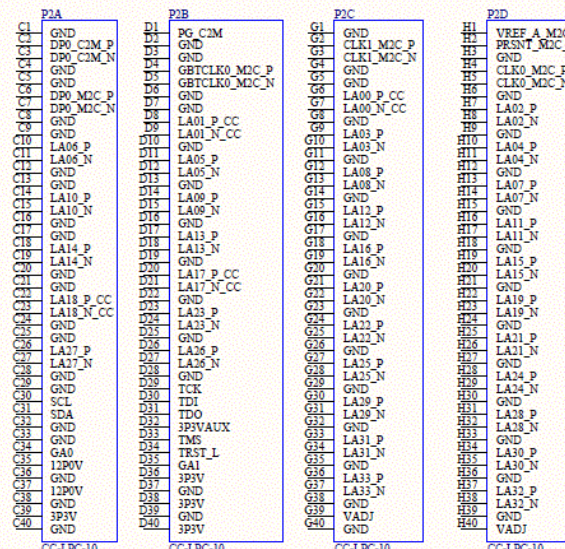
The schematic symbol requires all 160 pins for proper representation.

Low-pin count (LPC) connector. Mezzanine card side



The plug and receptacle are expected to be compatible for signal and mechanical connectivity.

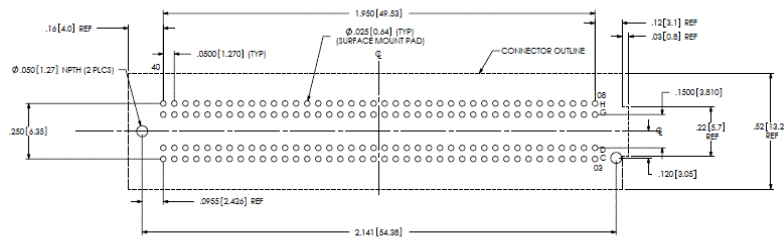
Long-pin count (1 PC) connector, Carrier card side



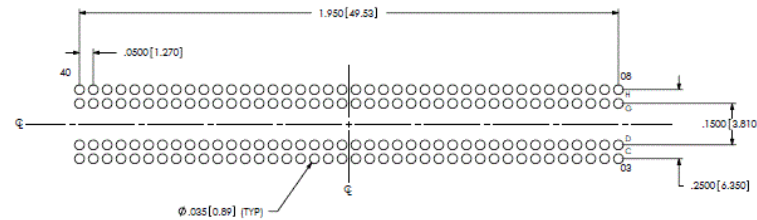
G	F	E	D	C
GND			PG_C2M	GND
CLK1_M2C_P			GND	DP0_C2M_P
CLK1_M2C_N			GND	DP1_C2M_N
GND			GBTCLK0_M2C_P	GND
GND			GBTCLK0_M2C_N	GND
LA09_P_CC			GND	DP5_M2C
LA09_N_CC			GND	DP6_M2C_N
GND			LA01_P_CC	GND
LA03_P			LA01_N_CC	GND
LA03_N			GND	LA06_P
GND			LA05_P	LA06_N
LA08_P			LA05_N	GND
LA08_N			GND	GND
GND			LA09_P	LA10_P
LA12_P			LA09_N	LA10_N
LA12_N			GND	GND
GND			LA13_P	GND
LA16_P			LA13_N	LA14_P
LA16_N			GND	LA14_N
GND			LA17_P_CC	GND
LA26_P			LA17_N_CC	GND
LA20_N			GND	LA18_P_CC
GND			LA23_P	LA18_N_CC
LA22_P			LA23_N	GND
LA22_N			GND	GND
GND			LA26_P	LA27_P
LA25_P			LA26_N	LA27_N
LA25_N			GND	GND
GND			TD0	GND
LA29_P			TD1	S0A
LA29_N			TD0	S0A
GND			3P3WAUX	GND
LA31_P			TMS	GND
LA31_N			TRST_L	GA0
GND			GA1	12P0V
LA33_P			3P3V	GND
LA33_N			GND	12P1V
GND			3P3V	GND
W0A0			GND	3P3V
GND			3P3V	GND

C1		H40
C2	GND	VADJ
C3	DP0_C2M_P	GND
C4	DP0_C2M_N	LA32_N
C5	GND	LA32_P
C6	GND	GND
C7	DP0_M2C_P	LA30_N
C8	DP0_M2C_N	LA30_P
C9	GND	GND
C10	GND	LA28_N
C11	LA06_P	LA28_P
C12	GND	GND
C13	GND	LA24_P
C14	GND	GND
C15	LA10_P	LA21_N
C16	LA10_N	LA21_P
C17	GND	GND
C18	LA14_P	LA19_N
C19	LA14_N	LA19_P
C20	GND	GND
C21	GND	LA15_N
C22	LA18_P_CC	LA15_P
C23	LA18_N_CC	LA15_N
C24	GND	LA11_N
C25	GND	LA11_P
C26	GND	GND
C27	LA27_P	GND
C28	LA27_N	LA07_N
C29	GND	LA07_P
C30	SCL	GND
C31	SDA	LA04_N
C32	GND	LA04_P
C33	GND	GND
C34	GA0	LA02_N
C35	I2P0V	LA02_P
C36	GND	GND
C37	I2P0V	CLK0_M2C_N
C38	GND	CLK0_M2C_P
C39	3P1V	GND
D1	GND	PRSENT_M2C_L
D2	DP0_C2M_P	VREF_A_VDC
D3	GND	GND
D4	GND	GND
D5	GBTCLK0_M2C_P	LA33_N
D6	GBTCLK0_M2C_N	LA33_P
D7	GND	GND
D8	LA01_P_CC	LA31_N
D9	LA01_N_CC	LA31_P
D10	GND	GND
D11	GND	LA29_N
D12	LA05_P	LA29_P
D13	LA05_N	GND
D14	LA09_P	LA25_N
D15	LA09_N	LA25_P
D16	GND	GND
D17	GND	LA22_N
D18	LA13_P	LA22_P
D19	LA13_N	GND
D20	GND	LA20_N
D21	LA17_P_CC	LA20_P
D22	GND	GND
D23	LA23_P	LA16_N
D24	LA23_N	LA16_P
D25	GND	GND
D26	LA26_P	LA12_N
D27	LA26_N	LA12_P
D28	GND	GND
D29	TCK	LA08_N
D30	TDI	LA08_P
D31	TDO	GND
D32	TPDMAUX	LA05_N
D33	TMS	LA05_P
D34	TRST_L	GND
D35	GA1	LA09_N_CC
D36	3P1V	LA09_P_CC
D37	GND	GND
D38	GND	GND
D39	3P1V	CLK1_M2C_N
D40	3P1V	CLK1_M2C_P

Schematic Symbol built to represent the Mezzanine FMC Connector Plug (in Altium)



RECOMMENDED PCB LAYOUT FOR ASP-134603-01
ALL DIMENSIONS SYMMETRIC ABOUT THE CENTERLINE



RECOMMENDED STENCIL LAYOUT FOR ASP-134603-01
ALL DIMENSIONS SYMMETRIC ABOUT THE CENTERLINE

VITA 57

FPGA Mezzanine Card (FMC)

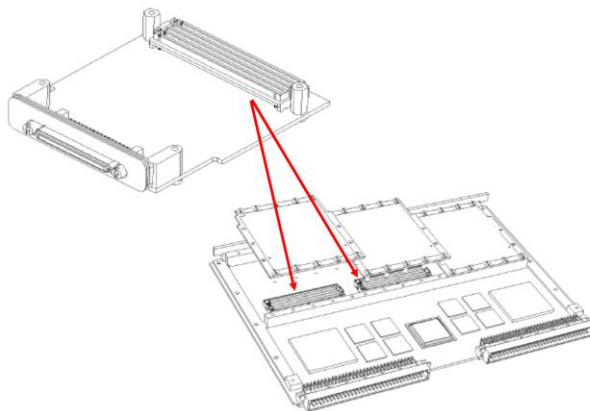
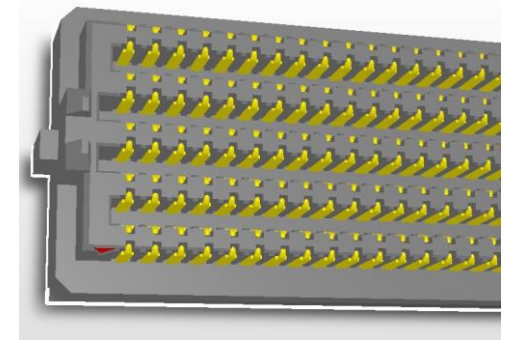
Plugs		
FMC Part No.	Samtec Part No.	Molex Part No.
MC-HPC-8.5L	ASP-134601-01	45970-4117
MC-HPC-8.5	ASP-134602-01	45970-4115
MC-HPC-10L	ASP-134487-01	45970-4317
MC-HPC-10	ASP-134488-01	45970-4315
MC-LPC-8.5L	ASP-134605-01	45970-4107
MC-LPC-8.5	ASP-134606-01	45970-4105
MC-LPC-10L	ASP-127797-01	45970-4307
MC-LPC-10	ASP-134604-01	45970-4305
Receptacles		
FMC Part No.	Samtec Part No.	Molex Part No.
CC-HPC-10L	ASP-134485-01	45971-4317
CC-HPC-10	ASP-134486-01	45971-4315
CC-LPC-10L	ASP-127796-01	45971-4307
CC-LPC-10	ASP-134603-01	45971-4305

CC = Socket (Carrier Side)

MC = Terminal (Module Side)

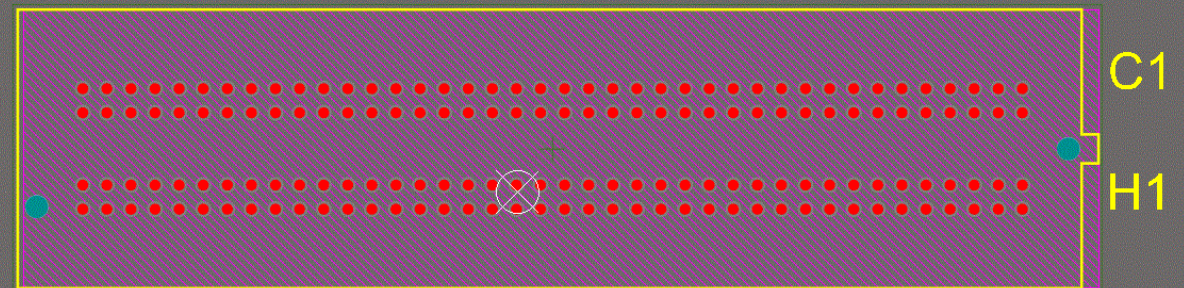
The Mezzanine Card side (PCB side) FMC Connector Plugs as LPC variant.
Selected for Adapter PCB: **ASP-134604-01**.

The Carrier Card side (FPGA side) FMC Connector Receptacles as LPC variant.



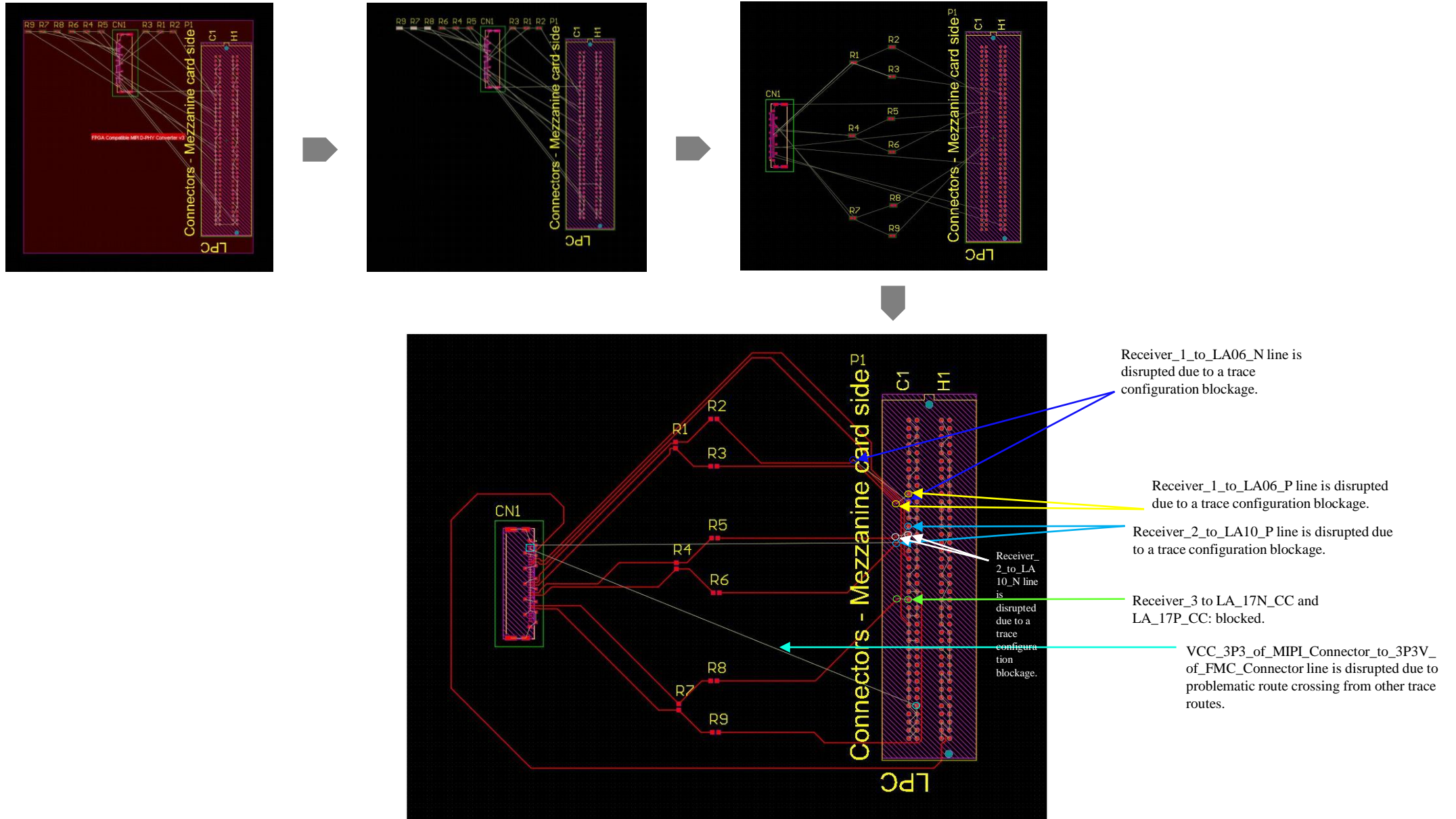
Connectors - Mezzanine card side

LPC

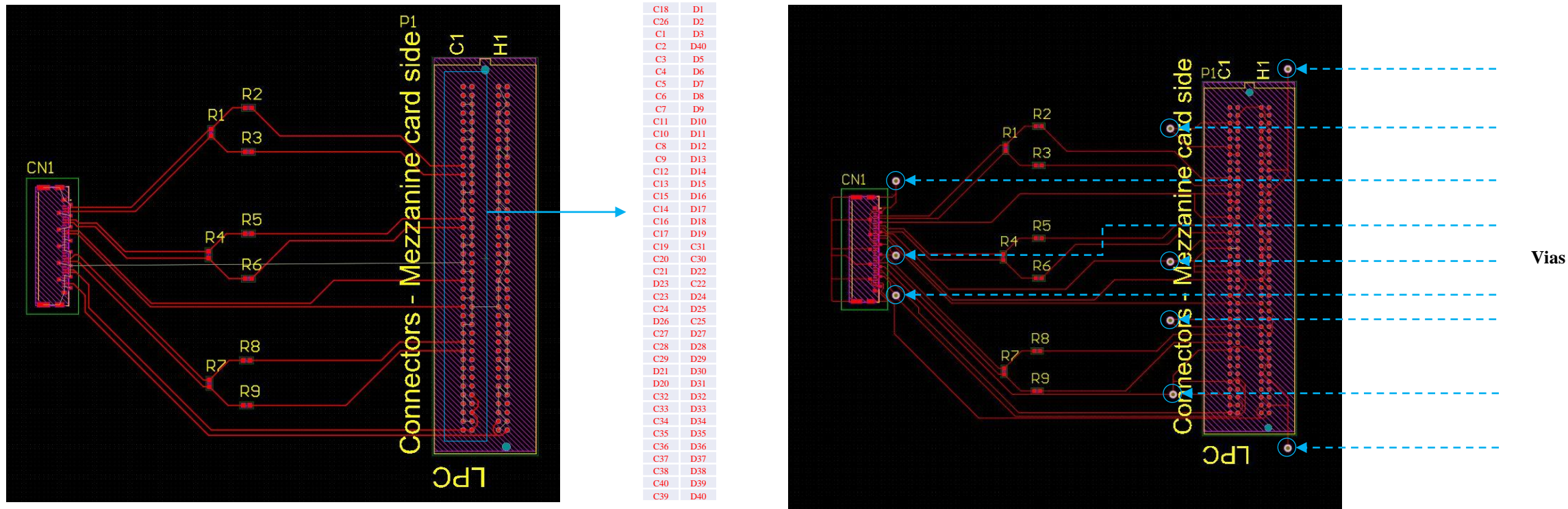


PCB footprint of FMC Connector Plug built and linked to its schematic symbol (in Altium)

Trace Routing Optimization from Default PCB Top Signal Layer



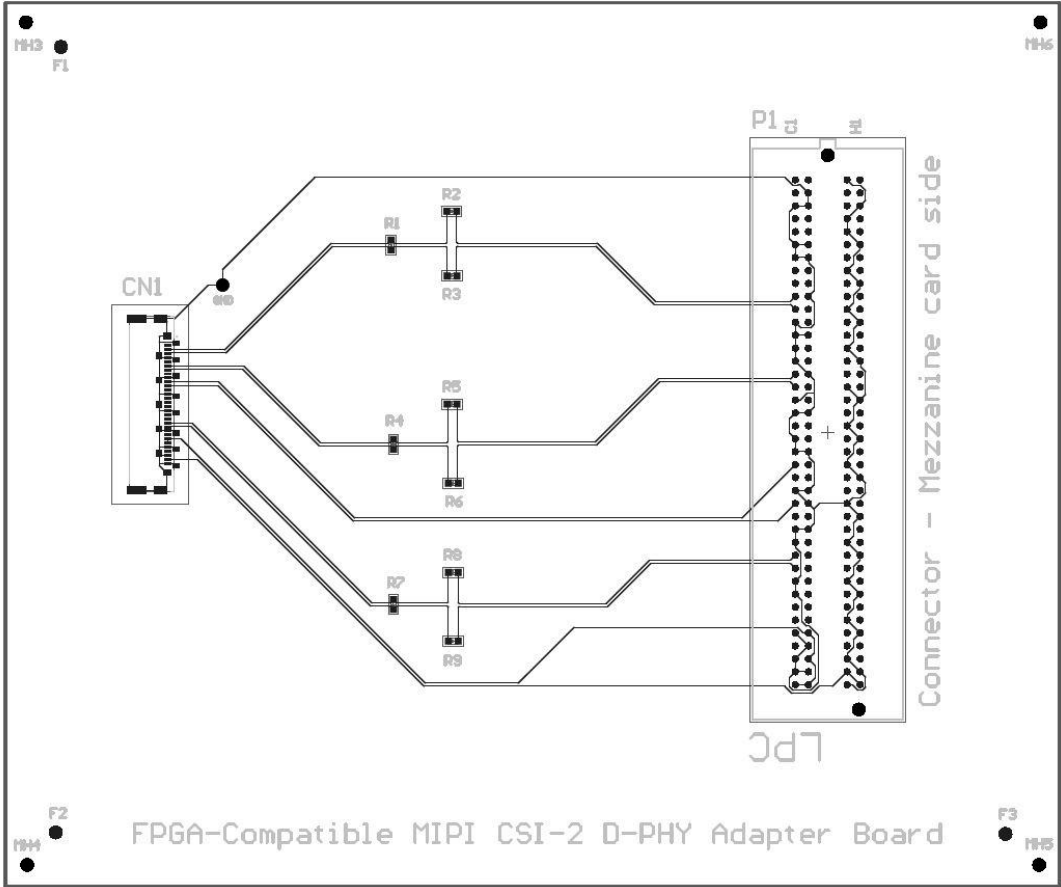
Optimization of Trace Routes and Via Placement



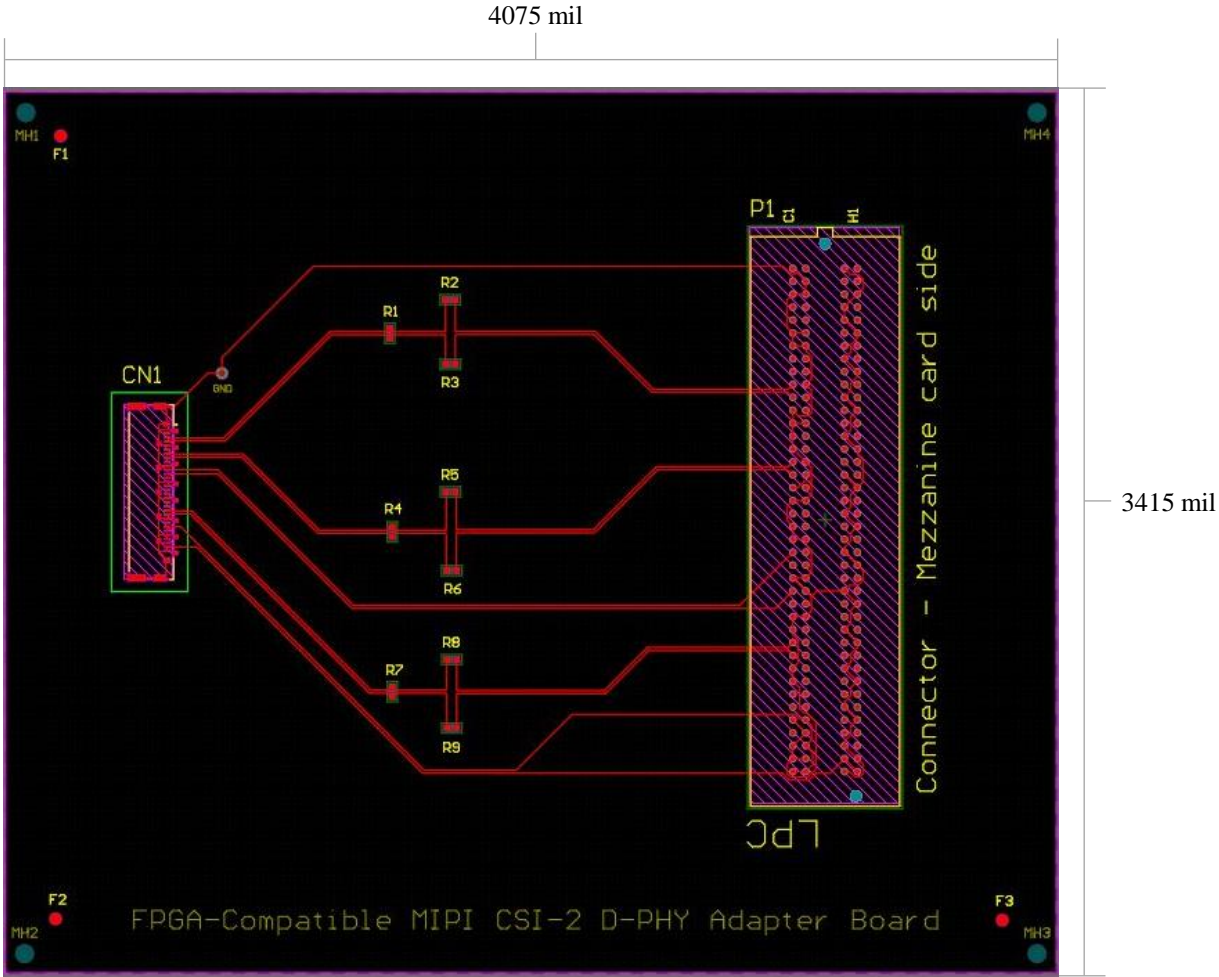
After pin swapping *within* and *between* the pin columns of the FMC Connector, the FMC Connector columns with pins routed to components and MIPI IPEX Connector pins have an alternative arrangement for the purpose of trace route optimization. The configuration still requires differential pair routing.

Via count minimization helps to reduce the number of trace routes on the board, ultimately reducing the amount of time spent on the board's signal connectivity.

Final PCB Configuration: FPGA- Compatible MIPI CSI-2 (Camera Serial Interface) D-PHY Adapter Board

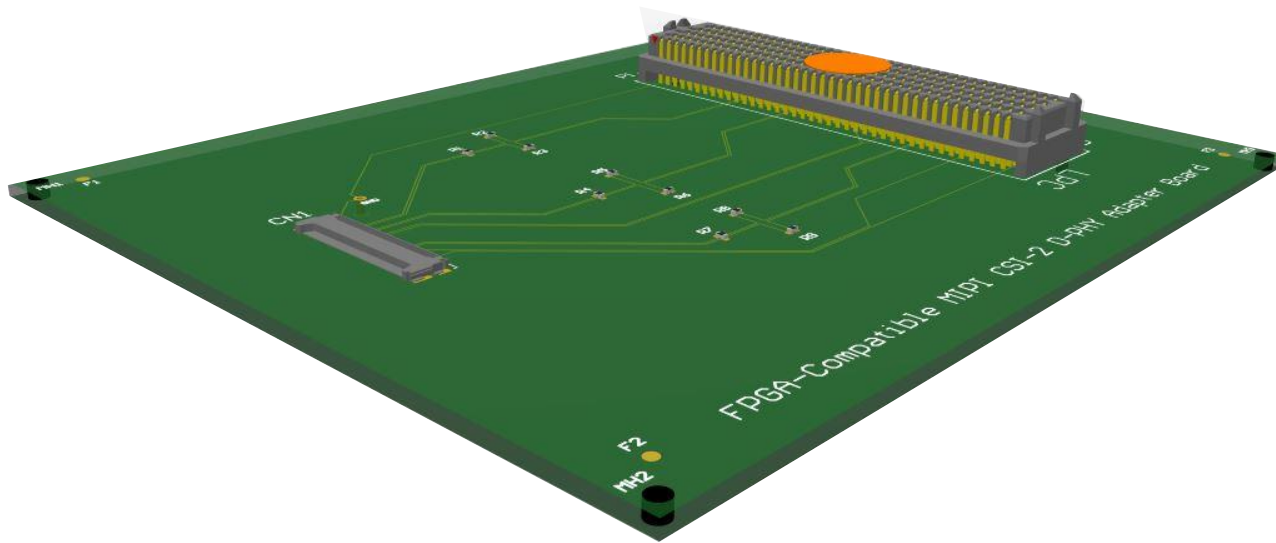


Final PCB Print (Assembly Drawing) of Adapter Board

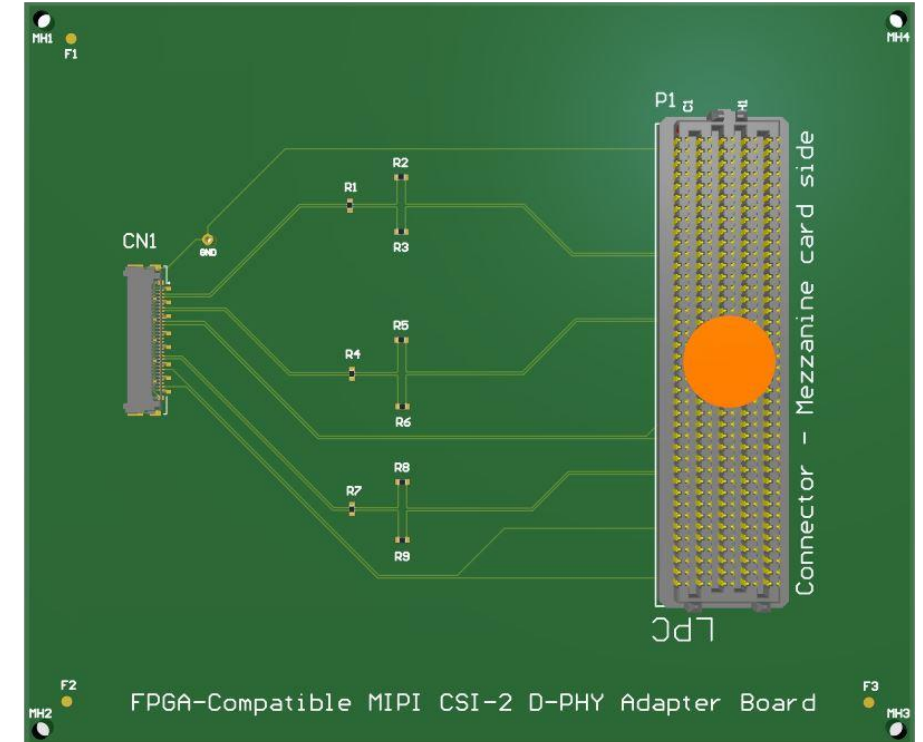


2D View of Final PCB layout of FPGA-Compatible MIPI CSI-2 D-PHY Adapter Board with both differential pairs and single routes

Final PCB Configuration in Altium's 3D View: FPGA-Compatible MIPI CSI-2 (Camera Serial Interface) D-PHY Adapter Board



Final PCB in Rotated View (XYZ Plane)



Final PCB in Top View

Once the adapter board PCB is fabricated and assembled, it can be used to demonstrate the validity of the circuit design prior to it being incorporated into the VADIR flight board design.



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- [2] C. Wilson, Science Data Processing Branch, Software Engineering Division, NASA GSFC, “SpaceCube. A Family of Reconfigurable Hybrid On-Board Science Data Processors,” Future In-Space Operations (FISO) Working Group Seminar, 2020, January.
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- [3] M. Defossez, Xilinx, “D-PHY Solutions. XAPP894 (v1.0.1),” 1, February, 2021.
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- [3] IPEX, <https://www.i-pex.com/>

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- [1] TI-TINA Simulation Tool Documentation, <https://www.ti.com/tool/TINA-TI>
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- [3] Altium Designer Documentation, <https://www.altium.com/documentation/altium-designer/>



Acronyms

Acronym	Definition
MIPI	Mobile Industry Processor Interface
CSI	Camera Serial Interface
D-PHY	500 Mbps Physical Layer
FPGA	Field Programmable Gate Array
I/O	Input Output
FMC, LPC	FPGA Mezzanine Card, Low Pin Count
PCB	Printed Circuit Board
VADIR	VADIR (Versatile Analog/Digital Interface)
LVDS	Low-voltage differential signaling
HS	High Speed
HSUL	High-Speed Unterminated Logic
LP	Low Power
CS ²	CubeSat Card Standard

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