Development of the MIPI Camera Interface Prototype Adapter Board

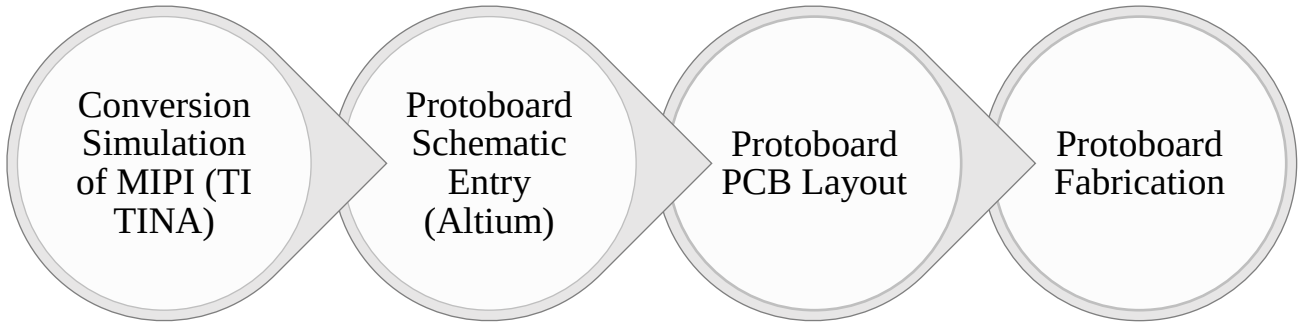
Intern: Haruka Kido
Bachelor of Science in Electrical Engineering
University of North Dakota

Mentor: Alessandro Geist. **Co-mentor:** Cody Brewer
Embedded Processing Group, Code 587. Data Processing Branch, Software Engineering Division,
Space Technology Mission Directorate, GSFC, NASA

Project Description

This project is the development of the **prototype FPGA-Compatible MIPI CSI-2 (Camera Serial Interface) D-PHY adapter board**. The FPGA used on the SpaceCube processor card does not have I/O that natively supports the D-PHY standard, and thus requires additional external components to adapt the interface to the FPGAs I/O. The goal of this project is to develop a prototype board with this external circuitry. The project tasks include **1)** preliminary research and analysis of the adapter circuit requirements involving waveform comparisons, **2)** signal processing chain tests for voltage measurements, **3)** calculations from I/O channel system simulations in TI-TINA, **4)** components' values and circuit configuration verifications, **5)** protoboard schematic entry, **6)** both PCB footprint builds and PCB layout in Altium Designer, and lastly, **7)** PCB manufacturing. This adapter board is useful in data conversion and transmission from the MIPI camera module to the FPGA, a D-PHY circuit arrangement used in NASA's SpaceCube Mini's VADIR (Versatile Analog/Digital Interface) between the MIPI Camera module and the Backplane Connector.

FPGA-Compatible MIPI CSI-2 D-PHY Adapter Board Development Methodology



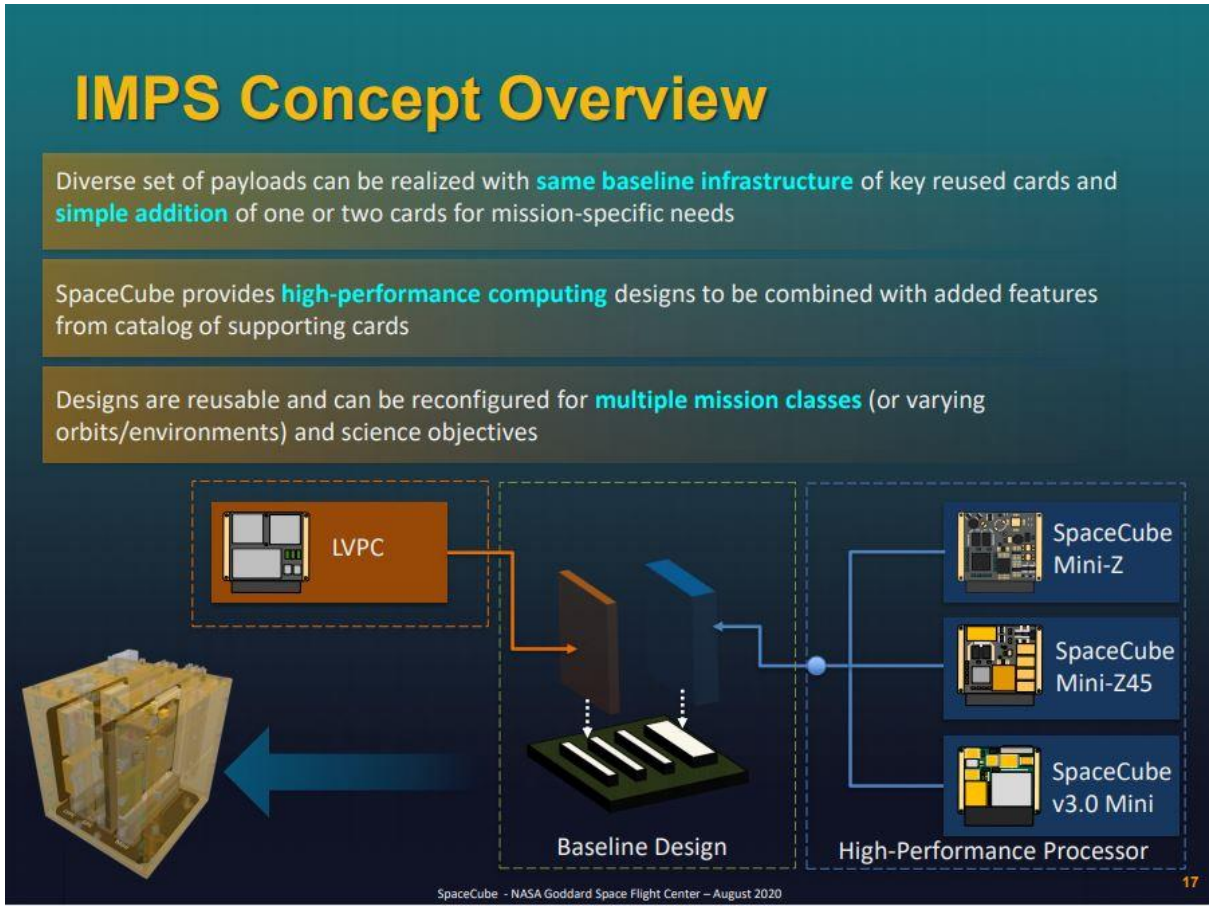
- Research MIPI D-PHY and LVDS: Expected Voltage Levels and Rates
- Transmitter and Receiver Circuit Simulations
- Waveform Outputs from signal processing chain tests for voltage measurements
- Calculations from I/O channel system simulations
- Components' values and circuit configuration verifications

- Parts selection and symbol builds
- Schematic Entry: Add and wire components, adjust I/O pin arrangements

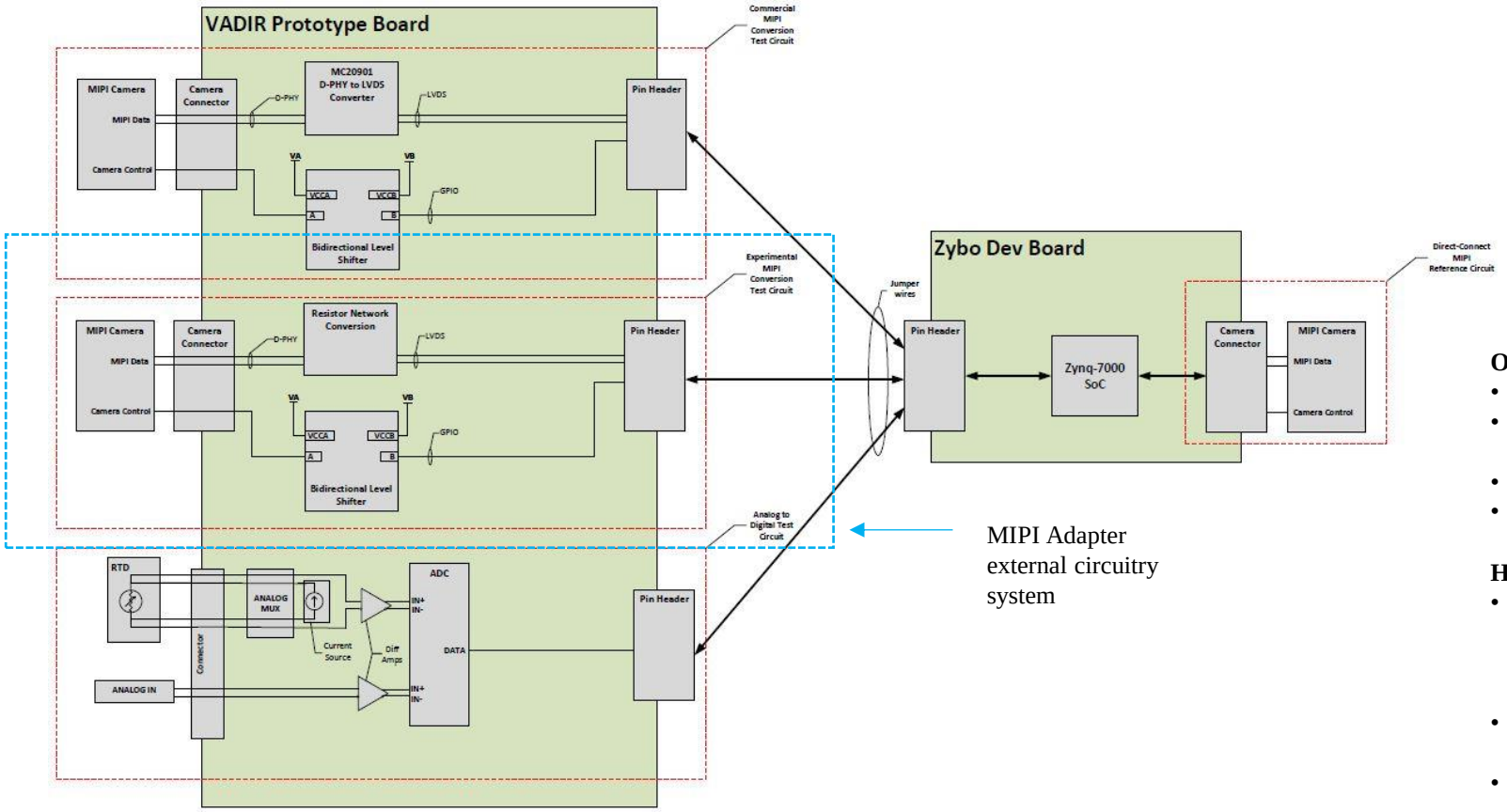
- PCB footprint builds > Component placements
- Determination of PCB Stack-Up and Rules (length-matching for differential pairs, controlled impedance, copper specifications: trace measurements) > Trace Routing

- Final gerber file output, assembly drawings, BOM
- Quotes
- Place Order

Engineering Contextualization: SpaceCube Configurable Slices



Engineering Contextualization: MIPI Adapter in SpaceCube's Versatile Analog-Digital Interface (VADIR) Card



MIPI Adapter external circuitry system

Overview:

- Multiple configurable analog inputs in CubeSat form-factor
- Selective population enables SWAP-C savings depending on mission needs
- On-board level shifter allows for multiple control voltages
- Conforms to CubeSat Card Standard (CS^2)

High-Level Specifications:

- 24-bit Science & Telemetry ADC
  - 2 independent ADCs, up to 52ksps each
  - 16x 4-wire RTD up to 45kΩ resistance
  - 15x Single-Ended or Differential Analog Inputs
- 12-bit Housekeeping ADC
  - 8x 0-5V Single-Ended Analog Inputs
- Bias Supplies
  - 2x LDO supplies, <1.5A, 1.2-3.3V
- Requires ±12V, +5V, and +3.3V
- Requires 16x I/O lines (1.8V or 3.3V)

Preliminary Research and Analysis: Schematics of Resistor Networks and System Integration Mapping of MIPI CSI-2 Transceiver Unit

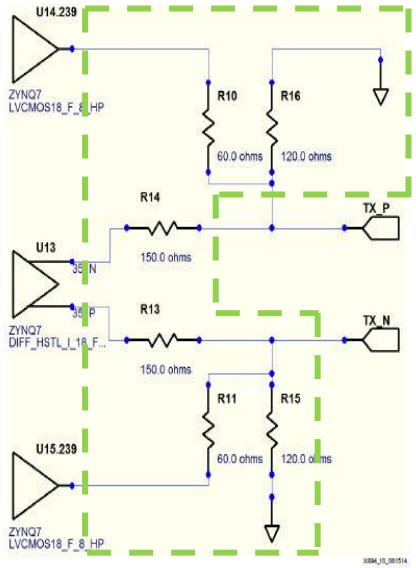


Figure 10: FPGA Compatible D-PHY Transmitter

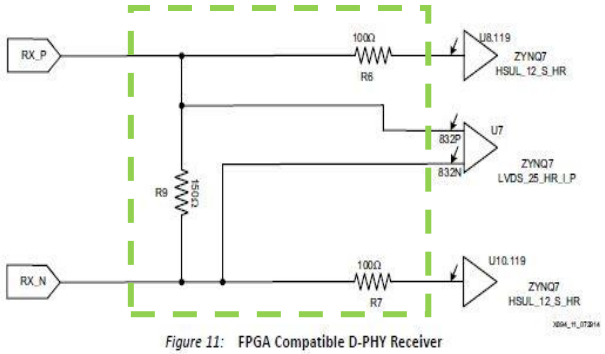
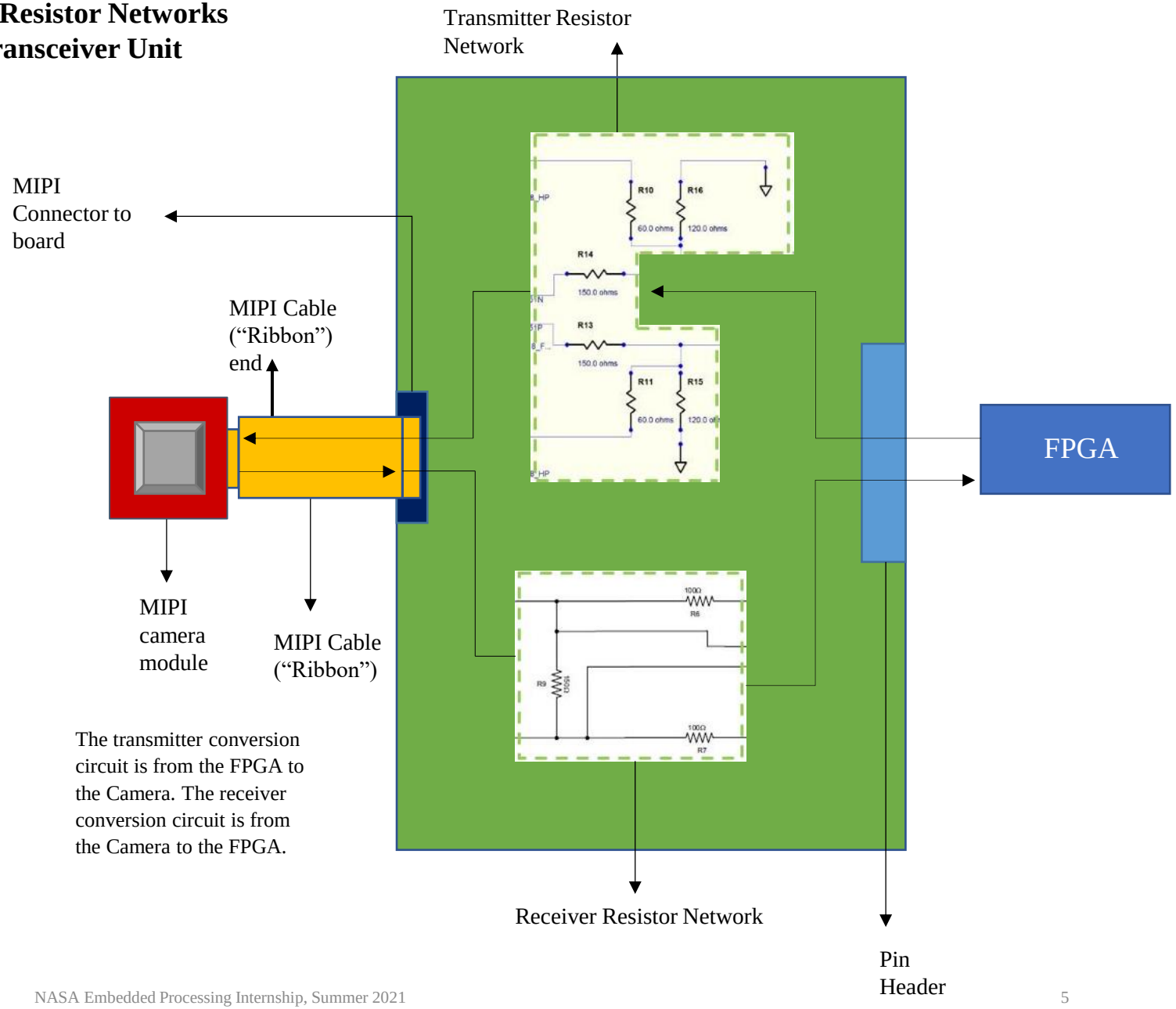


Figure 11: FPGA Compatible D-PHY Receiver



The transmitter conversion circuit is from the FPGA to the Camera. The receiver conversion circuit is from the Camera to the FPGA.

TI TINA Simulations for Receiver Network:

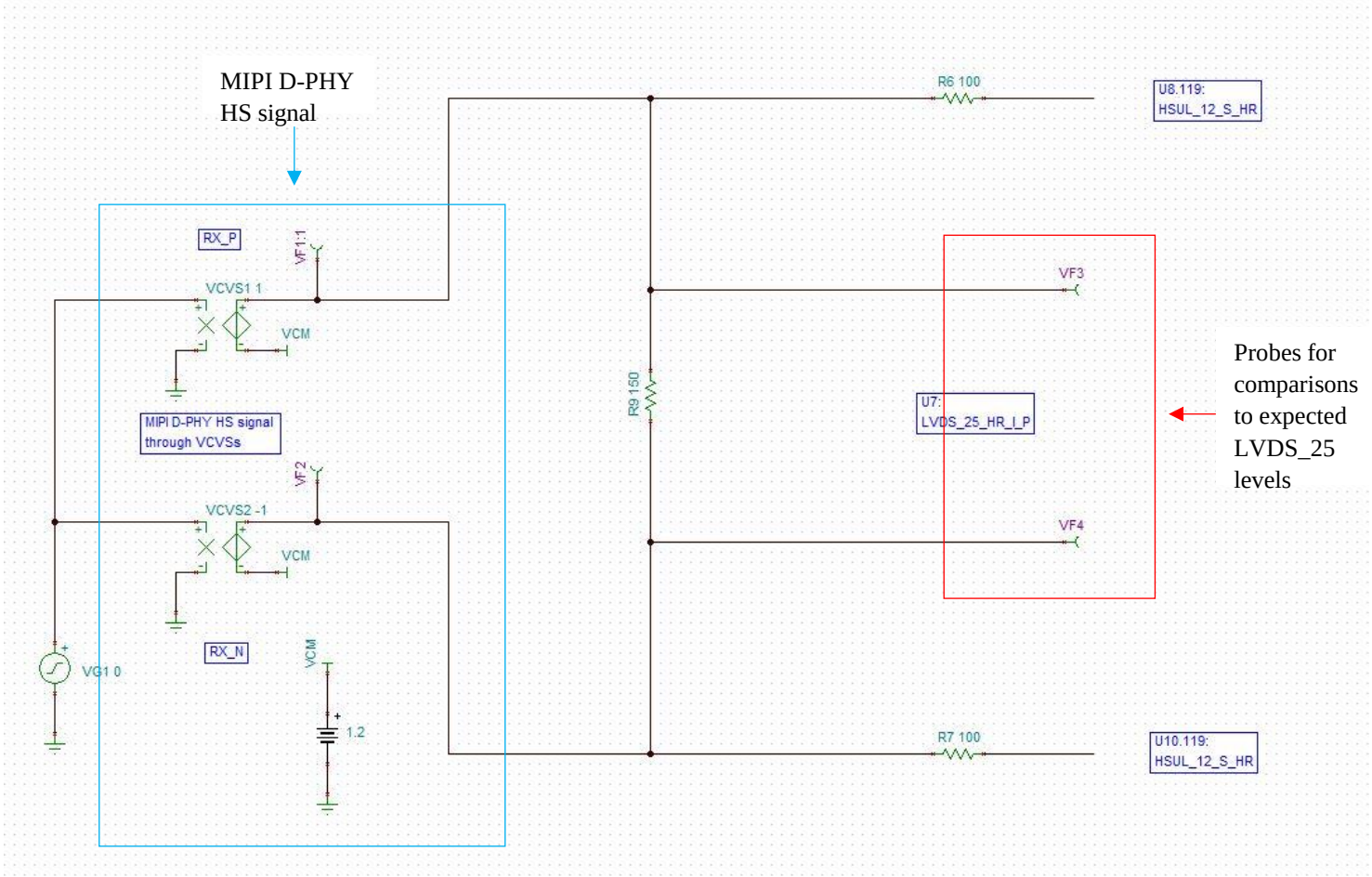
Signal-Processing Chain Tests, Waveform Analyses, Voltage Measurements and Calculations

U7 (LVDS_25) + U8/10 (HSUL)

FPGA-Compatible D-PHY Receiver
Baseline Circuit Simulations and Waveform Analyses:

- The FPGA inputs do not need to be simulated in attempting to verify that given a MIPI D-PHY input, the resistor network will output a signal that is compatible with the LVDS (for HS) or HSUL (for LP) I/O standard.
- The baseline simulation will be an attempt to see what is present at the resistor network output.
- U8 and U10 are assumed to be high impedance inputs (effectively open) and U7 is assumed to have an internal 100Ω differential termination.
- The **HS (LVDS_25)** and **LP (HSUL_12)** cases are analyzed separately.

U7; HS, (LVDS_25) Baseline Circuit Simulation



U7; HS, (LVDS_25_HR_I_P (Low-Voltage Differential Signaling)**)** Specifications:

- LVDS is a dedicated differential buffer, which runs at a higher speed compared to 2 single-ended differential buffers.
- The *HS receiver* has a *switchable parallel termination* (as differential signaling).

U7; HS, (LVDS_25) Waveform Analysis

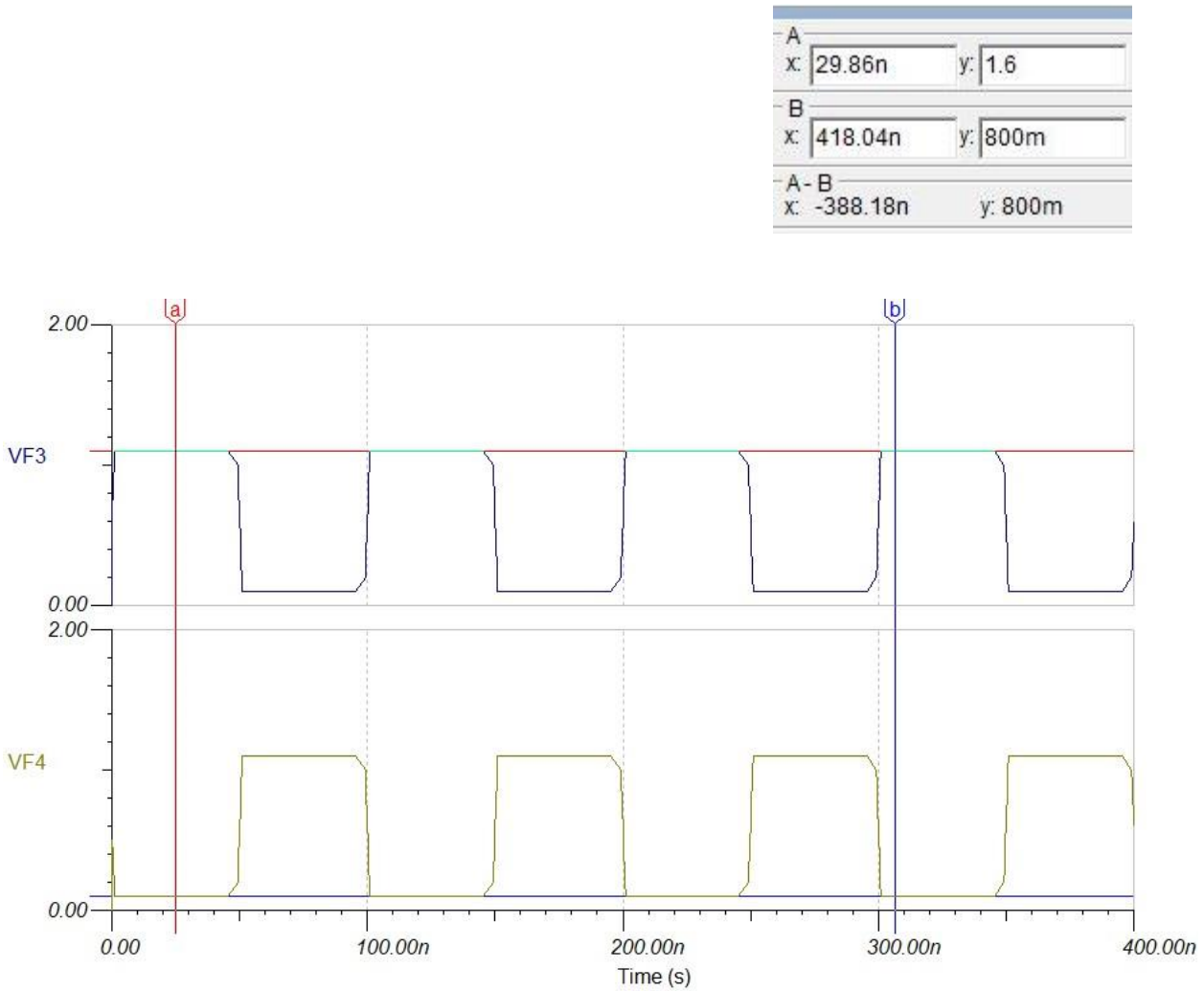
Xilinx Specifications (Expected Values):

V_{CCO} = 2.5V
2.375V < V_{CCO} (supply voltage) < 2.625V

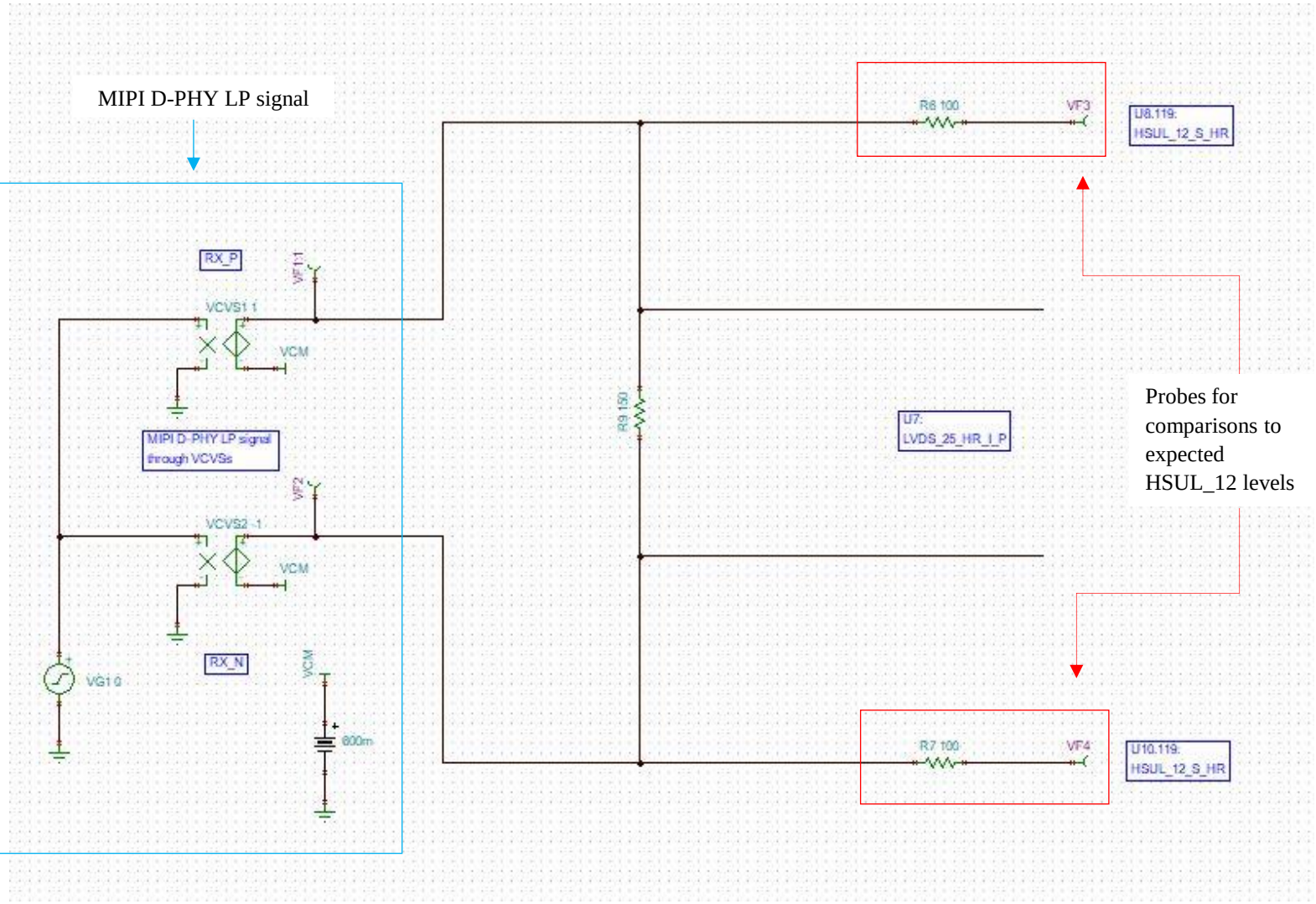
R_T = 100Ω
$V_{OH, MAX}$ = 1.675V
$V_{OL, MIN}$ = 0.700V
1V < V_{OCM} (output common-mode voltage) < 1.425V
.3 V < V_{ICM} < 1.5 V

Waveform Values (VF3 and VF4):

VG1 = 0V
Amplitude: 0.4V
VCM = 1.2V
V_{OL} = 0.8V
V_{OH} = 1.6V



U8/U10; LP, (HSUL_12) Baseline Circuit Simulation



U8/U10; LP, (HSUL_12_S_HR (High Speed Unterminated Logic)**)** Specifications:

- FPGAs support the HSUL_12 standard for single-ended signaling and differential signaling.
- The *LP receiver* function as a *low power signaling mechanism.*

U8/U10; LP, (HSUL_12) Waveform Analysis

Xilinx Specifications (Expected Values):

V_{REF} (Input) = 0.6V
V_{CCO} (Output) = 1.2 V
V_{CCO} (Input) = Any

$-0.300V < V_{IL} < V_{REF} - 0.130V$
$V_{REF} + 0.130V < V_{IH} < V_{CCO} + 0.300V$
$V_{OL, MAX} = 20\% (V_{CCO})$
$V_{OH, MIN} = 80\% (V_{CCO})$

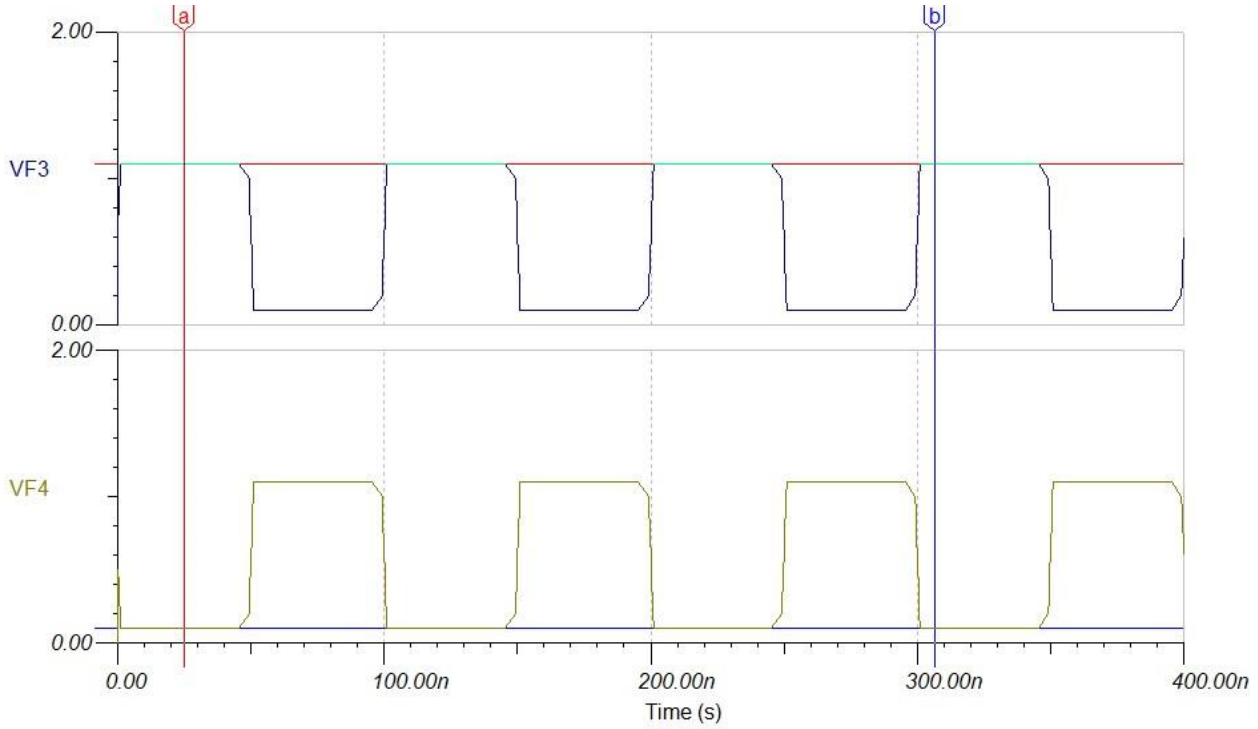
Calculations:

$V_{OL, MAX} = 20\% (V_{CCO})$
$V_{OL, MAX} = 20\% (1.2V)$
$V_{OL, MAX} = .24V$

$V_{OH, MIN} = 80\% (V_{CCO})$
$V_{OH, MIN} = 80\% (1.2V)$
$V_{OH, MIN} = .96V$

Waveform Values (VF3 and VF4):

VG1 = 0V
Amplitude = 0.5V
VCM = 0.6V
$V_{OL} = 0.1V$
$V_{OH} = 1.1V$

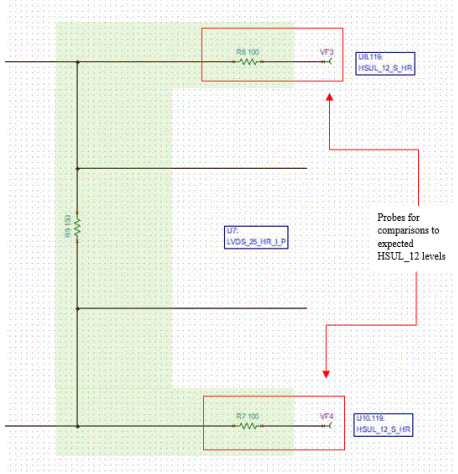


Circuit Schematic (.SchDoc):

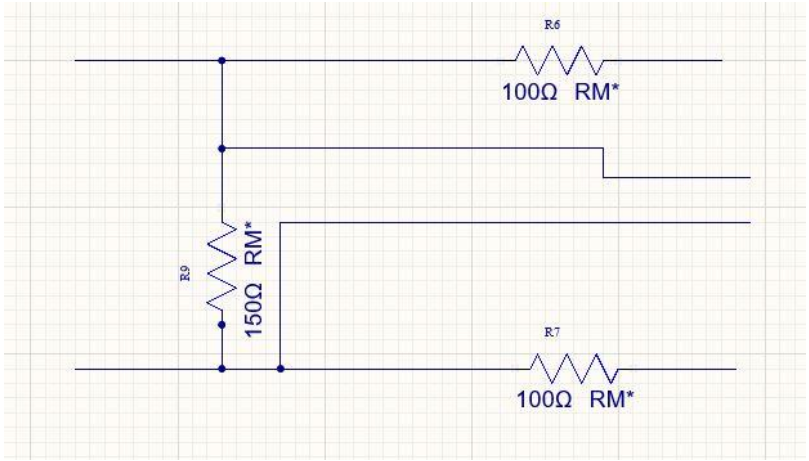
Pin Configuration Requirements:

- Connect 3 copies of the receiver between the FMC connector and the MIPI connector.
  - For the MIPI connector side, follow the pinout in the camera module datasheet (Table 3).
  - For the FMC side:
    - Use pins labelled LA##
    - Keep differential pairs together. For example, if MIPI_D1_P goes to LA03_P, then MIPI_D1_N should go to LA03_N.
    - Have the clock (MIPI_CLK) go to a clock-capable (_CC) LA pin.

- Connect the CSI pins directly between the MIPI connector and FMC connector.
  - For the MIPI connector side, follow the pinout in the camera module datasheet (Table 3).
  - For the FMC side:
    - Use pins labelled LA##
    - Use pins labelled _P

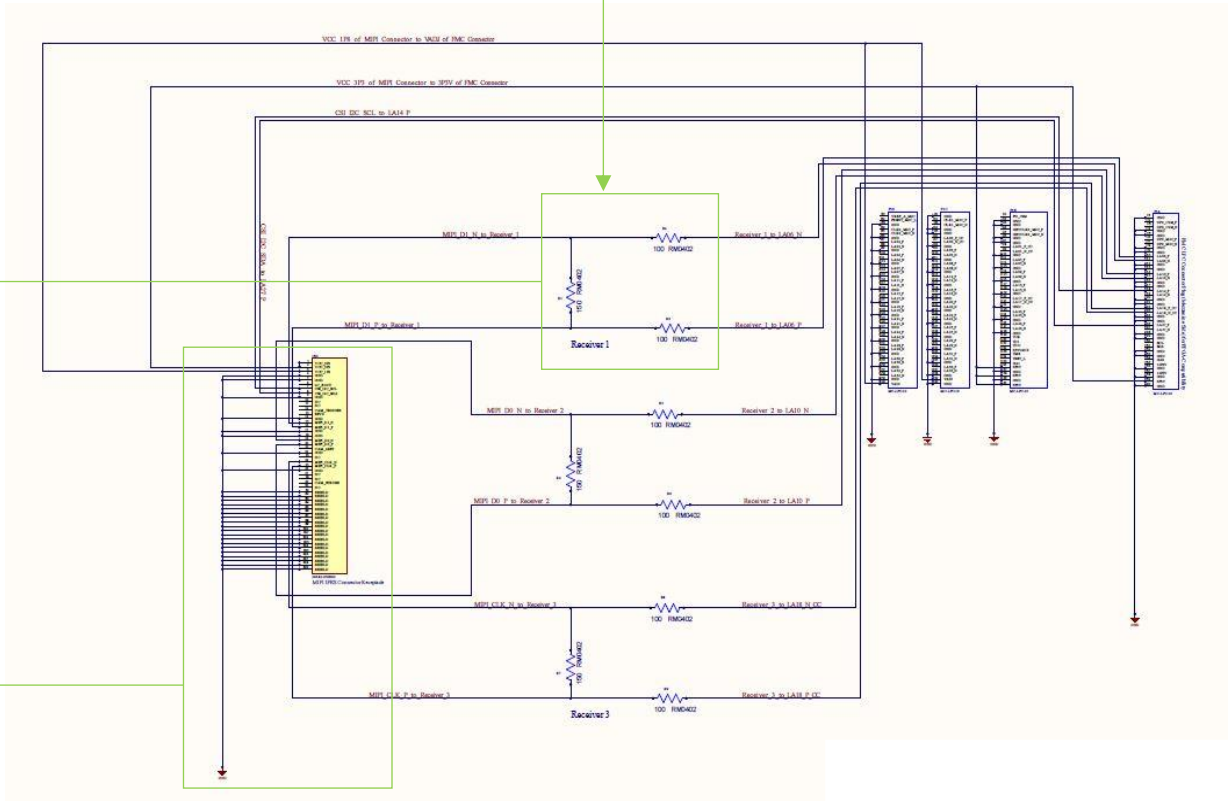


1 D-PHY Receiver network

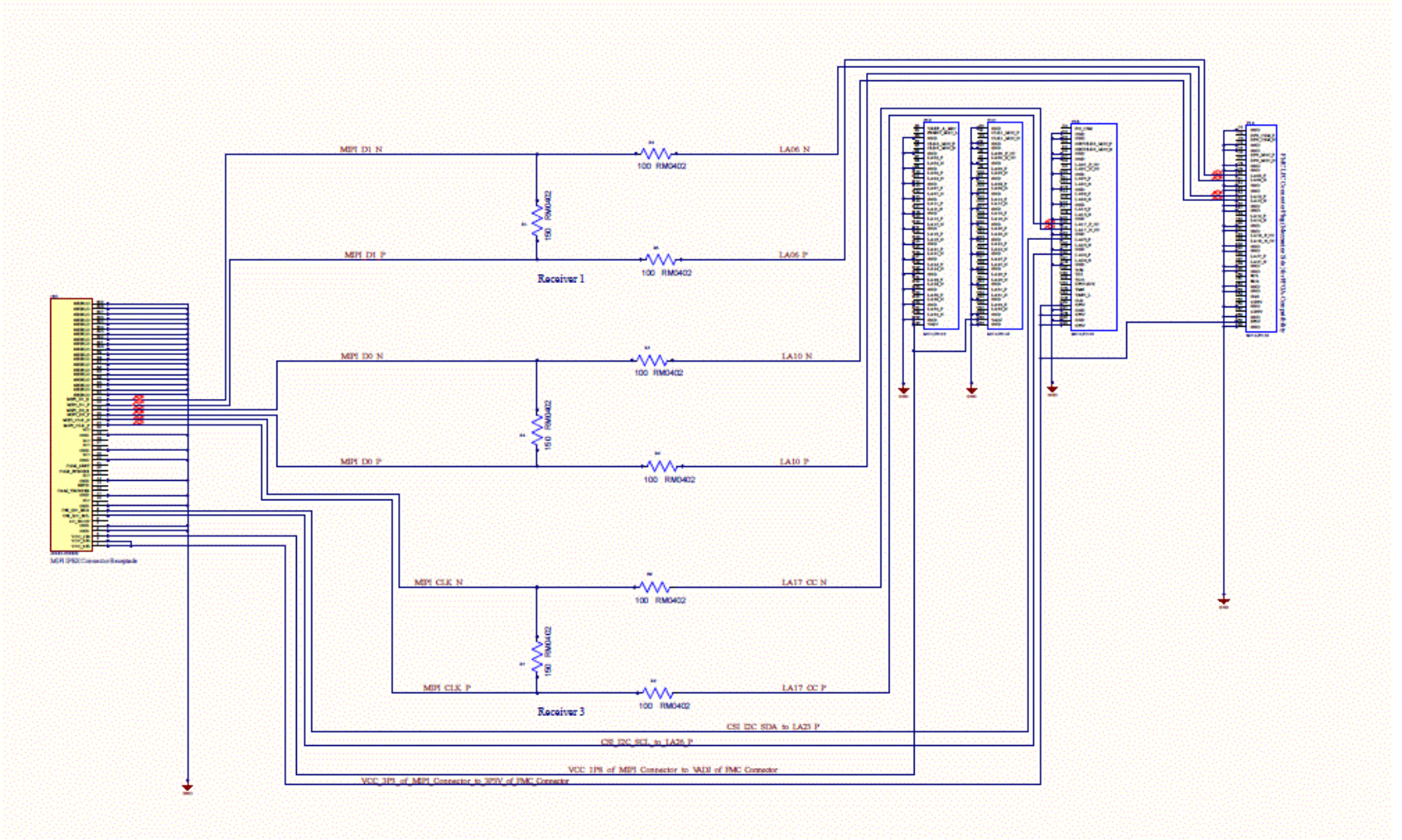


1 Receiver Network with verified resistor values

The MIPI IPEX Connector requires spatial reconfiguration during iterative design process. Its I/O pins are rearranged to meet trace routing requirements.

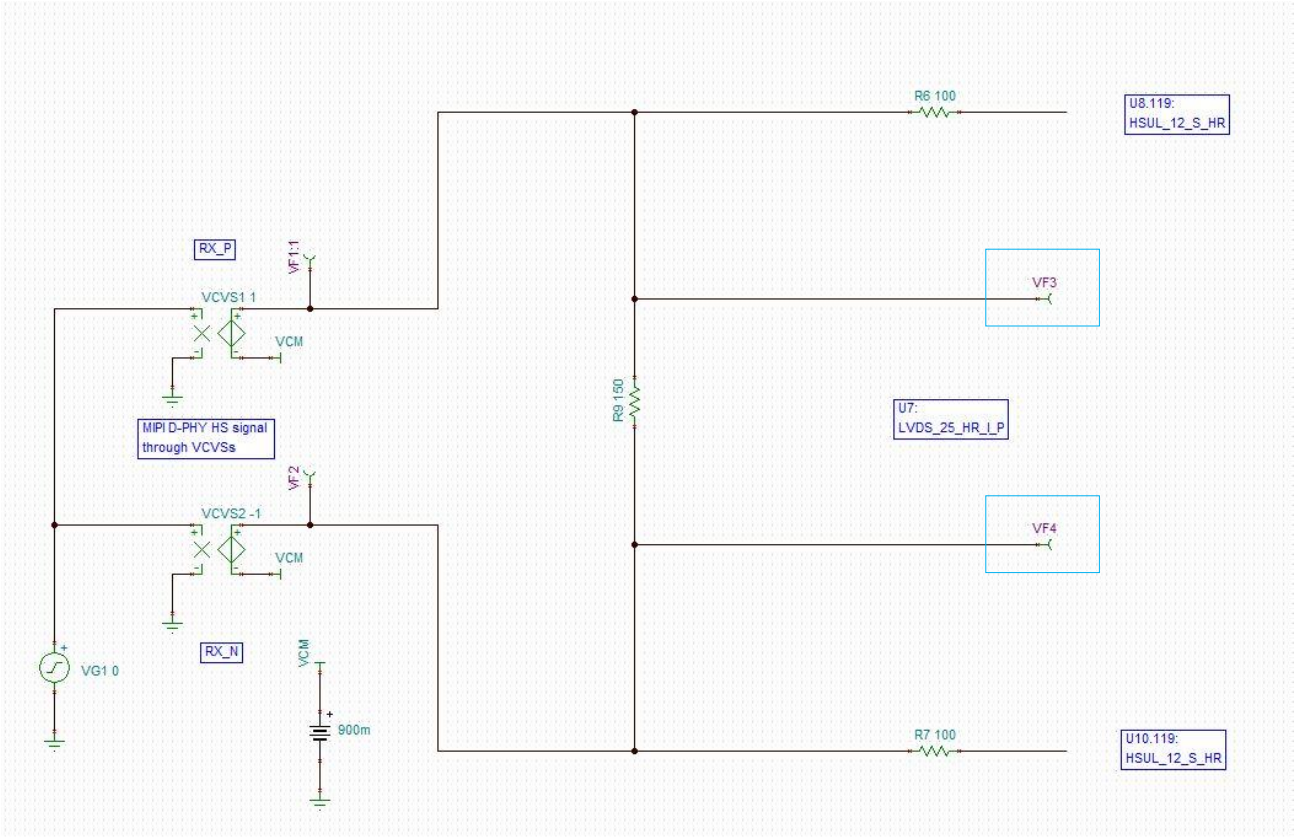


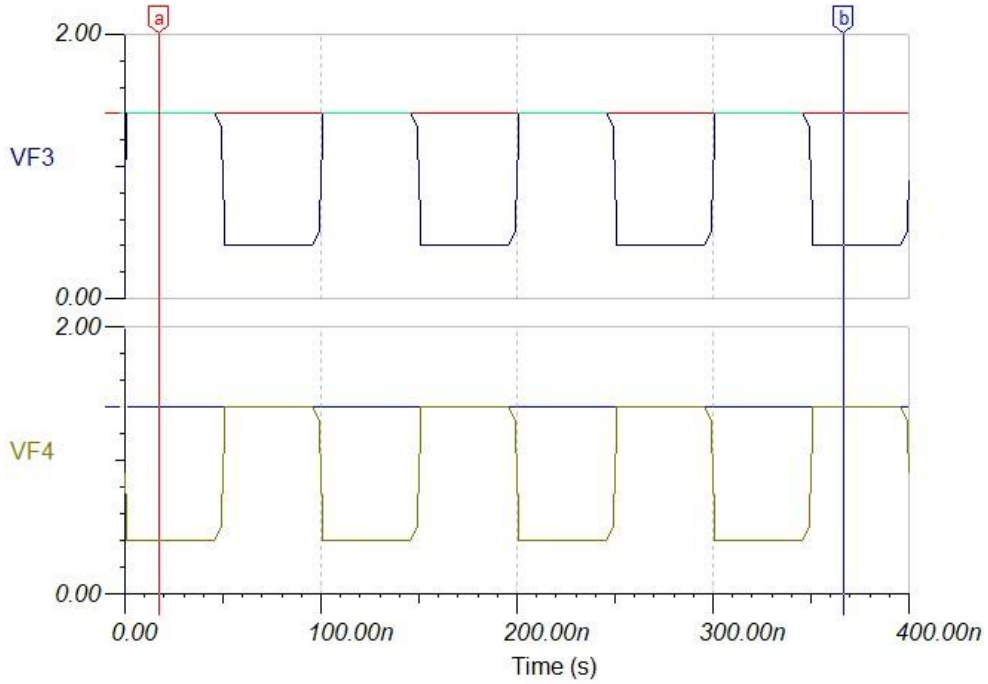
Final Circuit Schematic in Altium

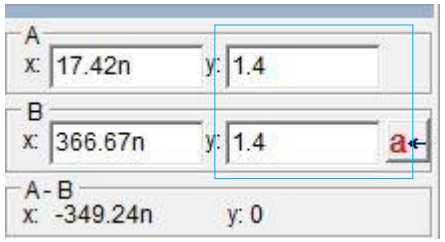


FPGA-Compatible MIPI CSI-2 D-PHY Adapter Board Circuit Schematic

Using the TI-TINA Simulation's Receiver Voltage Probe Results for verification of the 150 Ω resistor package type







Calculations of current and allowable dissipated power for verification of the 150 Ω resistor package type

(Using *NEP: Power Dissipation Ratings for Resistors (after 2007)*):

MIL-PRF-55342 Slash Sheet	Chip Size	Old Ratings (Before Oct. 2007)			New Ratings (After Oct. 2007)	
		Power (mW)		Volt	Power (mW)	Volt
		Thick Film	Thin Film		Thin & Thick Film	Thin & Thick Film
13	0302	40	40	15	40	15
11	0402	40	40	25	50	25
1	0502	20	10	40	50	40
2	0505	50	25	40	125	40
12	0603	70	70	50	100	50
6	0705	100	50	50	150	50
3	1005	100	50	40	200	75
10	1010 (FR4)	400	250	75	500	75
	1010 (Ceramic)	500	250			
7	1206	250	125	100	250	100
4	1505	150	100	40	150	125
8	2010 (FR4)	600	400	150	800	150
	2010 (Ceramic)	800	400			
5	2208	225	200	40	225	175
9	2512 (FR4)	750	500	200	1000	200
	2512 (Ceramic)	1000	500			

On calculating for the appropriate power rating for the **150Ω** resistor:

From the circuit simulation, V = **1.4 V.**

V = IR
1.4 V = (I)(**150 Ω**)
1.4 V/**(150 Ω)** = **0.00933 A** = I

$P_{dissipated} = I^2R$

$P_{dissipated}$ = (**0.0093333333** A)^2(**150 Ω**)

$P_{dissipated}$ = (0.00008711111111)(150) = **0.0130666667 W**

or simply from P = V^2/R = (1.4)^2/(150) = 1.96/150 = **0.0130666667 W**

If the **calculated dissipated power** does not exceed the power rating of the resistor for a particular package type, then there is no resistor degradation. Since **0.0130666667 W** does not exceed the **0402 package type power rating** of **50 mW** (or 0.05 W), the **0402 package type** is sufficient to use.

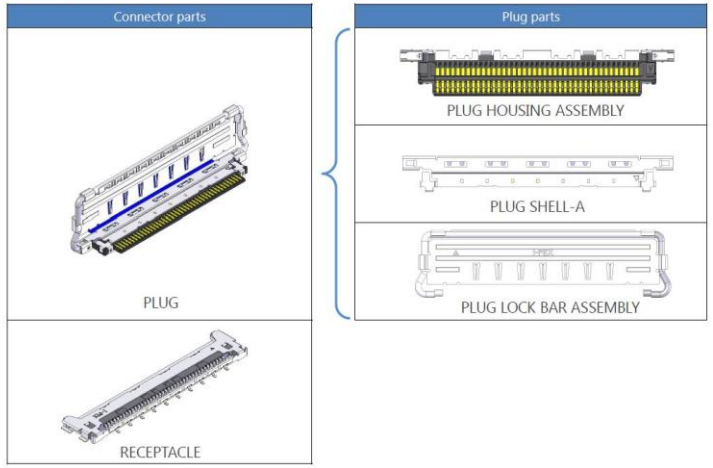
The power rating specifies the maximum steady state power the package allows to dissipate under given conditions (at the rated ambient temperature).

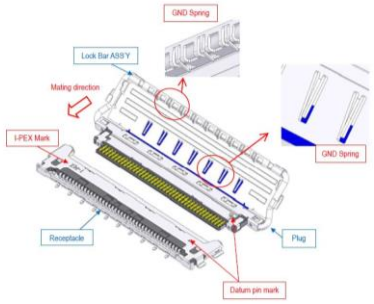
The **voltage rating** is typically for the resistor series and specifies the **maximum peak voltage** that can be continuously applied to a resistor at a rated ambient temperature without resistor degradation.

MIPI I-PEX Connector Receptacle

for high-speed signal transmission between the co-axial camera cable and a circuit board

Component Parts:



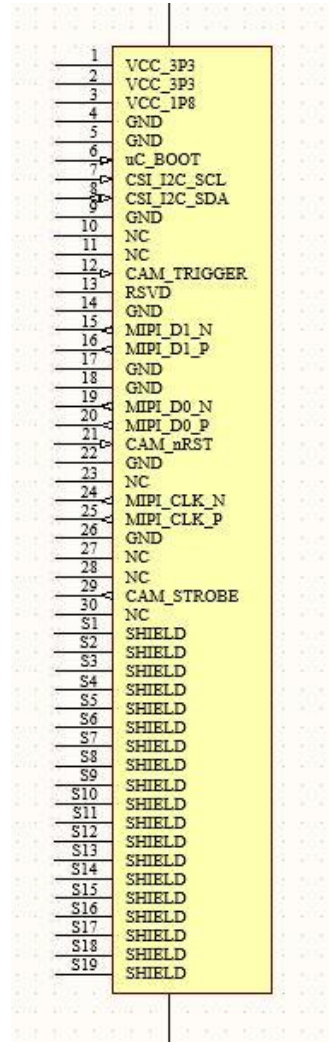


5 Pin Description

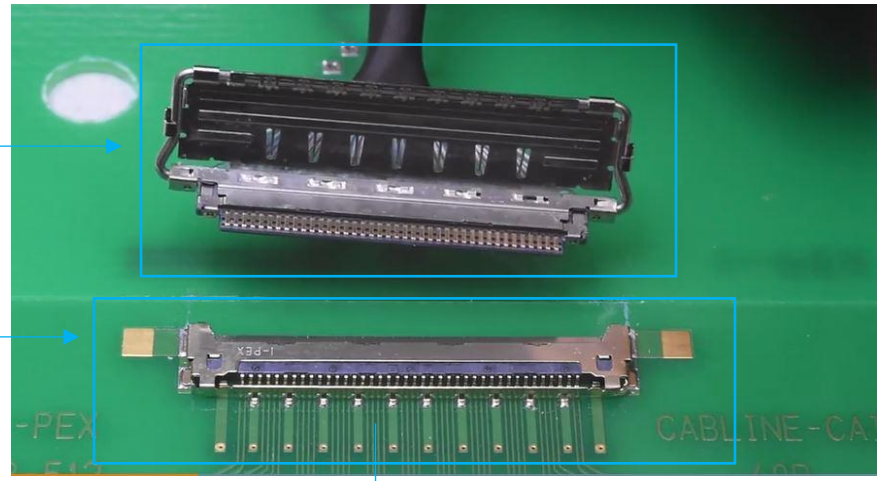
e-CAM222_CUMI2311_MOD has a I-PEX connector (CN1). The pin types are described from sensor perspective. The signal names and pin numbers are given below.

CN1 Pin No	Signal Name	Pin Type	Description
1	VCC_3P3	POWER	3.3V Power supply for camera and adaptor boards
2	VCC_3P3	POWER	3.3V Power supply for camera and adaptor boards
3	VCC_1P8	POWER	1.8V Power supply for camera and adaptor boards
4	GND	POWER	Ground signal for digital and analog
5	GND	POWER	Ground signal for digital and analog
6	uC_BOOT	INPUT	Camera Power down signal
7	CSI_I2C_SCL	INPUT	I2C Clock signal 1.8V I/O. Internal Pull ups are disabled
8	CSI_I2C_SDA	I/O	I2C Data Signal 1.8V I/O. Internal Pull ups are disabled
9	GND	POWER	Ground signal for digital and analog
10	NC	-	NC
11	NC	-	NC
12	CAM_TRIGGER	INPUT	Camera trigger signal 1.8V I/O. Internal PD to 1MΩ
13	RSVD	-	Reserved
14	GND	POWER	Ground signal for digital and analog
15	MIPI_D1_N	OUTPUT	MIPI Data Lane 1 Differential Pair -
16	MIPI_D1_P	OUTPUT	MIPI Data Lane 1 Differential Pair +
17	GND	POWER	Ground signal for digital and analog
18	GND	POWER	Ground signal for digital and analog
19	MIPI_D0_N	OUTPUT	MIPI Data Lane 0 Differential Pair -
20	MIPI_D0_P	OUTPUT	MIPI Data Lane 0 Differential Pair +
21	CAM_nRST	INPUT	Camera reset signal (Active low) 1.8V I/O
22	GND	POWER	Ground signal for digital and analog
23	NC	-	NC
24	MIPI_CLK_N	OUTPUT	MIPI Clock Lane Differential Pair -
25	MIPI_CLK_P	OUTPUT	MIPI Clock Lane Differential Pair +
26	GND	POWER	Ground signal for digital and analog
27	NC	-	NC
28	NC	-	NC
29	CAM_STROBE	OUTPUT	Camera Strobe signal 1.8V I/O
30	NC	-	NC

Table 3: CN1 Pin Descriptions



Schematic Symbol built to represent the MIPI IPEX Connector Receptacle (in Altium)



MIPI I-PEX Connector Receptacle (CN1 on the e-CAM222_CUMI2311_MOD module) Specifications

- **Description:** CONN Micro Coaxial CABLINE-CA II P-0.40mm 30Pos with Shield Cover Right Angle SMT
- **Manufacturer:** I-PEX
- **Part Number:** 20682-030E-02
- **Part Name**: Receptacle, 30 pins

CABLINE®-CA II

Fully-shielded with mechanical lock, high-data-rate transfer (20+ Gbps/lane), 0.4 mm pitch, horizontal mating type micro-coaxial connector

Building the MIPI I-PEX Connector Receptacle

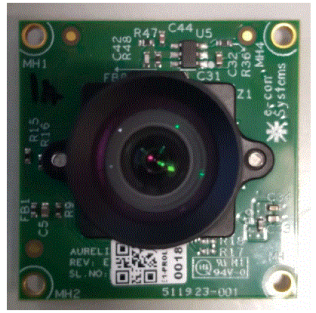


Figure 1: Front View of e-CAM222_CUMI2311_MOD Camera Module

Figure 2: Rear View of e-CAM222_CUMI2311_MOD Camera Module

Part Number: 20682-030E-02
Part Name: Receptacle, 30 pins

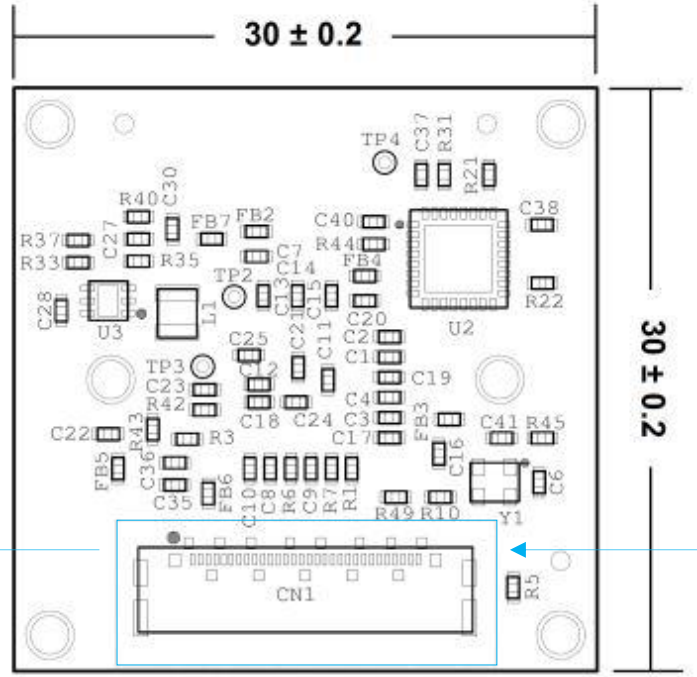


Figure 5: Bottom View of e-CAM222_CUMI2311_MOD

Building a corresponding Altium PCB footprint for the MIPI I-PEX Connector Receptacle (CN1 on the e-CAM222_CUMI2311_MOD module) to be added to NASA's "SC-Connector-Mech.PcbLib" in Altium:

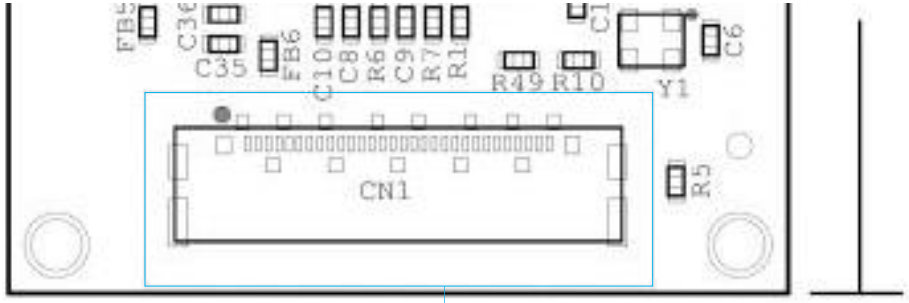
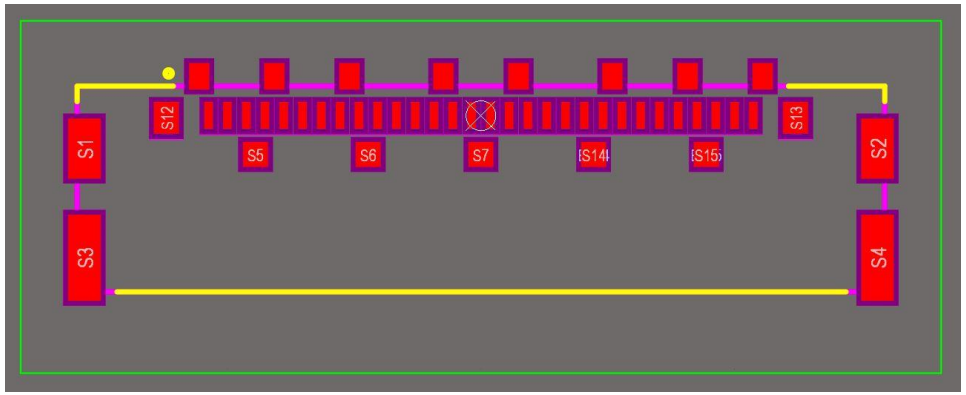


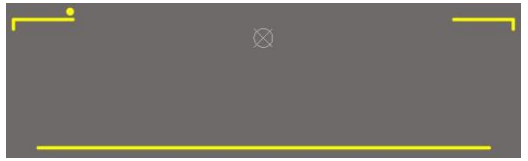
Figure 5: Bottom View of e-CAM222_CUMI2311_MOD



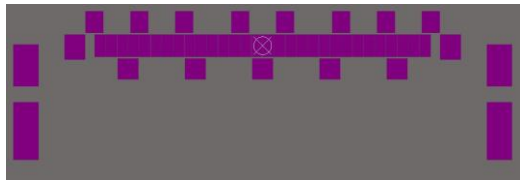
PCB footprint of IPEX MIPI Connector Receptacle built and linked to its schematic symbol (in Altium)

Top and Mechanical Layers

Top Overlay: silkscreen overlay

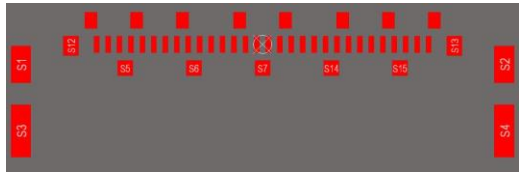


Top Solder: exposed surface mount pads; needs to be coated with solder paste before welding.

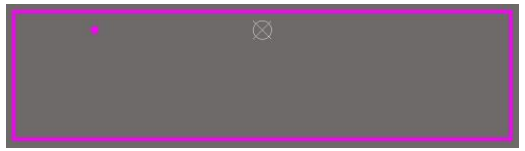


Top Paste:

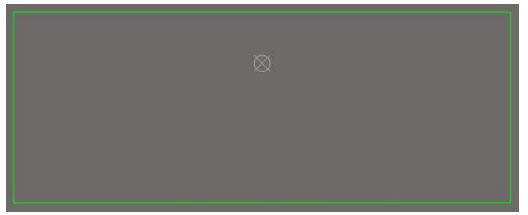
Top Layer: (*Signal Layer*); component layer, is mainly used to place components (electrical connections, aka the actual copper layers)



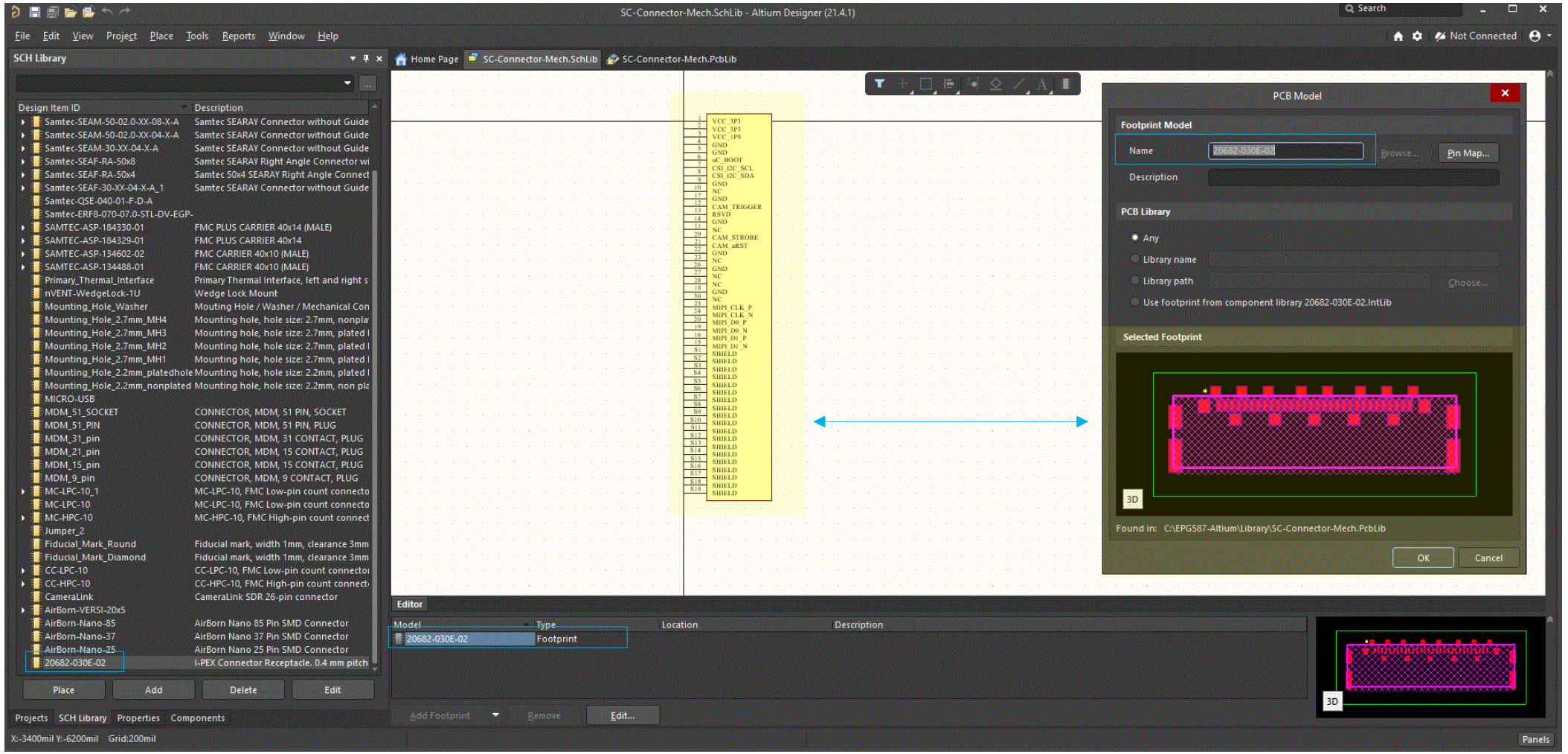
Mechanical 1:



Mechanical 2:



Linking the schematic symbol to the PCB footprint and 3D model between NASA's "SC-Connector-Mech.SchLib" and "SC-Connector-Mech.PcbLib" in Altium:



Building the FMC Connector Plug

for high-speed signal transmission between the PCB and FPGA

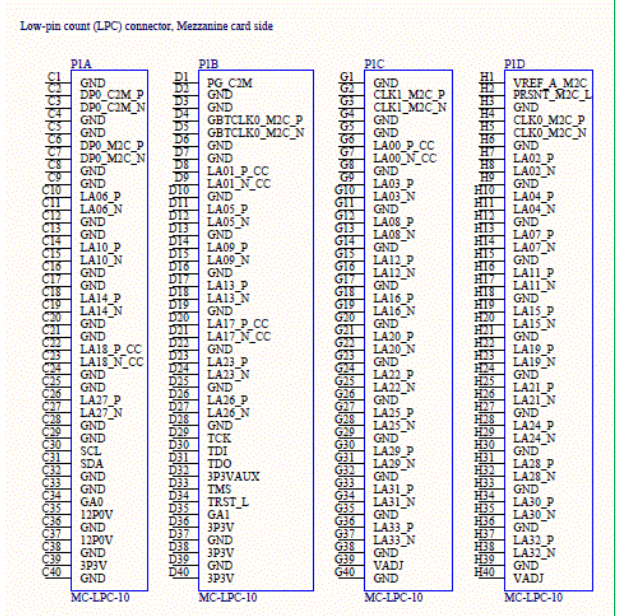
FMC Connector Plug (LPC; Low-Pin Count) Variant
(Mezzanine Card; PCB Side)
MC-LPC-10, Part A, FMC Low-pin count connector, lead free, 160 I/O pins, male, 10 mm mated stack height. **ASP-134604-01.**

The schematic symbol requires all 160 pins for proper representation.

G	F	E	D	C
GND			PG_C2M	GND
CLK1_M2C_P			GND	DP0_C2M_P
CLK1_M2C_N			GND	DP0_C2M_N
GND			GBTCLK0_M2C_P	GND
GND			GBTCLK0_M2C_N	GND
LA00_P_CC			GND	DP0_M2C_P
LA00_N_CC			GND	DP0_M2C_N
GND			LA01_P_CC	GND
LA03_P			LA01_N_CC	GND
LA03_N			GND	LA06_P
GND			LA05_P	LA06_N
LA08_P			LA05_N	GND
LA08_N			GND	GND
GND			LA09_P	LA10_P
LA12_P			LA09_N	LA10_N
LA12_N			GND	GND
GND			LA13_P	GND
LA16_P			LA13_N	LA14_P
LA16_N			GND	LA14_N
GND			LA17_P_CC	GND
LA20_P			LA17_N_CC	GND
LA20_N			GND	LA18_P_CC
GND			LA23_P	LA18_N_CC
LA22_P			LA23_N	GND
LA22_N			GND	GND
GND			LA26_P	LA27_P
LA25_P			LA26_N	LA27_N
LA25_N			GND	GND
GND			TCK	GND
LA29_P			TDI	SCL
LA29_N			TDO	SDA
GND			3P3VAUX	GND
LA31_P			TMS	GND
LA31_N			TRST_L	GA0
GND			GA1	12P0V
LA33_P			3P3V	GND
LA33_N			GND	12P0V
GND			3P3V	GND
VADJ			GND	3P3V
GND			3P3V	GND

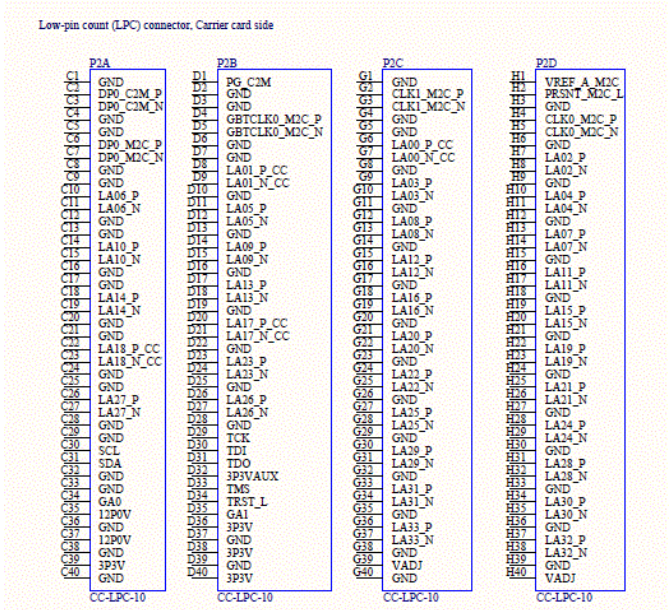
C1	GND	VADJ	H40
C2	DP0_C2M_P	GND	H39
C3	DP0_C2M_N	LA32_N	H38
C4	GND	LA32_P	H37
C5	GND	GND	H36
C6	DP0_M2C_P	LA30_N	H35
C7	DP0_M2C_N	LA30_P	H34
C8	GND	GND	H33
C9	GND	LA28_N	H32
C10	LA06_P	LA28_P	H31
C11	LA06_N	GND	H30
C12	GND	LA24_N	H29
C13	GND	LA24_P	H28
C14	LA10_P	GND	H27
C15	LA10_N	LA21_N	H26
C16	GND	LA21_P	H25
C17	GND	GND	H24
C18	LA14_P	LA19_N	H23
C19	LA14_N	LA19_P	H22
C20	GND	GND	H21
C21	GND	LA15_N	H20
C22	LA18_P_CC	LA15_P	H19
C23	LA18_N_CC	GND	H18
C24	GND	LA11_N	H17
C25	GND	LA11_P	H16
C26	LA27_P	GND	H15
C27	LA27_N	LA07_N	H14
C28	GND	LA07_P	H13
C29	GND	GND	H12
C30	SCL	LA04_N	H11
C31	SDA	LA04_P	H10
C32	GND	GND	H9
C33	GND	LA02_N	H8
C34	GA0	LA02_P	H7
C35	12P0V	GND	H6
C36	GND	CLK0_M2C_N	H5
C37	12P0V	CLK0_M2C_P	H4
C38	GND	GND	H3
C39	3P3V	PRSNT_M2C_L	H2
C40	GND	VREF_A_M2C	H1
D1	PG_C2M	GND	G40
D2	GND	VADJ	G39
D3	GND	GND	G38
D4	GBTCLK0_M2C_P	LA33_N	G37
D5	GBTCLK0_M2C_N	LA33_P	G36
D6	GND	GND	G35
D7	GND	LA31_N	G34
D8	LA01_P_CC	LA31_P	G33
D9	LA01_N_CC	GND	G32
D10	GND	LA29_N	G31
D11	LA05_P	LA29_P	G30
D12	LA05_N	GND	G29
D13	GND	LA25_N	G28
D14	LA09_P	LA25_P	G27
D15	LA09_N	GND	G26
D16	GND	LA22_N	G25
D17	LA13_P	LA22_P	G24
D18	LA13_N	GND	G23
D19	GND	LA20_N	G22
D20	LA17_P_CC	LA20_P	G21
D21	LA17_N_CC	GND	G20
D22	GND	LA16_N	G19
D23	LA23_P	LA16_P	G18
D24	LA23_N	GND	G17
D25	GND	LA12_N	G16
D26	LA26_P	LA12_P	G15
D27	LA26_N	GND	G14
D28	GND	LA08_N	G13
D29	TCK	LA08_P	G12
D30	TDI	GND	G11
D31	TDO	LA03_N	G10
D32	3P3VAUX	LA03_P	G9
D33	TMS	GND	G8
D34	TRST_L	LA00_N_CC	G7
D35	GA1	LA00_P_CC	G6
D36	3P3V	GND	G5
D37	GND	GND	G4
D38	3P3V	CLK1_M2C_N	G3
D39	GND	CLK1_M2C_P	G2
D40	3P3V	GND	G1

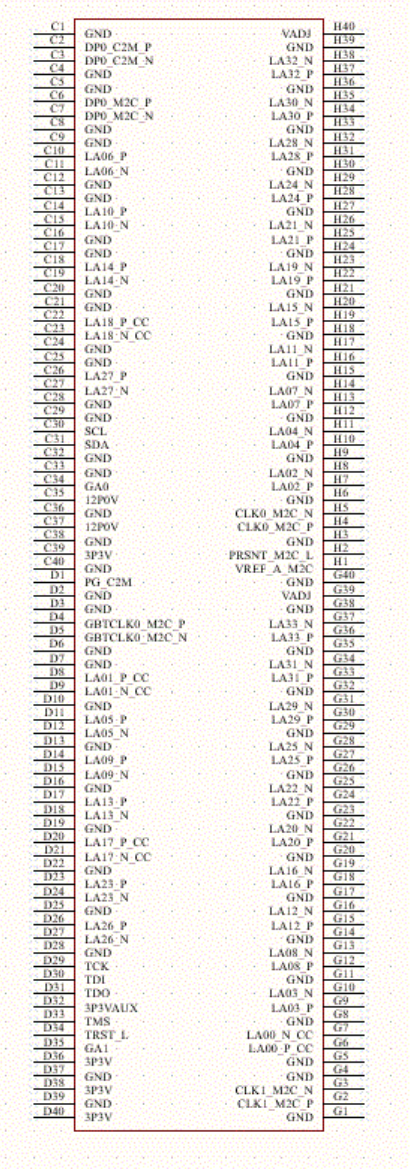
LPC FMC Connector Plug (Mezzanine Card; PCB Side):



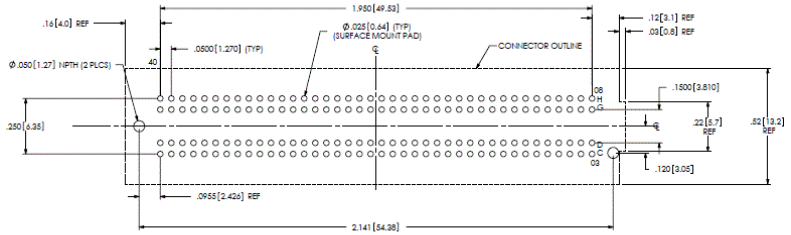
The plug and receptacle are expected to be compatible for signal and mechanical connectivity.

LPC FMC Connector Receptacle (Carrier Card; FPGA Side):

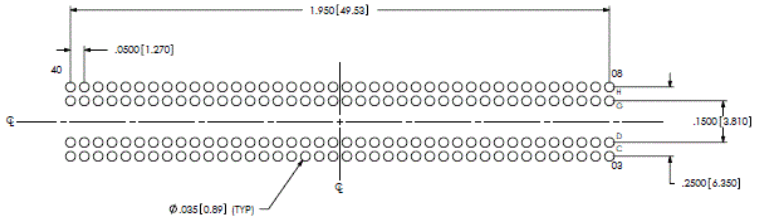




Schematic Symbol built to represent the Mezzanine FMC Connector Plug (in Altium)



RECOMMENDED PCB LAYOUT FOR ASP-134603-01
ALL DIMENSIONS SYMMETRIC ABOUT THE CENTERLINE



RECOMMENDED STENCIL LAYOUT FOR ASP-134603-01
ALL DIMENSIONS SYMMETRIC ABOUT THE CENTERLINE

VITA 57

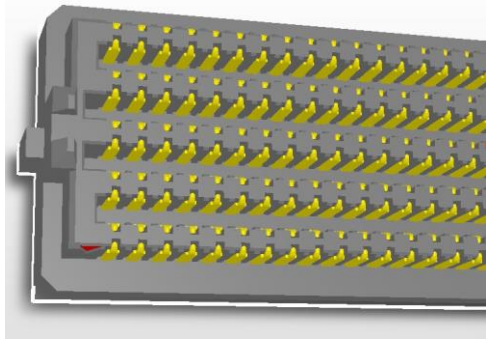
FPGA Mezzanine Card (FMC)

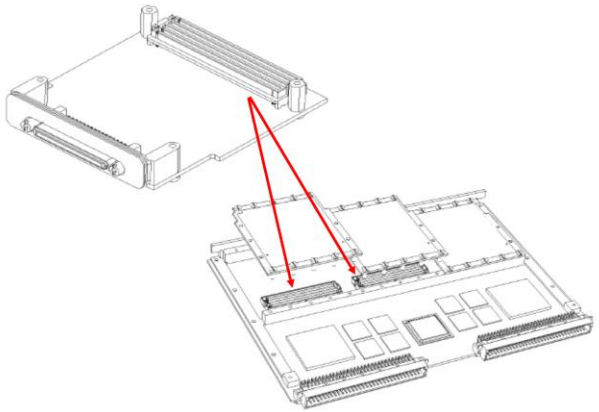
Plugs		
FMC Part No.	*Samtec Part No.*	*Molex Part No.*
MC-HPC-8.5L	ASP-134601-01	45970-4117
MC-HPC-8.5	ASP-134602-01	45970-4115
MC-HPC-10L	ASP-134487-01	45970-4317
MC-HPC-10	ASP-134488-01	45970-4315
MC-LPC-8.5L	ASP-134605-01	45970-4107
MC-LPC-8.5	ASP-134606-01	45970-4105
MC-LPC-10L	ASP-127797-01	45970-4307
MC-LPC-10	ASP-134604-01	45970-4305
Receptacles		
FMC Part No.	*Samtec Part No.*	*Molex Part No.*
CC-HPC-10L	ASP-134485-01	45971-4317
CC-HPC-10	ASP-134486-01	45971-4315
CC-LPC-10L	ASP-127796-01	45971-4307
CC-LPC-10	ASP-134603-01	45971-4305

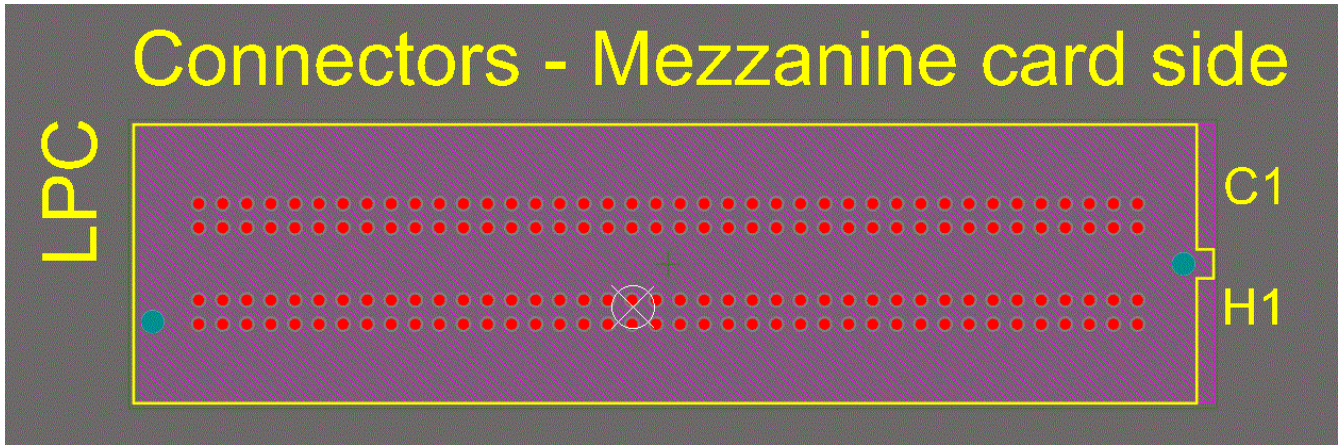
CC = Socket (Carrier Side) MC = Terminal (Module Side)

The Mezzanine Card side (PCB side) FMC Connector Plugs as LPC variant.
Selected for Adapter PCB: **ASP-134604-01.**

The Carrier Card side (FPGA side) FMC Connector Receptacles as LPC variant.

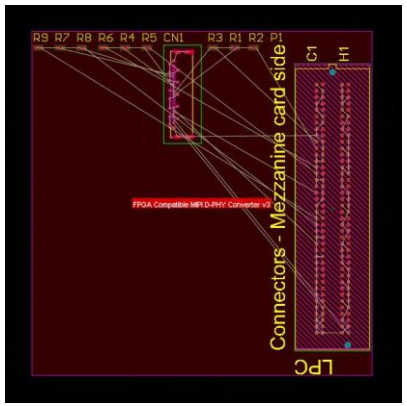


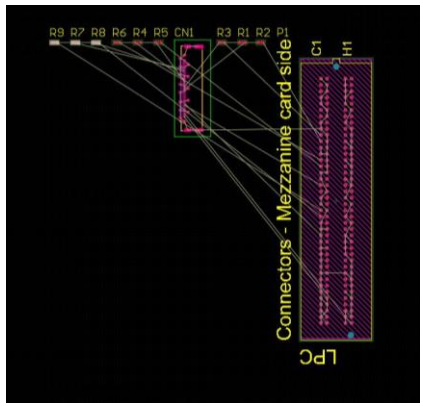


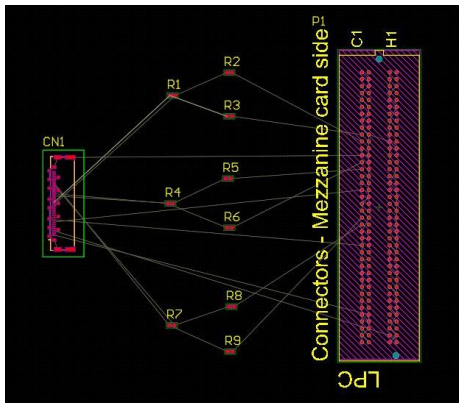


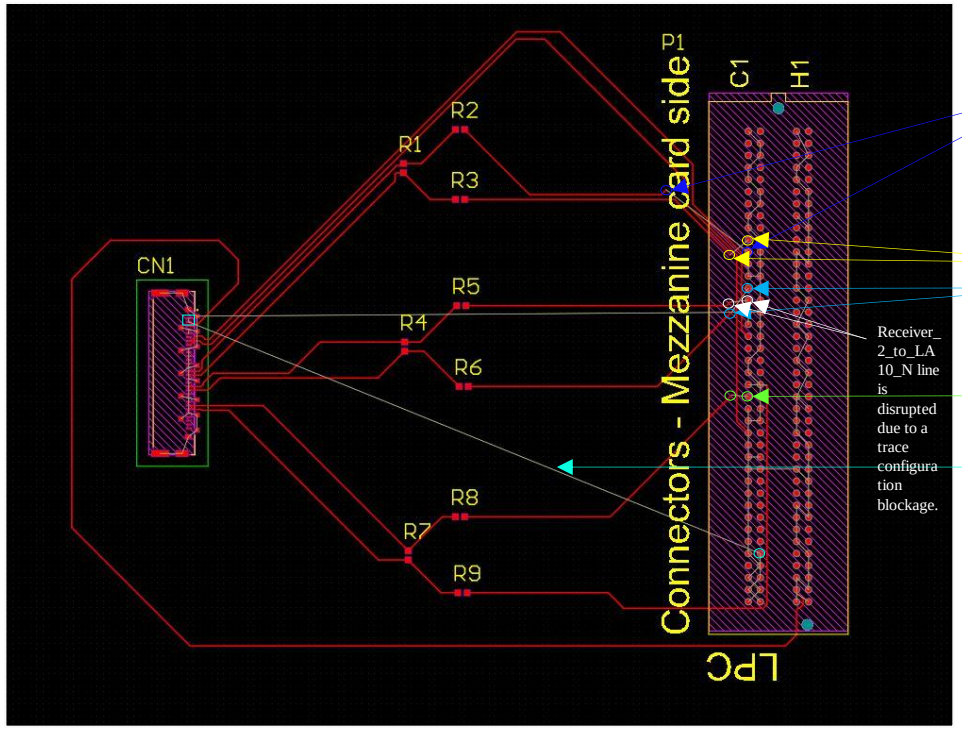
PCB footprint of FMC Connector Plug built and linked to its schematic symbol (in Altium)

Trace Routing Optimization from Default PCB Top Signal Layer









Receiver_1_to_LA06_N line is disrupted due to a trace configuration blockage.

Receiver_1_to_LA06_P line is disrupted due to a trace configuration blockage.

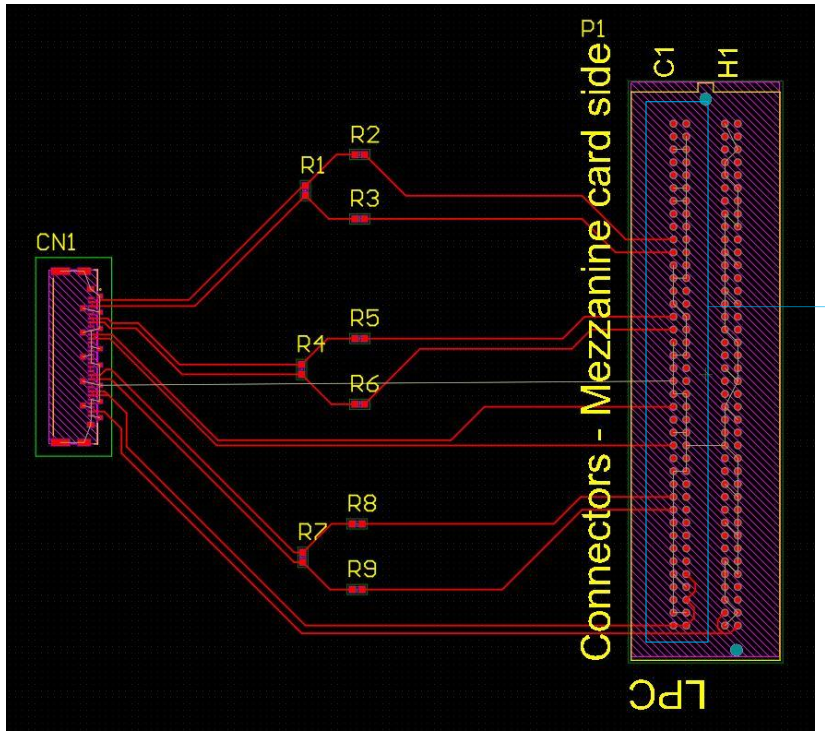
Receiver_2_to_LA10_P line is disrupted due to a trace configuration blockage.

Receiver_2_to_LA10_N line is disrupted due to a trace configuration blockage.

Receiver_3 to LA_17N_CC and LA_17P_CC: blocked.

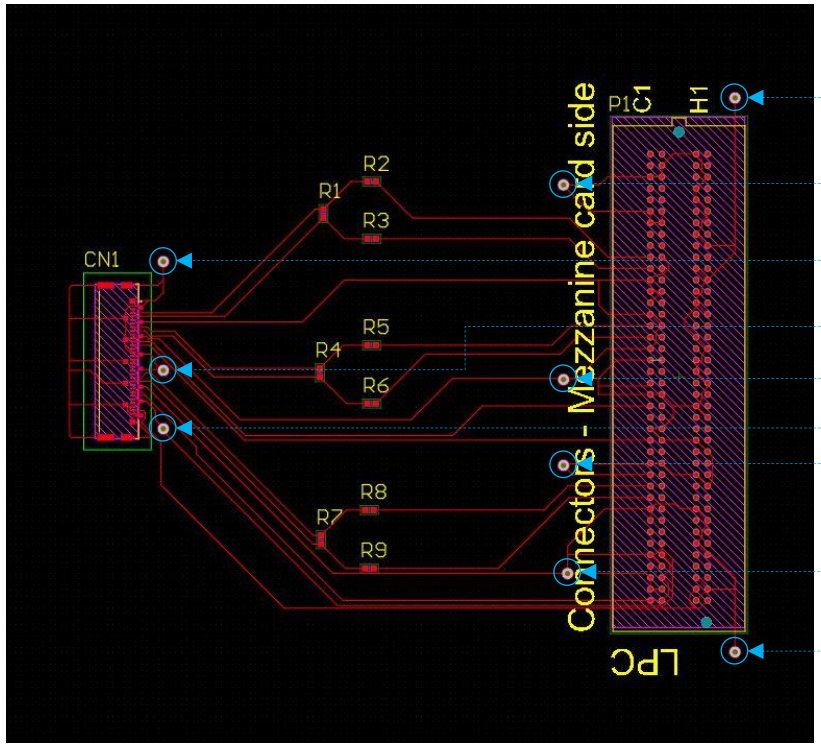
VCC_3P3_of_MIPI_Connector_to_3P3V_of_FMC_Connector line is disrupted due to problematic route crossing from other trace routes.

Optimization of Trace Routes and Via Placement



C18	D1
C26	D2
C1	D3
C2	D40
C3	D5
C4	D6
C5	D7
C6	D8
C7	D9
C11	D10
C10	D11
C8	D12
C9	D13
C12	D14
C13	D15
C15	D16
C14	D17
C16	D18
C17	D19
C19	C31
C20	C30
C21	D22
D23	C22
C23	D24
C24	D25
D26	C25
C27	D27
C28	D28
C29	D29
D21	D30
D20	D31
C32	D32
C33	D33
C34	D34
C35	D35
C36	D36
C37	D37
C38	D38
C40	D39
C39	D40

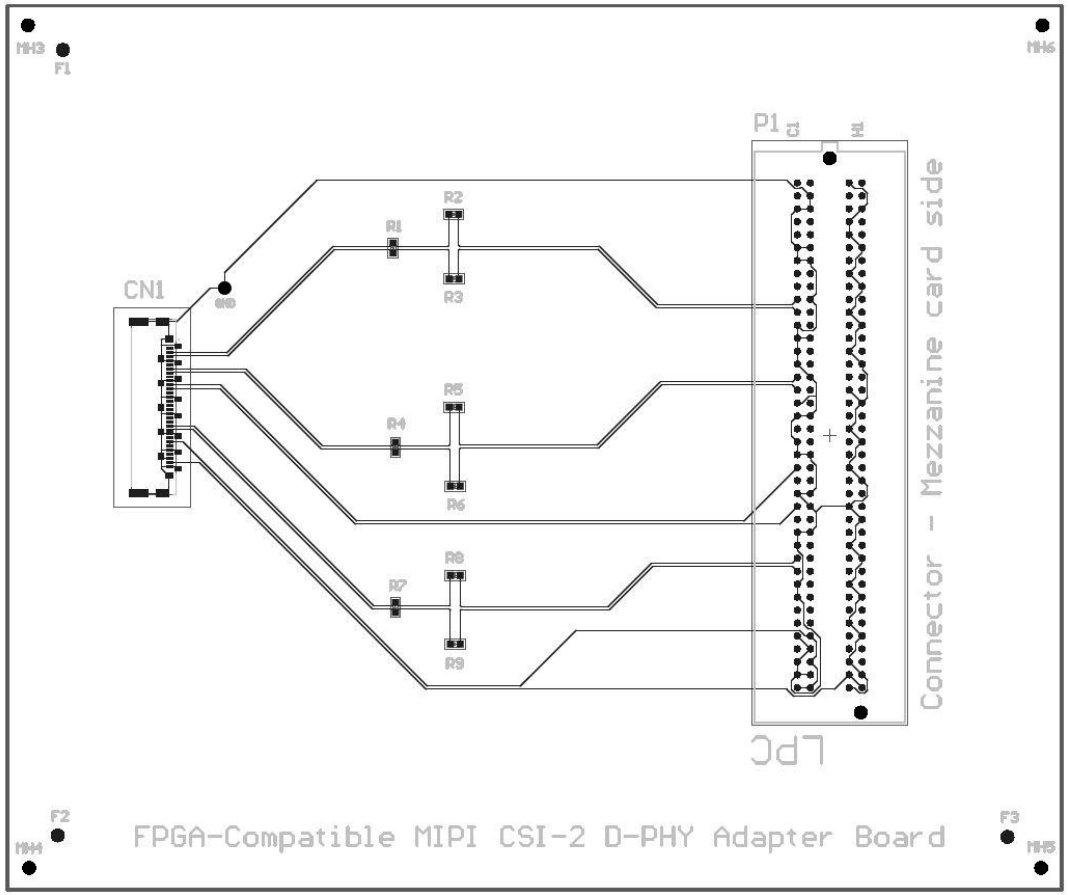
After pin swapping *within* and *between* the pin columns of the FMC Connector, the FMC Connector columns with pins routed to components and MIPI IPEX Connector pins have an alternative arrangement for the purpose of trace route optimization. The configuration still requires differential pair routing.



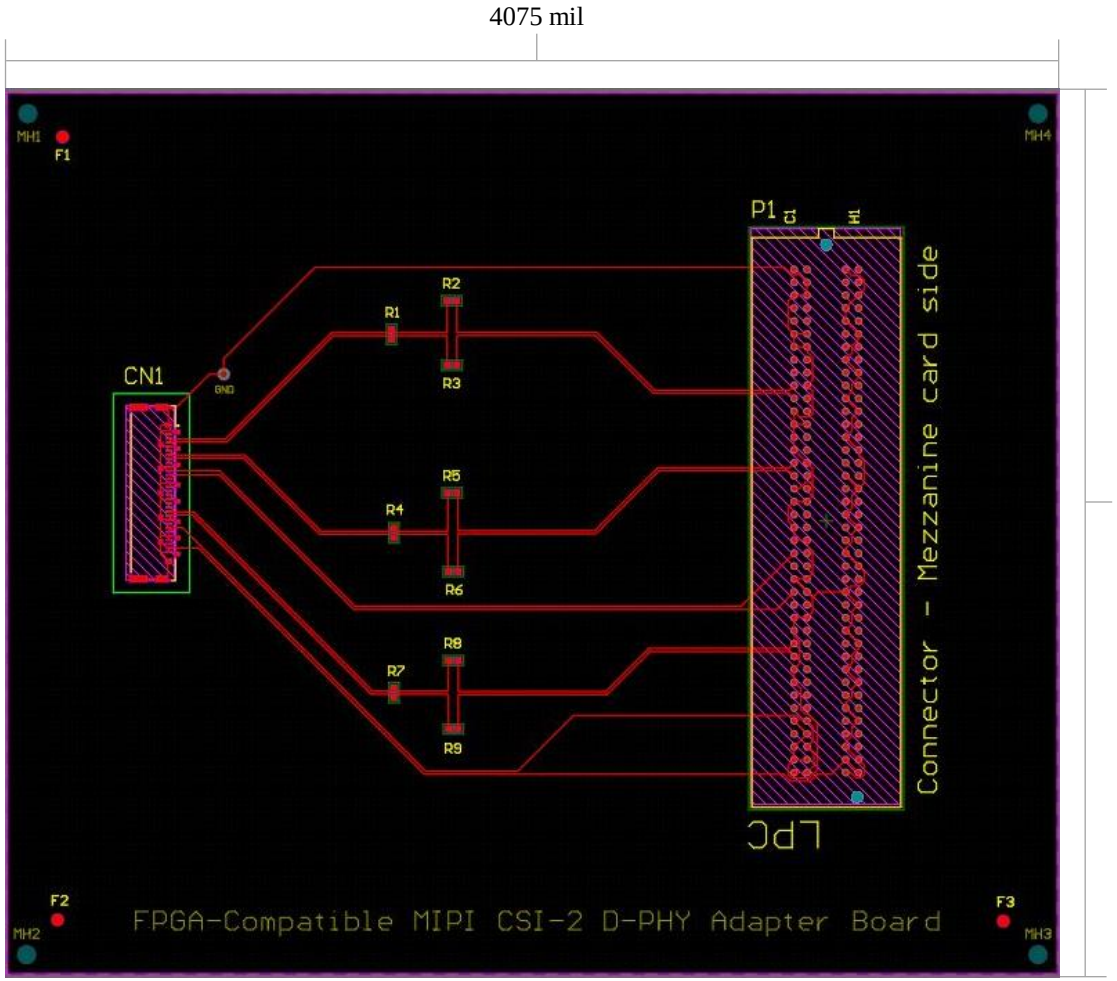
Vias

Via count minimization helps to reduce the number of trace routes on the board, ultimately reducing the amount of time spent on the board's signal connectivity.

Final PCB Configuration: FPGA-Compatible MIPI CSI-2 (Camera Serial Interface) D-PHY Adapter Board

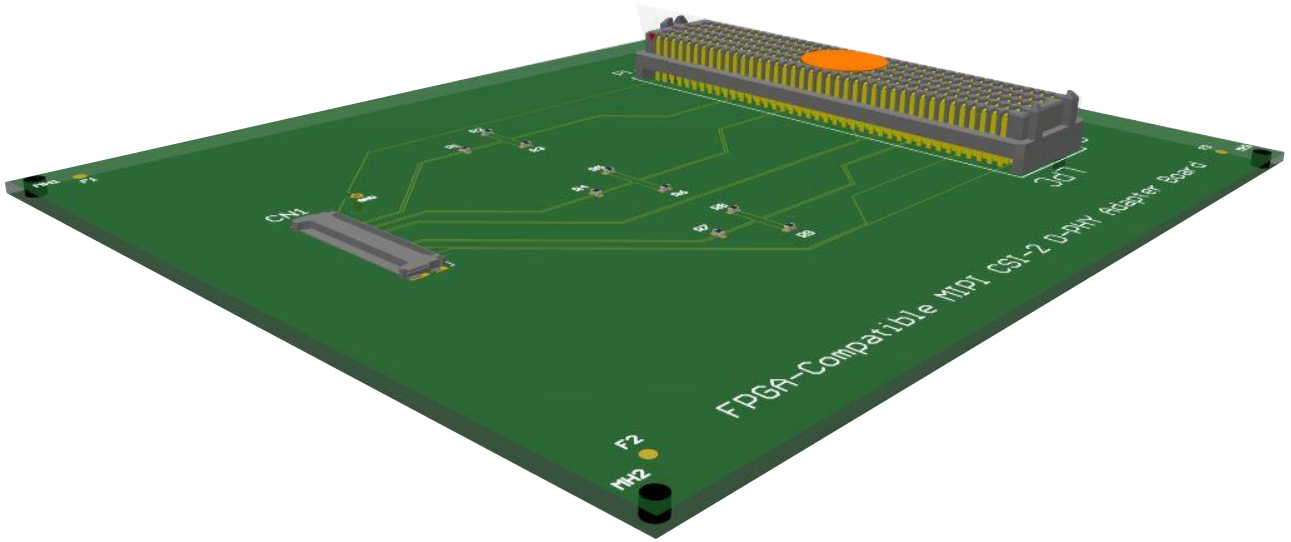


Final PCB Print (Assembly Drawing) of Adapter Board

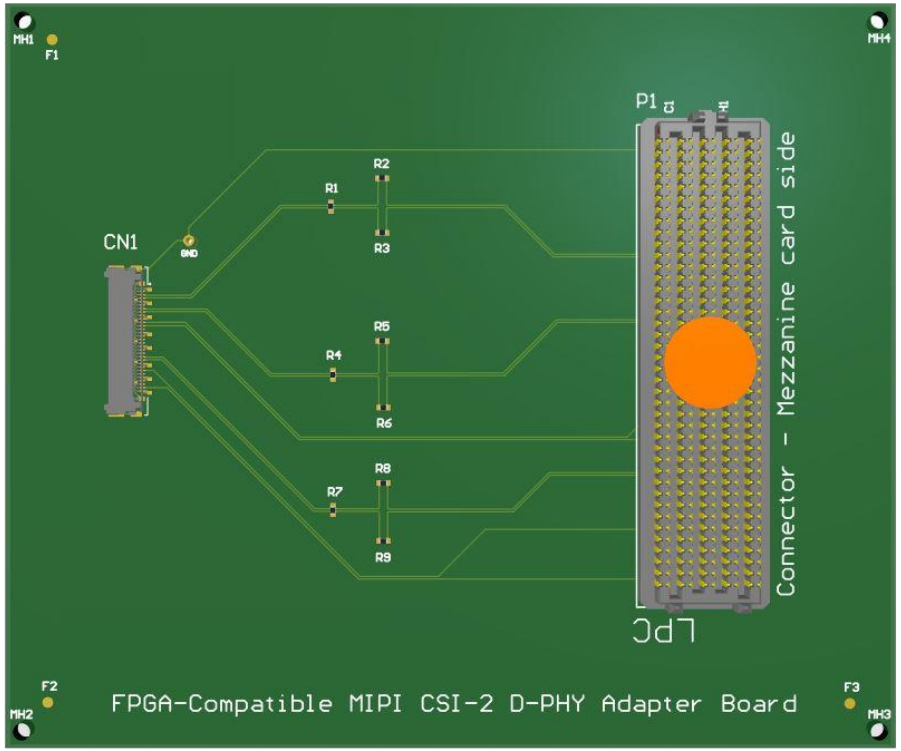


2D View of Final PCB layout of FPGA-Compatible MIPI CSI-2 D-PHY Adapter Board with both differential pairs and single routes

Final PCB Configuration in Altium's 3D View: FPGA-Compatible MIPI CSI-2 (Camera Serial Interface) D-PHY Adapter Board



Final PCB in Rotated View (XYZ Plane)



Final PCB in Top View

Once the adapter board PCB is fabricated and assembled, it can be used to demonstrate the validity of the circuit design prior to it being incorporated into the VADIR flight board design.

References and Acknowledgements

SpaceCube Publications:

[1] C. Wilson, Science Data Processing Branch, Software Engineering Division, NASA GSFC, "SpaceCube," 34th Annual Conference on Small Satellites, 2020, August.

[2] C. Wilson, Science Data Processing Branch, Software Engineering Division, NASA GSFC, "SpaceCube. A Family of Reconfigurable Hybrid On-Board Science Data Processors," Future In-Space Operations (FISO) Working Group Seminar, 2020, January.

[3] C. Brewer, N. Franconi, R. Ripley, A. Geist, T. Wise, S. Sabogal, G. Crum, S. Heyward, and C. Wilson, "NASA SpaceCube Intelligent Multi-Purpose System for Enabling Remote Sensing, Communication, and Navigation in Mission Architectures," 34th Annu. AIAA/USU Conf. on Small Satellites, SSC20-VI-07, Logan, UT, Aug. 1-6, 2020.

[4] A. Geist, C. Brewer, M. Davis, N. Franconi, S. Heyward, T. Wise G. Crum, D. Petrick, R. Ripley, C. Wilson, and T. Flatley, "SpaceCube v3.0 NASA Next-Generation High-Performance Processor for Science Applications," 33rd Annual AIAA/USU Conf. on Small Satellites, SSC19-XII-02, Logan, UT, August 3-8, 2019.

Additional Publications:

[1] MIPI Alliance, "MIPI Specification for D-PHY, Version 1.00.00," 2009, May.

[2] MIPI Alliance, "MIPI Specification for D-PHY, Version 1.2," 2014, September 10.

[3] M. Defossez, Xilinx, "D-PHY Solutions. XAPP894 (v1.0.1)," 1, February, 2021.

[4] B. Day, Xilinx, "Compact Camera Port 2 SubLVDS with 7 Series FPGAs High-Range I/O. XAPP582 (v1.0)," 2013, January 31.

[5] e-con Systems, "e-CAM222_CUMI2311_MOD Datasheet," Guindy, Chennai-600032, 10 February, 2021.

Manufacturer's Specifications:

[1] ANSI/VITA 57. 1-2008, ANSI/VITA 57 FMC - SIGNALS AND PINOUT (fmchub.github.io)

[2] OSHPARK Specifications, OSH Park Docs ~ Services ~ 2 Layer Prototype Service

[3] IPEX, https://www.i-pex.com/

Software Documentations:

[1] TI-TINA Simulation Tool Documentation, https://www.ti.com/tool/TINA-TI

[2] Texas Instruments, Editors: A. Kay, T. Green, "Analog Engineer's Pocket Reference," Addison, TX, 2020.

[3] Altium Designer Documentation, https://www.altium.com/documentation/altium-designer/

Acronyms

Acronym	Definition
MIPI	Mobile Industry Processor Interface
CSI	Camera Serial Interface
D-PHY	500 Mbps Physical Layer
FPGA	Field Programmable Gate Array
I/O	Input Output
FMC, LPC	FPGA Mezzanine Card, Low Pin Count
PCB	Printed Circuit Board
VADIR	VADIR (Versatile Analog/Digital Interface)
LVDS	Low-voltage differential signaling
HS	High Speed
HSUL	High-Speed Unterminated Logic
LP	Low Power
CS^2	CubeSat Card Standard

Thank you to:

Embedded Processing Group, Science Data Processing Branch, Code 587, NASA
Mentors: Alessandro Geist and Cody Brewer
GSFC OSTEM Internship Program
North Dakota Space Grant Consortium

Texas Instruments
Altium Designer


NASA


SpaceCube Hybrid Science Data Processor
FPGA
CPU
DSP
NASA GSFC