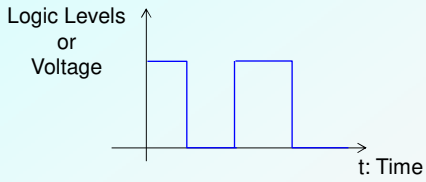
Timing Diagrams

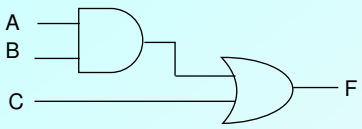
- Truth tables are not enough to illustrate some physical phenomena related to time in digital circuits (for example, delays). (Slide 7.3)

  In these cases, we need to use timing diagrams to describe the behavior of the circuit.
- Timing diagrams show various signals in the circuit (indicated as 0/1 or L/H on the vertical axis) as a function of time (on the horizontal axis).
- Several variables are usually plotted with the same time scale so that the times at which these variables change with respect to each other and the relationship between these variables can easily be observed.
- In more detailed timing diagrams, values of the outputs are written in terms of electrical voltage or current.

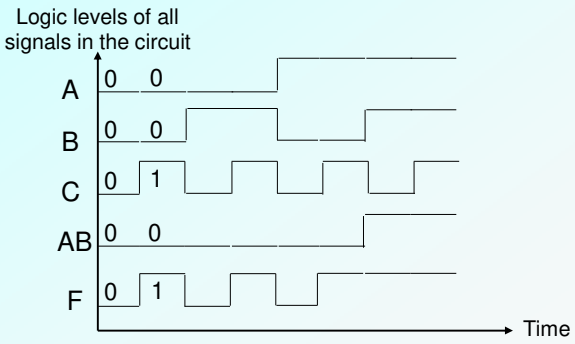


Timing Diagrams (cont'd)

Example:



In this diagram, we only show the logical behavior of the circuit and ignore time delays (described in the coming slides).



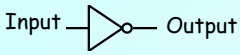
Propagation Delay

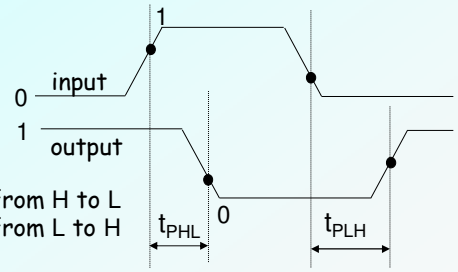
When the input to a logic gate is changed, the output will not change instantaneously.

The transistors and other switching elements within the gate take a finite time (a few nanoseconds) to react to a change in input so that the change in the gate output is delayed with respect to the input change.

The delay in the change in the output with respect to the input is called **propagation delay**.

Example: NOT Gate





t_{PHL}: delay of the transition from H to L
t_{PLH}: delay of the transition from L to H

The inputs of a circuit must be kept stable (constant) until it finishes its previous job. A new input value can be applied only after the previous input value has been processed.

The shorter the propagation delay, the higher the speed of the logic circuit.

We will cover this topic in Section 8 in detail.

Hazards caused by propagation delays

A digital circuit may malfunction due to timing problems.

Such timing problems, which arise due to delays are referred to as hazards.

If an input propagates through multiple paths to the output, unexpected output values (hazards) may appear at the output because these different paths may have different propagation delays.

Types of hazards:

a) Static 0: The output momentarily goes to 1 when it should stay at 0.
The output becomes 1 and goes back to 0 after a short time.
A static 0-hazard may occur in a product-of-sums implementation.

b) Static 1: The output momentarily goes to 0 when it should stay at 1.
The output becomes 0 (from 1) and goes back to 1 after a short time.
A static 1-hazard may occur in a sum-of-products implementation.

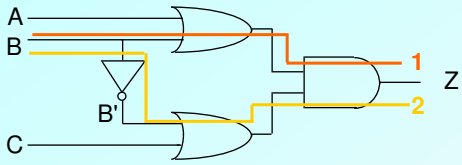
c) Dynamic: When the output is supposed to change from 0 to 1 (or 1 to 0), the output changes three or more times (i.e., oscillates).

Static 0 Static 1 Dynamic

Example: Static 0 Hazard

Z= (A+B)·(B'+C)

The circuit has a POS implementation.

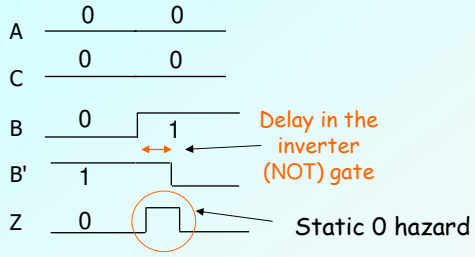


Input B has two different paths (shown with red and yellow lines) to the output Z.

When the inputs A, B, and C are all zero (A=0, B=0, C=0), the output will also be zero (Z=0).

In this state, if the value of input B is changed to 1, the output should not change its value (A=0, B=1, C=0 → **Z=0**).

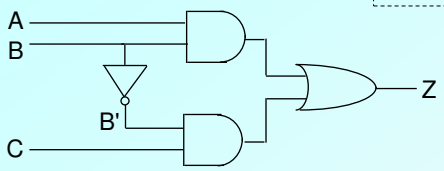
However, due to the different propagation delays in the paths from B to Z, a "short" change (hazard) appears at the output.



Example: Static 1 Hazard

Z= AB + B'C

The circuit has a SOP implementation.



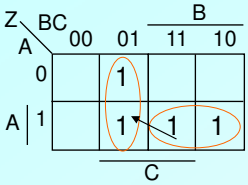
The circuit has output Z=1 when A=1, B=1, and C=1.

In this state, if B becomes 0 (1→0), the output should stay as Z=1.

However, **static 1 hazard** occurs at the output.

Avoiding hazards:

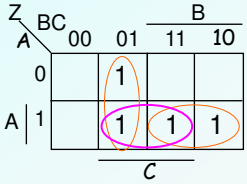
Possible hazards can be foreseen on a Karnaugh map.
Consider the circuit for Z= AB + B'C given on slide 7.6.



Z= AB + B'C

A change in B (1→0) causes a transition from one prime implicant to another. These types of transitions cause hazards because of delays.

To avoid hazards, the **consensus** of the prime implicants involved in the transition is added to the design. This increases the cost.



Z= AB + B'C + **AC**

In sections 8, 9, and 10, we will see how **the clock signal** is used to avoid timing problems that may arise due to delays.

BY NC ND