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MICROROC: MICRO-mesh gaseous structure Read-Out Chip

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ABSTRACT: MICRO MEsh GAseous Structure (MICROMEGAS) and Gas Electron Multipliers (GEM) detectors are two candidates for the active medium of a Digital Hadronic CALorimeter (DHCAL) as part of a high energy physics experiment at a future linear collider (ILC/CLIC). Physics requirements lead to a highly granular hadronic calorimeter with up to thirty million channels with probably only hit information (digital readout calorimeter).

To validate the concept of digital hadronic calorimetry with such small cell size, the construction and test of a cubic meter technological prototype, made of 40 planes of one square meter each, is necessary. This technological prototype would contain about 400 000 electronic channels, thus requiring the development of front-end ASIC. Based on the experience gained with previous ASIC that were mounted on detectors and tested in particle beams, a new ASIC called MICROROC has been developped. This paper summarizes the caracterisation campaign that was conducted on this new chip as well as its integration into a large area Micromegas chamber of one square meter.

KEYWORDS: Electronic detector readout concepts (gas, liquid); Analogue electronic circuits; CMOS readout of gaseous detectors; Front-end electronics for detector readout

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Contents

2012 JINST 7 C01029

1 MICROROC design

MICROROC is a 64 channels integrated circuit, made in AMS SiGe 0.35 µm technology. Its area is 20 mm^2. The digital part is the same as the HARDROC [1, 2] one, and the preamplifier is derived from the one of the DIRAC [3, 4] integrated circuit but with improved performance. Each channel consists in (figure 1):

- A spark protection network;
- A charge preamplifier;
- Two shapers (low gain and high gain);
- Three discriminators with a 2-bit encoder;
- A shared 127 event digital memory;
- A 24-bit bunch-crossing identifier counter @5 MHz (BCID).

The operation of MICROROC is optimized for the ILC beam structurew hich is divided into two main phases. During the first phase the beam is on (1 ms): for each channel, the detector signal is collected and the resulting voltage pulse amplitude is compared to three programmable thresholds. Every 200 ns, the result is latched and stored inside the digital memory if at least one channel

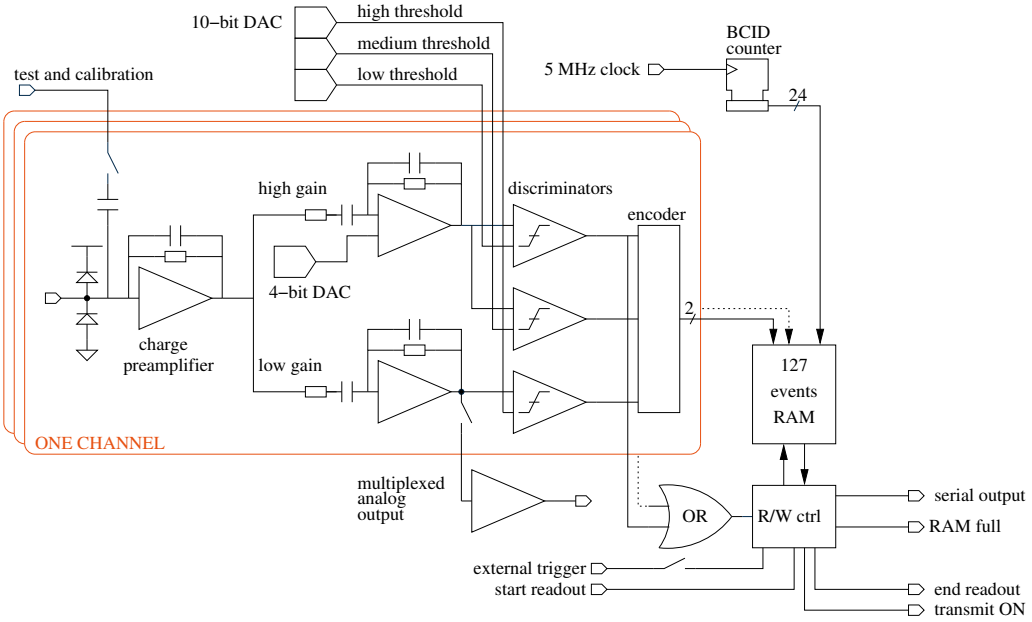


Figure 1. MICROROC architecture.

has a charge above the lowest threshold (auto-trigger mode), and associated with a 24 bit time stamp (BCID).

During the second phase (199 ms), i.e. between two bunch trains, the analog part is powered down, and a serial daisy-chained readout is performed. For test with cosmic or beam particles, an external trigger is available, as well as an analog multiplexed readout for detector fine characterization.

In order to reduce inter channels disparities, a 4-bit DAC per channel is included to tune the reference voltage of the high gain shaper and thus compensate its offset. This allows to have uniform low threshold for all channels of one chip.

In addition to the power-pulsing capability, the power consumption has been optimized for each stage, in order to minimize overall power dissipation. In particular, the trade-off between noise and power for preamplifier, and device matching and power for comparator has been carefully designed. The power consumptions are given table 1. The total current drawn for a chip is 68 mA, i.e. 3.7 mW@3.5 V per channel. After a power-down, a recovery time of 25 µs is needed to reach the nominal performances. Moreover, a 1% power pulsing ratio will be reachable at the ILC: the power consumption is therefore compliant with the 100 µW per channel foreseen dissipation limit.

2 Prototypes performances

The following characteristics have been established with the five prototypes of the MPW run:

- Dynamic range: 500 fC and 200 fC for low and high gain path respectively;
- Linear range: 350 fC and 90 fC for low and high gain path respectively (figure 2);
- Preamplifier gain of 2.38 mV/fC;

2012 JINST 7 C01029

Table 1. Summary of power consumption for each stage, under 3.5 V.

Stage	Number of stage	Stage Consumption (µA)	Total consumtion including bias (mA)
Preamplifier	64	850	54.7
Shapers	3×64	53	1.13
Discriminators	3×64	40	7.7
DAC	3	173	0.52
Bandgap	1	1200	1.2
Digital (FSM+RAM)	1	2400	2.4
Digital (Data tranmission)	1	400	0.4
Total			68

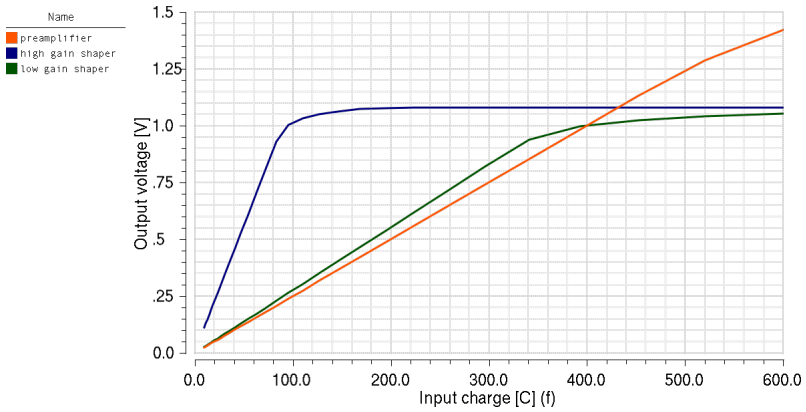


Figure 2. Linearity of preamplifier and shapers (simulation).

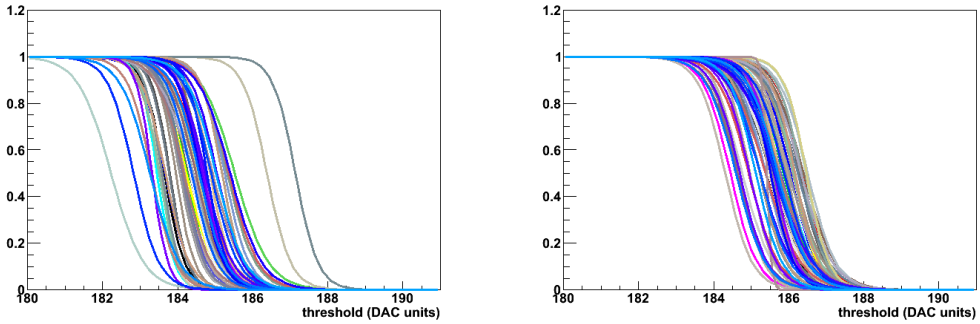
- Noise rms: 1 fC at preamplifier output, 0.24 fC with 200 ns shaping (C_{det}: 80 pF for 1 cm^2 anode);
- Peaking times: 75, 115, 150 and 200 ns (figure 4(a));
- 10-bit threshold DAC: linearity better than 3 DAC units (figure 4(b));
- 4-bit pedestal adjustment DAC: linearity better than 1 DAC unit;
- Cross-talk between adjacent channels lower than 1 %;
- Lowest threshold: about 1 fC.

All these measurements were in good agreement with simulation, except for the smallest peaking time (table 2). The discrepancy for the shortest shaping time has not yet been explained. Further simulations with extracted parasitics are under study. The threshold dispersion of the 64 channels of one chip is 5 DAC unit peak-to-peak. After the pedestal correction, the disparity is reduced to 2.5 DAC unit (figures 3(a) and 3(b)).

2012 JINST 7 C01029

Table 2. Summary of shaper peaking times and gains.

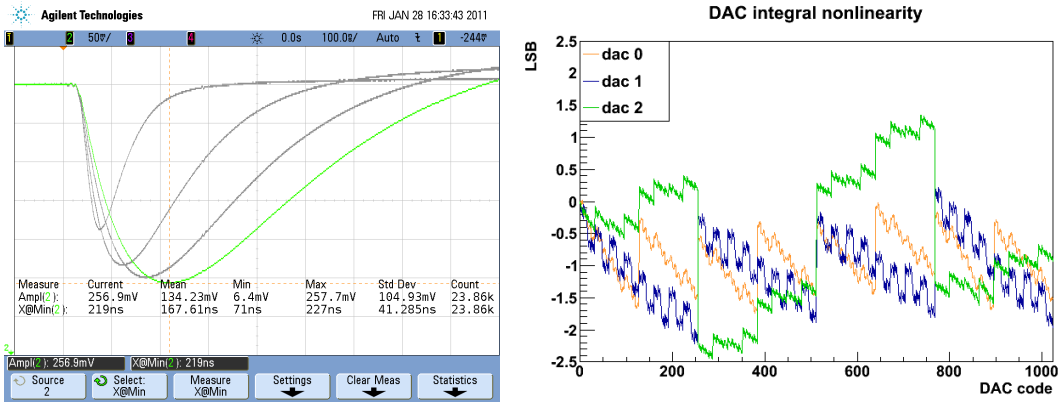
Setting	Measure		Simulation	
	Gain (mV/fC)	Tp (ns)	Gain (mV/fC)	Tp (ns)
00	7.6	76.3	10.5	30
01	9.7	114.2	11.0	100
10	9.8	157.4	11.1	150
11	10.2	192.3	11.2	200



(a) Before pedestal correction

(b) After pedestal correction

Figure 3. S-Curve spread (64 channels).



(a) High gain shaper Dirac impulse response

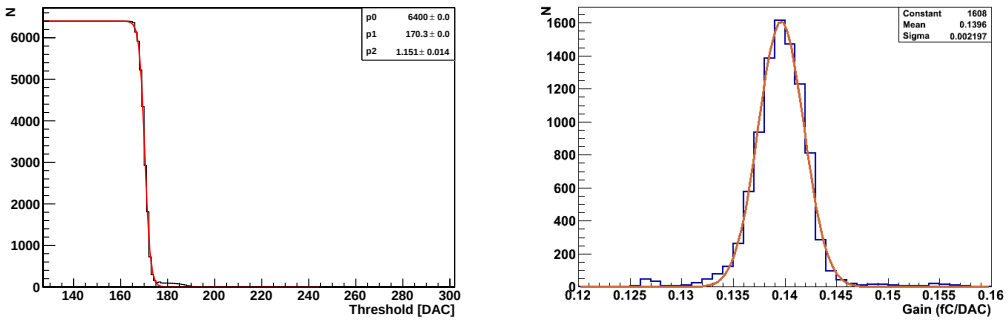
(b) Main DAC (threshold) integral non-linearity

Figure 4. Prototypes tests results.

3 Small production tests

After prototype characterization, 341 chips have been produced, packaged in TQFP160 and individually tested with a dedicated testboard and test socket. The testboard hosts a FPGA with the same firmware as the DIF board (see section 5) and is controlled with USB link by a PC and a Labview software. Input charge are generated with an Agilent pulse generator controlled with GPIB and an attenuator. The small production tests have consisted in:

2012 JINST 7 C01029



(a) Example of S-Curve with Fermi-Dirac fit

(b) Gain dispersion for 144 chip

Figure 5. Small production tests.

- Testing the digital interface of the chip, and its configuration registers;
- Testing the input bonding with external capacitors;
- Measuring the S-curve without injection, then extracting offline pedestal for each channel;
- Measuring the S-curve with 50 fC input signal, then extracting offline inflexion point;
- Plotting the gain for each channel and checking the value (must be within nominal $\pm$10%).

The S-curves have been reconstructed offline with a dedicated software framework based on ROOT, which is used also for the whole detector analysis (see section 6). All the different tests are automated with scripts, and the parameters of each channel of each chip are stored on disk for further use (see subsection 4.1).

A chip is identified as good if it has all its inputs working and gain deviation smaller than $\pm$10 % of the nominal gain (figure 5(b)). The test results are summarized below:

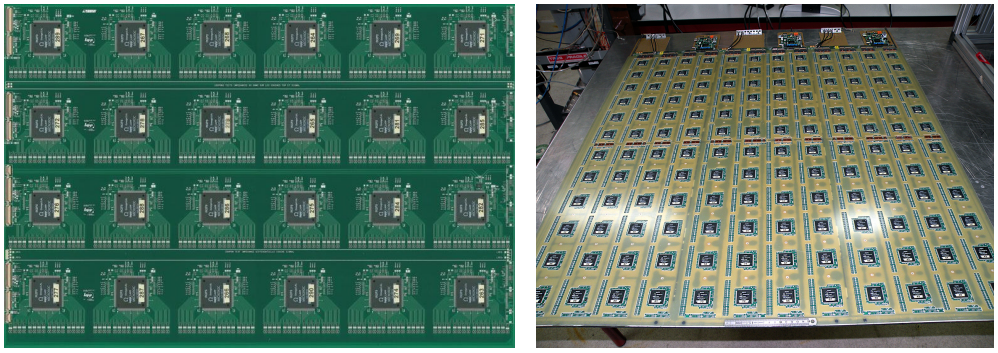
- 6 faulty chips (configuration errors);
- 11 with a packaging problem (bad bonding);
- 12 with bad gain (at least one channel);
- 2 to be retested (test socket problems);
- 312 good chips.

A yield of 91.5 % has been reached for this small production. 288 of these chips are cabled on 13 PCB of 32x4832$\times$48 cm^2, 12 of which are used to build 2 Micromegas chamber of 1 m^2. The last one is a spare used for laboratory tests, such as EMC improvement or firmware development.

4 MICROROC detector integration

To demonstrate the use of MICROROC for MICROMEGAS readout, a 1 m^2 chamber was built and equiped with MICROROC ASICs. The heart of the chamber is the printed circuit board, which hosts 24 ASIC on one side, and the MICROMEGAS bulk [5] on the other side.

2012 JINST 7 C01029



(a) ASU, components side (b) The square meter chamber during assembly

Figure 6. The MICROMEGAS chamber.

4.1 PCB design

The printed circuit board is a 8-layer PCB, with impedance controlled strips (50 Ω for calibration and 100 Ω for differential LVDS clocks), with 1.2 mm thickness. The anode pads are copper squares of 9.8×9.8 mm^2 with 1 cm pitch, and the PCB final dimension is 32×48 cm^2 (1536 pads), so that each PCB hosts 24 MICROROC circuits (figure 6(a)). There are two possible cabling, according to the place of the PCB inside the detector, i.e. without or with termination network for respectively first/middle and last PCB of a chain (see next subsection).

The ground plane below the anodes has been hatched to reduce detector capacitance, thus reducing noise. All via are blind or burried in order to ensure that the PCB is gas tight.

Each PCB is carefully tested (pedestal and charge injection for each channel) before and after each step of construction (mesh lamination, burn-in). Each PCB will be called Active Sensor Unit (ASU) once electronics components are soldered and bulk is laminated. When an ASU is ready, response of each anode is tested inside a gas-tight test chamber with an ^{55}Fe source. The ASU total thickness is less than 3.5 mm.

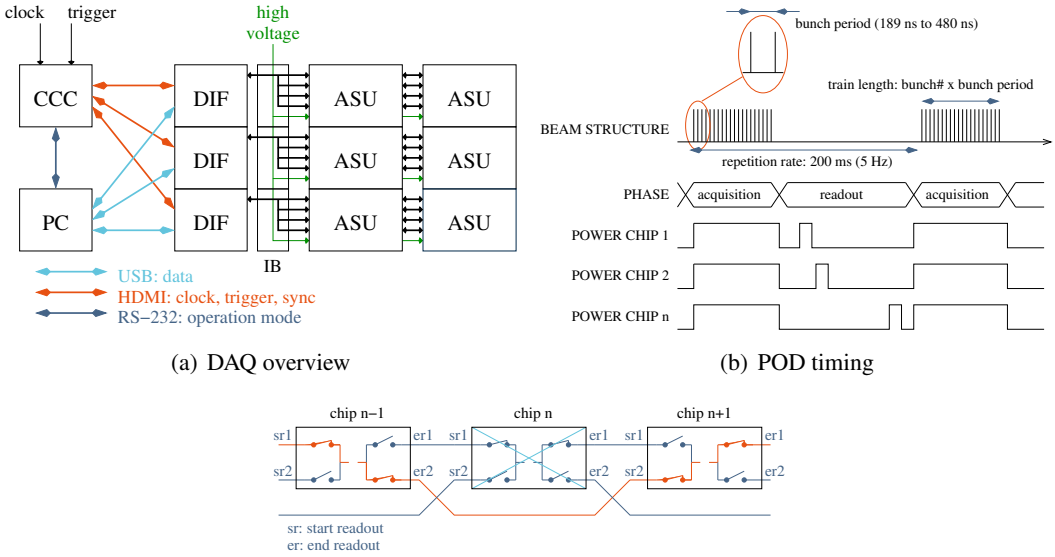
4.2 MICROMEGAS chamber construction

A square-meter MICROMEGAS is composed of 6 of the previously described ASUs. These are laid side-by-side, thus forming 3 lines of 2 ASUs. This scheme is scalable, so that larger detector may be build by increasing the number of ASUs per line, with a goal of 1×3 m^2 chambers. This scheme has been improved since the first HARDROC prototype [6]: especially access to ASIC is now possible for maintenance or debug purpose.

The 3 mm drift space is obtained by gluing spacers between ASUs and a frame on the bulk side, and a 2 mm thick stainless steel cover on top of this frame. A copper cathode and a glass/epoxy insulator have been deposited previously on this cover.

On the other side, a one square meter G11 mask have been machined and glued around the electronic components, to stiffen the whole detector (figure 6(b)). These masks have built-in nuts, to screw an additional 2 mm stainless steel stiffener, used for detector handling and transport.

2012 JINST 7 C01029



(a) DAQ overview

(b) POD timing

(c) By-passing

Figure 7. Data acquisition.

5 Readout

5.1 MICROROC readout

Because of the very high number of electronic channels foreseen in a complete calorimeter, MICROROC is embedded inside the detector and is designed to be chained without any external circuitry. Open collector output signals and daisy-chained token are used to minimize the number of output lines on the detector.

There is one serial output which is transferred to the DAQ during the inter bunch. Control tokens are daisy chained across the PCB. Moreover, to save power, during the inter bunch the POD (Power-On Digital) module shuts down the transceivers of chips which are not transmitting data (figure 7(b)).

The data format is: `chipID+BCID+depth×(data×channels)`

Both ASIC and PCB have two redundant lines for data acquisition control and readout, selectable by a configuration register. This allows to bypass one or several chip in the readout chain (figure 7(c)). Each ASU line is read independently, in order to ensure maximum reliability: if an unrecoverable hardware failure occurs, only a line is lost, not the whole detector.

5.2 Data aquisition (DAQ)

This kind of detector is foreseen to be read out by the so-called CALICE DAQ. At the moment, this system is under development, therefore a Labview based DAQ with USB link is used. An acquisition rate up to 500 Hz (200 Hz with telescope synchronisation) has been reached. All triggers and acquisition mode commands are distributed in a synchronous way, with the Clock and Control Card (figure 7(a)). The dedicated Labview software allows to manage the ASIC configuration files (pedestal, thresholds, offsets), test ASIC, test ASU, record data in testbox and record data of the

2012 JINST 7 C01029

whole detector, with or without external trigger, because of its versatility. It also provides a simple display which is used to verify the overall response of the detector. Data analysis are performed offline with the ROOT-based framework.

6 Preliminary test beam results

The first MICROMEGAS square meter prototype with MICROROC was tested in muon and pion beams at CERN/SPS in August 2011 during the CALICE and RD51 test beam periods. Two kinds of small MICROMEGAS detectors (pad for coarse and strips for fine spatial resolution) provided external tracking, and three scintillator paddles with PMT provided trigger signals. The following tests were performed:

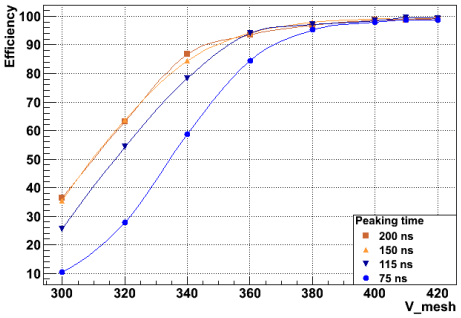
- Drift voltage scan (405 to 570 V);
- Mesh voltage scan (300 to 420 V) for different shaping times;
- Position scan (6 000 pads scanned: $2/3$ of the total area);
- Threshold scan (lowest threshold);
- Behaviour in hadron showers;
- Different beam angle of incidence (0°, 30° and 60°);
- Trigger-less data acquisition: so-called RAMFULL mode (ILC operation).

Preliminary results show that efficiency increases with shaping time, so that an optimum between hit rate and efficiency capability can be found for each mesh voltage (figure 8(a)). The detector multiplicity is not correlated with the shaping time (figure 8(b)). The dependence of the efficiency as a function of the readout threshold plot is in very good agreement with those obtained in previous test beams with analog readout MICROMEGAS [7] (figure 8(c)). Finally, the analog readout plot shows the expected Landau distribution of the charge in the detector (figure 8(d)).

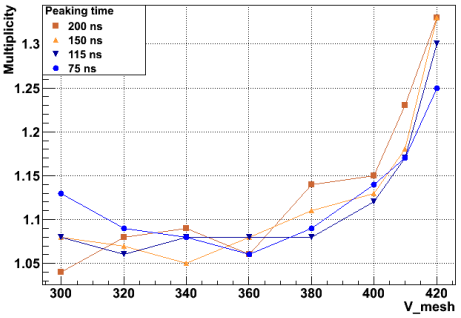
These results show that MICROROC ASIC performances when implemented on a detector are preserved. Moreover, they also show that MICROMEGAS detectors are a good option for hadronic calorimetry at future linear colliders. The next steps are:

- Launch a production to equip a cubic meter calorimeter of 40 layers;
- Use the full power pulsing capability in test beam;
- Rework the DAQ to deal with large number of planes (on going);
- Enlarge the detectors (aim: 1×3 m^2);
- Start a R&D to suppress protection networks on PCB.

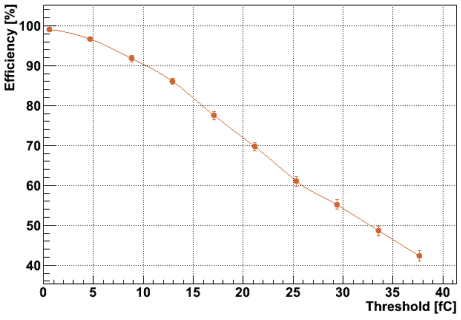
2012 JINST 7 C01029



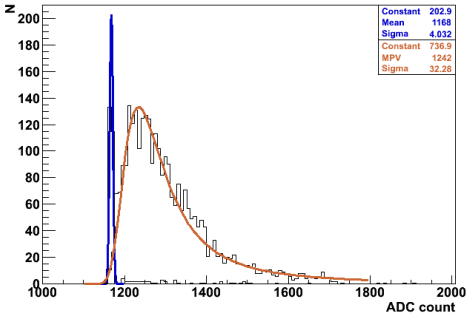
(a) Efficiency vs peaking time



(b) Multiplicity vs peaking time



(c) Efficiency vs threshold (Tp=200 ns)



(d) Analog readout

Figure 8. Testbeam preliminary results.

7 Conclusion

The MICROROC chip has been designed and built for MICROMEGAS readout in the frame of hadronic calorimetry at ILC. Both prototype tests and beam tests with detector show that MICROROC fulfills the requirements of an ASIC optimized for ILC. In particular, the ASIC low noise (0.24 fC) with a power consumption less than 100 µW per channel (1 % power pulsing) allows high efficiency detection (greater than 98 %). A very low bad hit contamination (5 Hz for 9216 channels) is achieved in auto-trigger mode after pedestal adjustment.

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2012 JINST 7 C01029

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2012 JINST 7 C01029