MICROROC

LAPP ANNECY, OMEGA

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Abstract –

MICRO MEsh GAseous Structure (MICROMEGAS) and Gas Electron Multipliers (GEM) detectors are two candidates for the active part of a Digital Hadronic CALorimeter (DHCAL) as part of a high energy physics experiment at the International Linear Collider. Physics requirements lead to a highly granular hadronic calorimeter with up to thirty million channels with probably only hit information (digital calorimeter).

To validate the concept of digital hadronic calorimetry, a cubic meter technological prototype, made of 40 planes of one squared meter each, is compulsory. Such a technological prototype involves not less than 400 000 electronic channels, thus requiring the development of ASIC.

Based on the experience of previous ASICs (DIRAC and HARDROC) and on multiple testbeam results, a new ASIC, called MICROROC (MICRO mesh gaseous structure Read-Out Chip), is currently being jointly developped at IN2P3 by OMEGA and LAPP microelectronics goups. It has been submitted to foundry in june 2010, and prototypes are expected to be delivered at the beginning of september.

MICROROC is a 64 channel mixed-signal integrated circuit based on HARDROC manufactured in AMS 350 nm SiGe technology. Analog blocks and the whole digital part are reused from HARDROC, but the very front end part ie the preamplifier and shapers, has been especially re designed for $1m^2$ MICROMEGAS detectors, which require HV sparks robustness for the electronics and also very low noise performance to detect signals down to 2fC.
Each channel of the MICROROC chip is made of a very low noise fixed gain charge preamplifier optimised for a detector capacitance of 80 pF and able to handle a dynamic range from 1fC to 500fC., two different adjustable shapers, three comparators and a random access memory used as a digital buffer. Other blocks, like 12-bit DAC, configuration registers, bandgap voltage reference, lvds receiver are included. All these blocks are power-pulsed, thus reaching a power consumption equal to zero in standby mode.

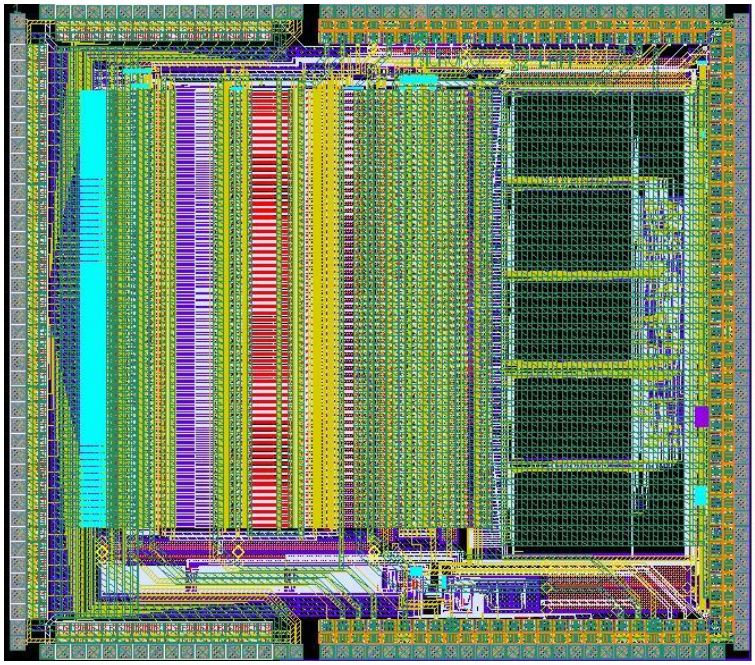

Figure 1 – Microroc layout

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3. ASIC pinout

It is compatible to HARDROC2 and HARDROC2b pinout except for the pin 119 which was unused in Hardroc2 and which corresponds to the hold input signal (was named "holdb" as it was active low and located pin 63 in HR2). **Slight differences with HARDROC2 are written in BLUE in the pinout list**.

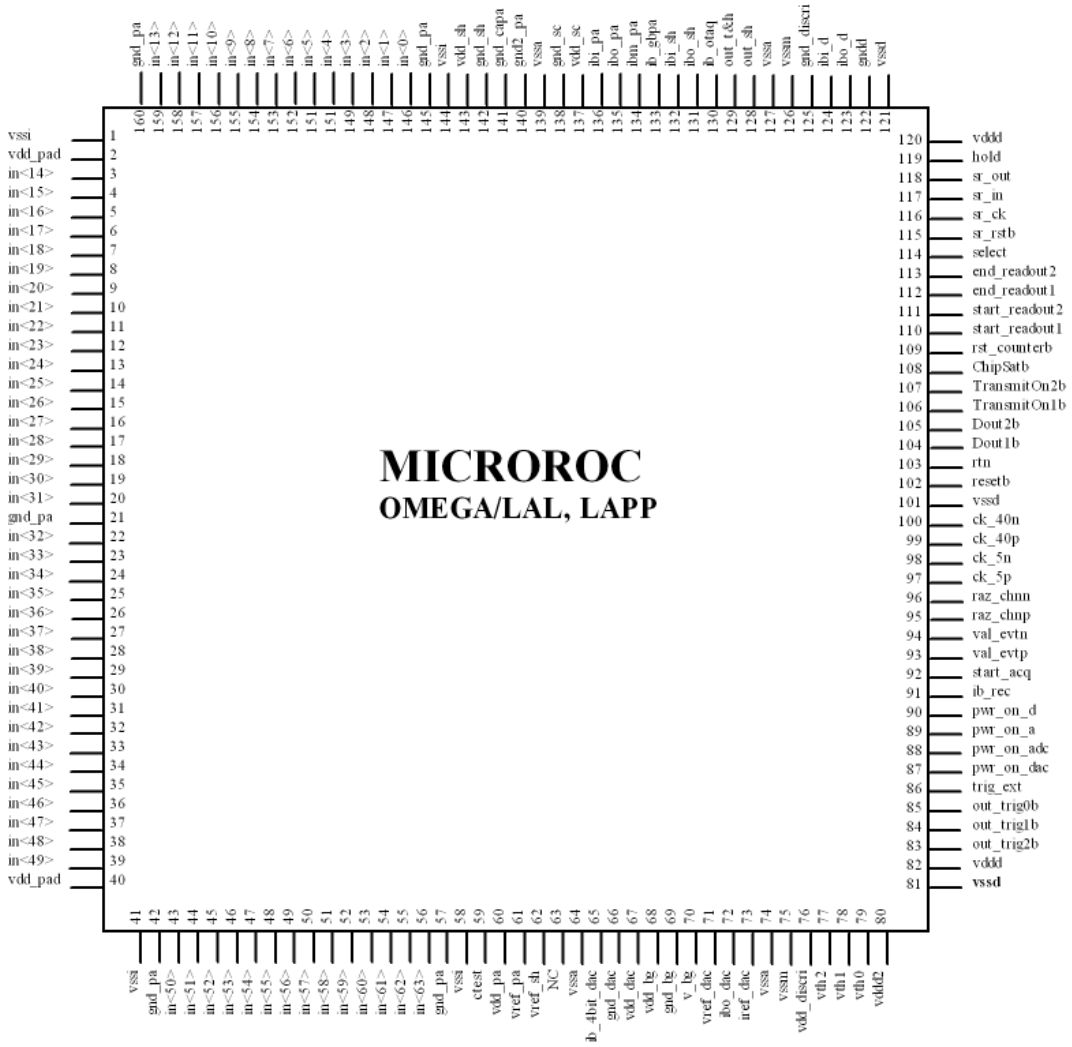


Figure 2 - Microroc pinout

Pin	Pin Name	Pin Type	Description	Comments	simulation
1	**vssi**	Power	Inputs Bulk	**to GND**	
2	**vdd_pad**	Power	Inputs Pads Protection		
3	in<14>	Analogue Input			
4	in<15>	Analogue Input			
5	in<16>	Analogue Input			
6	in<17>	Analogue Input			
7	in<18>	Analogue Input			
8	in<19>	Analogue Input			
9	in<20>	Analogue Input			
10	in<21>	Analogue Input			
11	in<22>	Analogue Input			
12	in<23>	Analogue Input			
13	in<24>	Analogue Input			
14	in<25>	Analogue Input			
15	in<26>	Analogue Input			
16	in<27>	Analogue Input			
17	in<28>	Analogue Input			
18	in<29>	Analogue Input			
19	in<30>	Analogue Input			
20	in<31>	Analogue Input			
21	**gnd_pa**	Power	Analogue (PreAmp) Ground	**to GND**	
22	in<32>	Analogue Input			
23	in<33>	Analogue Input			
24	in<34>	Analogue Input			
25	in<35>	Analogue Input			
26	in<36>	Analogue Input			
27	in<37>	Analogue Input			
28	in<38>	Analogue Input			
29	in<39>	Analogue Input			
30	in<40>	Analogue Input			
31	in<41>	Analogue Input			
32	in<42>	Analogue Input			
33	in<43>	Analogue Input			
34	in<44>	Analogue Input			
35	in<45>	Analogue Input			
36	in<46>	Analogue Input			
37	in<47>	Analogue Input			
38	in<48>	Analogue Input			
39	in<49>	Analogue Input			
40	**vdd_pad**	Power	Inputs Pads Protection		
41	**vssi**	Power	Inputs Bulk	**to GND**	
42	**gnd_pa**	Power	Analogue (PreAmp) Ground	**to GND**	**see Pin 21**
43	in<50>	Analogue Input			
44	in<51>	Analogue Input			
45	in<52>	Analogue Input			
46	in<53>	Analogue Input			
47	in<54>	Analogue Input			
48	in<55>	Analogue Input			
49	in<56>	Analogue Input			
50	in<57>	Analogue Input			

51	in<58>	Analogue Input			
52	in<59>	Analogue Input			
53	in<60>	Analogue Input			
54	in<61>	Analogue Input			
55	in<62>	Analogue Input			
56	in<63>	Analogue Input			
57	gnd_pa	Power	Analogue (PreAmp) Ground	to GND	
58	**vssi**	Power	Analogue part Bulk	**to GND**	
59	ctest	Analogue Input	Calibration input		
60	**vdd_pa**	Power	Analog (PreAmp) Power Supply	**to 3.3V**	
61	**vref_pa**	Analogue ref	Pre Amps bias voltage	40k, 10k to v_bg	2 V
62	**vref_sh**	Analogue ref	Pre Amps bias voltage	2.2k, 300 to v_bg	2.2 V
63	**NC**				
64	**vssa**	Power	Analogue part Bulk	**to GND**	
65	Ib_4bit_dac	Analogue Bias	4 bit dac bias	400k to gnd	6uA
66	gnd_dac	Power	Analogue Ground	to GND	
67	**vdd_dac**	Power	Analog Power Supply	**to 3.3V**	
68	**vdd_bg**	Power	Analogue bandgap Power Supply	**to 3.3V**	
69	gnd_bg	Power	Analogue (BandGap) Ground	to GND	
70	v_bg	Analogue Output	BandGap output		2.5V
71	vref_dac	Analogue Bias	10-bit triple DAC OTAs Input stage bias	200k,400k to v_bg	840m V or **940mV (see pin 73)**
72	ibo_dac	Analogue Bias	Bias dac	100k to vdd_dac	0.8V
73	Iref_dac	Analogue Bias	10-bit triple DAC bias current	**150k (vbg), 250k vrefdac External 200k to add in // with 150k => vref_dac=940mV**	1.9V **2.1V**
74	**vssa**	Power	Analogue part Bulk	**to GND**	
75	**vssm**	Power	Mixed part Bulk	**to GND**	
76	**vdd_discri**	Power	Mixed (Discriminator) Power Supply	**to 3.3V**	
77	vth2	Analogue Output	10-bit dual DAC output 2		
78	vth1	Analogue Output	10-bit dual DAC output 1		
79	vth0	Analogue Output	10-bit dual DAC output 0		
80	**vddd2**	Power	Digital (Digital ASIC) Power Supply	**to 3.3V**	
81	**vssd**	Power	Digital part Bulk	**to GND**	
82	**vddd**	Power	Digital (LVDS receivers & digital glue) Power Supply	**to 3.3V**	
83	**out_trig2b**	Digital Output	**Open collector signal (internal 30k)**		
84	**out_trig1b**	Digital Output	**Open collector signal (internal 30k)**		
85	**out_trig0b**	Digital Output	**Open collector signal (internal 30k)**		
86	trig_ext	Digital Input	External Trigger signal	Active ↑	
87	pwr_on_dac	Digital Input	DAC Power Pulsing Control	Active H	
88	pwr_on_adc	Digital Input	Slow shaper Power Pulsing Control	Active H	
89	pwr_on_a	Digital Input	Analogue Part Power Pulsing Control	Active H	
90	pwr_on_d	Digital Input	Digital Power Pulsing Control	Active H	
91	ib_rec	Analogue Bias	LVDS receiver bias current		25 µA
92	start_acq	Digital Input	Start & maintain acquisition	Active H	
93	val_evtp	Digital (LVDS) Input	Valid Events Signal	Active H	
94	val_evtn				
95	raz_chnp	Digital (LVDS) Input	External Raz Channel	Active H	
96	raz_chnn				
97	ck_5p	Digital (LVDS) Input	Slow Clock		
98	ck_5n				

99	ck_40p	Digital (LVDS) Input	40MHz Clock		
100	ck_40n				
101	**vssd**	Power	Digital part Bulk	**to GND**	
102	resetb	Digital Input	Reset ASIC digital part	Active L	
103	rtn	Power	Open Collector Ground	**to GND**	
104	Dout1b	Digital (OC) Output	Data Serial Output	Open Collector	
105	Dout2b	Digital (OC) Output	Data Serial Output	Open Collector	
106	TransmitOn1b	Digital (OC) Output	Active data readout	Open Collector / Active L	
107	TransmitOn2b	Digital (OC) Output	Active data readout	Open Collector / Active L	
108	ChipSatb	Digital (OC) Output	Chip is Full	Open Collector / Active L	
109	rst_counterb	Digital Input	Reset Gray Counter	Active L	
110	start_readout1	Digital Input	Digital RAM start reading signal	Active H	
111	start_readout2	Digital Input	Digital RAM start reading signal	Active H	
112	end_readout1	Digital Output	Digital RAM end reading signal	Active H	
113	end_readout2	Digital Output	Digital RAM end reading signal	Active H	
114	select	Digital Input	Select Slow Control Register (1) or Read Register (0)		
115	sr_rstb	Digital Input	Selected Register Reset	Active L	
116	sr_ck	Digital Input	Selected Register Clock	Active ↑	
117	sr_in	Digital Input	Selected Register Input		
118	sr_out	Digital Output	Selected Register Output		
119	**hold**	Digital Input	Hold Signal	Active H	
120	**vddd**	Power	Digital (LVDS receivers & digital glue) Power Supply	**to 3.3V**	**see Pin 82**
121	**vssd**	Power	Digital part Bulk	**to GND**	
122	**gndd**	Power	Digital (LVDS receivers & Digital glue) Ground	**to GND**	
123	ibo_d	Analogue Bias	Discriminator output stage bias current		2,3 V
124	ibi_d	Analogue Bias	Discriminator input stage bias current	100k to vdd_discri	0,8 V
125	**gnd_discri**	Power	Analogue (Discriminator) Ground	**to GND**	
126	**vssm**	Power	Mixed part Bulk	**to GND**	
127	**vssa**	Power	Analogue part Bulk	**to GND**	
128	**out_sh**	Analogue Output	multiplexed Shaper Output (HG or LG)		
129	**out_t&h**	Analogue Output	Multiplexed shaper Output after t&h		
130	ib_otaq	Analogue Bias	Analogue Outputs (Shapers) OTA bias current	15k to vdd_sh	0,8 V
131	**ibo_sh**	Analogue Bias	Shaper output stage bias	100k gnd_sh	2,1 V
132	**ibi_sh**	Analogue Bias	Shaper input stage bias	61k gnd_sh	2,3 V
133	**ibgb_pa**	Analogue Bias	pac bias	280k vdd_pa	0,7 V
134	**Ibm_pa**	Analogue Bias	pac bias current	50K to vdd_pa	0,7 V
135	**Ibo_pa**	Analogue Bias	pac bias current	250k to vdd_pa	0.7 V
136	**Ibi_pa**	Analogue Bias	pac bias current	7.3k vdd_pa	1.8 V
137	**vdd_sc**	Power	Slow control Power Supply	**to 3.3V**	
138	**gnd_sc**	Power	Slow control Ground	**to GND**	
139	**vssa**	Power	Analogue Ground	**to GND**	
140	**gnd2_pa**	Power	ground 2 of the PAC	**to GND**	
141	**gnd_capa**	Power	Analogue (Hold Capacitor) Ground	**to GND**	
142	**gnd_sh**	Power	Analogue (Shaper) Ground	**to GND**	
143	**vdd_sh**	Power	Analogue (Shaper) Power Supply	**to 3.3V**	
144	**vssi**	Power	Analogue part Bulk	**to GND**	
145	**gnd_pa**	Power	Analogue (PreAmplifiers) Ground	**to GND**	**see Pin 21**
146	in<0>	Analogue Input			
147	in<1>	Analogue Input			

148	in<2>	Analogue Input			
149	in<3>	Analogue Input			
150	in<4>	Analogue Input			
151	in<5>	Analogue Input			
152	in<6>	Analogue Input			
153	in<7>	Analogue Input			
154	in<8>	Analogue Input			
155	in<9>	Analogue Input			
156	in<10>	Analogue Input			
157	in<11>	Analogue Input			
158	in<12>	Analogue Input			
159	in<13>	Analogue Input			
160	gnd_pa	Power	Analogue (PreAmplifiers) Ground	to GND	see Pin 21

Table 1 - Pinout description

4. General description

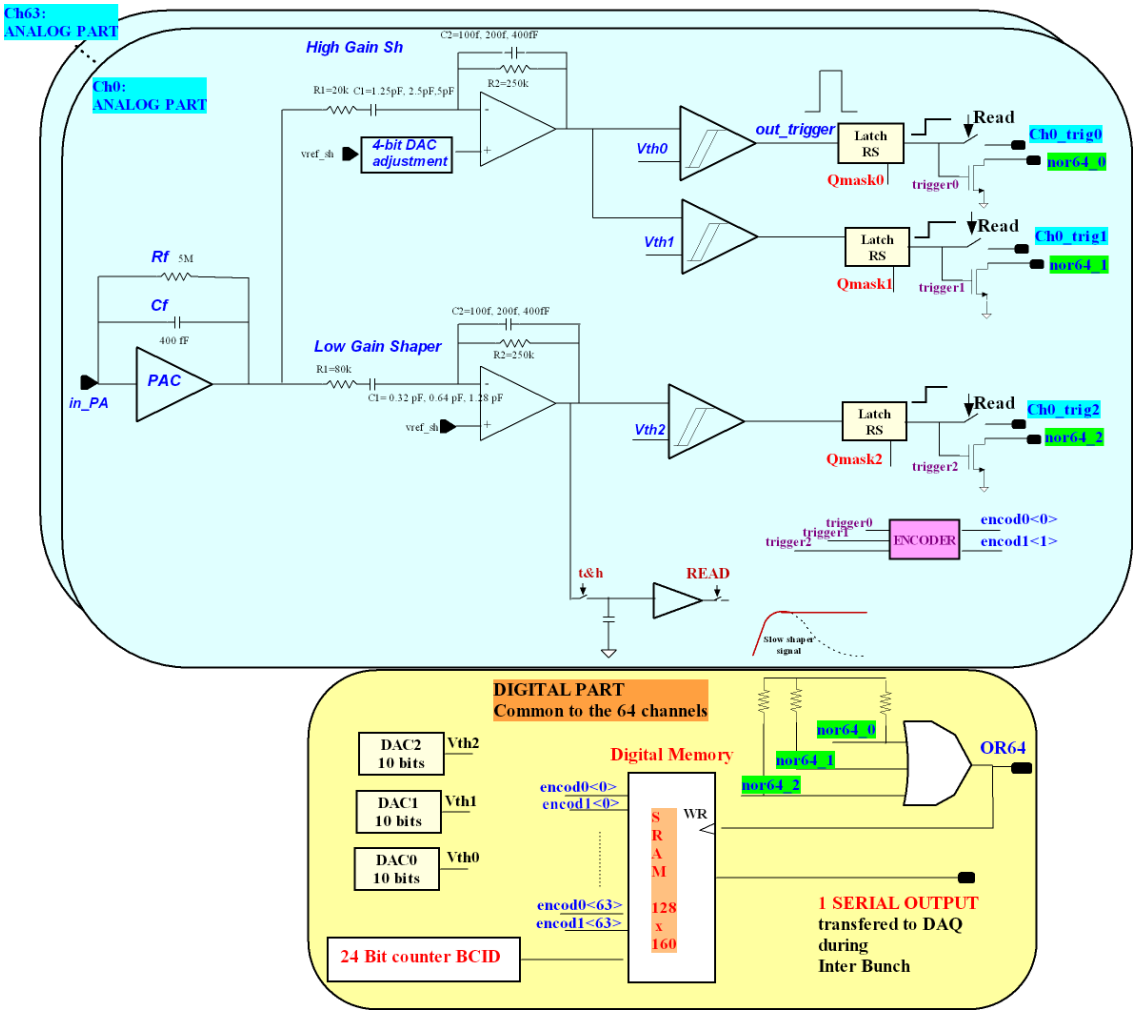


Figure 3 – Microroc simplified scheme

CELL	BIT#	BIT NAME	DEFAULT VALUE
One_channel0	1	(Srin_sc=d_test ->) ctest_ch0	off
One_channel1	2	ctest_ch1	off
…	…		
One_channel63	64	ctest_ch63=q_test=d_pwr	0 (off)
BIAS	65	on/off_pa for pp (+ pwr_on_a)	0=OFF
	66	en_gbst (enable gain boost)	1=> on
	67	On/off sh_hg for power pulsing (+pwr_on_a)	0 => off
	68	On/off sh_lg (depends on ON/FF sh_hg)	0 => off
	69	sw_lg<1>	1 => on
	70	sw_lg<0>	0 (off)
	71	On/off widlar for pp (+pwr_on_adc)	0 (off)
	72	valid_sh_hg (=q of the FF) And valid_sh_lg for READ register (qb of the FF)	0 (off) 1 (on)
	73	sw_hg<1>	1 => on
	74	sw_hg<0> = q1_sc_bias=d_4bit_dac	0=> off
One_channel0 4 bits dac	75	B0	0 (off)
One_channel0	76	B1	0 (off)
One_channel0	77	B2	0 (off)
One_channel0	78	B3	0 (off)
One_channel1 4 bits dac	79	B0	
One_channel1	80	B1	
One_channel1	81	B2	
One_channel1	82	B3	
…			
One_channel63 4bits dac	327	B0	
One_channel63	328	B1	
One_channel63	329	B2	
One_channel63	330	B3 = q_4bit_dac=d_pwr_4bitdac	0 (off)
BIAS	331	On/off dac_4bit for pp (+pwr_on_a)	0 (off)
	332	en_otaq	0 (off)
	333	On/off otaQ for pp (+pwr_on_adc)	0 (off)
	334	on/off discri0 for pp (+pwr_on_a)	0 (off)
	335	on/offdiscri2 depends on discri0	0 (off)
	336	on/off discri1 depends on discri0	0 (off)
	337	q2_sc_bias=d_mask=rs_or_discri	1
One_channel0	338	Mask discri0 ch0	1 (no mask)
One_channel0	339	Mask discr1 ch0	1 (no mask)
One_channel0	340	Mask discri2=qmask ch0	1 (no mask)
One_channel1	341	mask0 ch1	1 (no mask)
One_channel1	342	mask1 ch1	1 (no mask)
One_channel1	343	mask2=qmask ch1	1 (no mask)

…	…	…	
One_channel63	527	mask0 ch63	1 (no mask)
One_channel63	528	mask1 ch63	1 (no mask)
One_channel63	529	mask2 ch63=qmask	1 (no mask)
TOP LEVEL	530	header<0>	1
	531	header<1>	1
	532	header<2>	1
	533	header<3>	1
	534	header<4>	1
	535	header<5>	1
	536	header<6>	1
	537	header<7> = srin_triple dac	1
Triple DAC :	538	En_pp_bandgap	1
Bias DAC	539	On/off bg	0
	540	En_pp_dac	1
	541	On/off dac	0
DAC0 (for Vth0)	542	Bb0<0> ! MSB and low active !	1 (off)
	543	Bb0<1>	1 (off)
	544	Bb0<2>	1
	545	Bb0<3>	1
	546	Bb0<4>	1
	547	Bb0<5>	1
	548	Bb0<6>	1
	549	Bb0<7>	1
	550	Bb0<8>	1
	551	Bb0<9>	1 (off)
DAC1 (for Vth1)	552	Bb1<0>	1
	553	Bb1<1>	1
	554	Bb1<2>	1
	555	Bb1<3>	1
	556	Bb1<4>	1
	557	Bb1<5>	1
	558	Bb1<6>	1
	559	Bb1<7>	1
	560	Bb1<8>	1
	561	Bb1<9>	1 (off)
DAC2 (for Vth2)	562	Bb2<0>	1
	563	Bb2<1>	1
	564	Bb2<2>	1
	565	Bb2<3>	1
	566	Bb2<4>	1
	567	Bb2<5>	1
	568	Bb2<6>	1
	569	Bb2<7>	1

	570	Bb2<8>	1
	571	Bb2<9> =q_dac	1 (off)
Trigger cell	572	trig2b (nor64_2)	1 (=valid ON)
	573	trig1b (nor64_1)	1 (=valid ON)
	574	trig0b (nor64_0)	1 (=valid ON)
	575	EN_trig_out	1 (=valid ON)
	576	disc_or_or	1 (=or)
	577	trig_ext validation	1
	578	raz_chn_int validation	1
	579	raz_chn_ext validation=qt_sc	0
TOP LEVEL	580	Sc_on 5MHz and 40MHz (+lvds_on5 and lvds_on40)	0 (off)
	581	Ck_mux: choice between sroand sro_pod, ck5 and ck5_pod, ck40 and ck40_pod	1=> sro,ck5,ck40 validated (pod bypassed)
	582	Sel_raz1 (raz_chn width)	1 (on)
	583	Sel_raz0 (mux raz_chn width)	1 (on)
	584	NC	1
	585	NC	1
	586	Sel endreadout 1 or 2	1 (endreadout1)
	587	Sel startreadout 1 or 2	1 (startreadout1)
	588	EN_OC chipsatb	1
	589	EN_OC transmiton2b	1
	590	EN_OC transmiton1b	1
	591	EN_OC dout2b	1
	592	EN_OC dout1b	1
	592b	*Q_sc = Srout_sc (d clocked on ckb)*	1

Table 2 - Slow Control parameters

4.1. Analogue channel description

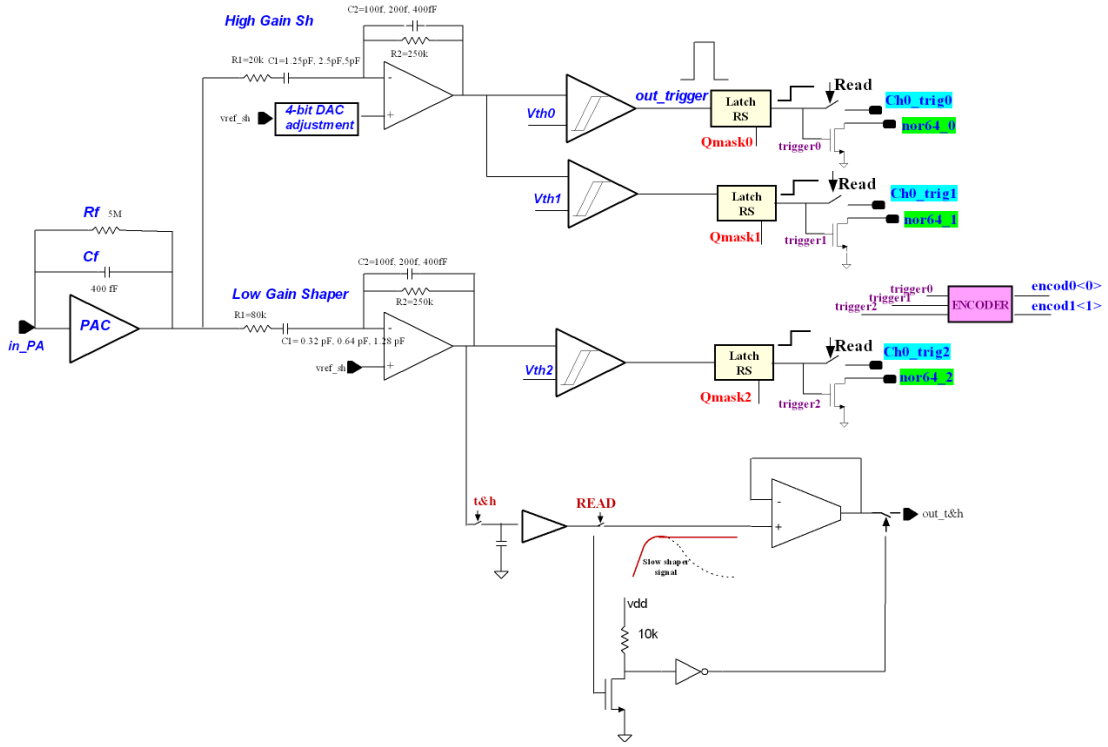


Figure 4 – Microroc analog part

4.1.1. Preamplifier description

Low noise charge preamp optimised for a detector capacitance of 80 pF and a dynamic range up to 500 fC.
Feedback network Rf=5 MΩ and Cf=400 fF
HV protection

4.1.2. Shaper description

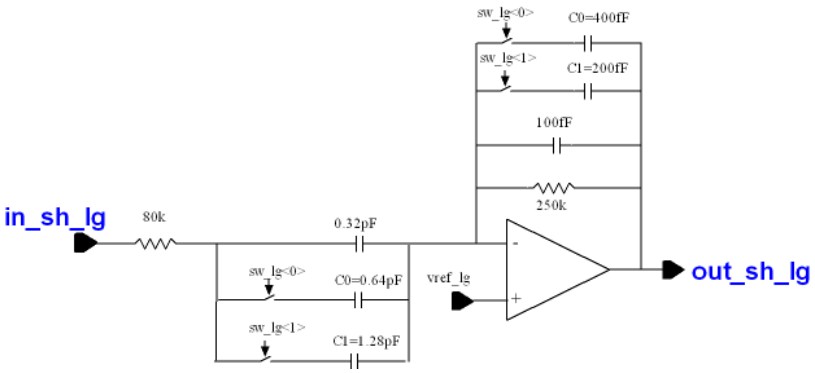


Figure 5 – Low Gain shaper

A high gain (g=4) and a low gain (gain=1) CRRC shapers follow the charge preamp.

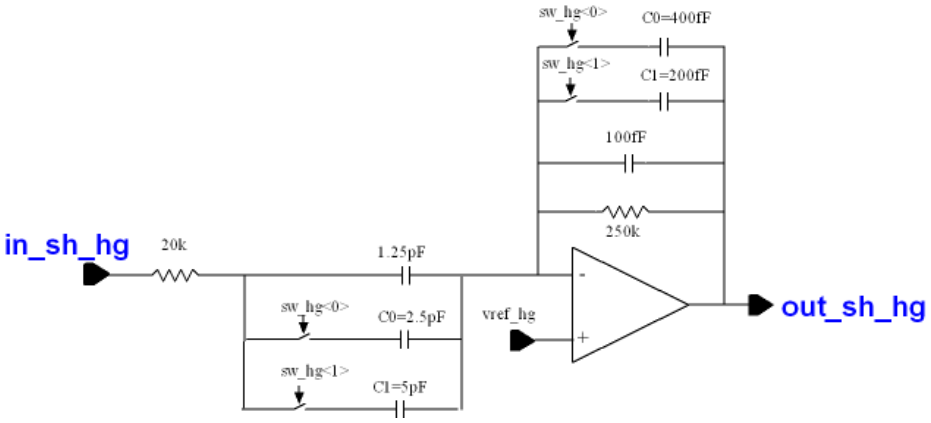


Figure 6 – High Gain shaper

The time constant can be changed for both using SC parameters (SC 69 and SC 70 for the low gain, SC 73 and 74 for the high gain) allowing a peaking time of 30ns, 100ns, 150ns or 200 ns as shown on Figure 7.

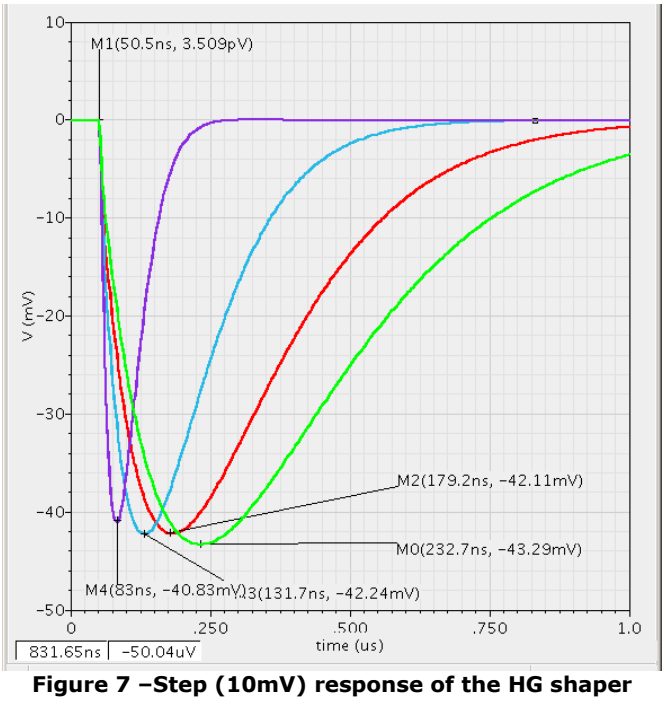


Figure 7 –Step (10mV) response of the HG shaper

The noise of the PAC followed by the HG shaper (tp=200 ns) have been simulated and found equal to 0.25 fC which allows to set the threshold of the discriminator that follow the HG shaper to a very low value such as 2fC.

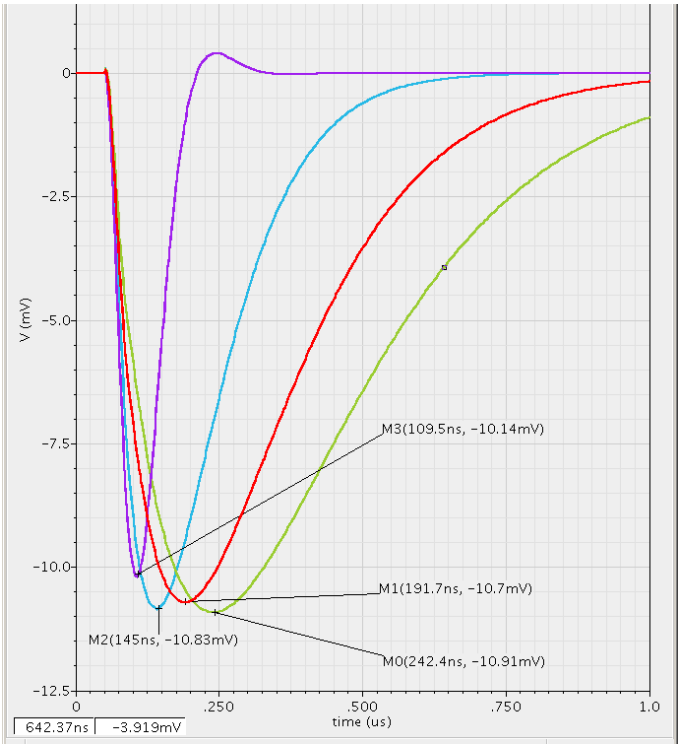


Figure 8 –Step (10mV) response of the LG shaper

The Low Gain shaper can be also used for charge measurement. Its output is sent to a track and hold buffer to store the charge in a 2 pF capacitor. An HOLD signal can be sent from outside (pin 119). The output of the charge (= out_t&h, pin 129) can be read by selecting a channel among the 64 using the read register (No SC parameter are needed). This output can be daisy chained.

The amplifier of these 2 shapers is slightly different. The transistors of the differential pair of the low gain shaper are 10 times bigger than those used in the high gain shaper. The expected offset with such big transistors is about 350 µV.
For the high gain shaper, the transistors of the differential pair are rather small and the offset can be compensated thanks to a 4 bit-dac used to tune the reference voltage of the shaper amplifier.

4.1.3.4bit-dac

There is a 4bit_dac per channel to tune the reference voltage of the High Gain shaper and thus compensate its offset. This dac is made of 4 switched current sources (using the SC parameters: SC 75, 76 etc). With a 14k resistor and a 52nA reference current, the slope is 700µV/DAC unit and the maximum value is 10.9mV.
The reference current can be changed using an external R.

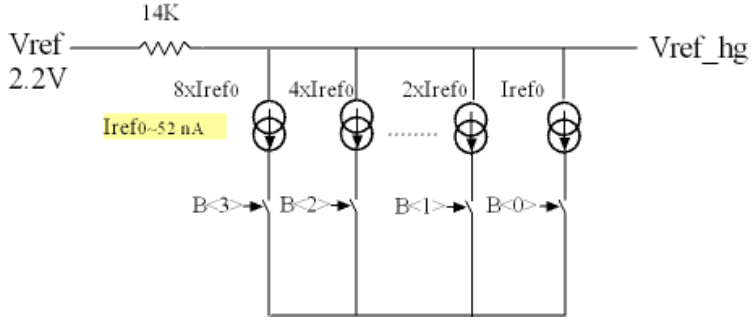


Figure 9 –4bit_dac schematics

4.1.4.Discriminators and triple 10bit-dac

The shapers are followed by 2 discriminators: the High Gain shaper by the discri0 and the discri1 and the Low Gain shaper by discri2. Their corresponding thresholds Vth0, Vth1 and Vth2 are set thanks to 3 10 bit DACs. Vth0 is set around 2fC, Vth1 around 20fC and Vth3 around 200 fC.

Out_dac= Vref_dac + 80K x Iref x(B<0>x2 + B<1>x1+ … +B<8>x1/128 + B<9>x1/256)
with Vref_dac=840 mV and Iref=7.8 µA
2.43mV/DAC Unit (840 mV to 2.9V)

Bb<0>, Bb<1> … Bb<9> are set using the SC parameters 542, 543 etc.

DAC dynamic range optimisation: Iref to be divided by 2. Add external 200k between pin 73 and V_BG.
=> slope 1.37 mV/DAC Unit, from 940mV to 2.34V

4.2. Analog to Digital interface

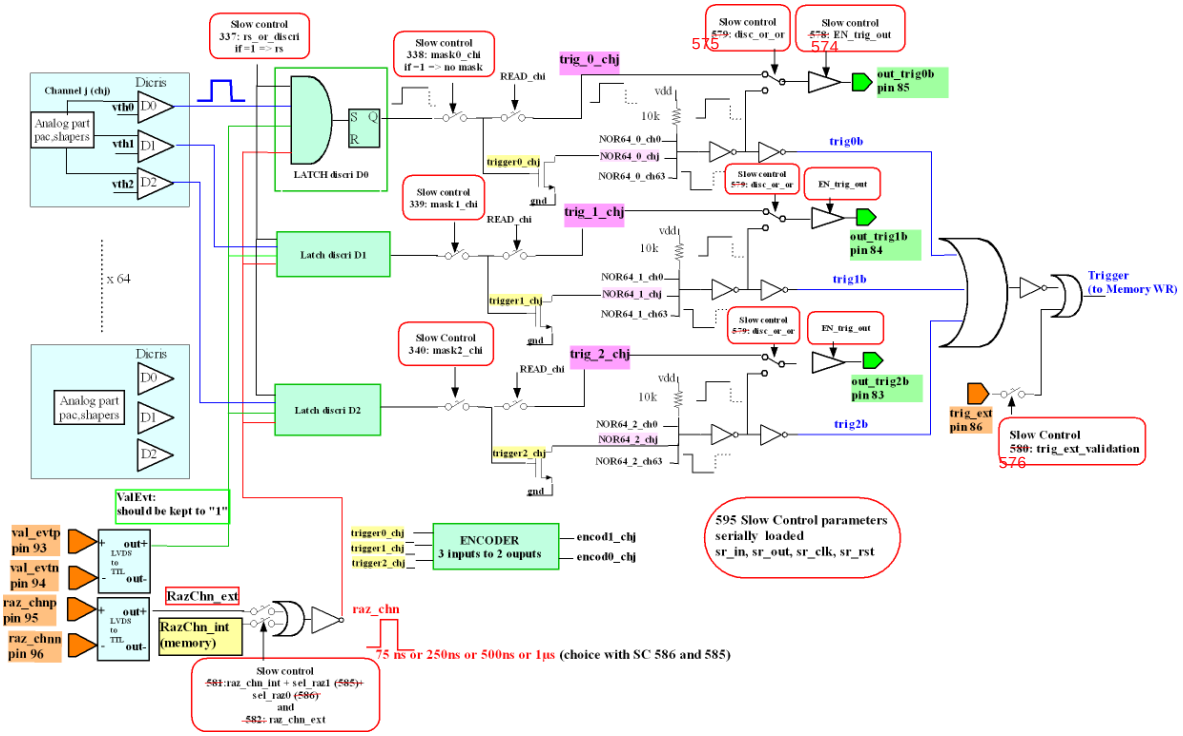


Figure 10 – Analog to Digital interface

The Val Evt signal can be kept to 1. The acquisition begins as soon as the **Start acquisition signal (Start_Acq pin 92)** is received by the ASIC

4.2.1. Read and SC (Slow Control) registers

2 shift registers are integrated: a 64 flip flops Read register to select (or multiplex) one channel among the 64 and a 595 flip-flops SC register to load serially the SC parameters (Table 2).
The data input (sr_in, pin 117), clock (sr_ck, pin 116) and reset (sr_rstb, pin115) of these 2 registers are sent to the SC or Read register inputs depending of the level of the external select signal (pin 114). When select=0 (default value), the inputs are connected to the Read register. When select=vdd, the inputs are connected to the SC register.

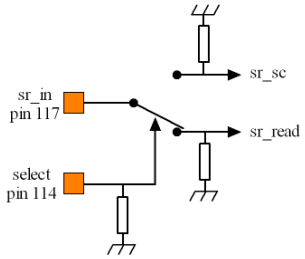


Figure 11 - Selection of the Read/SC register

4.2.2.Latches (RS)

For each channel, the 3 discrisminators outputs (D0, D1,D2) are latched during the acquisition phase initiated by the "StartAcq" signal(pin92). The razchan (=reset) of the latch has to be performed before the acquisition of a new event.
The width of this raz_chn must be changed according to the chosen peaking time to avoid "re triggering". This is illustrated in the plot above showing the RS output (= violet curve) when the Raz_Chn width is 75ns and the shaper peaking time is 200ns.The "retriggering" can be avoided using a 500ns width internal raz Chn.
This width selection is made using the SC parameters sel_raz0 (585) and sel_raz1 (586) and according to the table below.

Sel_raz1	Sel_raz0	Raz witdth
0	0	75 ns
0	1	250 ns
1	0	500 ns
1	1	1 µs

Figure 12 – Internal Raz_Chn width selection

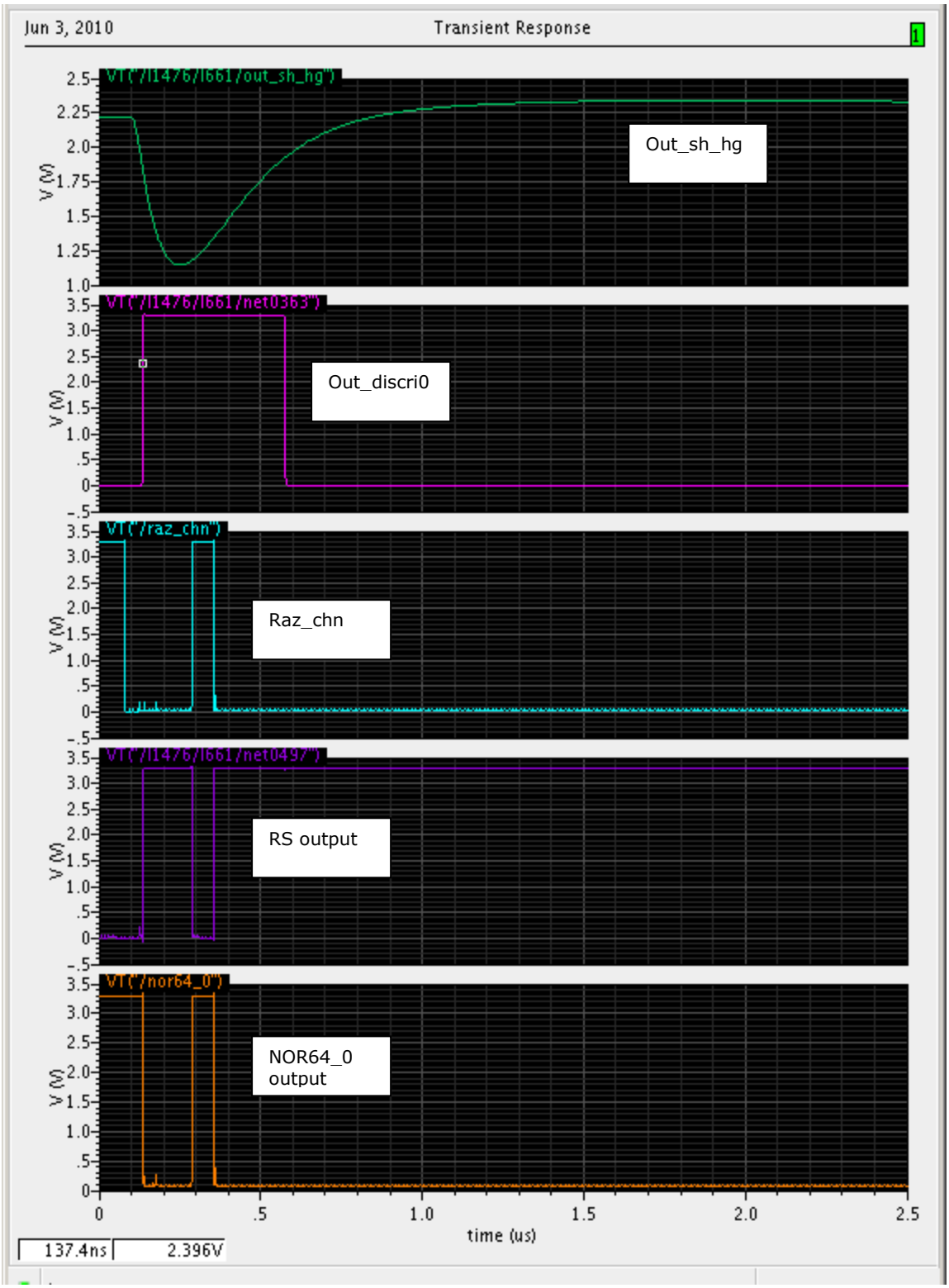


Figure 13 – Effect of the Raz_Chn width

The SC parameters EN_raz_chn_int (SC 581) and En_raz_chn_ext (SC 582) allow choosing between the internal raz_chn generated by the state machine of the memory or an external one (pins 95 and 96).

4.2.3. Triggers

For debug, it is possible to select internal points of the trigger chain. Thus, using *rs_or_discri* (SC 337) and the *disc_or_or* (SC 579) SC parameters, the latched or direct discriminator output or the OR64 ouput can be selected to be seen on scope.
Each trigger output can be masked in case of problem using the *mask0,1 or 2* SC parameters available for each channel.
An encoder 3->2 has been integrated to deliver 2 trigger encoded outputs for each channel: encod0 and encod1 are stored in the digital memory which is similar to those integrated in hardroc1 (except for the bug pointer).

Discri3	Discri2	Discri0	enc <1>	enc <0>
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Figure 14 -Encoder

WARNINGS:
"rs_or_discri" has to be set to "rs" (=default value of the SC parameter) to be able to use the Memory.

4.3. Digital part

4.3.1. Digital Memory

The "rs_or_discri" SC parameter must be set to "rs" (latch mode).

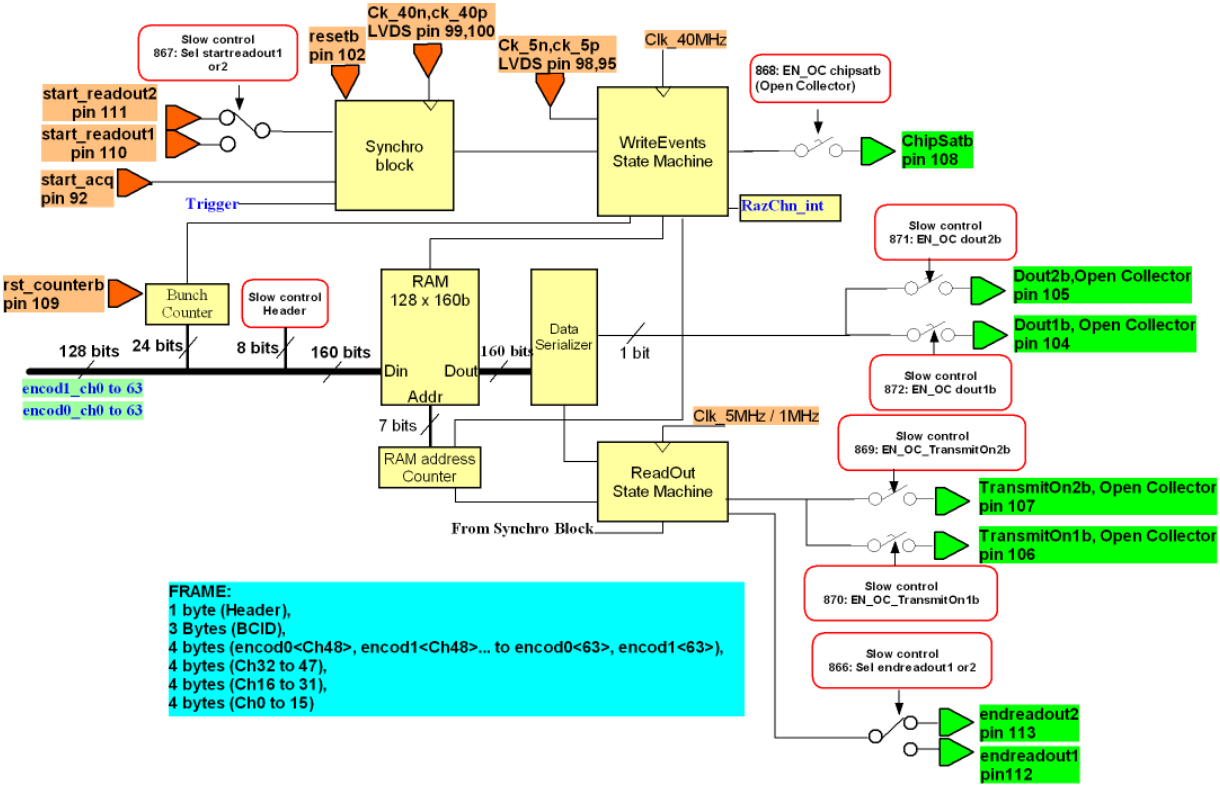


Figure 15 – Simplified schematics of the digital memory

4.3.2. Open Collector buffer

Dout1b, Dout2b, TransmitOn1b, TransmitOn2b, Chipsatb are open collector signals.

4.3.3.Redundancy of the OC lines:

To ensure the realibility of the lines used in the daisy chain, the Doutb, transmitonb, start and end readout signals have been doubled. The selection of the line to be daisy chained is made using SC parameters.

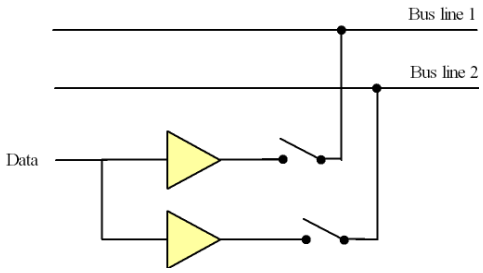


Figure 16 - Extra buffers for redundancy

4.3.4.StartReadout and EndReadout bypass:

The bypass of one bad ASIC of the daisy chain can be performed as the StartRO and EndReadout signals have been doubled.
The bypass has to be made on the PCB using switches or resistors (Figure 19). The selection of the line is made using the SC parameters.

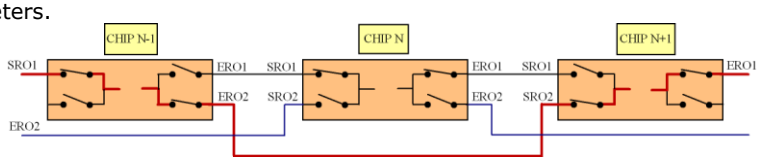


Figure 17 - StartReaout and EndReaout bypass

4.4. Power consumption and power pulsing timings

The maximum available power is 10µW/channel with a 0.5% duty cycle which means 180µA for the 64 channels chip. The power pulsing mode consists in switching OFF the bias current of the various cells during the interbunch.

PA	1.1mA
shapers	1.13mA
3 Discris	0.12mA
DAC	0.52mA
BG	1.2mA
vddd	2.4 mA
vddd2	0.4mA (=0 if 40MHz OFF)
TOTAL	6.9 mA

Table 3 - Power consumption

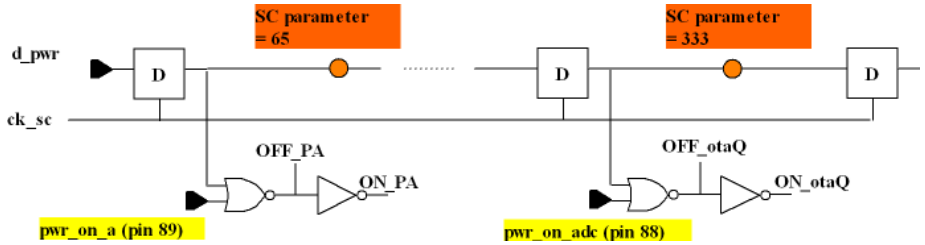


Figure 18 - Power pulsing logic

Thanks to the SC parameters (65=on/off pa, 67=on/off hg, on/off lg, on/off w, on/off dac 4bit, on/off otaq, on/off discri, on/off discri1, on/off discri2, on/off dac, on.off otabg) and the ASIC pins pwr_on_a, pwr_on_adc (=pwr_on_ss), pwr_on_dac, pwr_on_d (digital), we can select the cells to be power pulsed.
This logic (Figure 26) is used for all the cells ***except for the fast shapers (fsb0,1,2) and the corresponding discriminators (d0,d1 and d2)***.

WARNING: PARTICULAR CASE OF HG and LG shapers and Discri 0,1,2
The 2 shapers and the 3 discriminators can be power pulsed using pwr_on_a (pin 89) and the SC parameters: 67 and 68 corresponding respectively to ON/OFF shaper HG and LG, and 334, 335 and 336 corresponding respectively to ON/OFF discri0, 2 and 1). Only a few combinations are available. It is indeed irrelevant to power pulse only one shaper (or one discri).
The ON/OFF SC parameters for shaper LG (and for discri1 and 2) are set to 0 only when we do not want to use them at all: In this particular case, they are powered OFF permanently by setting to 0 the corresponding ON/OFF SC parameters (335 and 336 for discri2 and 1, 68 for sh_lg). In this case, 2 configurations are available (same logic for d0, d1, d2):

1- ON/OFF sh_hg, ON/OFF sh_lg = 10 => the HG shaper can't be power pulsed, the LG shaper is switched OFF permanently

2- ON/OFF fsb0, ON/OFF fsb1, ON/OFF fsb2= 00 => The HG shaper can be power pulsed, the LG shaper is OFF permanently.

When the 2 shapers (and the 3 corresponding discriminators) are used, there are only 2 available and relevant configurations (same logic for d0, d1, d2):

3- ON/OFF sh_hg, ON/OFF sh_lg= 11 => the 2 shapers are ON but the power pulsing is not possible for any of the shapers.

4- ON/OFF sh_hg, ON/OFF sh_lg = 00 => The 2 shapers can be power pulsed using the pwr_on_a pin.

Required timings to power pulse chips:
The pwr_on_adc is used to power pulse the widlar and OTA used for the charge measurement. As this part is not used for ILC applications, this pwr_on_adc signal must be kept to 0 to minimise the power consumption.
The start_acq signal has to be set at least 25µ s after the pwr_on_dac and at least 8 µs after the pwr_on_a according measurements performed on HARDROC2. It means that T1+T2= 25 µs (minimum value). The recommended value is 100µs.
As soon as the acquisition is finished (1ms in the case of ILC), the pwr_on signals must be disabled: first the pwr_on_d signal (to stop the clks) 2µs after the falling edge of the start acq signal, then the other pwr_on signals after 2 more µs as illustrated below

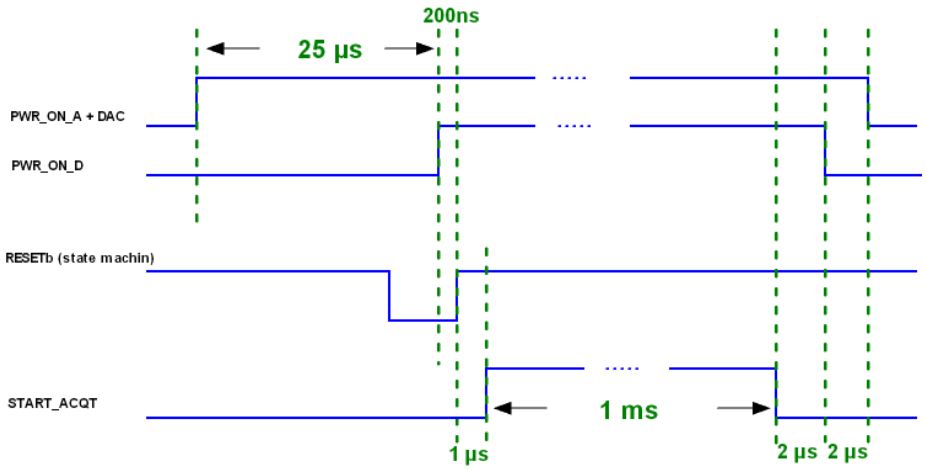


Figure 19 - Power pulsing timing

4.4.1.Power On Digital module (POD)

This module has been integrated to manage the 40MHz and 5 MHz clocks which are necessary during the readout that is performed during the 199ms interbunch. These 2 external clocks are sent to a LVDS receiver the bias current of which is 50µA. To meet the power budget this bias current has to be powered off as soon as the readout of the corresponding ASIC is finished.

The internal PowerOnInt of each chip is generated by the POD and corresponds to the digital OR of the PowerOn Digital (common to all the ASICs) and a pwr on generated by the POD from the StartReadout signal. PowerOnDigital and StartReadout are both generated by the DAQ (=Digital Interface=DIF).

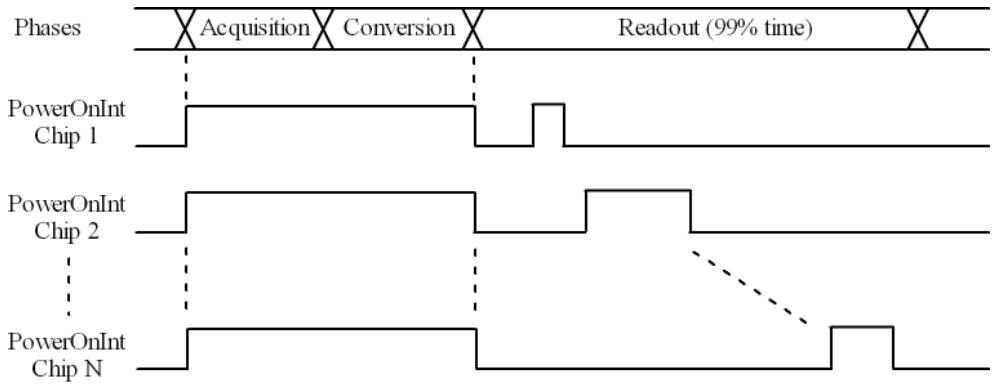
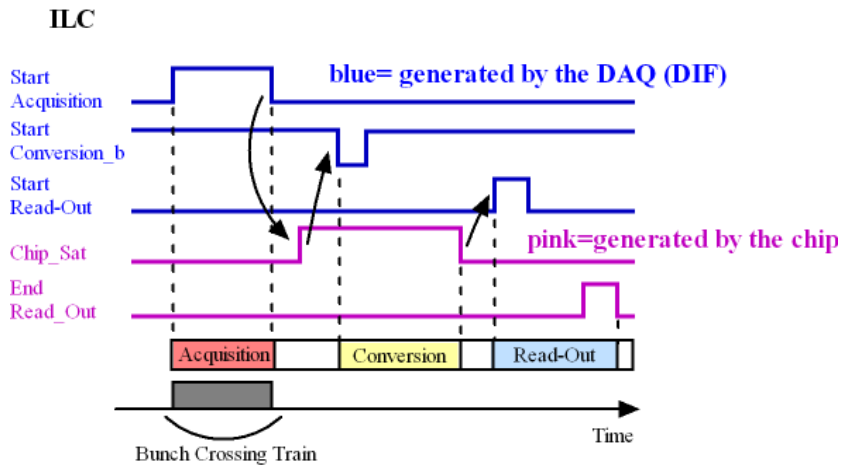


Figure 20 - POD timing

The timing diagrams below exhibit 2 different timing. In the ILC mode, it will be quite unlikely to have a chip full before the end of a bunch crossing train. This is not the case in testbeam where the chips are quickly full. Thus the testbeam timing exhibit the timing of the signals in the testbeam configuration.
This timing is common to all the ROC chips as SPIROC and SKIROC which integrate both ADCs. As there is no internal conversion in HARDROC, the "Conversion signals" are not used for hardroc.



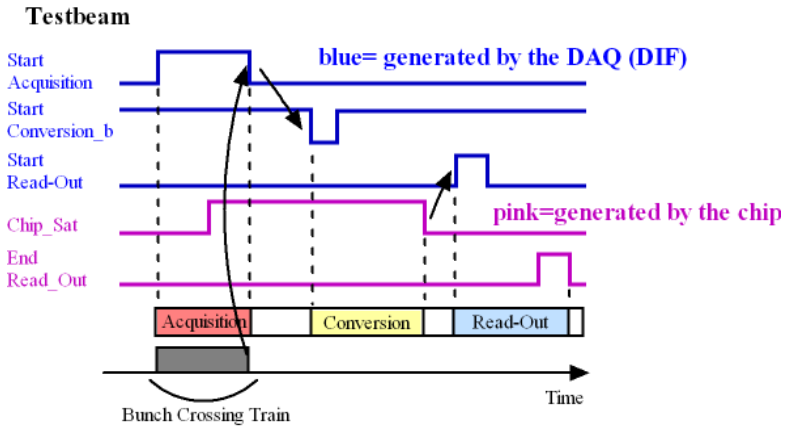


Figure 21 - Timing in ILC and testbeam modes

The Figure below exhibits the detailed timing of the POD when the ASICs are daisy chained.
CAREFUL: The pwr_on a and dac are not represented on this timing but they must be set ON at least 25 µs before the pwr_on_d. 25 µs is indeed the minimum required time for the DC levels to achieve their correct value. (see section 5.8)

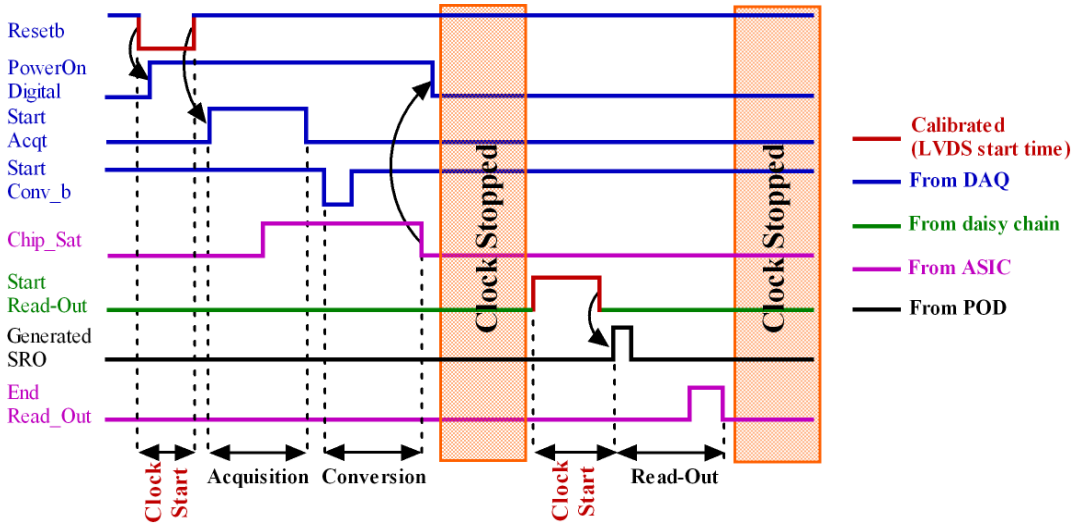


Figure 22 - POD timing

4.5. Calibration

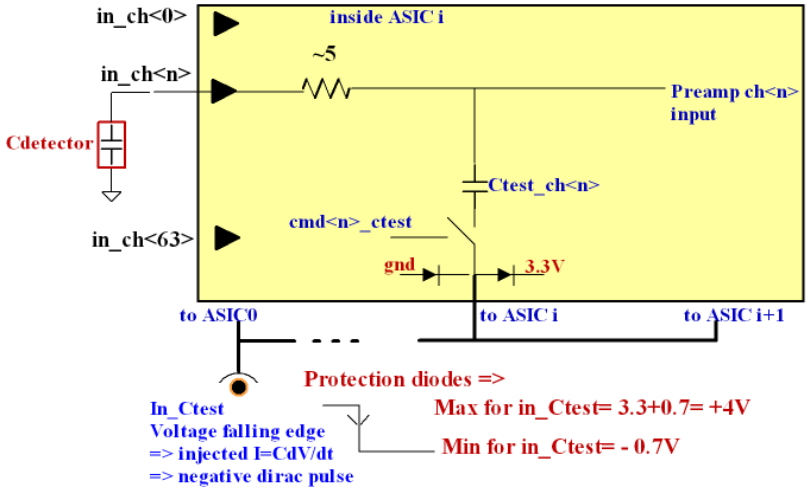
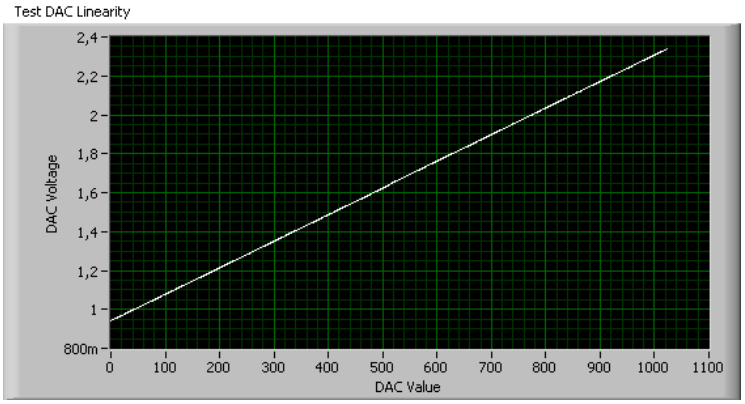


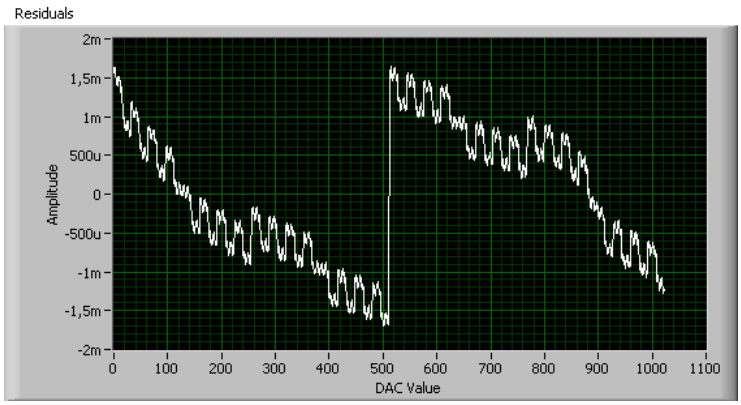
Figure 23 – Calibration using Ctest

Each channel can be calibrated using the Ctest input which is common to the 64 channels. A voltage pulse has to be sent on this Ctest input. There are 64 Ctest capacitors which have been designed to be equal to **500 fF** but the absolute value is within ±20% depending on the foundry runs. Nevertheless the dispersion between the 64 capacitors is within ±1% inside one chip and also within ±1% from chip to chip of the same foundry.

5. Testbench Measurements

5.1. DAC linearity

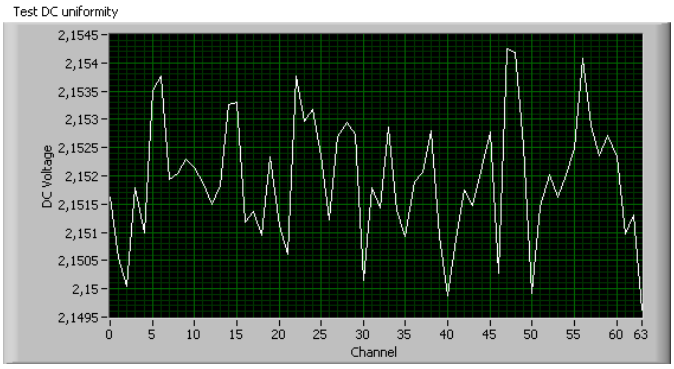




Slope: 1.37mV/DACU
Similar results for DAC 1 and DAC 2 (slope= 1.37 mV/DACU and residuals within ±1.5 mV)

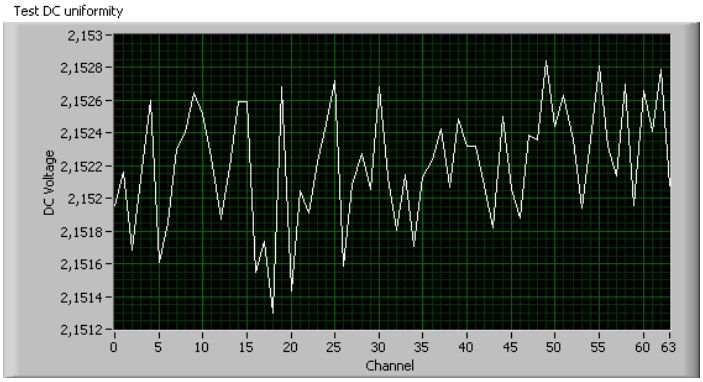
5.2. DC measurements

5.2.1.DC uniformity of the HG shaper



- <> 2,15194
- Min 2,14963
- Max 2,15424
- **Std 1.088mV**

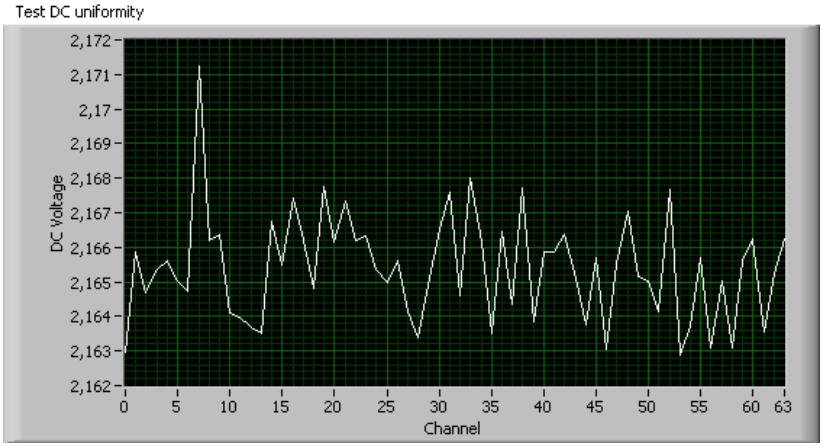
After 4 bits DAC correction:



- 2,15221
- Min 2,1513
- Max 2,15284
- **Std 360,71µ**

5.2.2.DC uniformity of the LG shaper:

Max=2.17125 Min= 2,16289 Mean= 2,1654 std= 1,54015m



6. Scope measurements:

HG shaper with detector capacitance= 20pF

	Qinj=10 fC	*Qinj=100fC*	*Noise*
Sw= 00	-72 mV, 65 ns	*-771 mV, 60 ns*	*sdev=1.58 mV*
Sw=01	-93 mV, 103 ns	*-971, 103 ns*	*sdev= 1.60 mV*
Sw= 10	**-100 mV, 152 ns**	***-1041 mV, 152 ns***	***sdev 1.61 mV***
Sw=11	-103 mV, 202 ns	*1.07V, 202 ns*	*sdev 1.61 mV*

HG shaper with Cd= 88 pF

	Qinj=10 fC	*Qinj=100fC*	*Noise*
Sw= 00	-67 mV, 79 ns	*-70 mV, 72 ns*	*sdev=3.3mV*
Sw=01	-94 mV, 121 ns	*-970 mV, 121 ns*	*sdev=3.6mV*
Sw= 10	**-101.2 mV, 168 ns**	***1.05V, 168 ns***	***sdev= 3.55mV***
Sw=11	-105 mV, 215 ns	*1.09V, 215 ns*	*sdev= 3.46mV*

7. Scurves performed on HG shaper

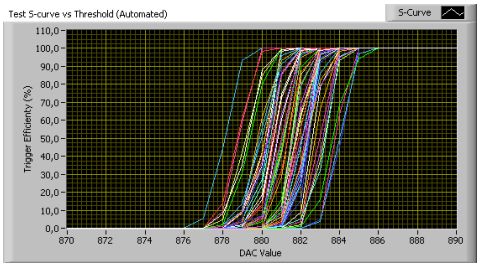
Chosen config: sw_hg=10

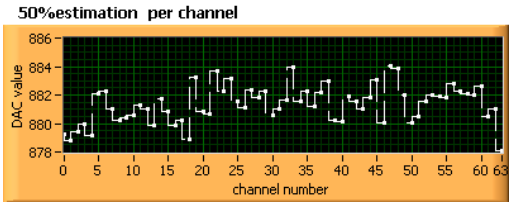
7.1. Cd=20pF

	Qinj=10fC	Qinj=100fC	Noise
Sw= 10	**-100 mV, 152 ns**	**-1041 mV, 152 ns**	**sdev 1.61 mV (equiv. to 0.16 fC)**

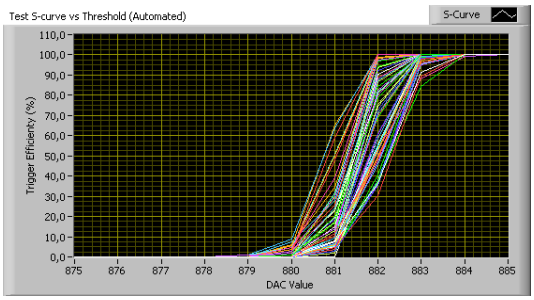
7.1.1.Pedestal without and with4Bit-DAC correction:

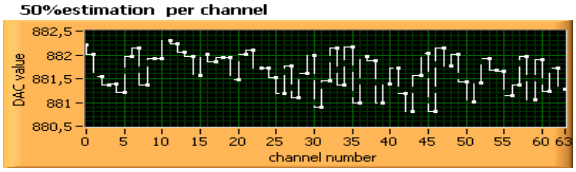
Without correction:

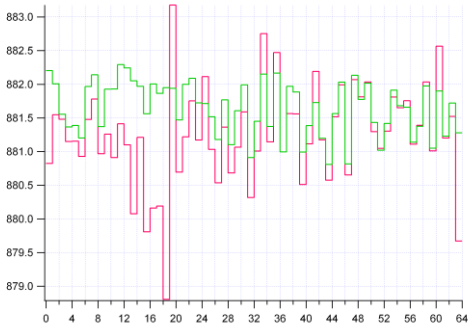




With 4bit-DAC correction:



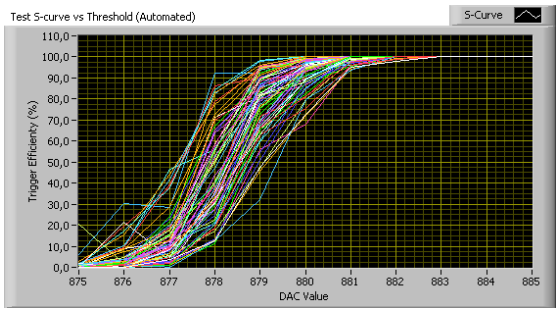


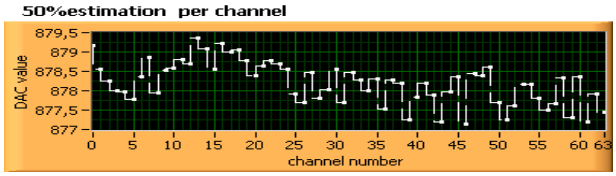


Pedestal wo 4bit DAC correction
V_avg= 881.242;
V_sdev= 0.735335

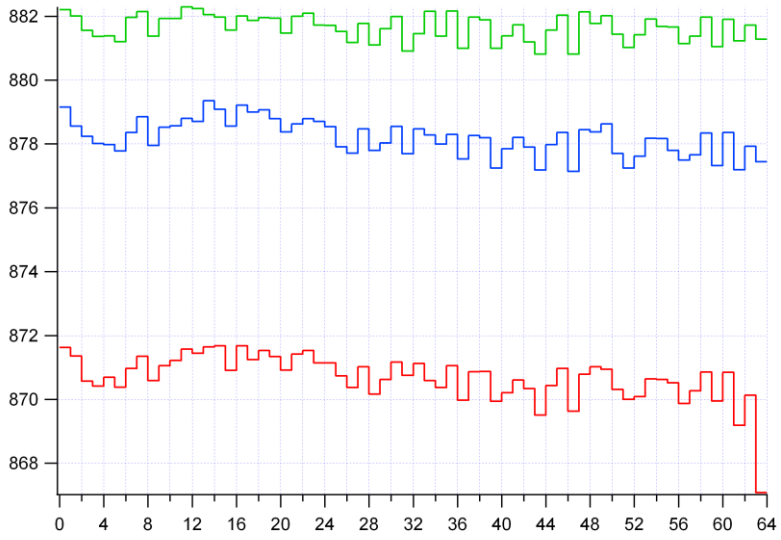
Pedestal with 4 bit-DAC correction
V_avg= 881.644;
V_sdev= 0.397194

7.1.2.Injection of 1fC (HG after 4 bits DAC correction)

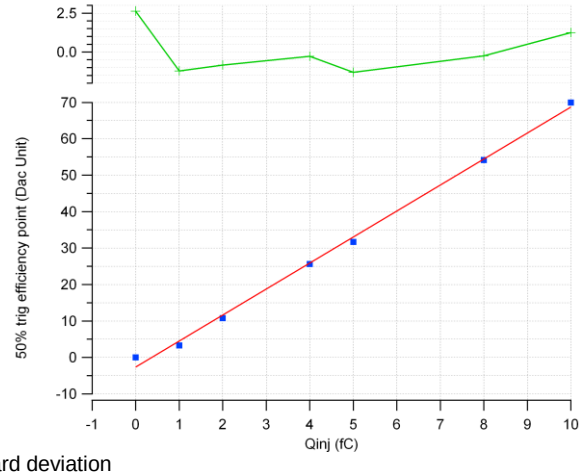




0, 1fC, 2 fC



50% efficiency vs Qinj:



Coefficient values ± one standard deviation
a =7.1299 ± 0.175
b =-2.6274 ± 0.958

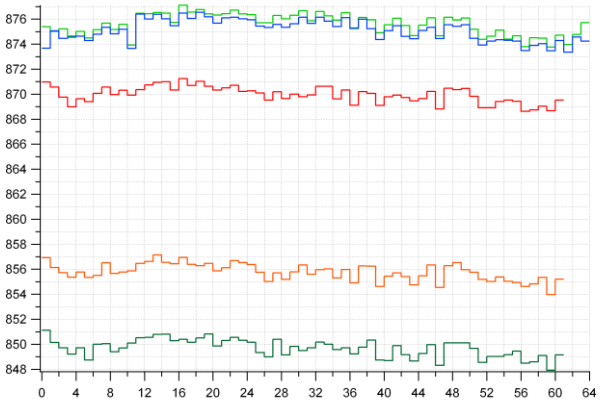
7.13 DacU/fC

Minimum possible threshold = 1 fC which corresponds to the 5σ noise. (Noise= 0.2fC or 1250 e-)

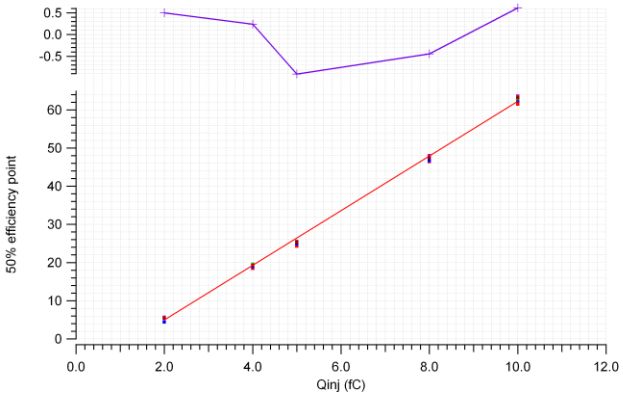
7.2. With Cd=88 pF

	Qinj=10 fC	*Qinj=100fC*	*Noise*
Sw= 10	-101.2 mV, 168 ns	*1.05V, 168 ns*	*sdev= 3.55mV (equiv. to 0.35 fC)*

pedestal, 1fC, 2fC, 4fC, 5fC



50% efficiency point vs Qinj:



Coefficient values ± one standard deviation (avec Cd=88pF)
a=7.1561 ± 0.118
b=-9.3565 ± 0.765

7.15 DACU/fC

Minimum possible threshold = 2 fC which corresponds to the 5σ noise (Noise=0.4 fC or 2500 e-)