HARDROC/MICROROC

SOFTWARE & TEST BOARD USER GUIDE

Version: 11 May 2015

Abstract

HARDROC and MICROROC are 64-channel front end ASIC dedicated to the read-out of gaseous detectors (respectively RPCs and Micromegas). The chips have the same pinout as they are quite similar but they don't handle the same dynamic range: 2fC up to 500 fC for MICROROC (dedicated for MICROMEGAS or GEM detectors), 20fC up to 20 pC for HARDROC.

The software developed is therefore common for HARDROC and MICROROC and this guide explains how to install & use the test board for HARDROC or MICROROC and how to operate with the associated software.

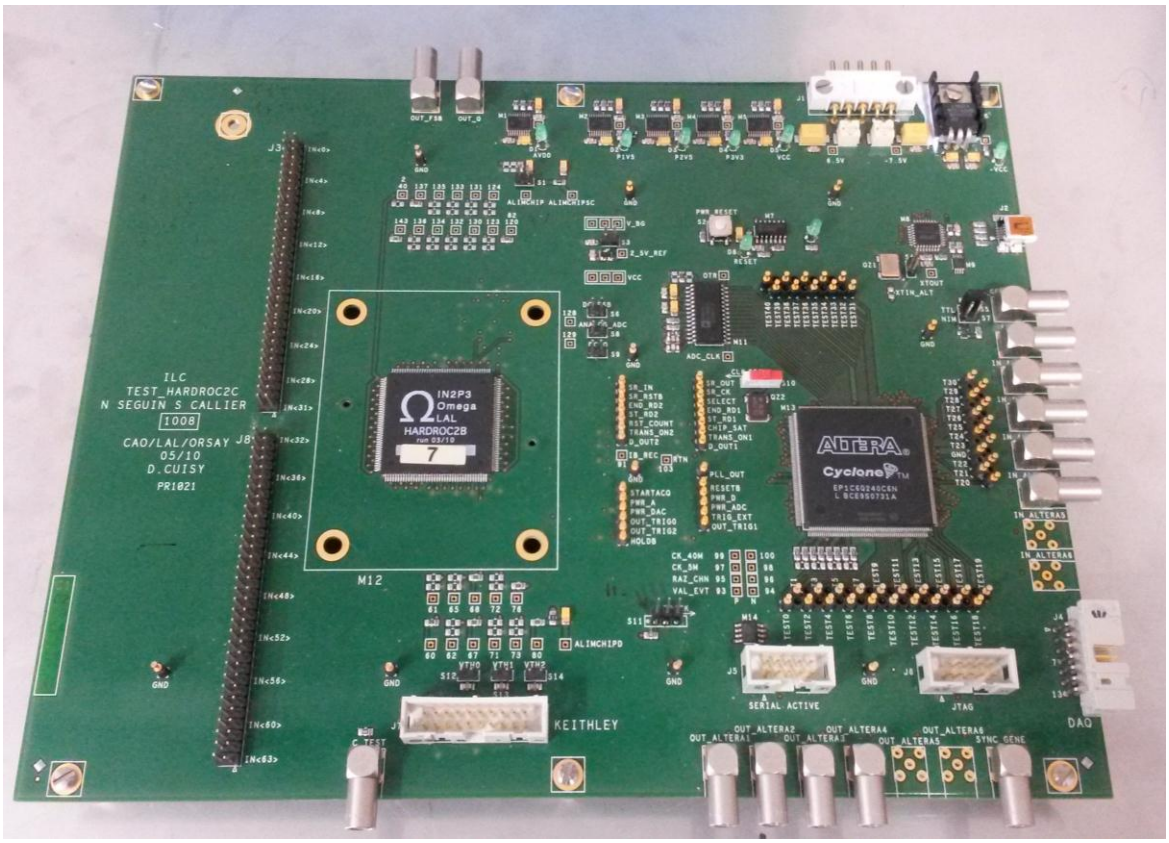


Table of content

1. Installation & Test of the Test Board

1.1. Pre requisites

The use of this PCB requires:

- A computer (windows OS) with USB connection
- A USB-A to mini-USB cable
- LabVIEW software version **2010** or later (*note that only **32-bit** version is supported*)
- A dual-output power supply (delivering 400mA for positive supply ***+6V*** and 100mA for negative supply ***-7V***)

1.2. Installation guide

Before connecting the board and running the LABVIEW software, the user has to follow some steps:

1. The user has to create the following folder : **C:\DATA\DRIVERS\FTDI**
2. He/she has to download the driver of the **FT245B**[1] and unzip the file inside this folder.
3. He/she has to install in few steps the **LAL_USB** [2] package (software setup application). This will also install the **Test245** software and add a shortcut on the desktop.
4. He/she has to power and connect the test board to his/her computer through the USB cable, and then the computer will ask for the test board driver. The user has just to indicate the folder in which he/she unzipped the file previously mentioned: **C:\DATA\DRIVERS\FTDI.**
5. During the LabVIEW installation, the user has to select and install the **NI VISA** package.
6. Then, the user must install the latest **NI IVI Compliance Package (ICP)**[3].
7. He/she has to install the **Keithley 2000 Driver (IVI version)**[4] for LabVIEW. Note: This tool is needed even if the user does not use this material.
8. He/she has to install the **Agilent E3631A (IVI version)**[5] for LabVIEW. Note: This tool is needed even if the user does not use this material.
9. He/she has to launch **National Instrument Measurement & Automation Explorer**, select in the **Tools** menu, **NI-VISA**, then **VISA options**, and in **passport**, he/she has to enable **NI-VISA Tulip**.
10. He/she has to launch the program **Test245**: This will check if the USB device (the test board) is well recognised. *This program has to be run prior using the LabVIEW software if the test board power supply has been switched off.*

[1] Available at http://www.ftdichip.com/Drivers/D2XX.htm
[2] Available at http://lalusb.free.fr/software.html
[3] Available at http://www.ni.com/ivi/ivi_prod.htm
[4] Available at http://www.ni.com/devzone/idnet
[5] Available at http://www.ni.com/devzone/idnet

Figure 1 show results when a test board has been found. Device Description and Serial Number are displayed and surrounded by a red circle. These 2 parameters have to be provided to the LabView software for a proper operation.

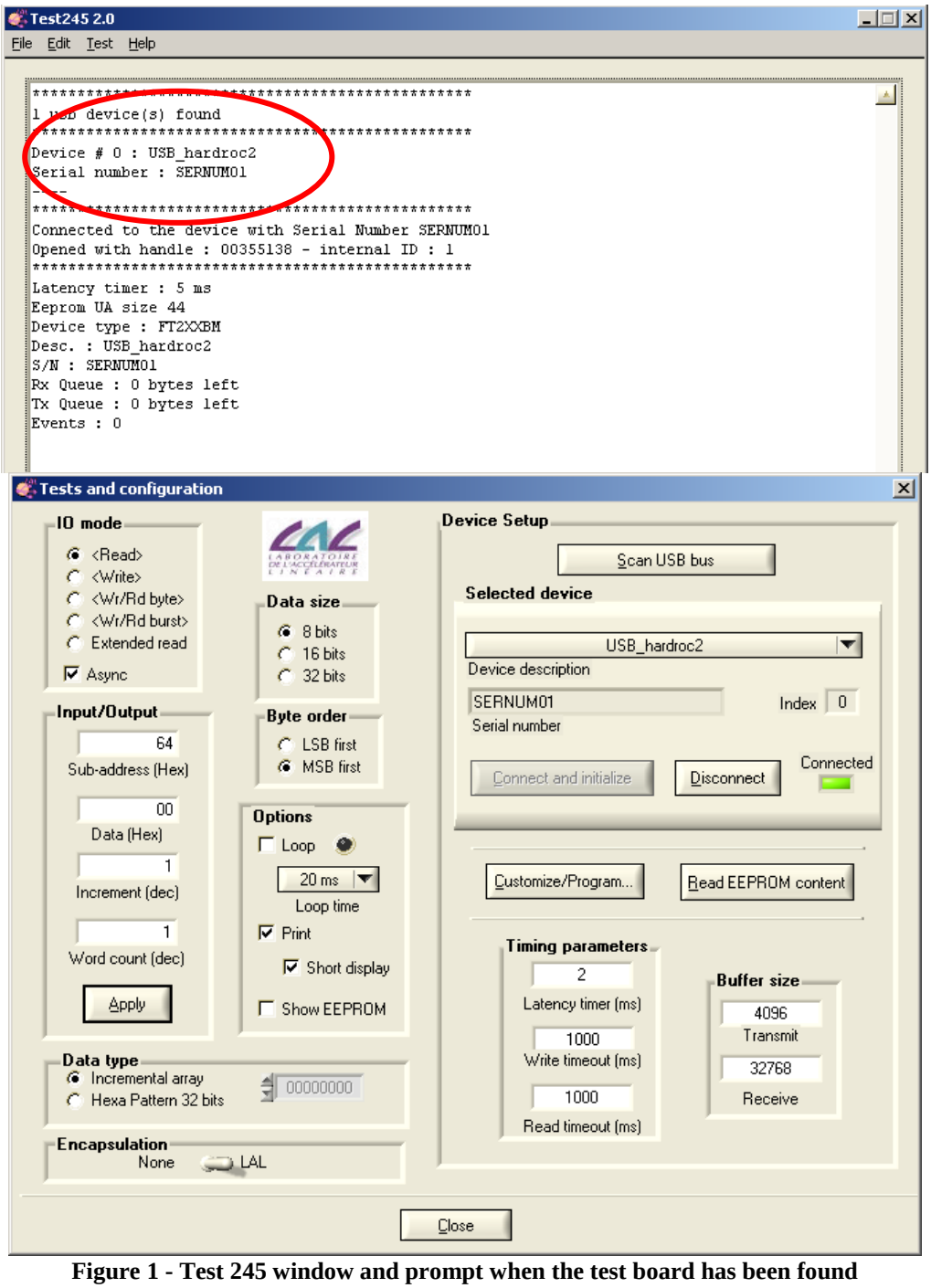


Figure 1 - Test 245 window and prompt when the test board has been found

2. PCB presentation

The test board has mainly been developed to allow characterization and debug of the ASIC HARDROC/MICROROC. Some features were added on the PCB or in the firmware/software to allow its use with real detector or within an experiment. The schematics of the PCB, the firmware and software sources are provided, thus, users can modify anything to fit their own requirements.

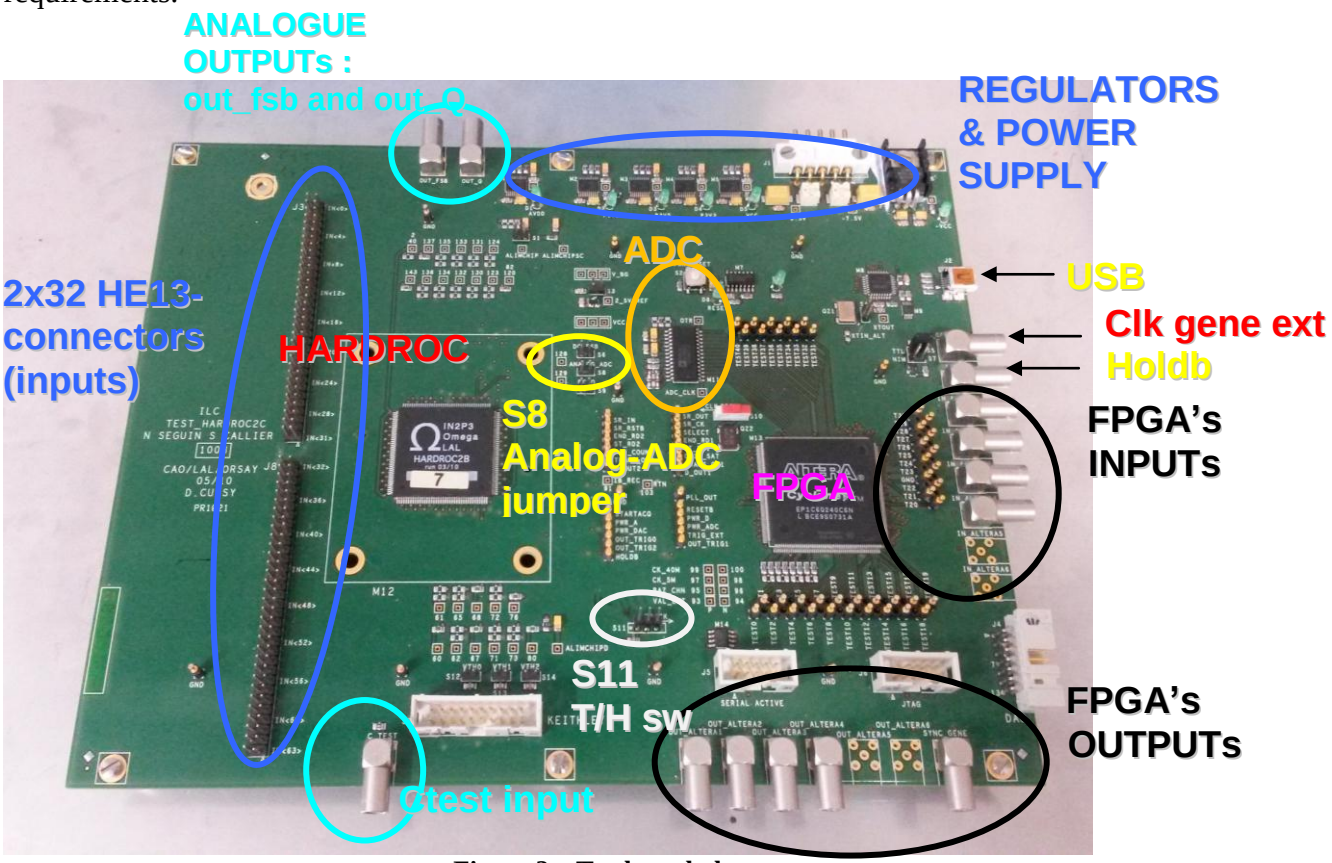


Figure 2 – Testboard photo

- The PCB allows easy access to each HARDROC/MICROROC's pin, as all the analogue pins are connected to "square" holes (where the pin number is written on the silkscreen layer) and as all the digitals I/Os are connected to probes between the ASIC and the FPGA.
- Many test points are also connected to the FPGA, outputting digital internal nodes.
- The 3 OR64 trigger signals outputs are available on LEMO connectors
- 2 analogue buffers provide ASIC's analogue outputs on LEMO connectors: out_fsb for the output of the fast shaper (0, 1 or 2) and out_Q for the output of the charge (analogue memory after the slow shaper).
- 1 external ADC is on-board, allowing ASIC data acquisitions. A jumper must be put on S8 to send the analog output to the ADC as well as on S11 to select the "Hold" position.

Note that HARDROC/MICROROC power consumption can be monitored on connector S1 as a 10 Ω resistor is inserted in series with the power line.

3. The Software

To start the test board you need to:

1) Provide power supply to the PCB
2) Connect the USB cable from the PCB to your Computer where software is running
3) Start the software

When this software is launched, the number of devices detected is displayed, and no error should occur, meaning that the installation has been successfully achieved. The USBid number should be changed to 1.

4) Select the chip soldered/used on the board you have (HARDROC2/HARDROC2B/MICROROC)
5) Then you can transmit the slow control to the ASIC, the LED should turn to green, showing that the ASIC was well configured.

If crash occurs, restart the procedure and check both USB cable and Power Supply. Ensure also that a 40 MHz clock is well provided to the FPGA by checking the status of the LED (D7). Whenever no light is emitted, remove the on-board switch (S10) from the "CLK OFF" position.

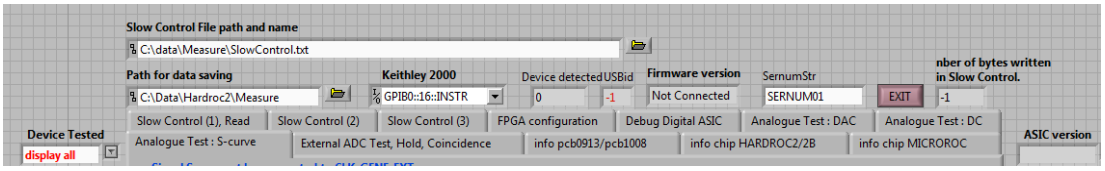


Figure 3 - Setup entry cells (Inputs: white boxes, Outputs: grey boxes)

Note that the Firmware Version is automatically detected by the software. When bugs are discovered, either the firmware or the software (or both) is (are) corrected. Please visit our website http://omega.in2p3.fr , in the download centre area, to check the available updates. If update of the software is very simple (only download and replace the old one), the update of the firmware requires an external bundle. Indeed update is performed by an ALTERA "USB Blaster™" connected to the connector "Serial Active" (for definitive programming) or "JTAG" (for temporary update, until power supply is shut down).

3.1. Informative pages

To avoid the need of many papers, datasheets, applications notes and so on, three informative front pages have been added to provide useful information concerning the chip pinout and the PCB, its connectors and tests points.

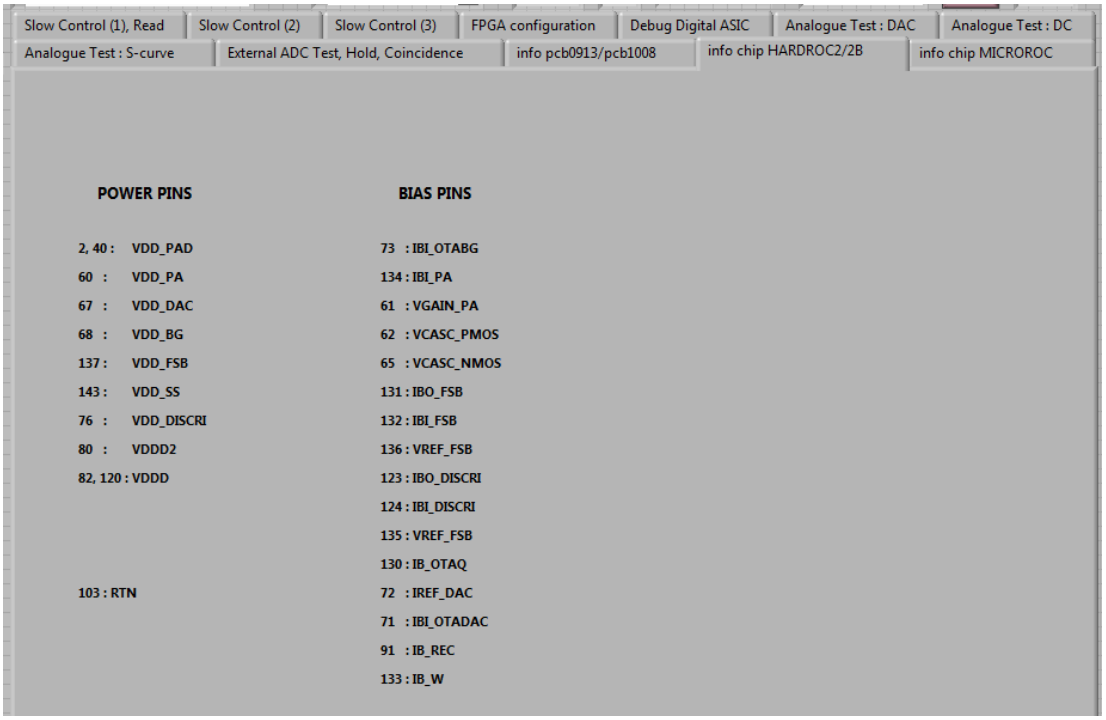


Figure 4 - Chip informations page

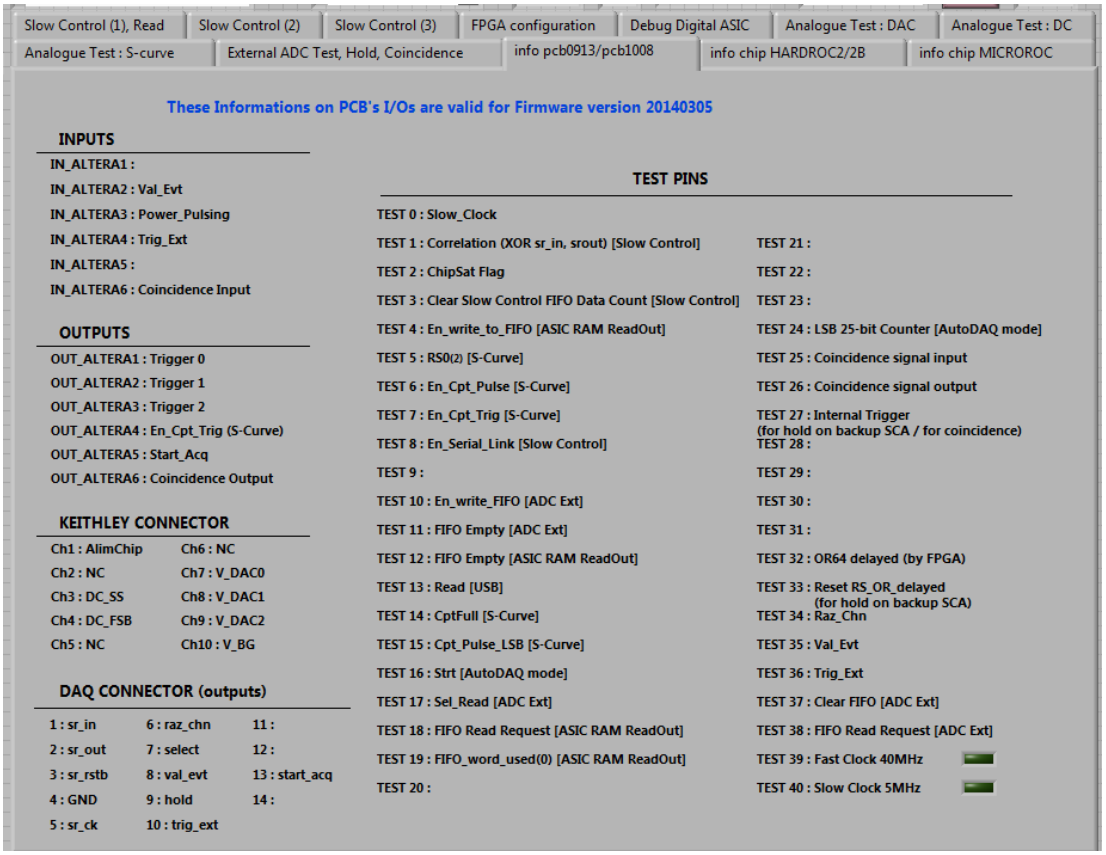


Figure 5 - PCB information page [connectors + FPGA I/O + Test points]

3.2. The slow control pages

All the slow control parameters of the HARDROC/MICROROC are displayed on these 2/3 pages, allowing tuning & tests of different settings. (Pink for Hardroc2, blue for Microroc)

To program the ASIC, just click on the "Transmit Slow Control" button. A front page indicator displays the status of this SC register and should be green after a "Transmit SC" command. This SC register can be reset by the "Reset Slow Control" order.

The settings of the front pages can be saved in a text format file thanks to "Save -> File Slow Control" button, and reloaded from this file by the "File -> Load Slow Control" command. This is very helpful as there are more than 500 slow control bits! Note that the path & name for this file has to be provided in the cell of the setup entry. Refer to the datasheet to know the meaning of every individual bit!

Depending only on the Slow Control configuration (preamplifiers, fast shapers, 10-bit DACs discriminators mask and RS_or_discri, RazChnExt, RazChnInt) and on the Pwr_On, Val_Evt & Raz_Chn commands, the triggers should be immediately available on the 3 OR64 outputs after the transfer of the slow control.

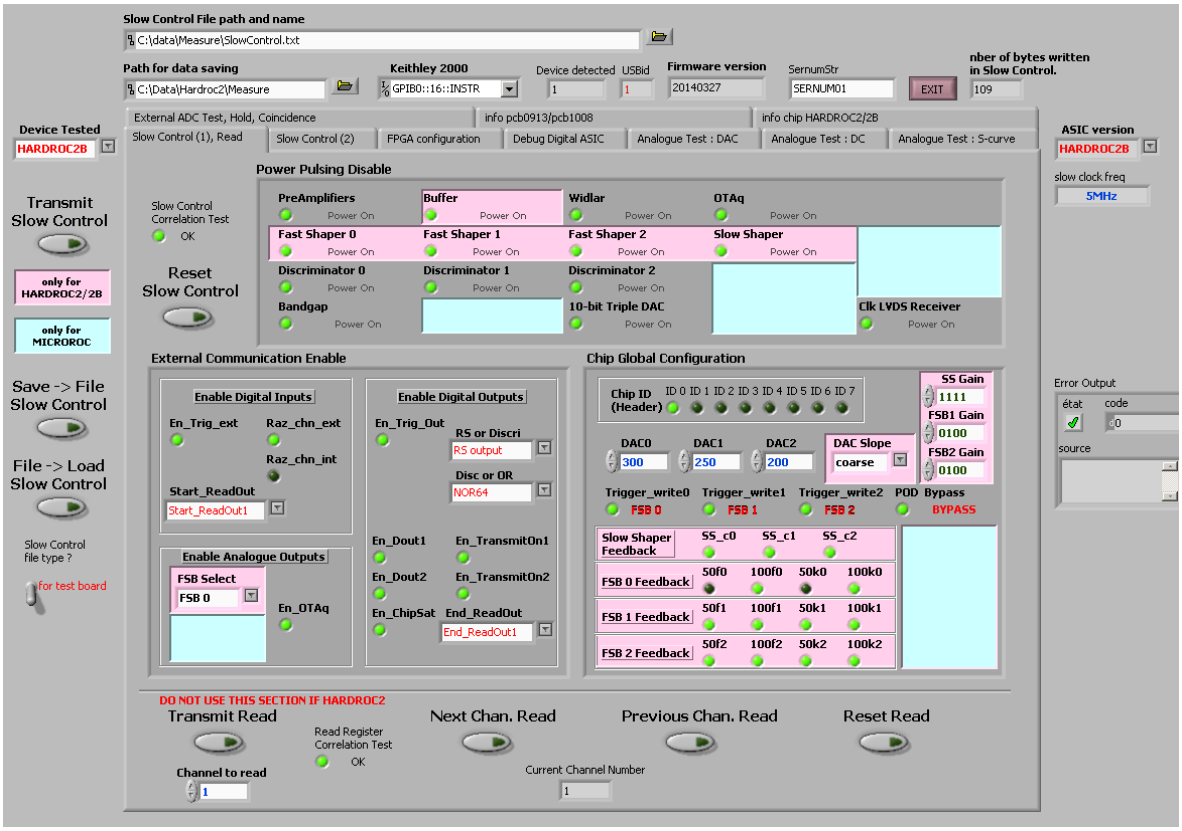


Figure 6 - Slow Control page (1)

On “Slow Control (1)” and “Slow Control (2)” pages, some settings are individual for each channel (Test Capacitance & Trigger). A 3-position cursor allows forcing all these control bits active or inactive. For these 2 cases, no matter is the status of the LED inside the box shown close to the cursor. Only the third position (in the middle) takes care of the bits position inside the associated box.

For the 8-bit Gain setting and 4-bit DAC (respectively in HARDROC and MICROROC), the 3-position cursor allow to either have an individual value for each channel, or have a common value for all channel, or have only one channel which has a different value of all other channels.

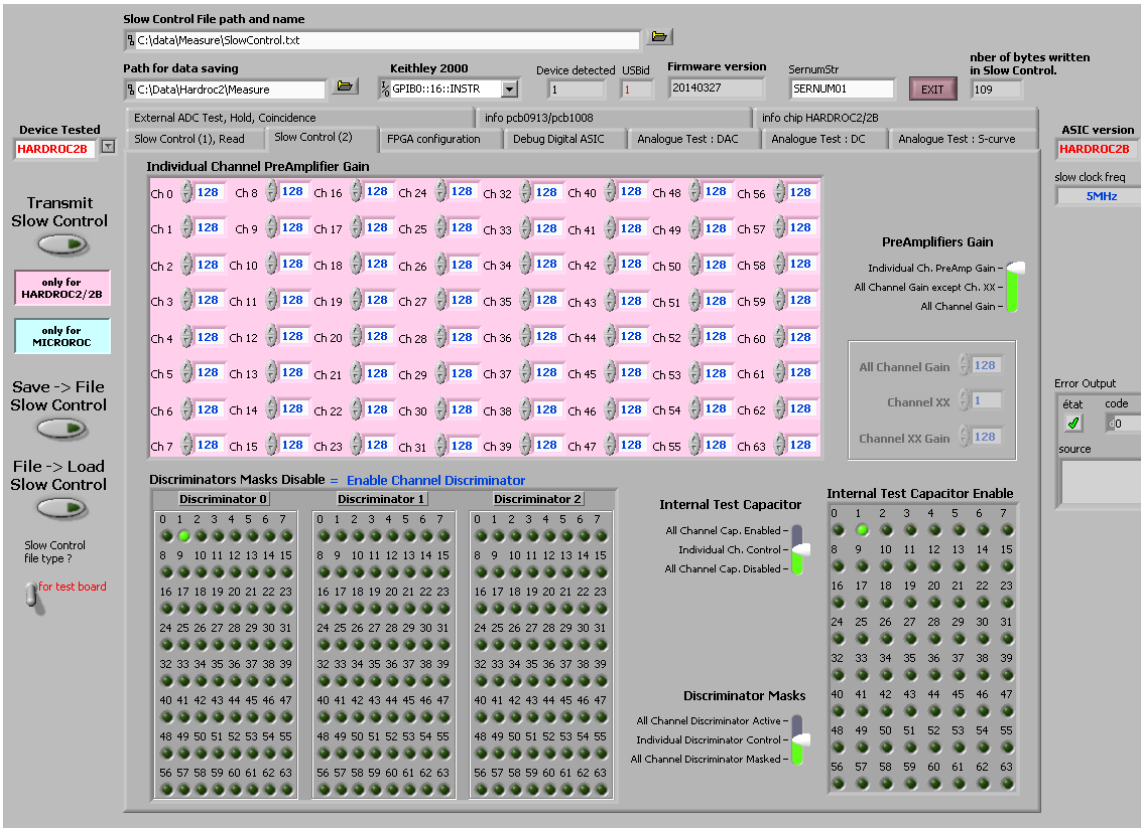


Figure 7 - Slow Control page (2)

Note on the Slow Control configuration / bits meaning:

The *Power Pulsing* bits can/should be left ON, except if user need to power down the stages to save power during dead time.

The DAC Threshold and the shaping time can be changed in the *Chip Global Configuration*, as well as the OR64 allowed to write in the memory during Data Acquisition.

The *External Communication Enable* is focused on the I/Os used by the ASIC. Most of the settings can be left as default values are for both analogue display and digital readout of the ASIC except few. The “Raz Chn Int” signal must be basically enabled for digital acquisitions, and disabled for displaying the triggers. The “RS or discri” should be set to RS during digital acquisitions and set to discri in order to get the trigger not latched by the internal RS cell. Note that advanced users can manage by themselves the behaviour of this RS cell using the external “Raz Chn” (which should hence be enabled in the Slow Control).

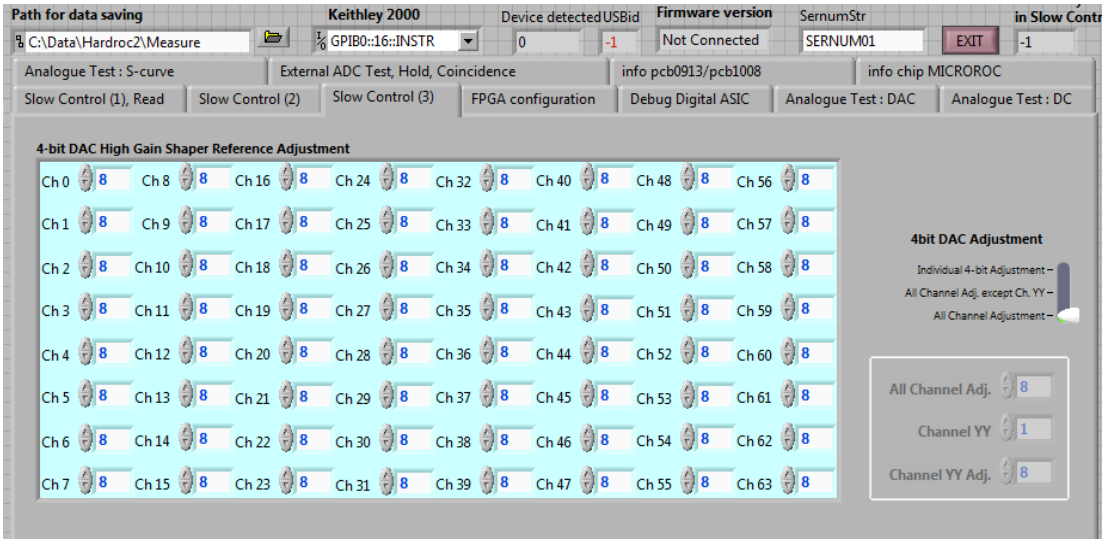


Figure 8 - Slow Control page (3) for MICROROC

Refer to the datasheet to know the effects of all of the "Slow Control" bits.

Note that LabView allows choosing the start-up values, which is achieved by the "Make Current Values Default" command in the Edition/Tools/Execution Menu. You can save your preferred values thanks to this feature. The Load/Save option is preferred to this method.

3.3. Bias voltages

When the testboard is powered for the first time or when the board is not working properly, the user should check with a multimeter the bias voltages on the test points available on the testboard (and provided in the informative page shown in Figure 4). The power supplies (pin 2, 40, 60, 67, 68, 76, 80, 82, 120, 137) must be equal to ~ 3.3V.
The approximate expected values are listed below. Before doing this test, the SC parameters must be sent using the Labview Program.

Pin	*Pin Name*	*Pin Type*	*DC Measurement*
61	vgain_pa	Analogue Bias	2.8 V
62	vcasc_pmos	Analogue Bias	1.0 V
65	vcasc_nmos	Analogue Bias	1.5 V
70	v_bg	Analogue Output	2.5 V
71	ibi_otadac	Analogue Bias	0.8 V
72	iref_dac	Analogue Bias	0.4 V
73	ibi_otabg	Analogue Bias	0.5 V
77	vth2	Analogue Output	Depends on SC
78	vth1	Analogue Output	Depends on SC
79	vth0	Analogue Output	Depends on SC
123	ibo_d	Analogue Bias	2.5 V
124	ibi_d	Analogue Bias	0.8 V
128	out_fsb	Analogue Output	DC = 2.2 V
129	out_q	Analogue Output	DC = 1 V
130	ib_otaq	Analogue Bias	0.9 V
131	ibo_fsb	Analogue Bias	2.3 V
132	ibi_fsb	Analogue Bias	2.5 V
133	ib_w	Analogue Bias	0.8 V
134	ibi_pa	Analogue Bias	0.65 V
135	vref_ss	Analogue Bias	1.1 V
136	vref_fsb	Analogue Bias	2.2 V

3.4. The read page (bottom of Slow Control page 1)

The "Read Register" is a shift register which allow outputting sequentially the analogue hold data from the Analogue Memory (SCA) (OUT_Q) and shaper output (OUT_FSB) to pins 129 and 128 (also buffered on LEMO connectors and DC level monitored on S9 & S6 respectively). This register is controlled either manually by the 4 buttons (read ch., next ch., previous ch. and reset register) on the bottom of this page or automatically by the software during acquisition using external ADC.

The fast shaper output is directly displayed on the shaper output of the chip, once a channel was selected, no other command is requested.

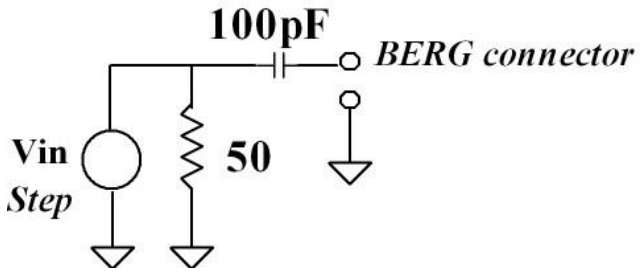
A hold signal has to be provided to the board at the maximum signal of the charge, and the switch S11 has to be set on the "HOLDB" mode, otherwise, no hold is performed on the analogue memory. The "TRACK" mode is only useful for debug. Note that display shown using that mode does not indicate the maximum value of the charge, as internal buffers have low biasing current for saving power consumption and thus slow down the signal displayed. Note that, as the polarity of this signal was changed on MICROROC with respect to HARDROC, the switch in track position for MICROROC is an always hold command.

Note that in order to see the Triggers from the chip, "Raz_Chn_Int" has to be disabled and "RS_or_discri" has to be set on discri in the Slow Control. AutoDAQ has to be disabled too.

Note also that the direct individual triggers can be displayed, this requires to use this Read Register and have the Slow Control setting "Disc_or_OR" set to "Read Ch. Discri" instead of OR64.

3.5. Setup to inject signals

First tests to be more familiar with the board and the software should be done using the following setup. A negative voltage step can be injected in one channel through a 100pF capacitor in series with the signal. A 50 Ω resistor for the cable adaptation is also necessary. A specific cable with a female "BERG" female connector can be "homemade" to inject in each individual channel using the input connector which is a male HE13 - 2x32pins. A 1mV-step in 100pF simulates an injected charge of 100fC.



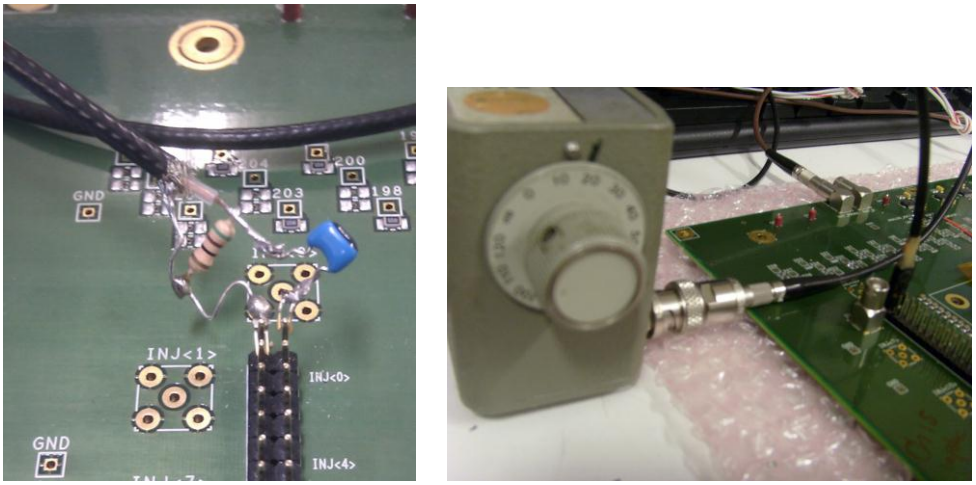


Figure 9 – Injection in one channel

Another way to inject charges in each channel is to use the Ctest input LEMO which is also available on the testboard. The step voltage is then distributed through the internal 2pF capacitor of each channel. The Ctest capacitor must be selected using the Front panel 2. You should select only one of the Ctest, as the number of selected Ctest impacts the amplitude of the input step signal.

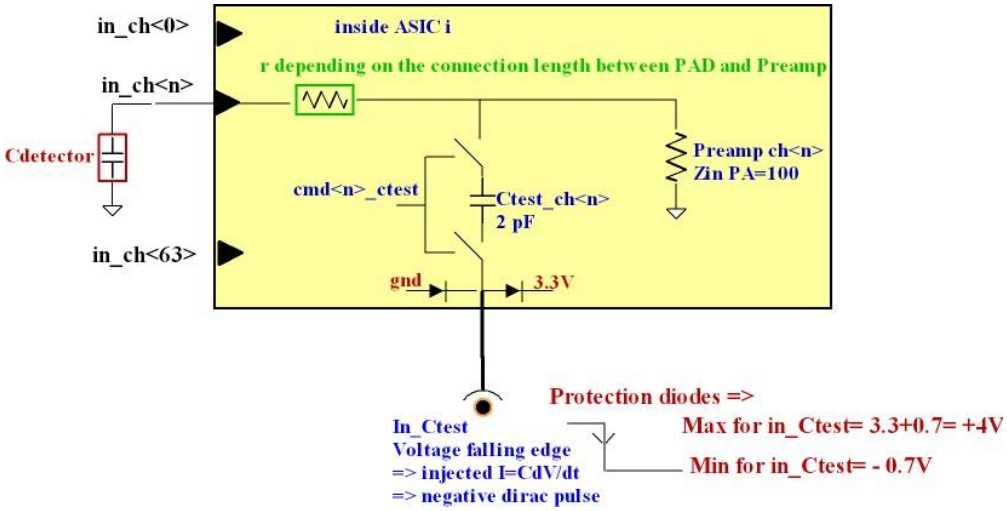


Figure 10 – Injection using Ctest

The waveform of the injected signal is displayed below. Using the 100pF capacitance as injector, 1V@60dB corresponds to 100fC.

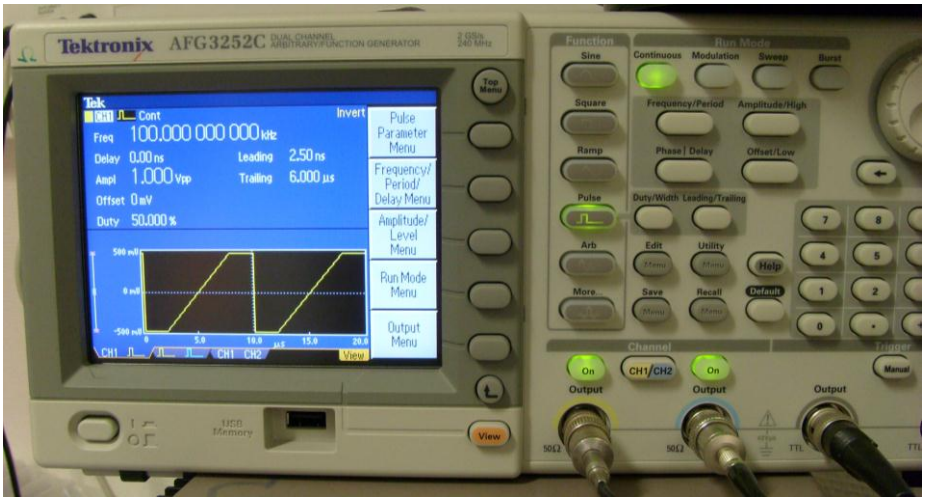


Figure 11 – Injection in each channel

You can then probe the output of the shaper (out_Q=out_ssh) of a selected channel using the "Read" page (Front panel 1) and check the waveform on the scope. The waveforms displayed below were obtained when a voltage step injected through the Ctest of channel 1 (See Front Panel 2, Figure 6) and using the shaper SC parameters for the fsb0 and the slow shaper shown in Front Panel 1 (Figure 5).

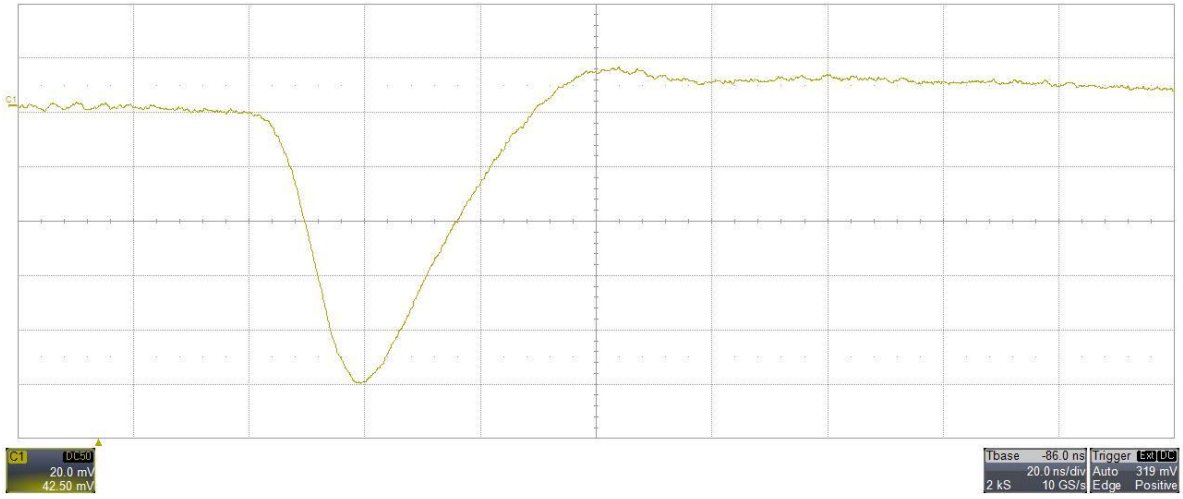


Figure 12 –Fast shaper 0 (fsb0) output: 100fF, 100K ON, 1V@26dB in Ctest

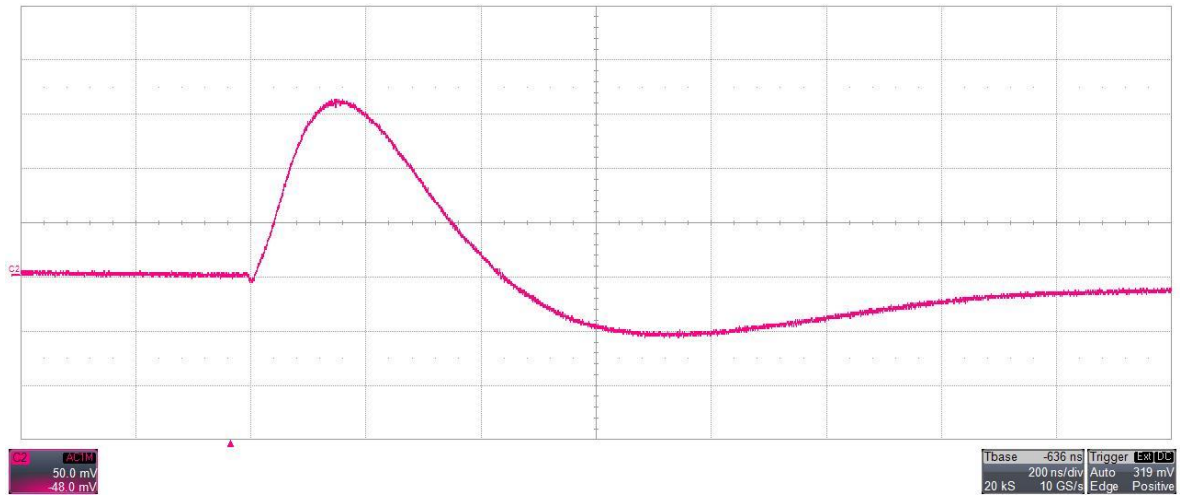


Figure 13 –Slow shaper (ssh) output: all SS_c_i ON, 1V@6dB in Ctest

3.6. The DAC(s) characterization

The software allows performing a linearity scan on the three Threshold DAC. Data acquisition of the measured voltage has been developed using a Keithley 2000 DMM. GPIB address of this tool has to be provided in the adequate white box, as well as the address where data will be saved.

Maximum DAC tested value has to be provided. Note that name of the saved files are clearly distinctive and no confusion in the resulting files can be seen (ie. DAC0, DAC1 or DAC2).

When a linearity scan is performed on the Threshold DAC0 / DAC1 / DAC2, analogue data is available respectively on S12 / S13 / S14.

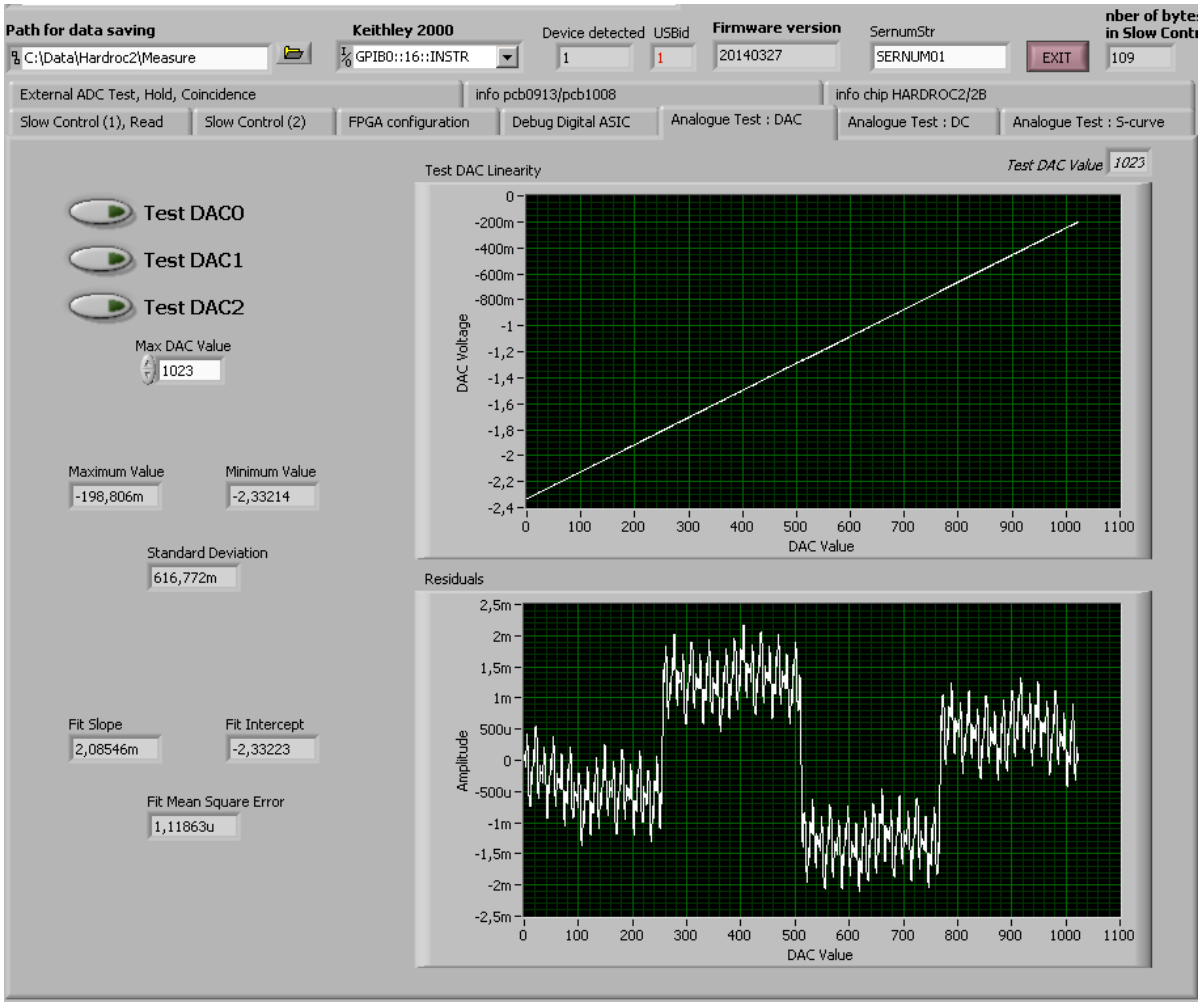


Figure 14 – DAC0 linearity test (coarse mode)

3.7. The S-curve test

The S-curve test is useful to check the trigger efficiency of each channel as well as the uniformity between channels. The dispersion can be then corrected by setting the gain of each preamp which is tuneable over 8 bits (Front panel 2). The trigger efficiency versus DAC code has been automated in this software.

Note that this test requires that the OR64 (of the selected DAC) output is enabled.

As specified on the S-curve page, RazChnInt must be OFF, RazChnExt must be ON and the Latch mode (= RS output) must be selected (Slow Control page 1). You must also specify the 10-bit DAC swing (min and max value).

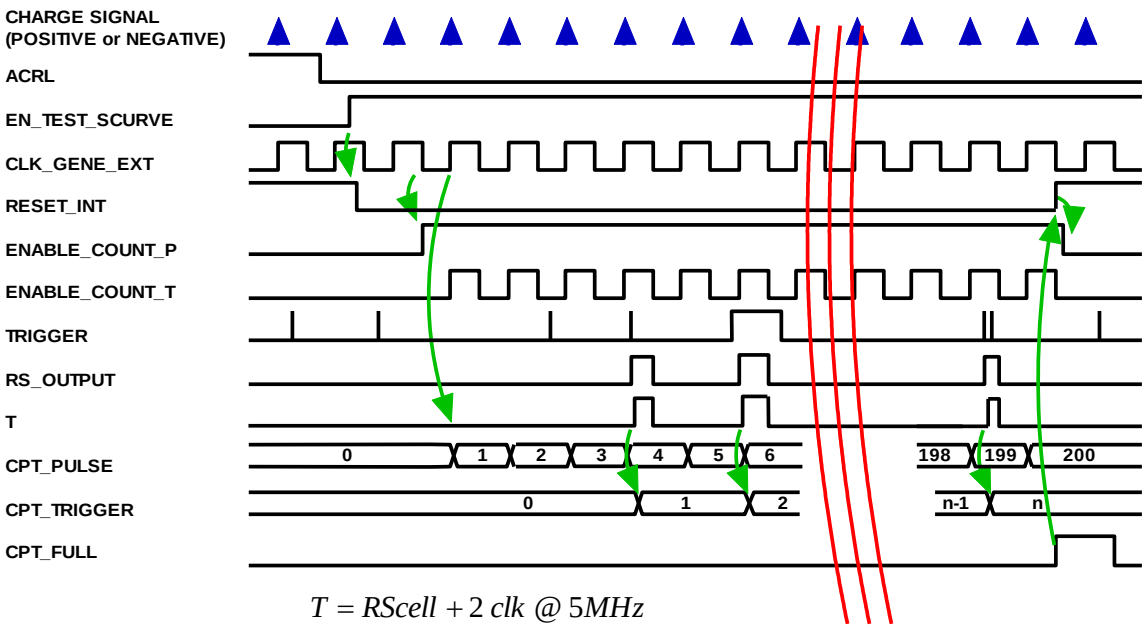
Three small grey boxes allow a live monitoring of the number of injected pulses and of the triggers counted by the FPGA, as well as the current DAC value.

A reference clock must be provided on the CLK_GENE_EXT Lemo connector. For that, a TTL signal must be generated by the channel 2 of your pulse generator, with the same phase and frequency (10KHz-100KHz) as the injected signal generated by the channel 1.

The injected charge must occur more or less at the same time as the rising edge of this clock (Figure 14). Besides, En_count_T (available on a test pin), must also be synchronous with this signal.

The “Single Custom Test” does not change any slow control parameter (no trigger masked, no injector Capacitance enabled/disabled). Triggers occurring while performing this test are due to any channel, depending on your slow control setup. As this test will not perform a loop on all channels, it is a fast test. Final results of this test are displayed on the top right graph.

The test “Scurve Fully automated” allows testing the trigger efficiency channel-by-channel using the Ctest injector. Once the 64 channels have been measured, the final result is plotted on the top right graph, using different colours to distinguish each channel. The injection capacitance “Ctest” and discriminator are automatically activated for the channel under test. The “Ctest” of all the other channels are automatically disabled as well as the corresponding triggers. The currently tested channel and DAC value are displayed in the grey boxes in the middle and right side of the page. The results of the last channel tested are shown on the bottom left graph. After the 64-turn loop is achieved, the final result is plotted on the bottom right graph, using different colours to distinguish each channel.



$$T = RScell + 2\ clk\ @\ 5MHz$$

T is RS delayed by from 200ns to 400ns randomly

Figure 15 - S-curve test working mode

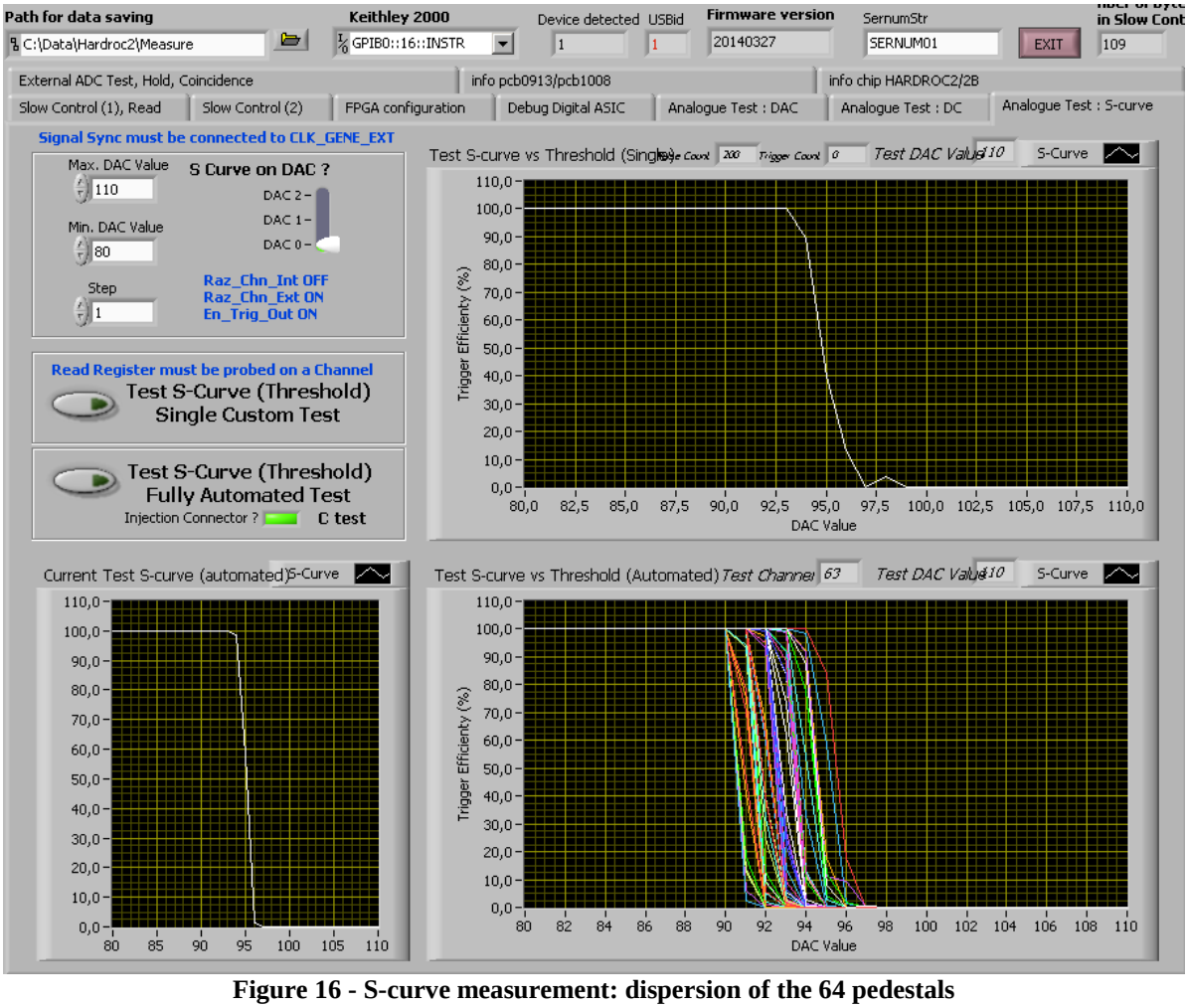


Figure 16 - S-curve measurement: dispersion of the 64 pedestals

3.8. External ADC acquisition

HARDROC/MICROROC has one analogue output, which can be digitized using an external ADC (AD9220 from Analog Devices embedded on the testboard).

This tool is the only "experiment oriented" test. Indeed, all the other tests are only useful for the characterisation of the HARDROC/MICROROC chip, whereas this one allows acquiring data, with a detector connected to the board for physics analysis.

A jumper must be put on S8 to connect the ASIC output to the ADC input.
A jumper must also be put on S11 (track/Hold switch) to set it in the hold mode.

Note that the hold command must be provided. This signal can be delivered externally by injected an HOLDb (active Low for HARDROC / active High for MICROROC) signal through the dedicated LEMO connector (see Figure 2). It can also be provided by a delayed OR64 Trigger signal or be supplied by a delayed coincidence trigger signal (coincidence between internal OR64 and external signal). The hold command should arrive at the maximum value of the analogue charge (corresponding to the peaking time).

The following example illustrates the case you have chosen an external Holdb signal (active low signal for HARDROC): this holdb signal has been provided by the Ch2 of the pulse generator and the delay between the injected signal (Ch1) and this Holdb signal has been tuned manually (this delay is about 110ns when all the SS_ci slow control parameters of the slow shaper are set ON as shown on Panel 1). This delay optimization can be made on the scope, visualizing the "out_Q" output (= out_slow shaper of the chosen channel).

If you choose the delayed OR64 Trigger signal to provide this Holdb signal, the RS_or_discri slow control parameter must be set to "Discri" (Panel 1). Note that, in that case, a hold scan can be directly performed by the software to find the optimized delay.

The result of live acquisition is shown on the top right part of the page: for each channel, the converted value is displayed. The "Out of The Range" (OTR) signal is not monitored on the screen but saved in the file. However, this should never occur, as data coming from the chip are within the dynamic range of the external ADC.

The histogram shown on the left corresponds to the results of the channel you have specified in the "ADC Channel?" field.

This test is not very fast, and it is recommended to clean the folder where the files are saved before each acquisition as a large number of saved files slows significantly the software.

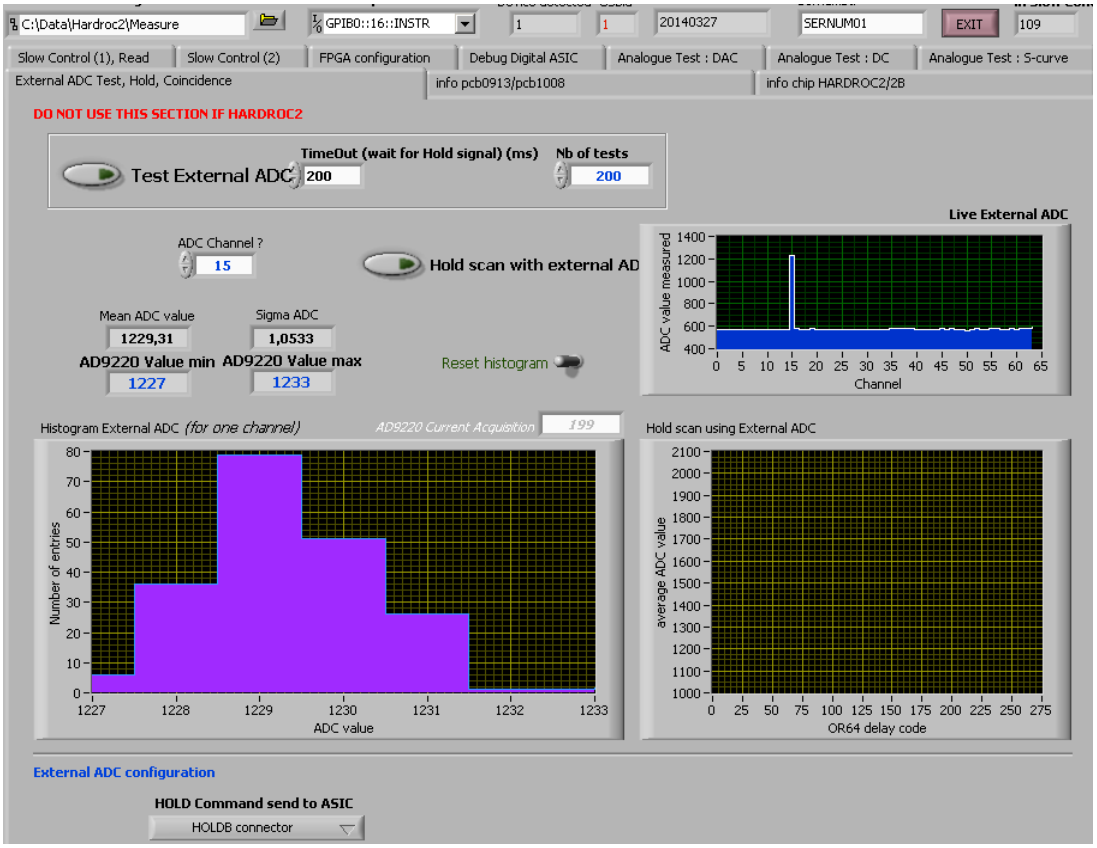


Figure 17 – External ADC test using an external Holdb
with a 1V step signal injected through Ctest (Ch15) - Vth0 =150 DACUnit

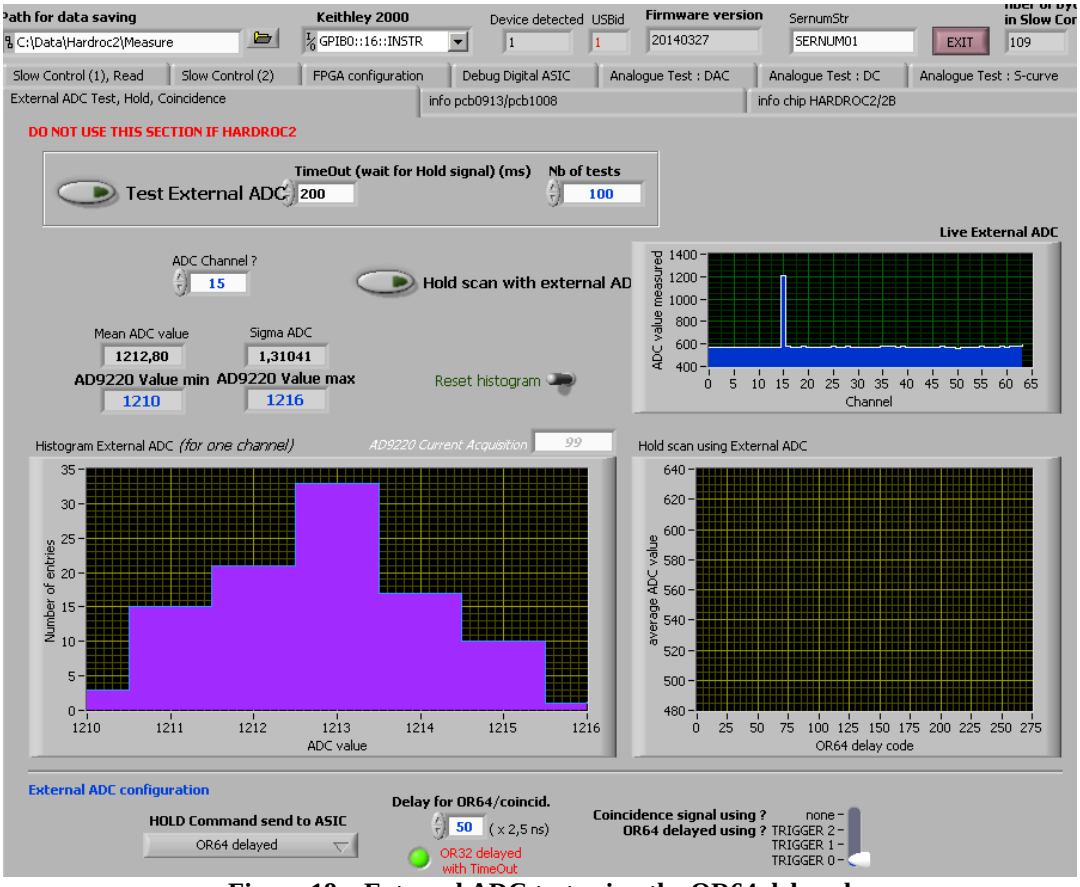


Figure 18 – External ADC test using the OR64 delayed
with a 1V step signal injected through Ctest (Ch15) - Vth0 =150 DACUnit

After launching the test (by clicking on the “Test External ADC)” command), the FPGA wait for the specified time. If a hold command is provided, then the automate will start the following sequence: reset of the read register (if enabled in external ADC configuration page, recommended), then set the channel 0 on the output, then digitize it, then switch to channel 1, then convert it, and so on until last channel (channel 63). Digital data are sampled by the FPGA and saved to a build-in FIFO.

On the screenshot below, analogue output is displayed in yellow, and digitized data in the software fit well with the data on the scope. In this case, channel 0 received an injected charge.

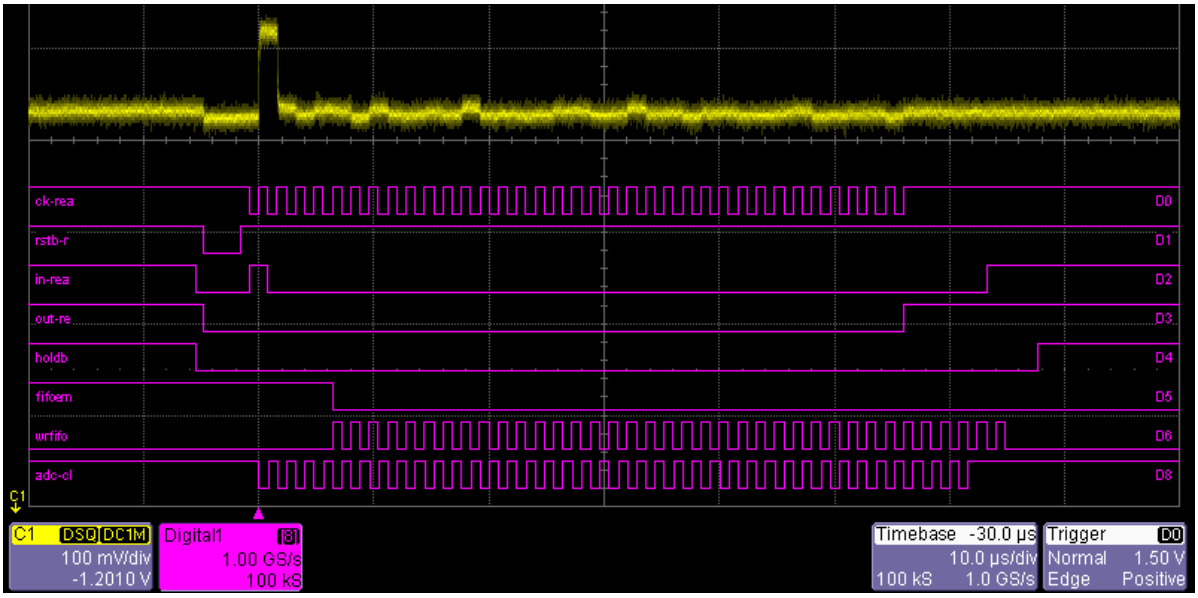


Figure 19 - Scope screenshot of an External ADC acquisition

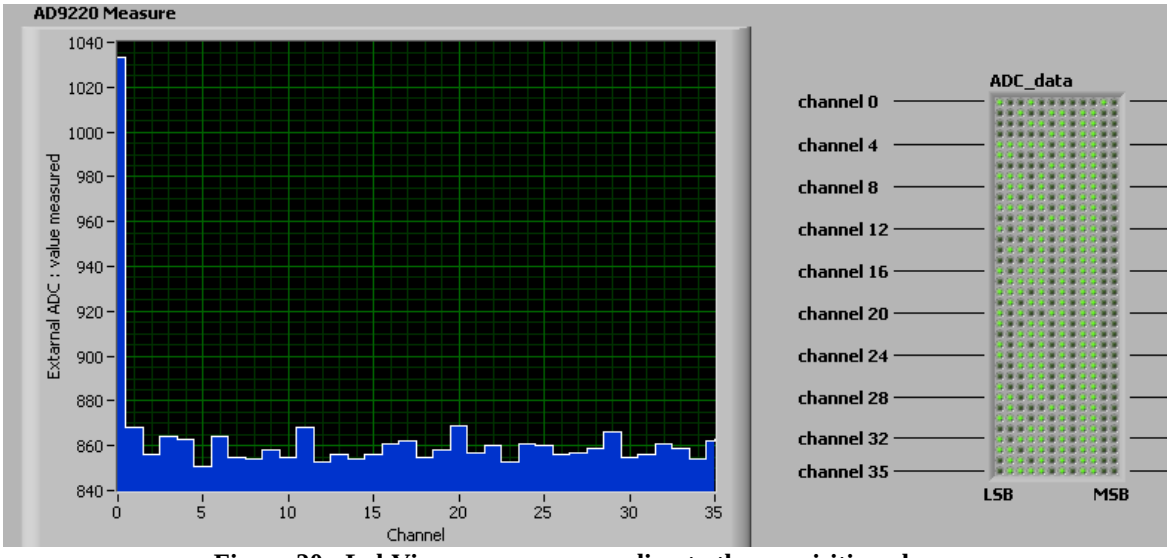


Figure 20 - LabView page corresponding to the acquisition above

3.9. The FPGA configuration page

This page is essentially used for the configuration of the board.

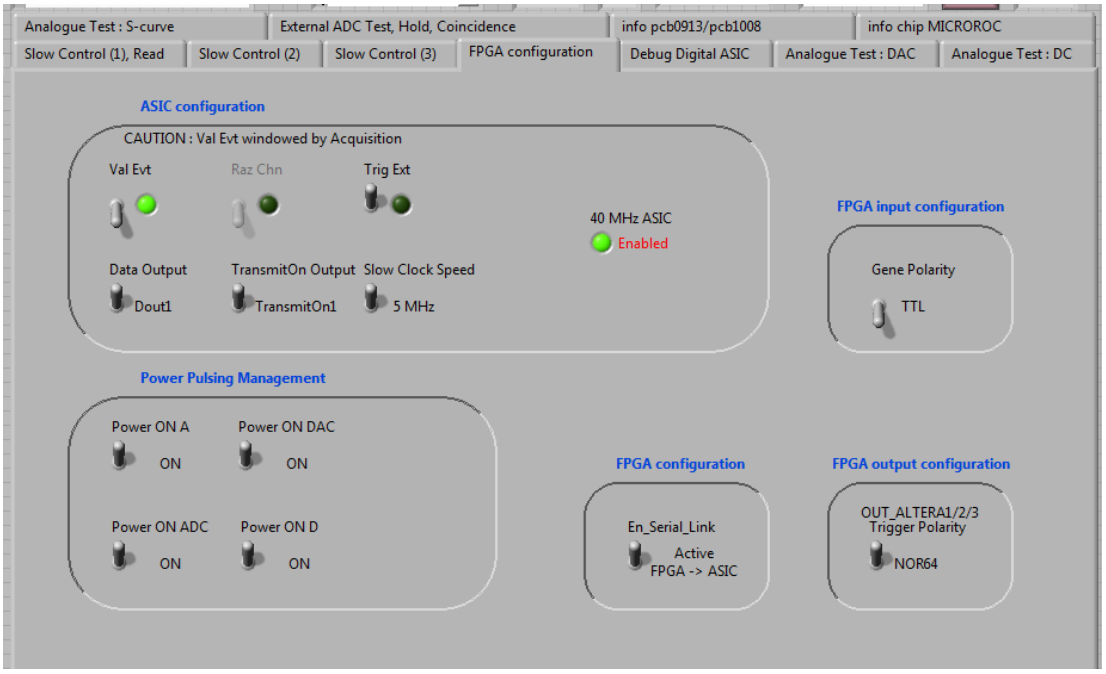


Figure 21 - FPGA configuration page

On this page, the ASIC configuration can be changed depending on the signals displayed on this panel. The setting for some signals is displayed by a LED: a green LED on the front page corresponds to a logic "1"/ON (example: "Val_Evt" or "Raz_Chn").

When the switch of the Power_ON bit is set to "High", the PWR_ON pin of the ASIC is set to logic 1. Otherwise, when this bit is set to "Low/In_altera3", data presented to the PWR_ON pin is the same as data provided to IN_ALTERA3 LEMO connector. If nothing is connected, the PWR_ON pin is tied to logic 0.

3.10. The Digital ASIC page

This page is useful to perform digital acquisitions using the digital part of the ASIC. Two modes are available. In any case, the user has to specify the clock used by the ASIC, which will be used as time tagging reference. It can be either the FPGA internal one (5 or 2.5 MHz) or external clock provided by the user (low down to 300 kHz and up to 5 MHz), in that case, the user can control the phase of the injected charge with respect to the clock. Note that in that case, in order to get the correct time tag in second, the user has to provide the frequency used to the software.

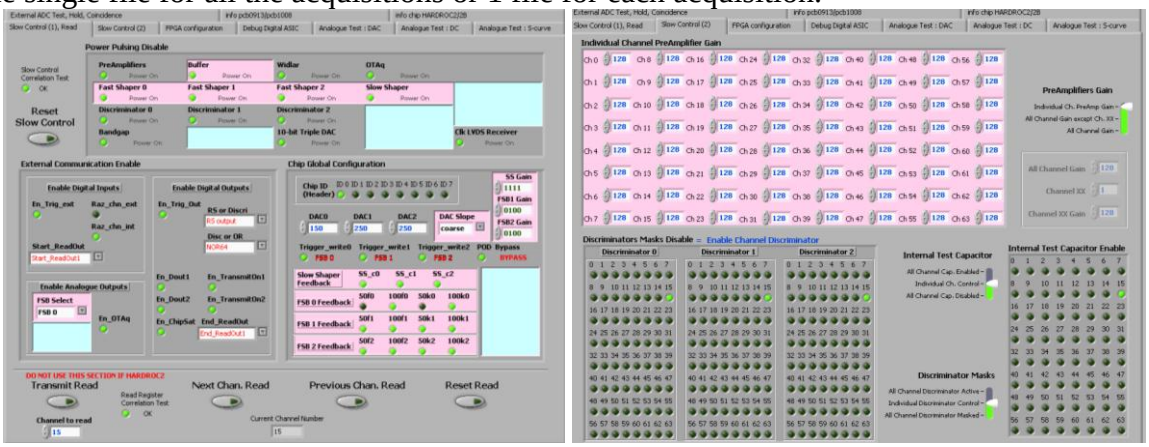
The chip must be properly configured in order to acquire data with the digital part: in the Slow control panel 1, the "Raz Chn Int" must be enabled and "RS or discri" mode must be set to "RS". Moreover, the user must be sure that the settings in Panel 2 are well configured (Masks, Threshold).

A “manual” Data Acquisition system can be used (ie. “Automatic DAQ” is not selected). Each buttons are available for a step-by-step control of the digital part of the ASIC. Refer to HARDROC/MICROROC datasheet to understand the full working mode of these ASICs.

Basically, when the acquisition is started, data (= triggers which may occur) are stored in the internal RAM of the ASIC. The acquisition must then be stopped and after that, the ReadOut Sequence can be started.

An automated DAQ is also available. When using this mode, the user needs to provide the number of acquisitions and then start the test. Note that it is recommended to erase previous data before taking a huge amount of data, as LabVIEW is slowed by the number of files written on the Hard Disk Drive.

Digitized data are displayed in the software (raw data, decoded data with either the BCID or the absolute time referring to the clock used) and saved to files. The user can choose either one single file for all the acquisitions or 1 file for each acquisition.



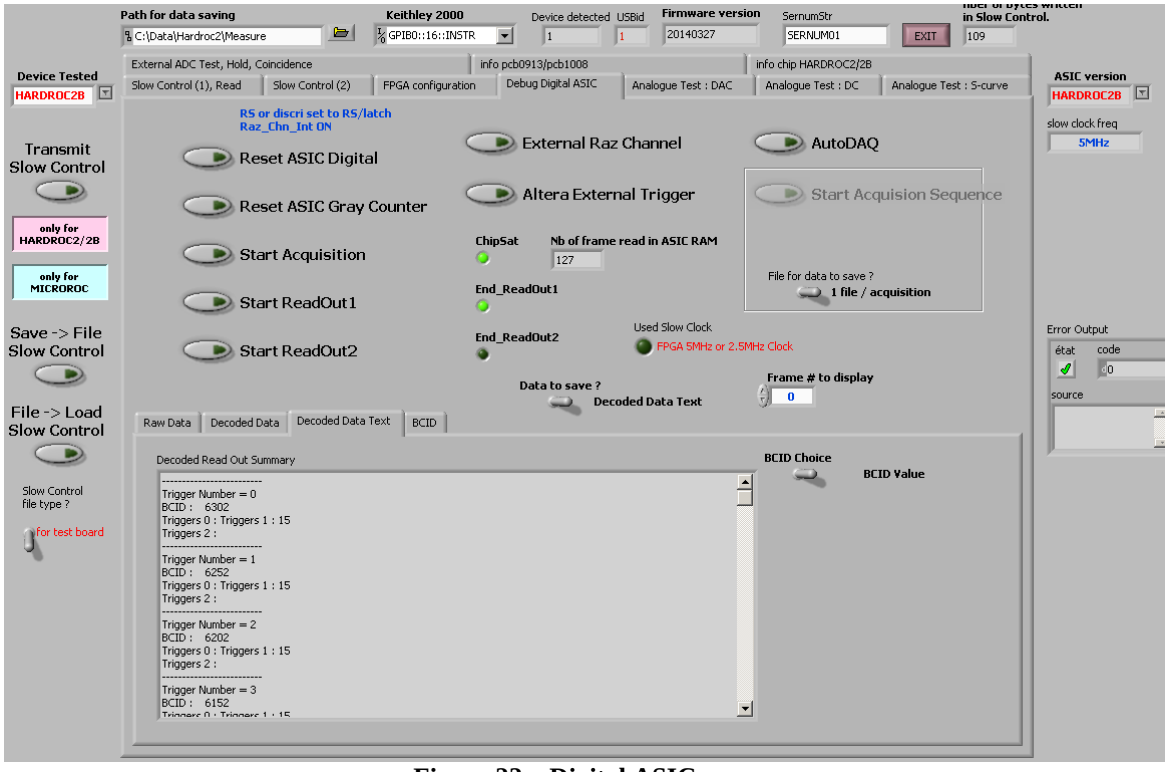


Figure 22 – Digital ASIC page

Annex A: Testboard's FPGA Internal Registers

Hardroc2 Test Board ALTERA Registers

LSB MSB

WORD 0

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
sel_val_evt	Raz_chn	Val_Evt_LV	sel_trig_ext	en_serial_link	sel_Dout	sel_Transmit	test_chk_sr
Select Data to send to (ASIC) Val_Evt : '0' Lemo Conn. In_altera2, '1' Val_Evt_LV	'1' : clear last event	'1' : Valid Event	Select Data to send to (ASIC) Trig_Ext : '0' Clk_Gene_Ext, '1' Alt_trig_ext	'1' : Enable sr_ck, sr_in. '0' all Hi Z	'1' : Dout1b '0' Dout2b	'1' : TransmitOn1b '0' TransmitOn2b	'1' : SR Register Correlation Test query

WORD 1

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
	StartCycle (config)	resetb	reset_counterb	select	ASIC selection_0	ASIC selection_1	sr_rstb
	'↑' : Start Data (Slow Control, SCA Read or Probe) Shift	'0' : Altera Output / ASIC input : ASIC Digital part Reset	'0' : Altera Output / ASIC input : ASIC BCID counter Reset	'0' : Select Read Register '1' Select Slow Control	Select the ASIC tested: '0' => HARDROC2 '1' => HARDROC2B '3' => MICROROC		'0' : Altera Output / ASIC input : SR Register Reset

WORD 2

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
StartAcq	Start_ReadOut2	Start_ReadOut1	Alt_trig_ext	gene_polarity	40MHz_ASIC	DVDD_level	DAQ_mode
'1' :Altera Output / ASIC input : Enable Acquisition	'1' : Altera Output / ASIC input : Start ReadOut Signal	'1' : Altera Output / ASIC input : Start ReadOut Signal	Data send to ASIC trig_ext if Sel_trig_ext = '1'	Select CLK_GENE_EXT or not(CLK_GENE_EXT)	'1' : Enable 40MHz Clock to ASIC '0': no Clock	set DVDD to 4,0V ('0') or 3,3V ('1')	'0' manual DAQ, '1' Auto DAQ

WORD 3

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
sel_pwr_on_d	sel_pwr_on_a	trig_out_polarity	sel_pwr_on_adc	sel_pwr_on_dac	En_Test_Scurve	resetb_Scurve	sclkspeed
Select Data to send to (ASIC) pwr_on_d : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	Select Data to send to (ASIC) pwr_on_a : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	Out_altera1,2,3 provides trigger output : '1' : OR64, '0' NOR64	Select Data to send to (ASIC) pwr_on_adc : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	Select Data to send to (ASIC) pwr_on_dac : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	'1' : Enable Scurve Tests	'0' : Reset Counters for Scurve Tests	Slow Clock (5MHz) Speed : '0' 1.25MHZ, '1' 5MHz

WORD 4

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
		ChipSatb	End_ReadOut1	End_ReadOut2			chksum_sr
							SR Register Test Result

WORD 5

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7

WORD 6

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
Trig_coincid_0	Trig_coincid_1	en_test_5M	sel_OR2hold	EN_TimeOut	Data delayed for hold	en_test_40M	used slow clock
Selection of Internal Trigger and of Trigger to use for coincidence : '0' = TRIGGER 0, '1' = TRIGGER 1, '2' = TRIGGER 2, '3' = none		'1' : Allow Slow clock on test pin 40. '0' : no data	'1' : Select OR64/coincidence delayed as hold command. '0' : select HOLD connector.	'1' : Enable TimeOut for latched OR64delayed.	'1' : Select coincidence signal to delay. '0' : Select OR64 to delay.	'1' : Allow Fast clock on test pin 39. '0' : no data	'0' FPGA internal 5/2.5MHz ; '1' External connector

Adress 7	
Adress 8	Scurve Pulse Counter (8-bit) LSB
Adress 9	Scurve Trigger DAC0 Counter (8-bit) LSB
Adress 10	SR (Slow Control (select=1) and Read (select=0)) Register
Adress 11	Scurve Trigger DAC1 Counter (8-bit) LSB
Adress 12	Scurve Trigger DAC2 Counter (8-bit) LSB
Adress 13	0 & 0 & 0 & 0 & Word Used in ReadOut FIFO [11..8]
Adress 14	Word used in ReadOut FIFO [7..0]
Adress 15	ReadOut FIFO (8-bit)
Adress 16	
Adress 17	
Adress 18	
Adress 19	
Adress 20	StartADC ReadOut & 0 & 0 & ADC OTR & ADC ReadOut [12..9]
Adress 21	ADC ReadOut [8..1]
Adress 22	ADC FIFO1 Empty & ADC FIFO2 Empty & 0 & 0 & 0 & 0 & 0 & 0 & 0
Adress 23	Start_DAQ_Sequence & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
Adress 24	
Adress 100	Firmware version

Annex B: Firmware of the PCB (Top level only)