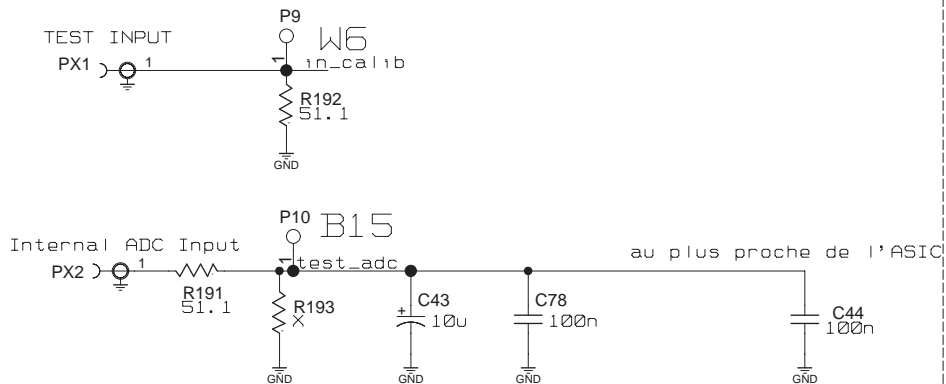
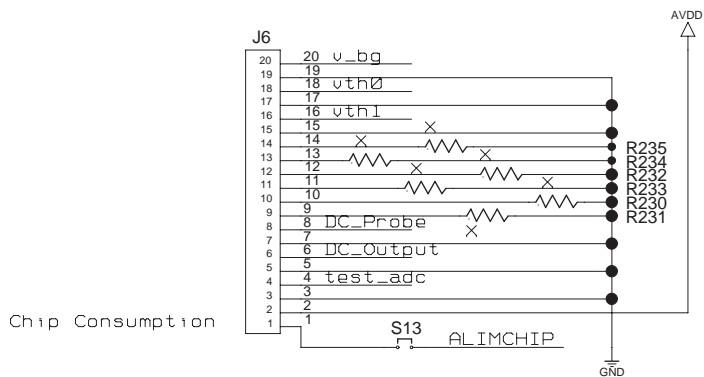


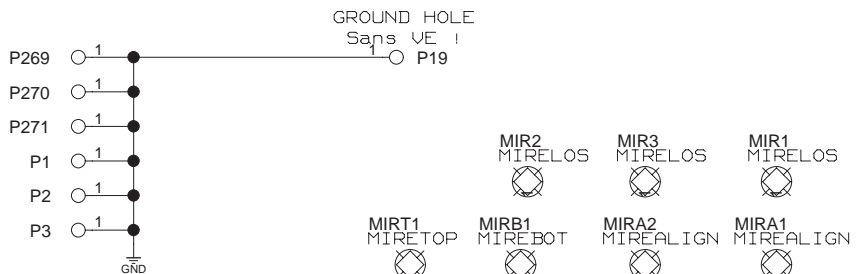
ANALOG INPUTS



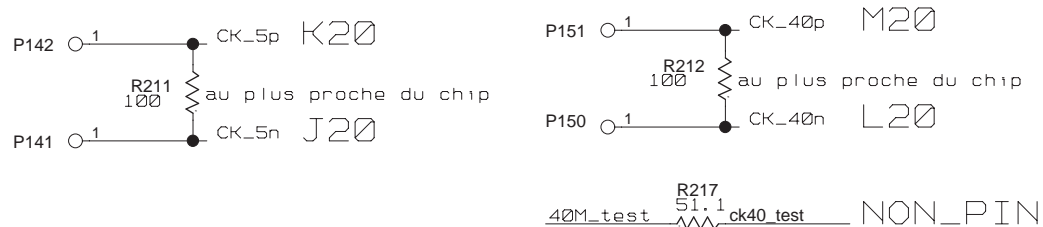
KEITHLEY DMM 2000 - CONNECTOR



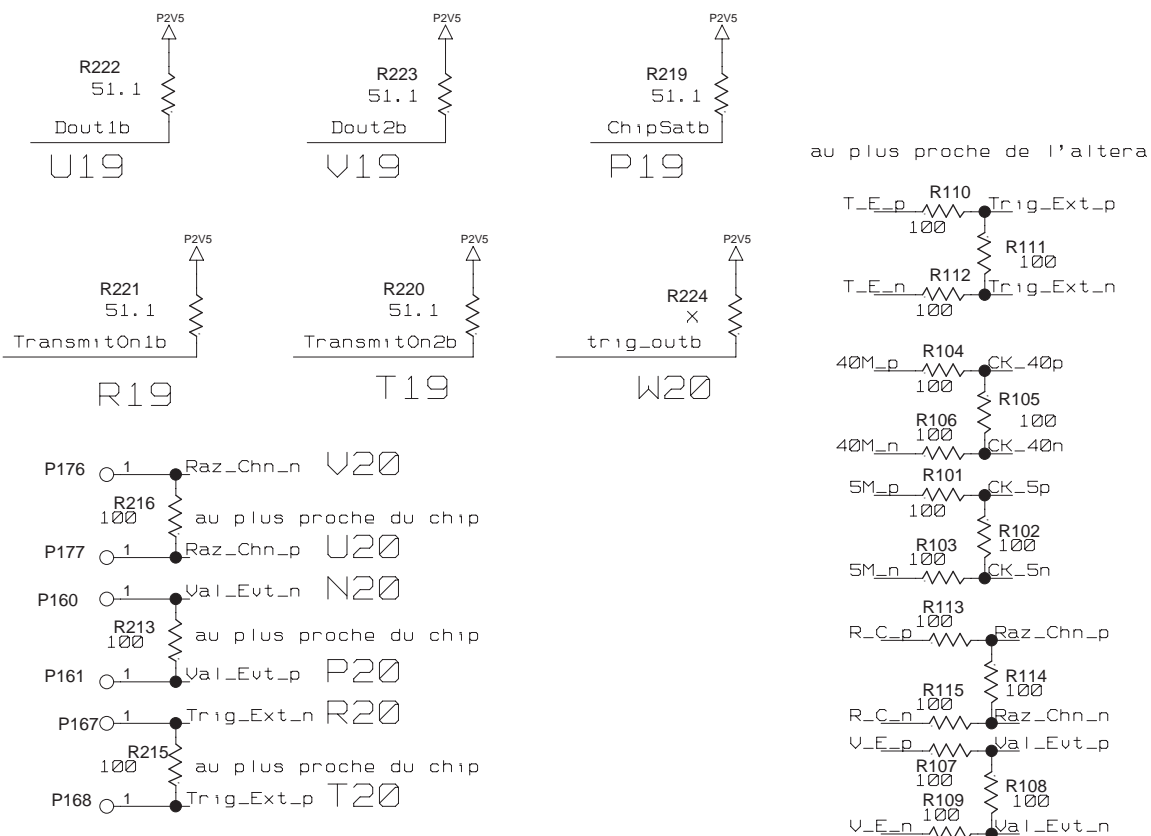
PASTILLES MÉCANIQUES POUR ENTRETOISES




CLOCKS INPUTS

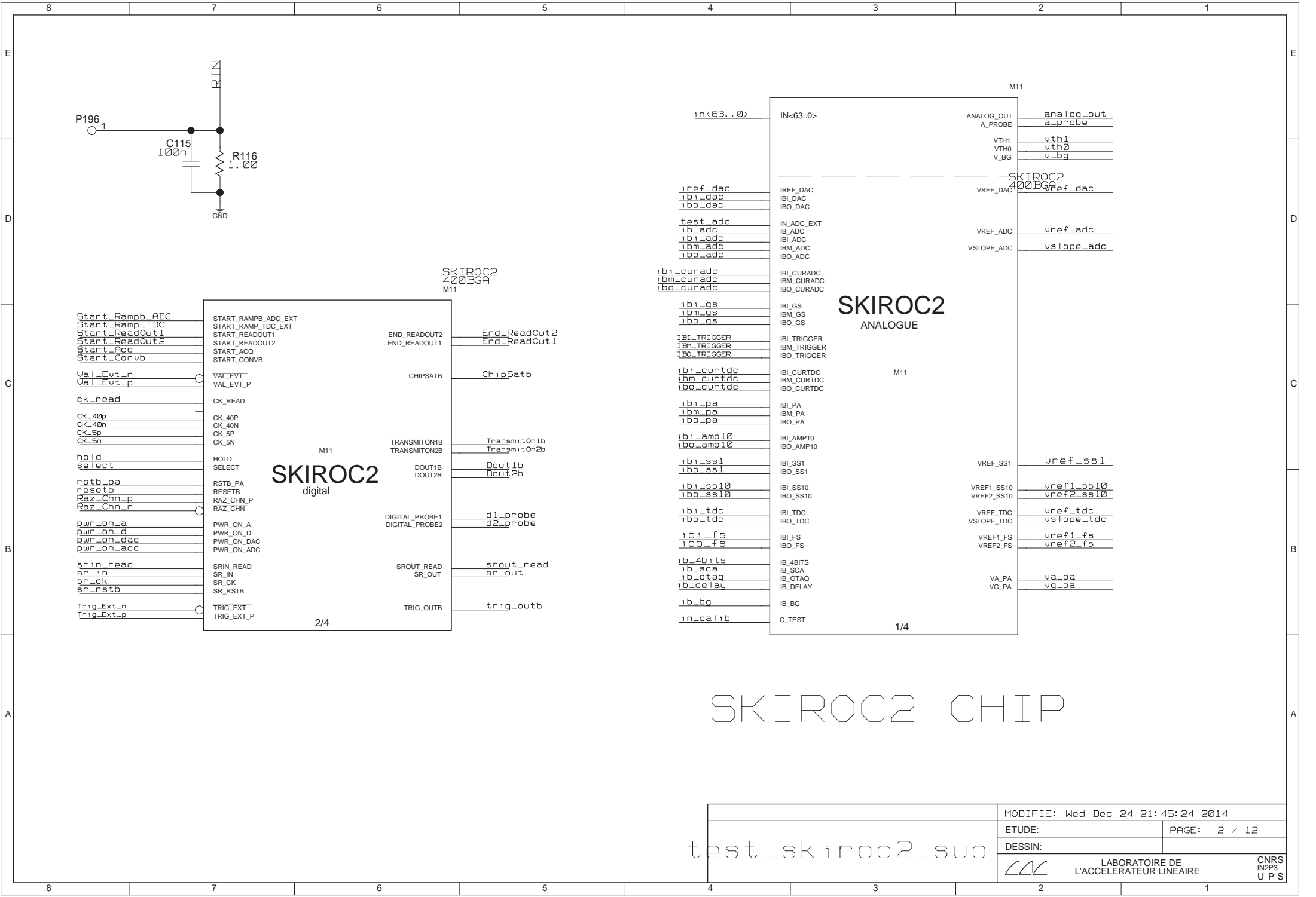


I/O ASIC

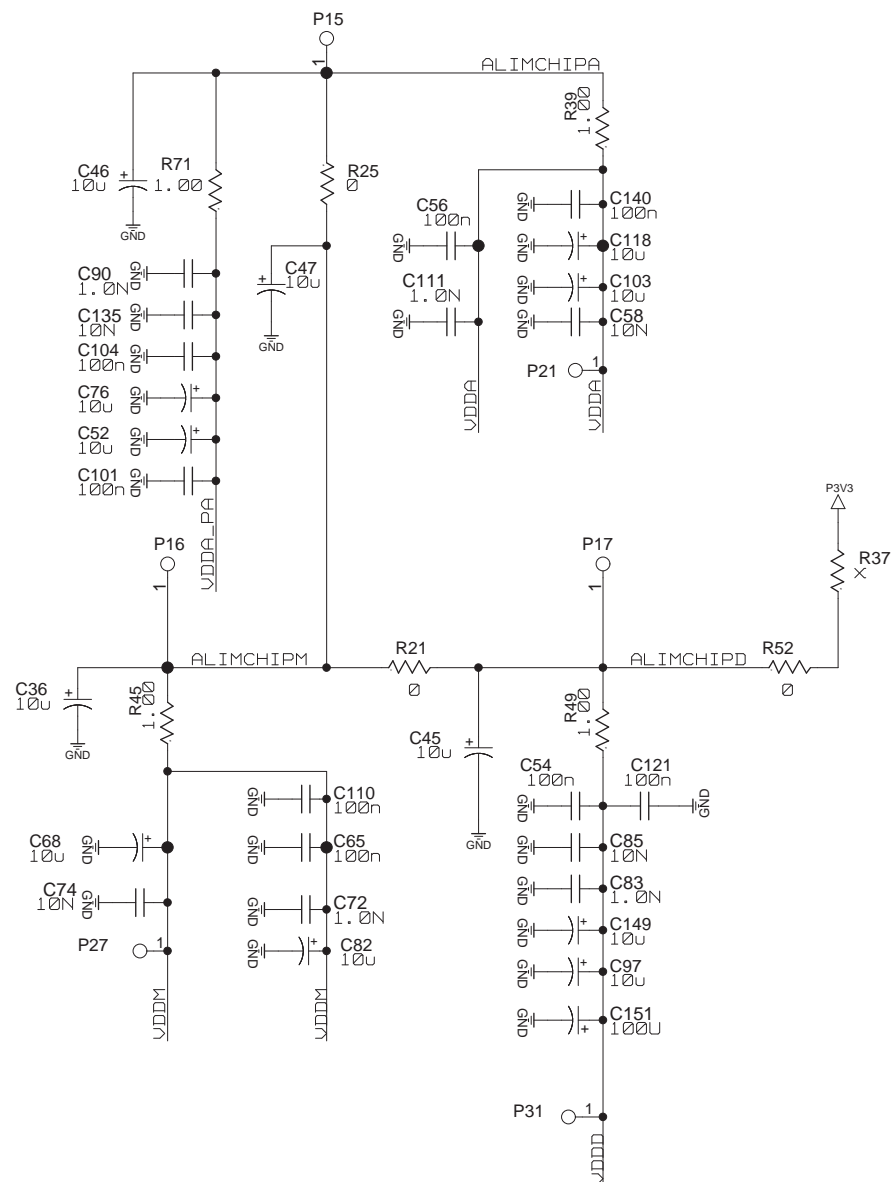


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test_sk iroc2_sup
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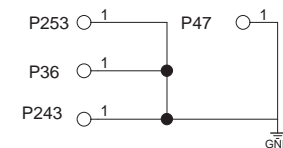
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ETUDE:	PAGE: 1 / 12
DESSIN:	
 <div style="display: inline-block; vertical-align: middle; text-align: center;"> LABORATOIRE DE L'ACCELERATEUR LINEAIRE </div> <div style="display: inline-block; vertical-align: middle; text-align: center; margin-left: 20px;"> CNRS IN2P3 UPS </div>	



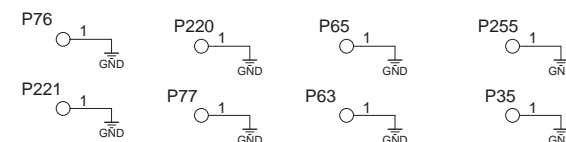
DECOUPLAGE DU VDD(pres du chip)



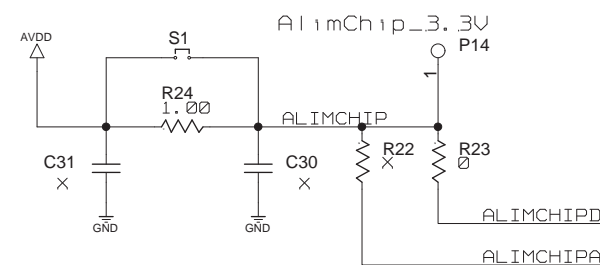
Reprises de GND pour R traversant




TEST PINS DES PRISES DE MASSE



Conso Chip 3.3V



test_sk iroc2_sup

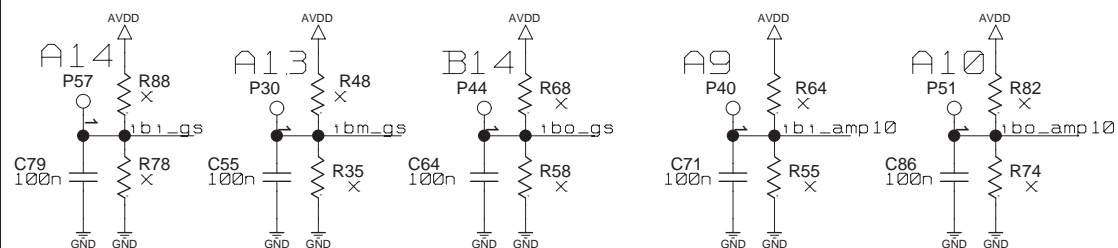
MODIFIE: Tue Feb 24 16:11:24 2015	
ETUDE:	PAGE: 3 / 12
DESSIN:	
 LABORATOIRE DE L'ACCELERATEUR LINEAIRE	
CNRS IN2P3 U P S	

SERIGRAPHIE: Nom equipot OU Pin ASIC

Capa decouplage au plus pres du chip

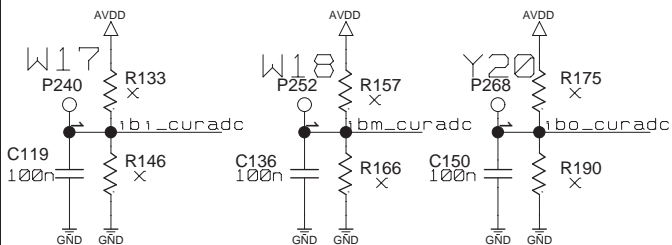
BIAS CURRENT

REFERENCE VOLTAGE

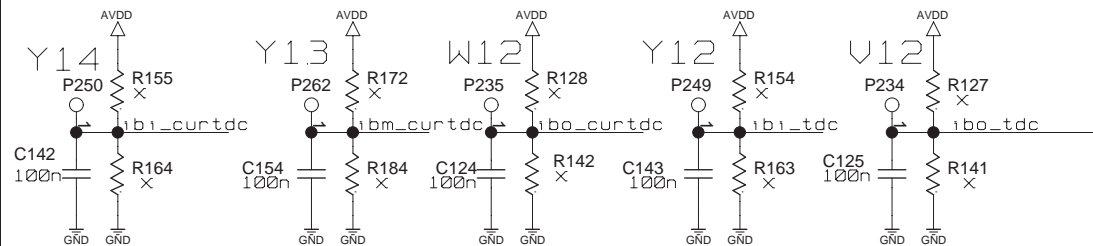


GS

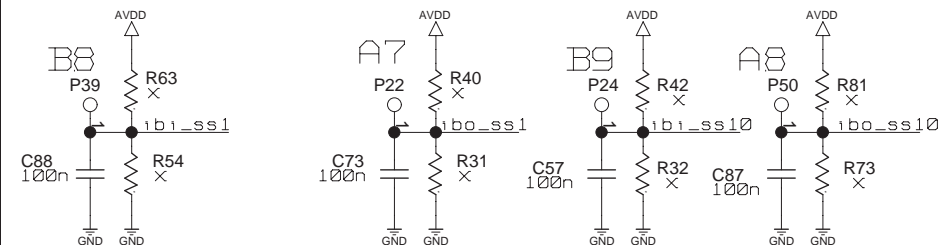
AMPLI G10



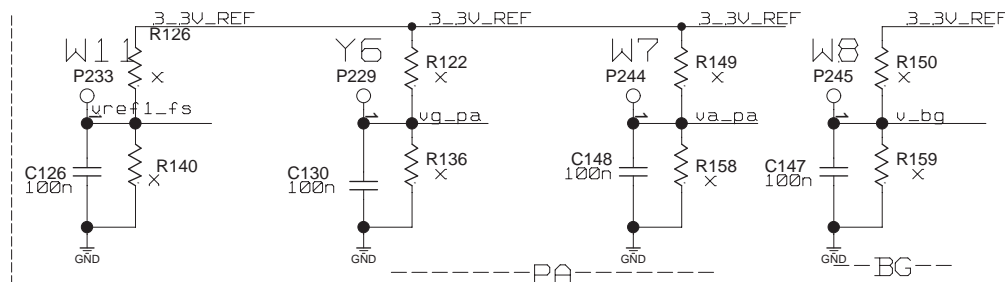
ADC RAMP



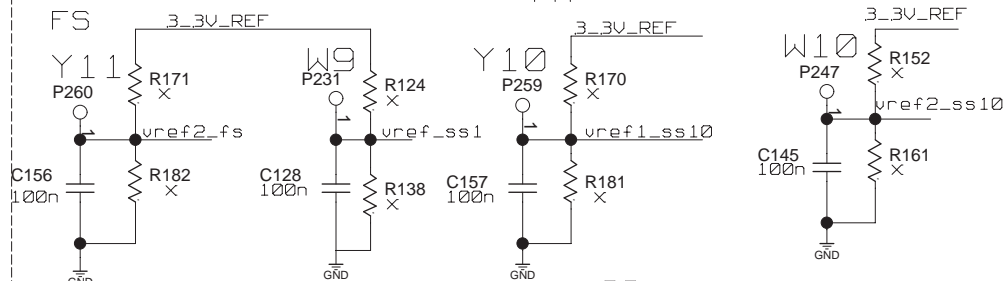
TDC RAMP



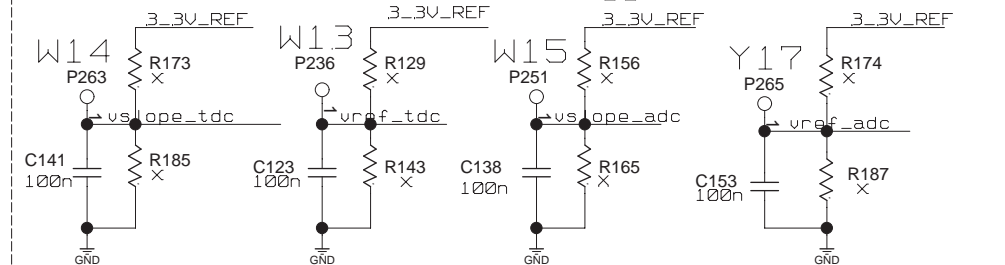
SS



PA



SS



TDC

ADC

REFERENCE CURRENT



DAC

test_sk_iroc2_sup

MODIFIE: Wed Nov 12 21:27:42 2014

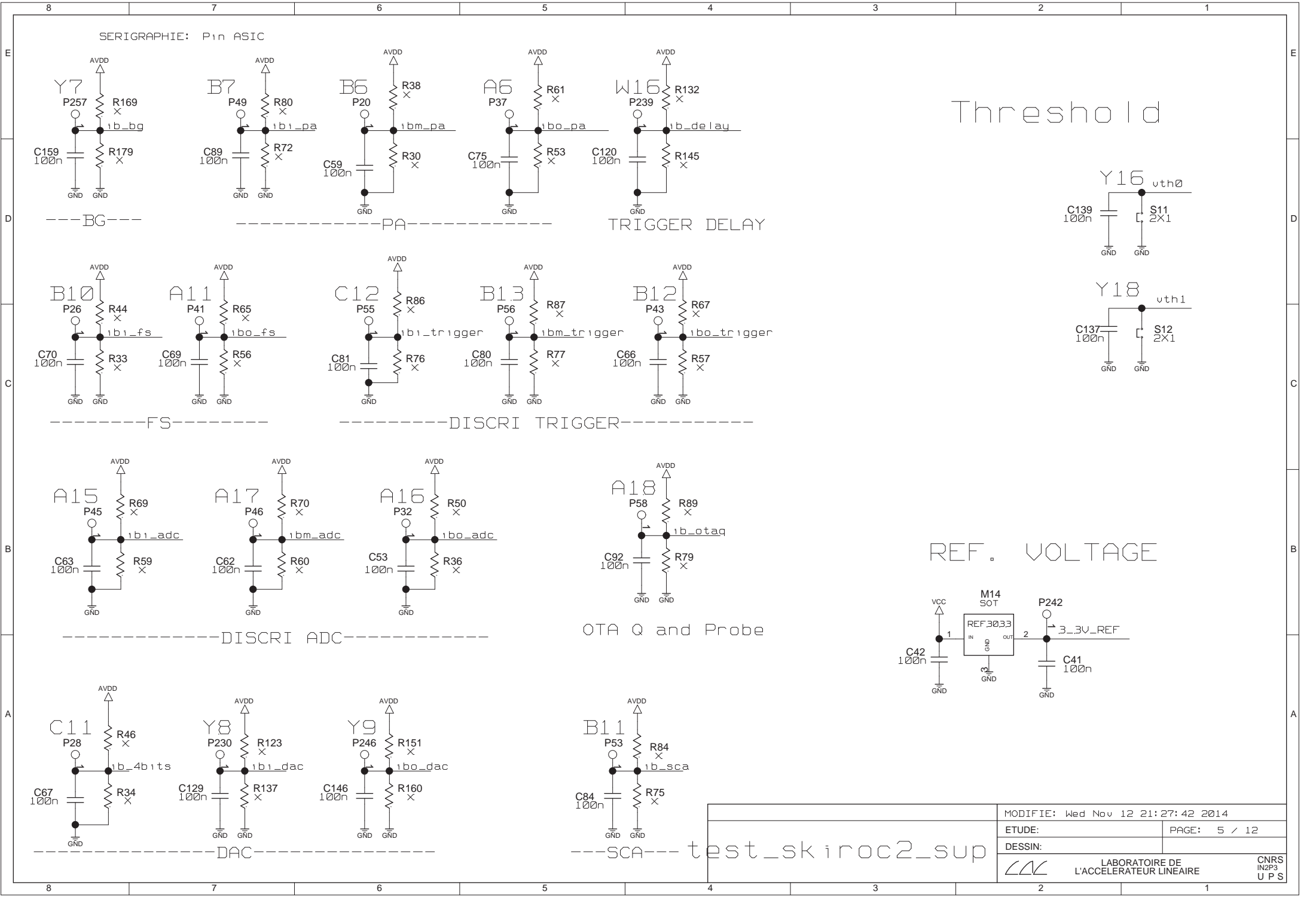
ETUDE:

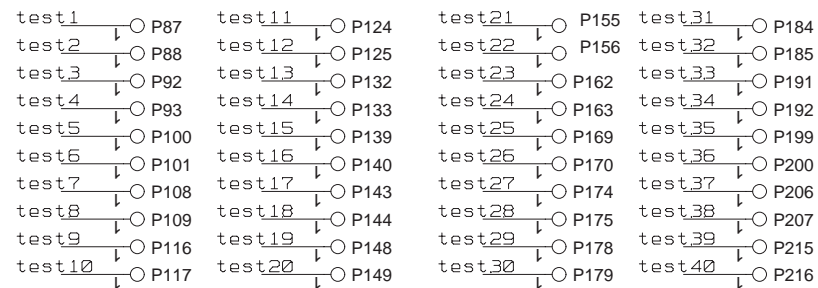
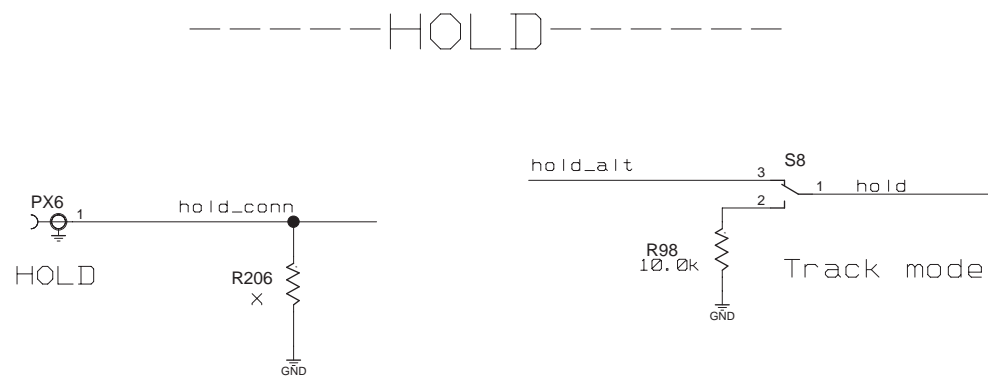
PAGE: 4 / 12

DESSIN:

CAC

LABORATOIRE DE
L'ACCELERATEUR LINEAIRECNRS
IN2P3
U P S



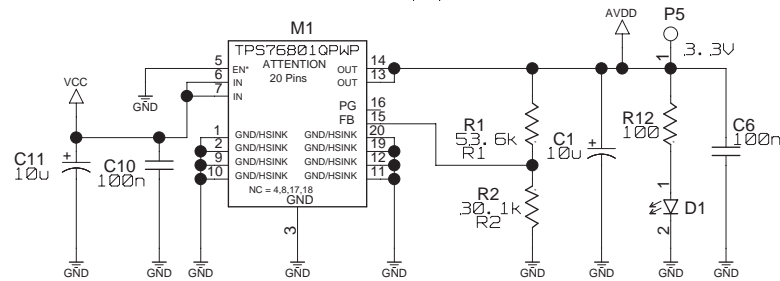


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test_sk iroc2_sup
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POWER SUPPLY

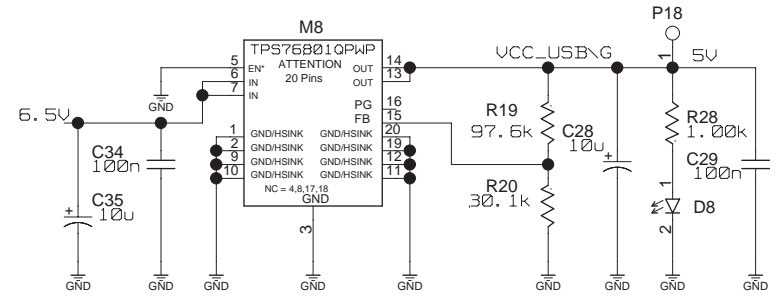
alim entation ASIC

Alim ASIC 3.3V

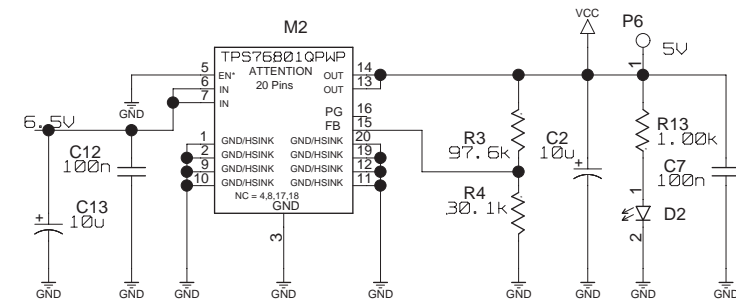


R 0805 a 1% pour les regulateurs
Vreg=1.1834*(1+R1/R2) et R2=30.1k

Vcc_USB



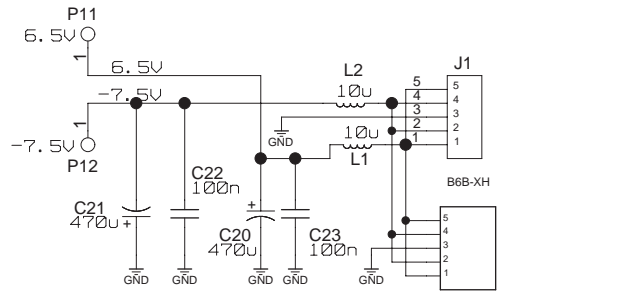
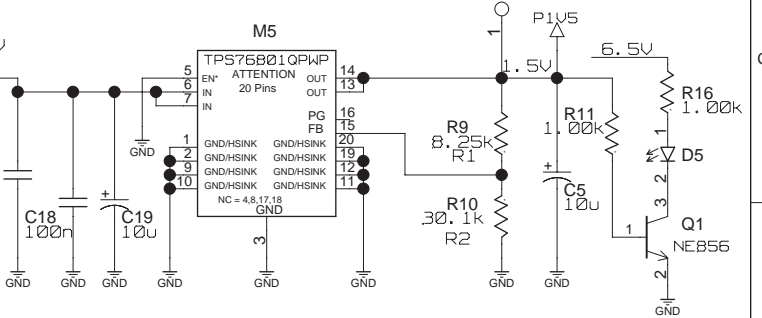
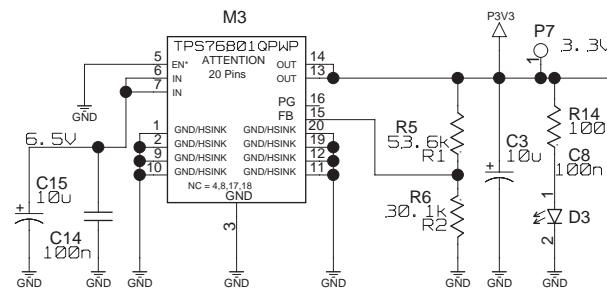
Vcc pour external ADC & buffers



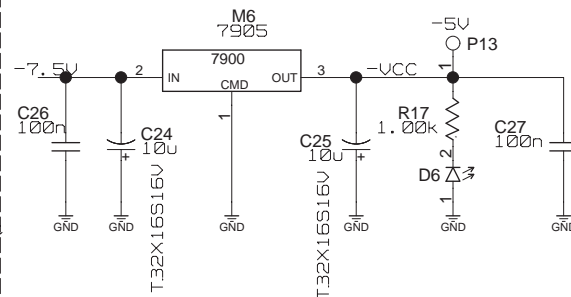
alim entation ALTERA

3.3V pour les banks 1

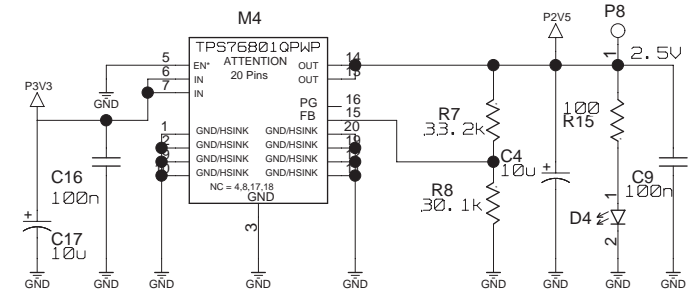
1.5V pour alim interne et bank 4



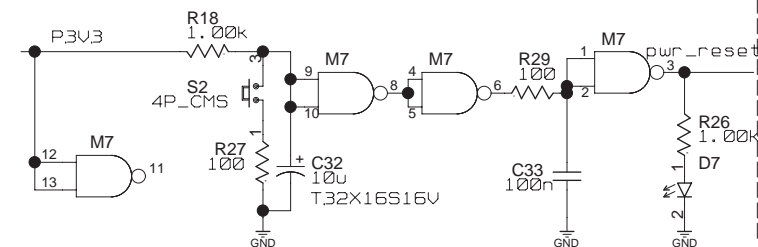
Alim negative pour buffers



2.5V pour le bank 2 et 3 (LVDS)

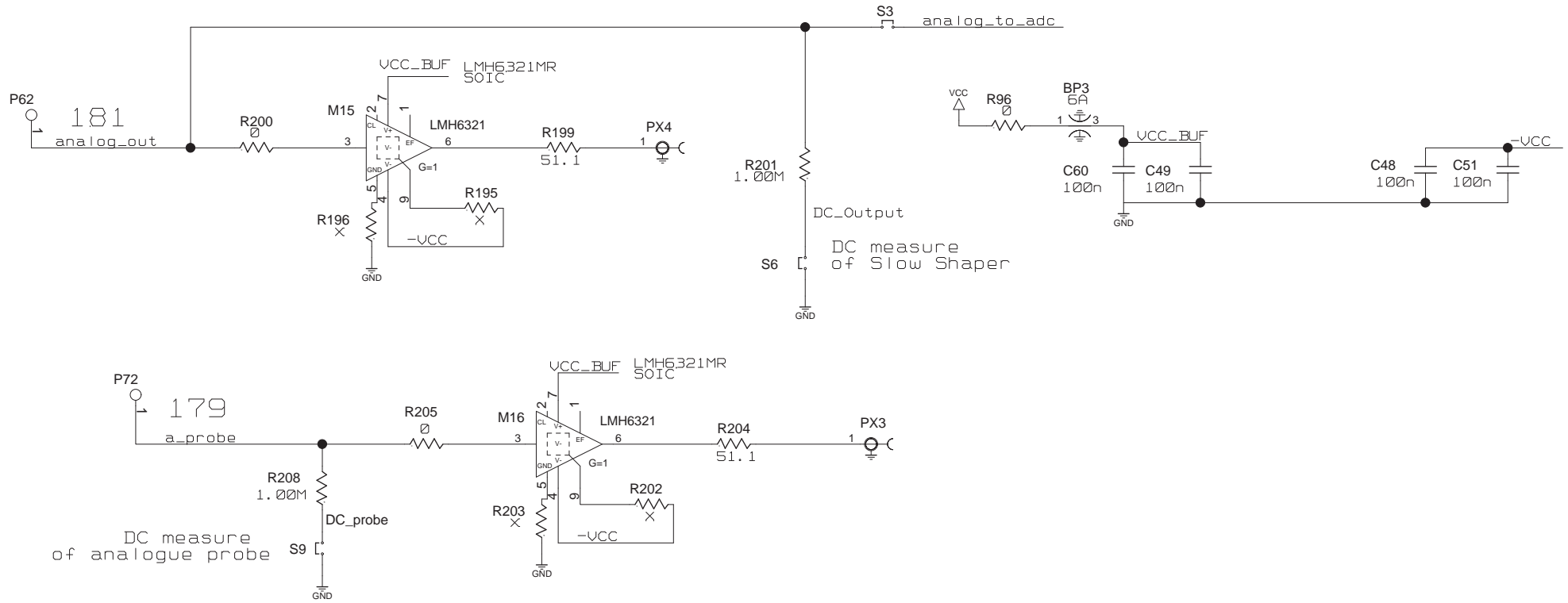


Power-on reset

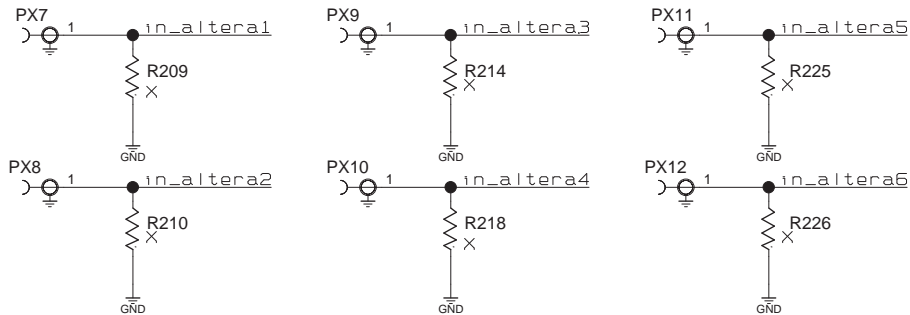


test_sk iroc2_sup

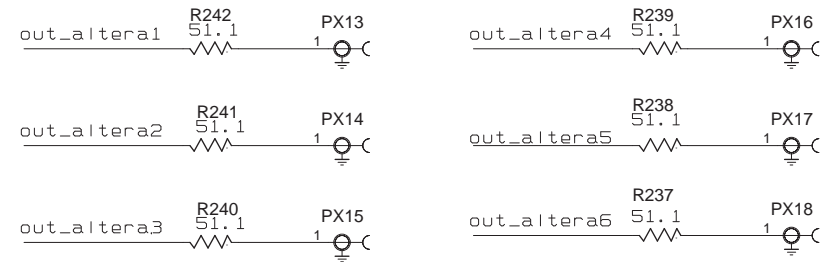
BUFFERED OUTPUTS




I/O to ALTERA



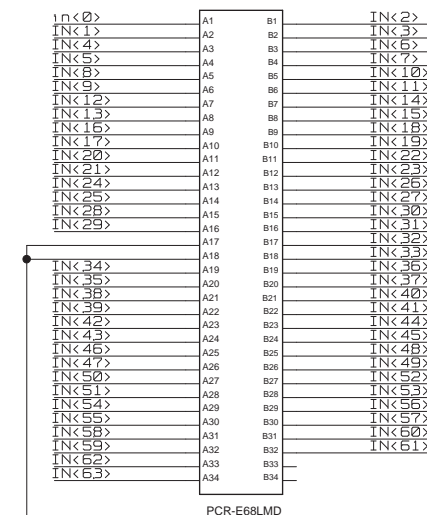
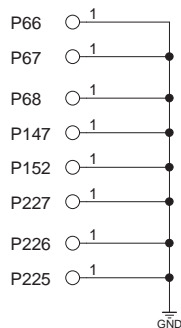
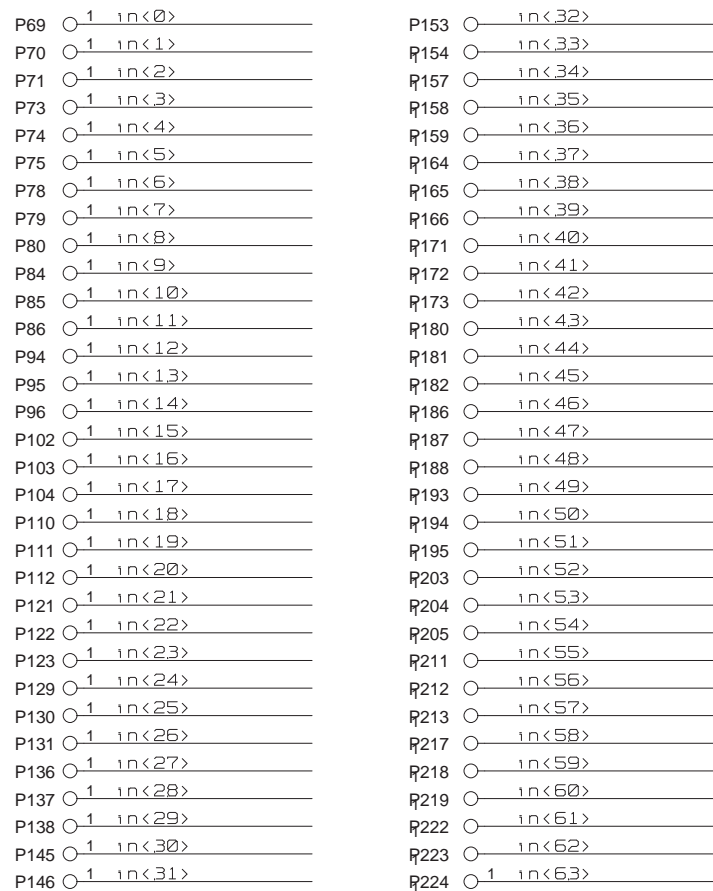
I/O from ALTERA



test_sk_iroc2_sup

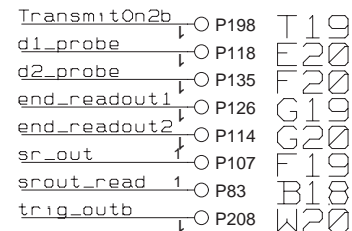
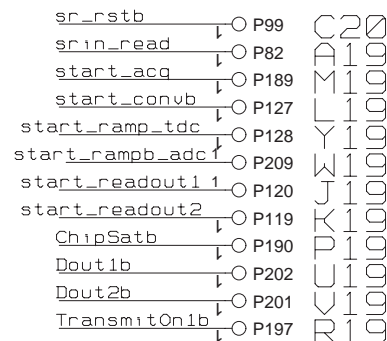
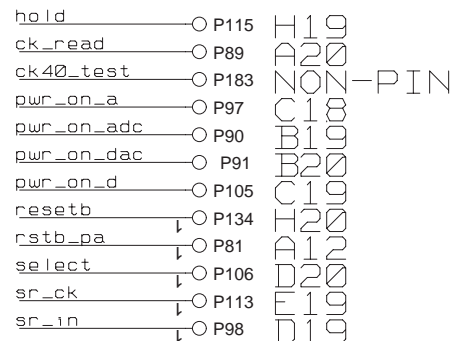
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 LABORATOIRE DE L'ACCELERATEUR LINEAIRE	
CNRS IN2P3 U P S	

Connection to PIN diodes

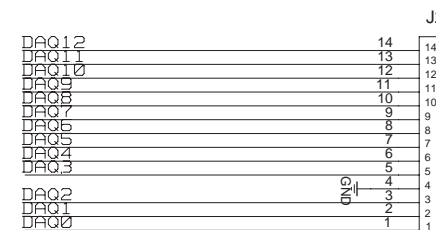


test_sk iroc2_sup

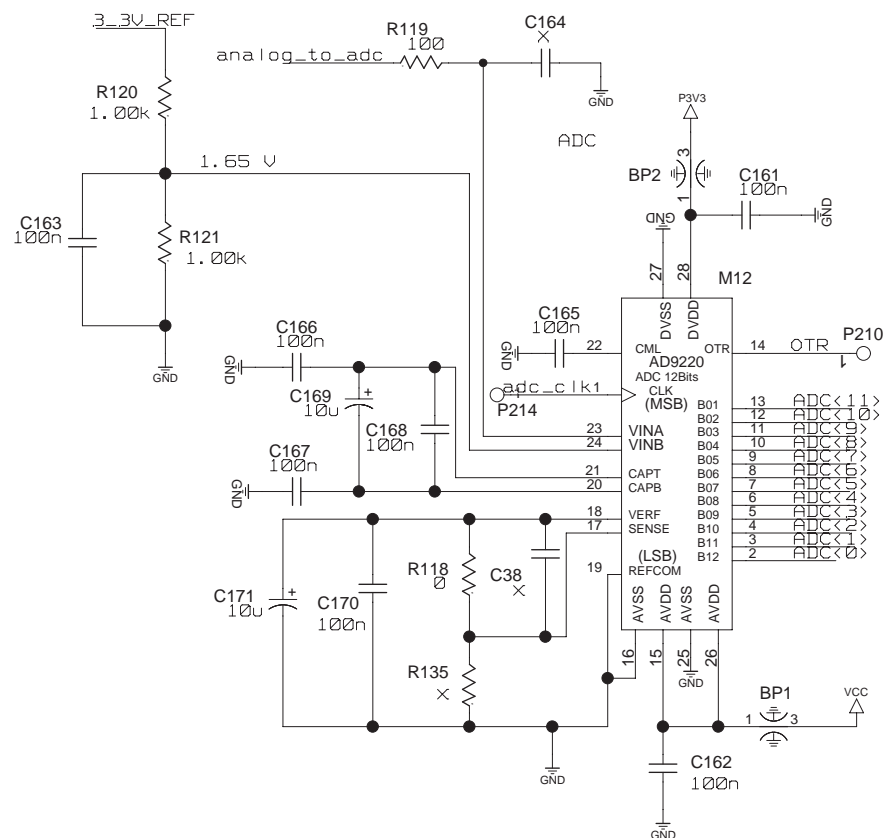
Digital ASIC



DAQ Connector



-external ADC



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test_sk i roc2_sup
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