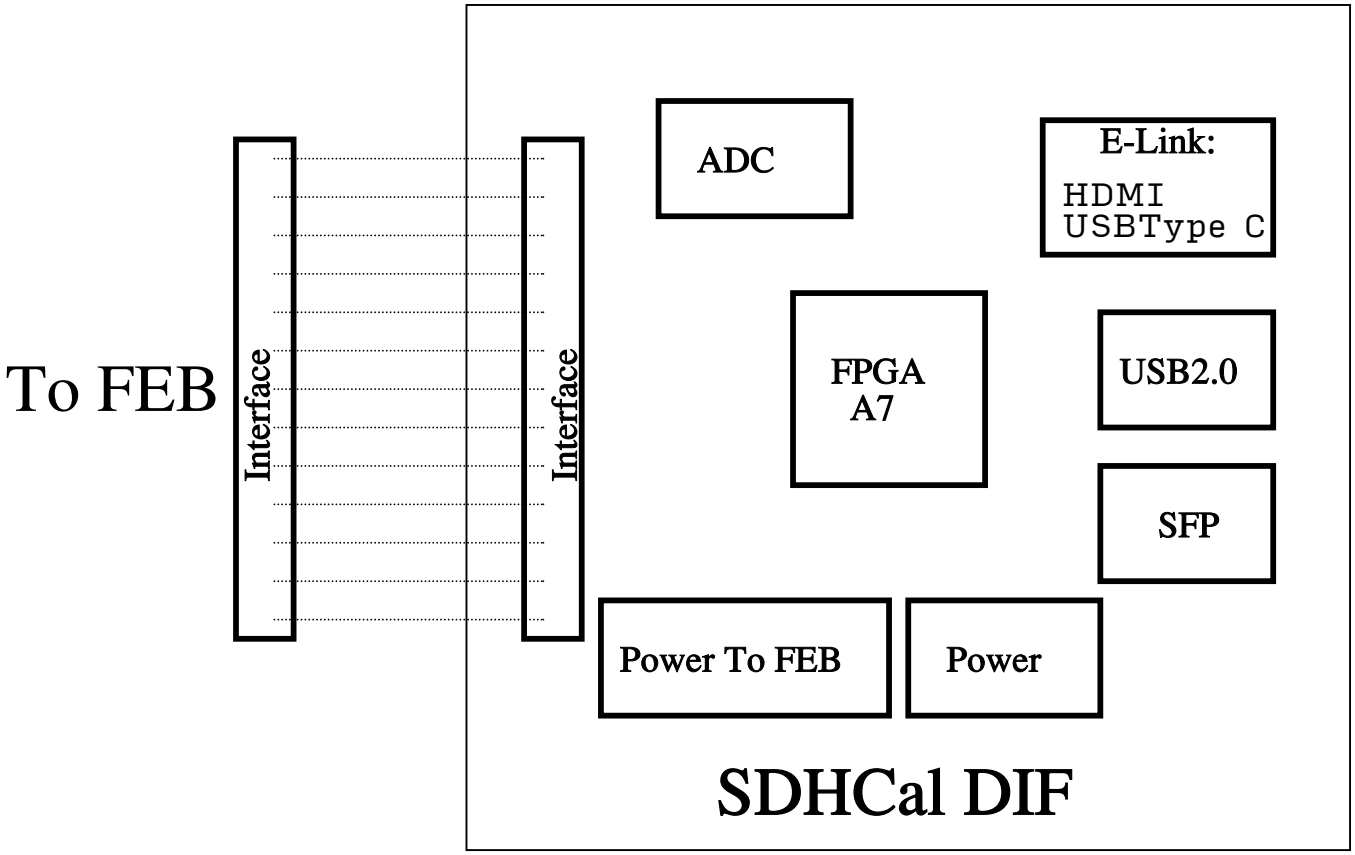


SDHCal DIF

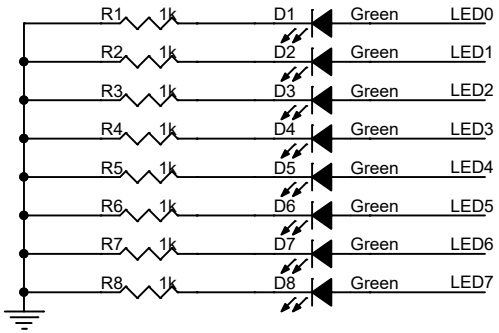
SDHCal DIF
Version: 1.0
Design Tools: Cadence 16.6
Finish Date: 2018/04/22
Engineer: Yu Wang
Company: USTC

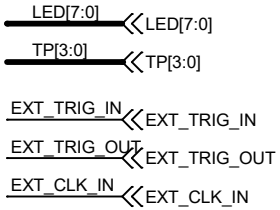
This study was supported by National Key Programme for S&T Research and Development (Grant NO.: 2016YFA0400400) and National Science Natural Science Foundation of China (Grant No.11635007).

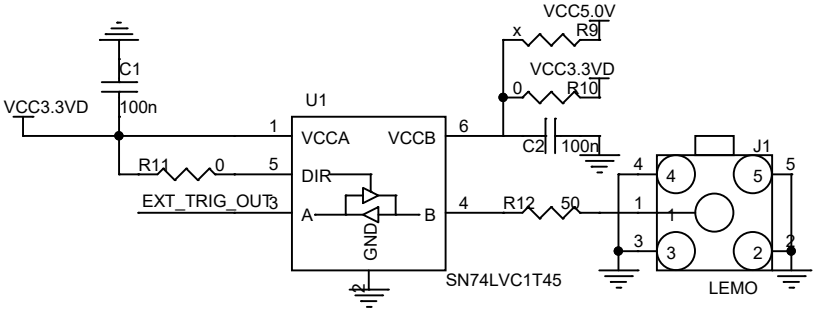
Title: SDHCalDIF		
Size: A4	Document Number: Top Viev	Rev: V1.0
Date: Thursday, April 26, 2018	Sheet 1 of 18	

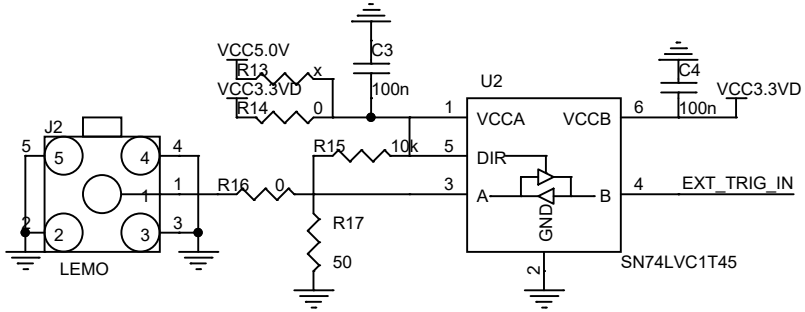
Title	SDHCal DIF	
Size: Custom	Document Number: Top Each	Rev: V1.0
Date: Wednesday, April 25, 2018	Sheet 2 of 18	

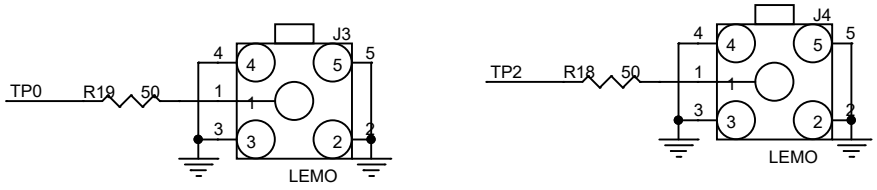
LED indicator

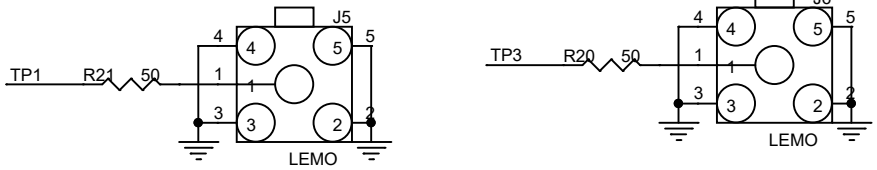


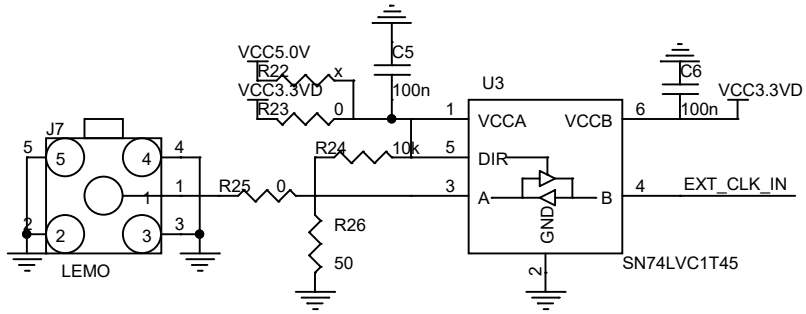












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Size A4	Document Number **A7_Auxiliary**	Rev V1.0
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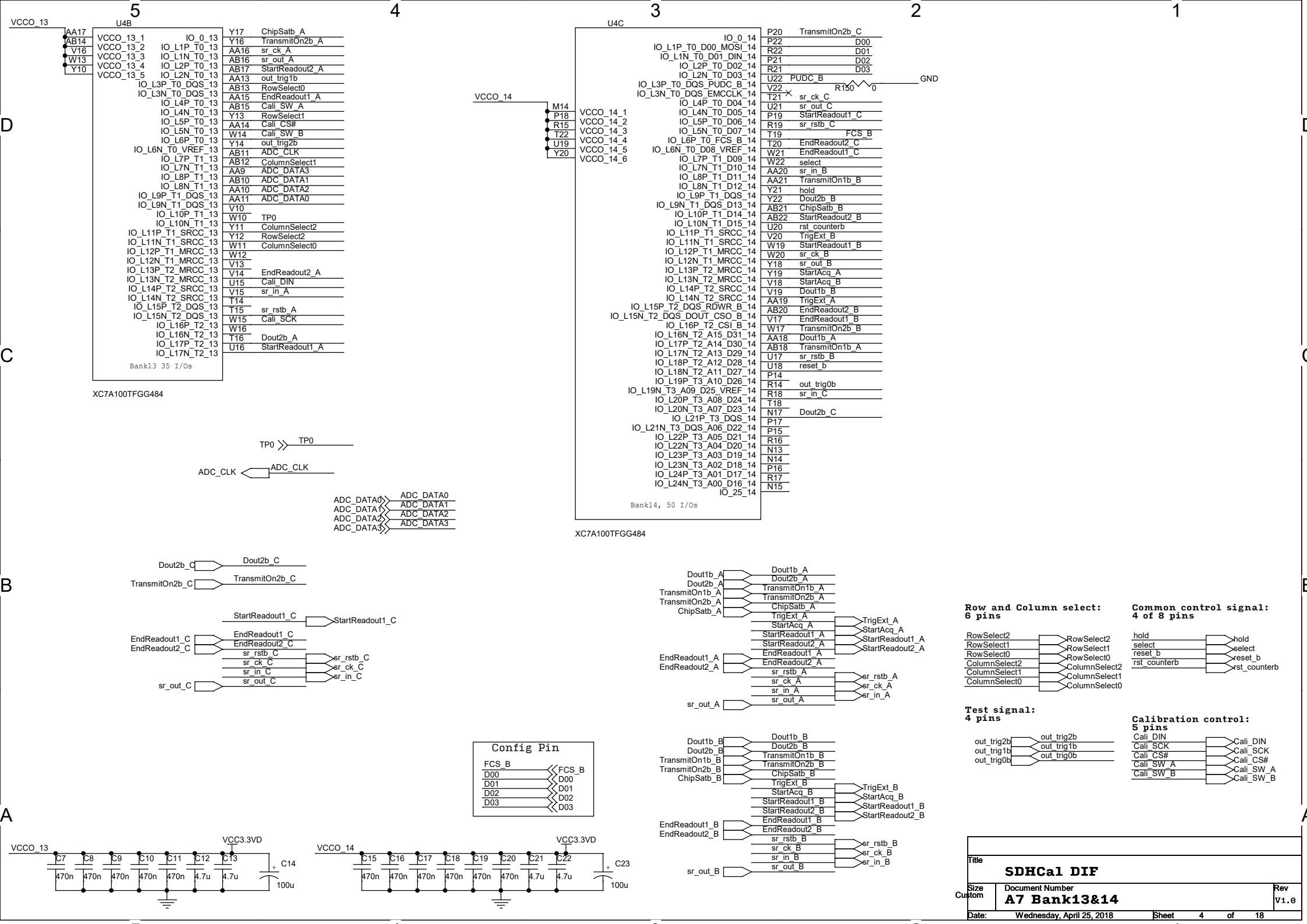
5
4
3
2
1
D
C
B
A
U4B
VCCO_13
AA17
AB14
V16
W13
Y10
VCCO_13_1
VCCO_13_2
VCCO_13_3
VCCO_13_4
VCCO_13_5
IO_0_13
IO_L1P_T0_13
IO_L1N_T0_13
IO_L2P_T0_13
IO_L2N_T0_13
IO_L3P_T0_DQS_13
IO_L3N_T0_DQS_13
IO_L4P_T0_13
IO_L4N_T0_13
IO_L5P_T0_13
IO_L5N_T0_13
IO_L6P_T0_13
IO_L6N_T0_VREF_13
IO_L7P_T1_13
IO_L7N_T1_13
IO_L8P_T1_13
IO_L8N_T1_13
IO_L9P_T1_DQS_13
IO_L9N_T1_DQS_13
IO_L10P_T1_13
IO_L10N_T1_13
IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13
IO_L16P_T2_13
IO_L16N_T2_13
IO_L17P_T2_13
IO_L17N_T2_13
Bank13 35 I/Os
Y17 ChipSatb_A
Y16 TransmitOn2b_A
AA16 sr_ck_A
AB16 sr_out_A
AB17 StartReadout2_A
AA13 out_trig1b
AB13 RowSelect0
AA15 EndReadout1_A
AB15 Cali_SW_A
Y13 RowSelect1
AA14 Cali_CS#
W14 Cali_SW_B
Y14 out_trig2b
AB11 ADC_CLK
AB12 ColumnSelect1
AA9 ADC_DATA3
AB10 ADC_DATA1
AA10 ADC_DATA2
AA11 ADC_DATA0
V10
W10 TP0
Y11 ColumnSelect2
Y12 RowSelect2
W11 ColumnSelect0
W12
V13
V14 EndReadout2_A
U15 Cali_DIN
V15 sr_in_A
T14
T15 sr_rstb_A
W15 Cali_SCK
W16
T16 Dout2b_A
U16 StartReadout1_A
XC7A100TFGG484
U4C
VCCO_14
M14
P18
R15
T22
U19
Y20
VCCO_14_1
VCCO_14_2
VCCO_14_3
VCCO_14_4
VCCO_14_5
VCCO_14_6
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
Bank14, 50 I/Os
P20 TransmitOn2b_C
P22 D00
R22 D01
P21 D02
R21 D03
U22 PUDC_B
V22
T21 sr_ck_C
U21 sr_out_C
P19 StartReadout1_C
R19 sr_rstb_C
T19 FCS_B
T20 EndReadout2_C
W21 EndReadout1_C
W22 select
AA20 sr_in_B
AA21 TransmitOn1b_B
Y21 hold
Y22 Dout2b_B
AB21 ChipSatb_B
AB22 StartReadout2_B
U20 rst_counterb
V20 TrigExt_B
W19 StartReadout1_B
W20 sr_ck_B
Y18 sr_out_B
Y19 StartAcq_A
V18 StartAcq_B
V19 Dout1b_B
AA19 TrigExt_A
AB20 EndReadout2_B
V17 EndReadout1_B
W17 TransmitOn2b_B
AA18 Dout1b_A
AB18 TransmitOn1b_A
U17 sr_rstb_B
U18 reset_b
P14
R14 out_trig0b
R18 sr_in_C
T18
N17 Dout2b_C
P17
P15
R16
N13
N14
P16
R17
N15
XC7A100TFGG484
PUDC_B
R150
0
GND
TP0
ADC_CLK
ADC_DATA0
ADC_DATA1
ADC_DATA2
ADC_DATA3
Dout2b_C
TransmitOn2b_C
StartReadout1_C
EndReadout1_C
EndReadout2_C
sr_rstb_C
sr_ck_C
sr_in_C
sr_out_C
Dout1b_A
Dout2b_A
TransmitOn1b_A
TransmitOn2b_A
ChipSatb_A
TrigExt_A
StartAcq_A
StartReadout1_A
StartReadout2_A
EndReadout1_A
EndReadout2_A
sr_rstb_A
sr_ck_A
sr_in_A
sr_out_A
Dout1b_B
Dout2b_B
TransmitOn1b_B
TransmitOn2b_B
ChipSatb_B
TrigExt_B
StartAcq_B
StartReadout1_B
StartReadout2_B
EndReadout1_B
EndReadout2_B
sr_rstb_B
sr_ck_B
sr_in_B
sr_out_B
Config Pin
FCS_B
D00
D01
D02
D03
Row and Column select:
6 pins
RowSelect2
RowSelect1
RowSelect0
ColumnSelect2
ColumnSelect1
ColumnSelect0
Common control signal:
4 of 8 pins
hold
select
reset_b
rst_counterb
Test signal:
4 pins
out_trig2b
out_trig1b
out_trig0b
Calibration control:
5 pins
Cali_DIN
Cali_SCK
Cali_CS#
Cali_SW_A
Cali_SW_B
VCCO_13
VCC3.3VD
C7
C8
C9
C10
C11
C12
C13
C14
470n
4.7u
100u
VCCO_14
C15
C16
C17
C18
C19
C20
C21
C22
C23
Title
SDHCal DIF
Size
Custom
Document Number
A7 Bank13&14
Rev
V1.0
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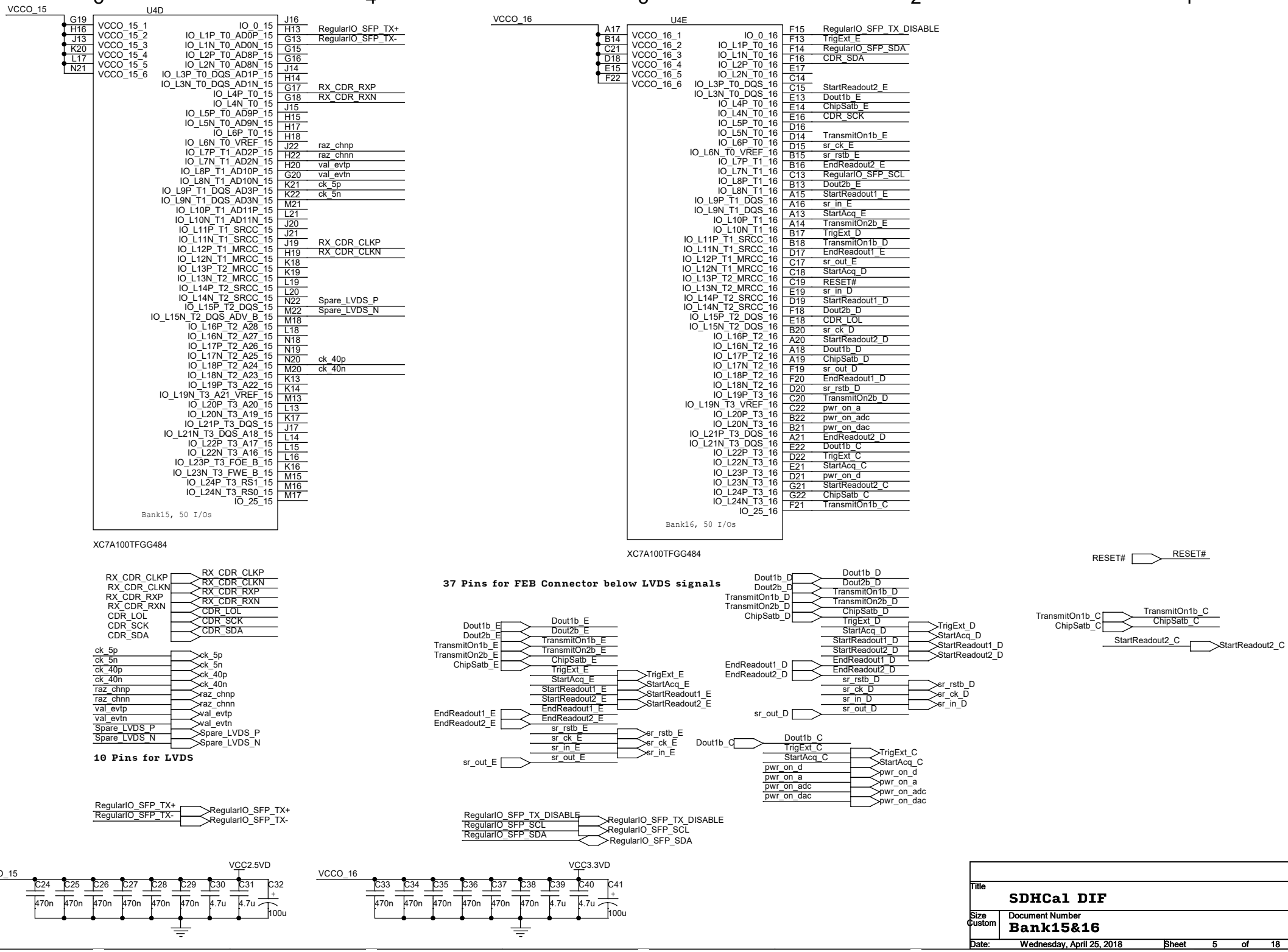
U4D
VCCO_15
VCCO_15_1
VCCO_15_2
VCCO_15_3
VCCO_15_4
VCCO_15_5
VCCO_15_6
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_15
IO_L4N_T0_15
IO_L5P_T0_AD9P_15
IO_L5N_T0_AD9N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD2P_15
IO_L7N_T1_AD2N_15
IO_L8P_T1_AD10P_15
IO_L8N_T1_AD10N_15
IO_L9P_T1_DQS_AD3P_15
IO_L9N_T1_DQS_AD3N_15
IO_L10P_T1_AD11P_15
IO_L10N_T1_AD11N_15
IO_L11P_T1_SRCC_15
IO_L11N_T1_SRCC_15
IO_L12P_T1_MRCC_15
IO_L12N_T1_MRCC_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_ADV_B_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
Bank15, 50 I/Os
XC7A100TFGG484
RegularIO_SFP_TX+
RegularIO_SFP_TX-
RX_CDR_RXP
RX_CDR_RXN
raz_chnp
raz_chnn
val_evtp
val_evtn
ck_5p
ck_5n
Spare_LVDS_P
Spare_LVDS_N
ck_40p
ck_40n
U4E
VCCO_16
VCCO_16_1
VCCO_16_2
VCCO_16_3
VCCO_16_4
VCCO_16_5
VCCO_16_6
IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
IO_L12N_T1_MRCC_16
IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16
Bank16, 50 I/Os
XC7A100TFGG484
RegularIO_SFP_TX_DISABLE
TrigExt_E
RegularIO_SFP_SDA
CDR_SDA
StartReadout2_E
Dout1b_E
ChipSatb_E
CDR_SCK
TransmitOn1b_E
sr_ck_E
sr_rstb_E
EndReadout2_E
Dout2b_E
sr_in_E
StartAcq_E
sr_out_E
TransmitOn2b_E
StartReadout1_E
RegularIO_SFP_SCL
RegularIO_SFP_SDA
RESET#
RESET#
37 Pins for FEB Connector below LVDS signals
Dout1b_D
Dout2b_D
TransmitOn1b_D
TransmitOn2b_D
ChipSatb_D
TrigExt_D
StartAcq_D
StartReadout1_D
StartReadout2_D
EndReadout1_D
EndReadout2_D
sr_rstb_D
sr_ck_D
sr_in_D
sr_out_D
Dout1b_C
TrigExt_C
StartAcq_C
pwr_on_d
pwr_on_a
pwr_on_adc
pwr_on_dac
TransmitOn1b_C
ChipSatb_C
StartReadout2_C
RX_CDR_CLKP
RX_CDR_CLKN
RX_CDR_RXP
RX_CDR_RXN
CDR_LOL
CDR_SCK
CDR_SDA
ck_5p
ck_5n
ck_40p
ck_40n
raz_chnp
raz_chnn
val_evtp
val_evtn
Spare_LVDS_P
Spare_LVDS_N
10 Pins for LVDS
RegularIO_SFP_TX+
RegularIO_SFP_TX-
RegularIO_SFP_TX_DISABLE
RegularIO_SFP_SCL
RegularIO_SFP_SDA
VCCO_15
VCC2.5VD
C24
C25
C26
C27
C28
C29
C30
C31
C32
470n
4.7u
100u
VCCO_16
VCC3.3VD
C33
C34
C35
C36
C37
C38
C39
C40
C41
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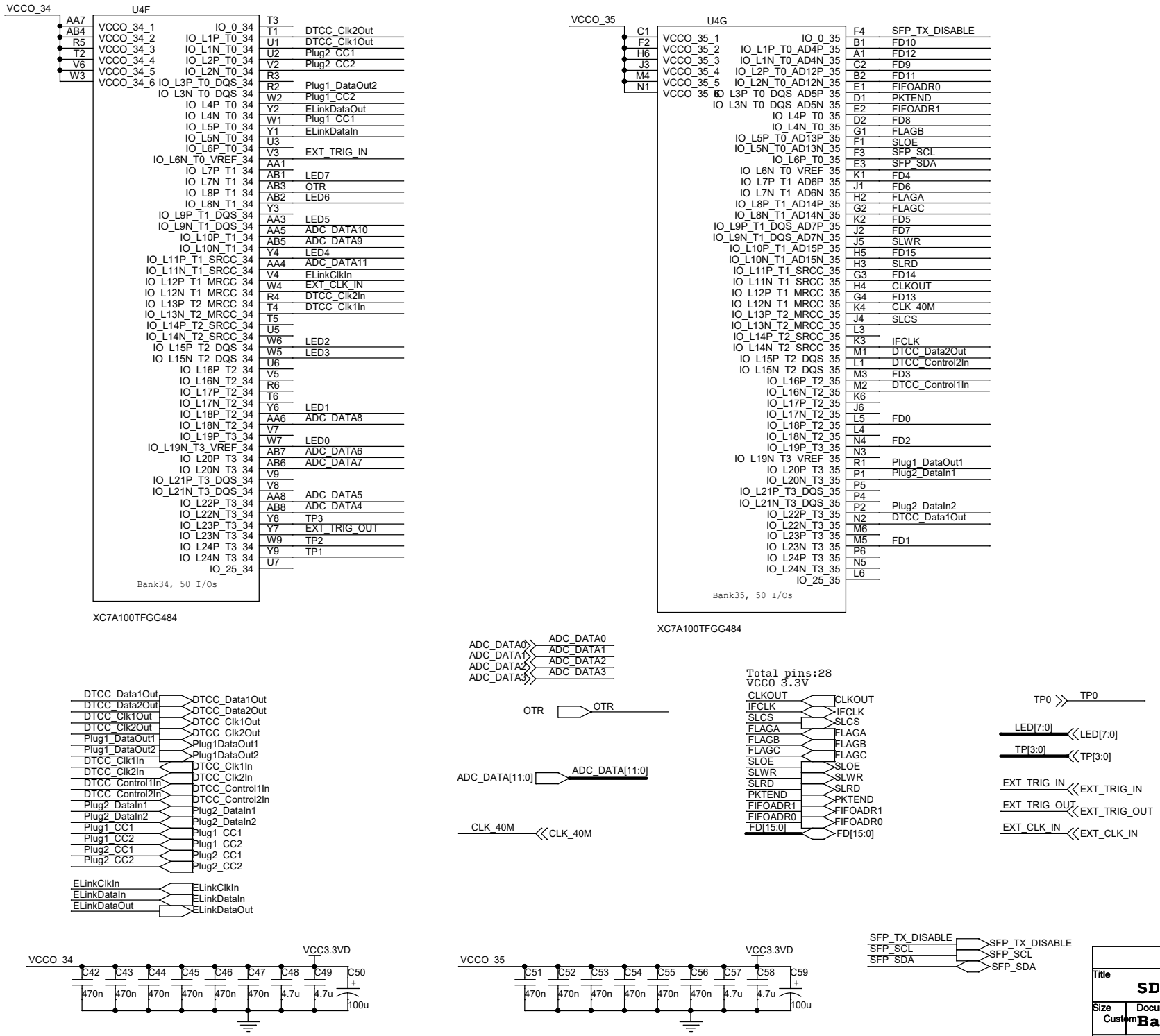

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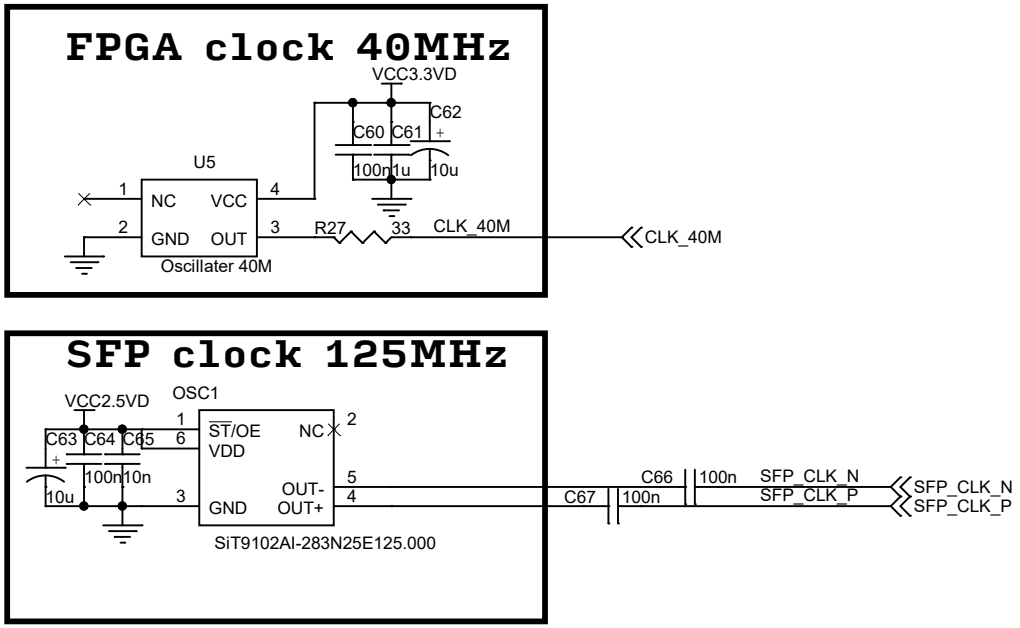

Title	SDHCal DIF	
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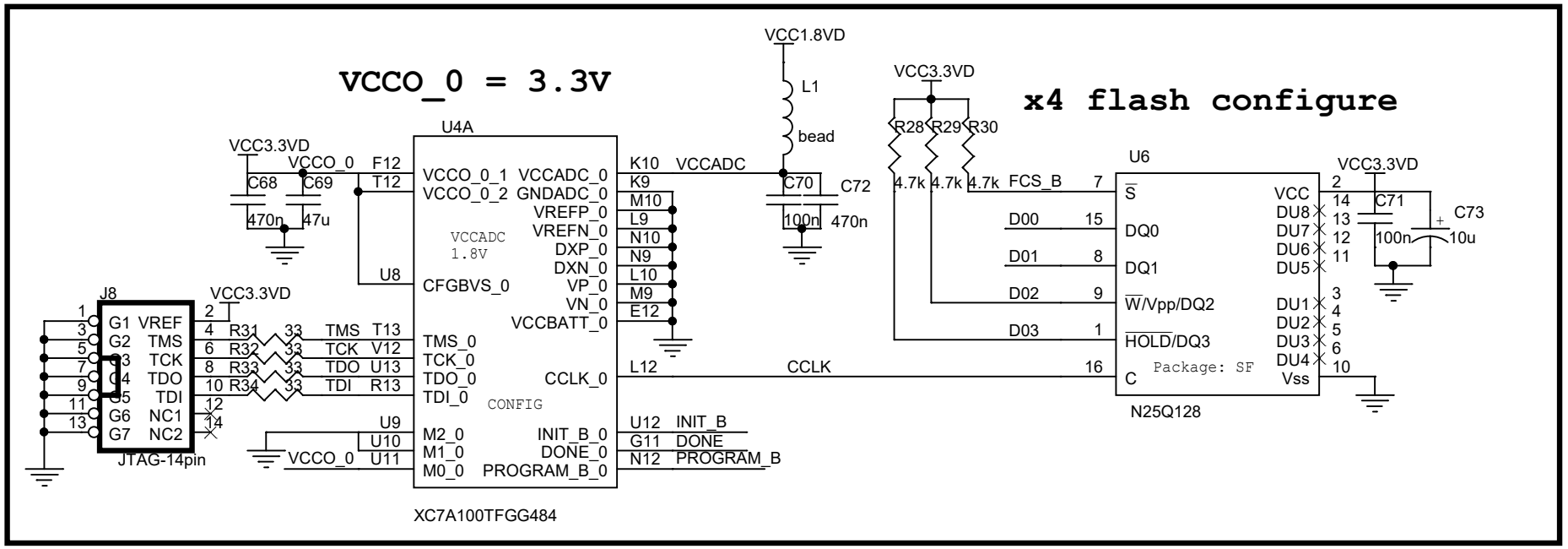
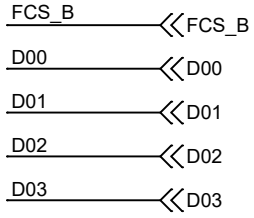
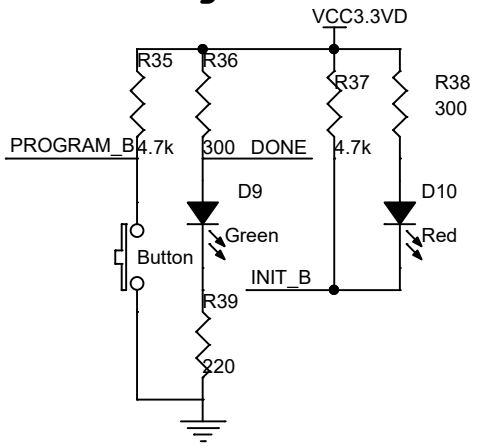


Connect to Bank14



Configure LED



VCCADC: Analog supply for ADC, tied to 1.8V, never be tied to GND even if ADC is not used.
GNDADC、VREFP/N、VP/N、DXP/N tied to GND if ADC is not used.
VCCBATT is requied only when using bitstream encryption. If battery is not used, connect VCCBAT to GND or VCCAUX
M[2:0]: M[2:0] = 001 for master SPI flash mode.
Connect each mode pin either directly, or via a 1k resister to VCCO_0 or GND.
INIT_B: this pin acts as an indicator for CRC error.
PROGRAM_B: Active-Low asynchronous full-chip reset.
PUDC_B:Controls IO pull-up resistor during configuration.
0=Pull-up resistor during configuration
1=3-State output during configuration
EMCCLK:An input for supplying an external configuration clock(optional)
FCS_B: Drive the SPI flash SS/pin Low during configuration to enable the SPI flash.
DOUT: Only used in x1 SPI flash configuration.
DONE: Active-High signal indicating configuration is complete.
0 = FPGA not configured.
1 = FPGA configured.
CFGBVS: For the Axtix and Kintex, this pin determines the voltage standard supported in the configuration IO banks.
1 = 2.5V or 3.3V
0 = 1.8V or less

Title: **SDHCal DAQ**		
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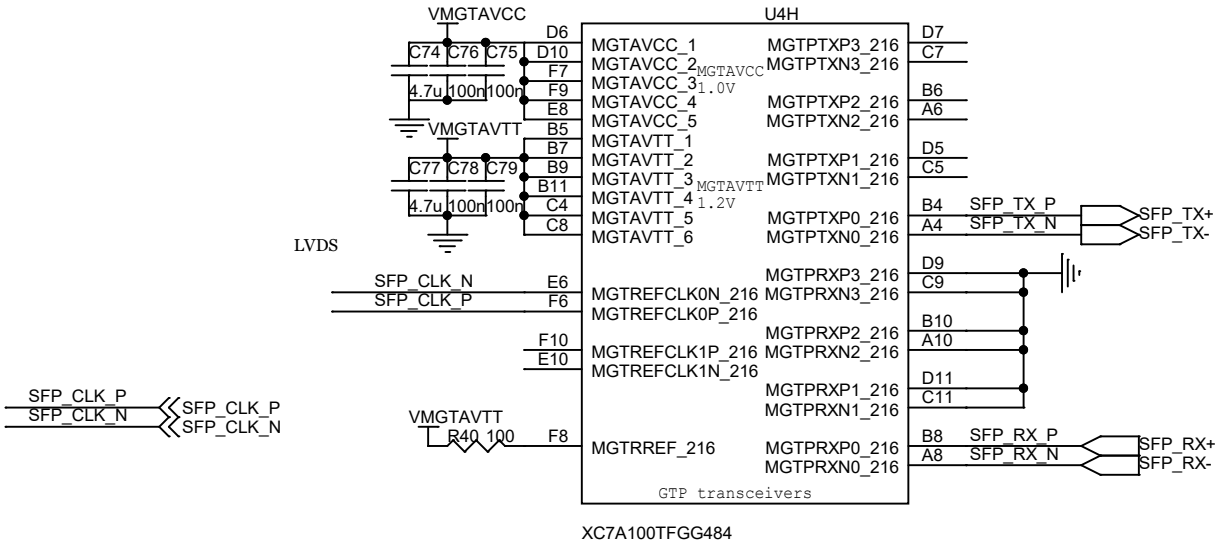
Capacitor	Package Pins MGTAVCC	MGTAVTT	GND	Value
Cap1	D6		C6	
Cap2	D10		C10	0.1uF
Cap3		C4	C3	
Cap4		B11	B12	

Pin or Pin Pair of the Unused GTP Quad	Connectioon
MGTAVCC	AVCC
MGTAVTT	AVTT
MGTREFCLKP/MGTREFCLKN	Float (if not used)
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Float
MGTRREF	MGTAVTT through a 100Ωresistor

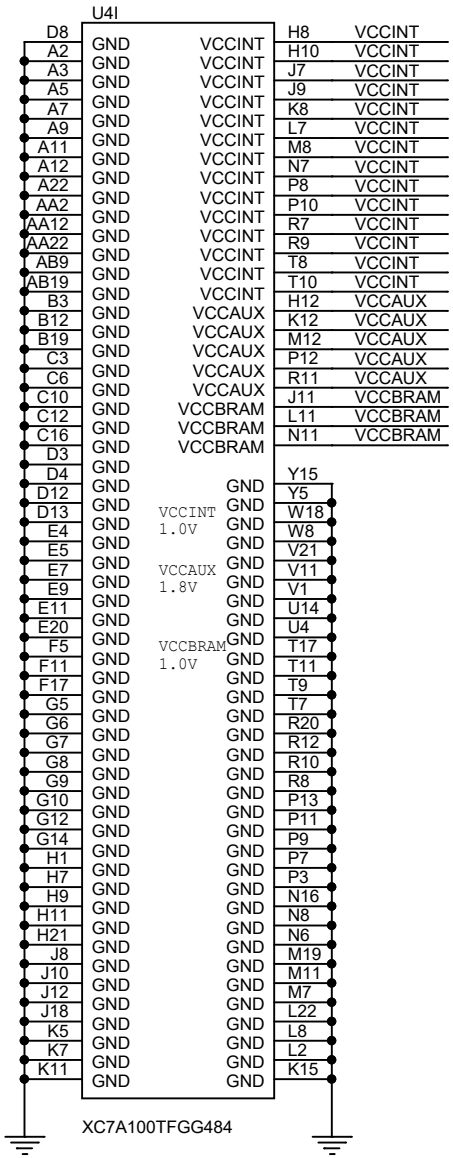


MGTRERCLK: Differential clock input pin pair for the reference clock of the GTP transceiver Quad.
MGTAVCC\MGTAVTT: analog power supply, need 2 dedicated LDO power supply
MGTRREF: Calibration resistor input pin for the termination resistor calibration circuit.
Connect to a 100 ohm resistor that is also connected to MGTAVTT.

Required PCB Capacitor Quantities per Device:Artix7(XC7A100T FGG484)

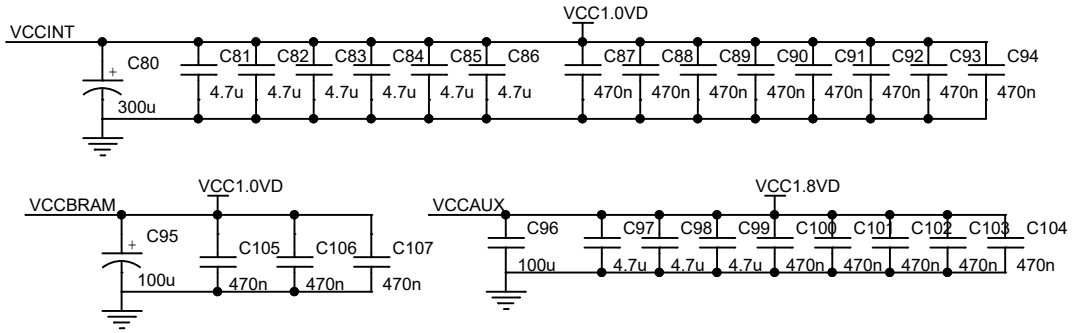
MGTAVCC: 4.7uF(1), 0.1uF(2,SC0402)--> placement(D6-C6,D10-C10) using filled via in pad
MGTAVTT: 4.7uF(1), 0.1uF(2,SC0402)--> placement(C4-C3,B11-B12) using filled via in pad

Title: SDHCal DIF			
Size: A4	Document Number: GTP		Rev: V1.0
Date: Wednesday, April 25, 2018	Sheet 9 of 18		



Required PCB Capacitor Quantities per Device:Artix7(XC7A100T FGG484)

VCCINT: 330uF(1), 4.7uF(6), 0.47uF(8)
VCCBM: 100uF(1), 0.47uF(2)
VCCAUX: 47uF(1), 4.7uF(3), 0.47uF(5)
VCCO(Bank0): 47uF(1)
VCCO: 47uF or 100uF(1), 4.7uF(2), 0.47uF(4)
Capacitor Specifications: >100uF Tantalum, others Ceramic



Title	SDHCal DIF	
Size: A4	Document Number: FPGA Power	Rev: V1.0
Date: Wednesday, April 25, 2018	Sheet 10 of 18	

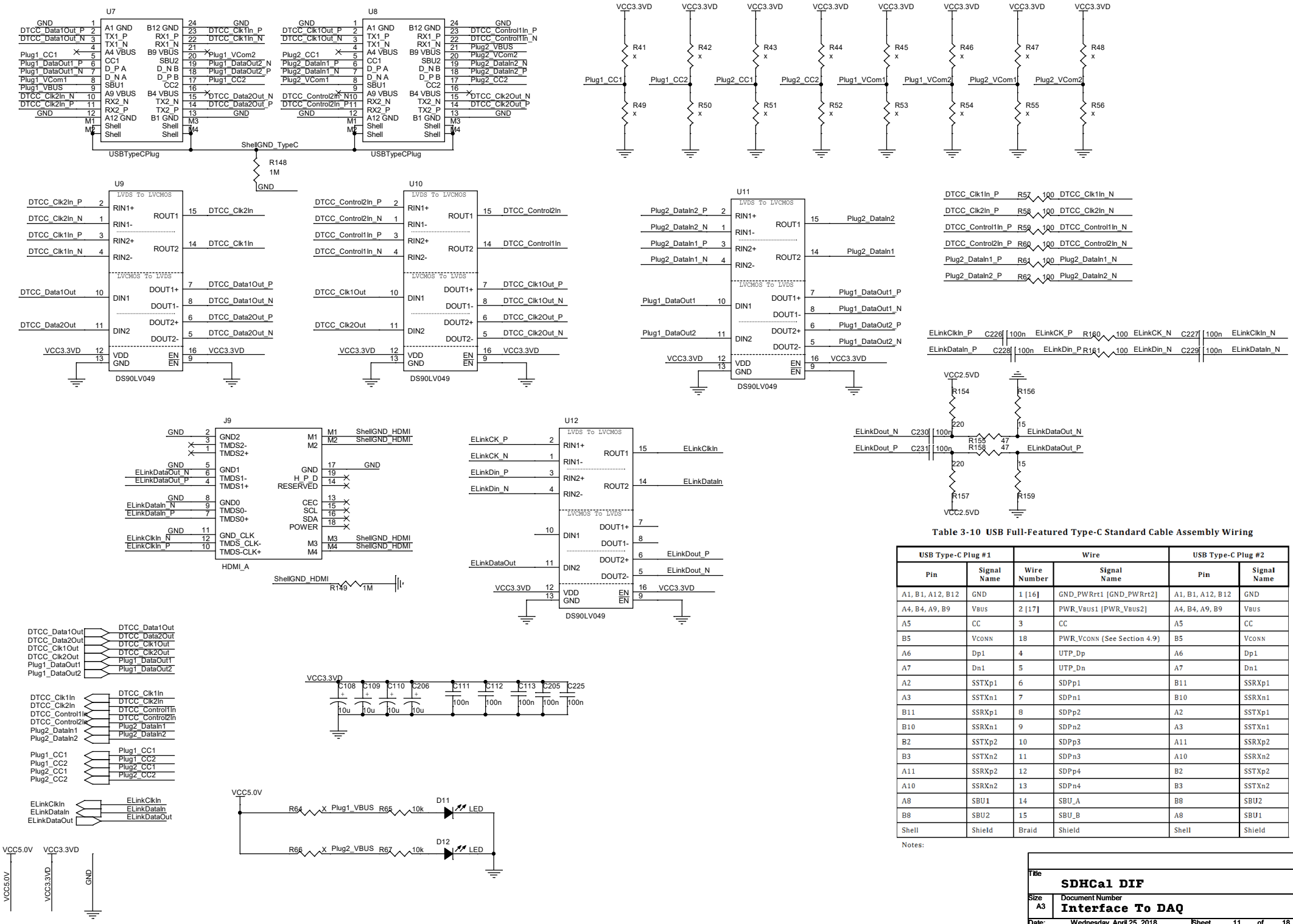


Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	SSTXp1	6	SDPp1	B11	SSRXp1
A3	SSTXn1	7	SDPn1	B10	SSRXn1
B11	SSRXp1	8	SDPp2	A2	SSTXp1
B10	SSRXn1	9	SDPn2	A3	SSTXn1
B2	SSTXp2	10	SDPp3	A11	SSRXp2
B3	SSTXn2	11	SDPn3	A10	SSRXn2
A11	SSRXp2	12	SDPp4	B2	SSTXp2
A10	SSRXn2	13	SDPn4	B3	SSTXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

Title	SDHCal DIF		
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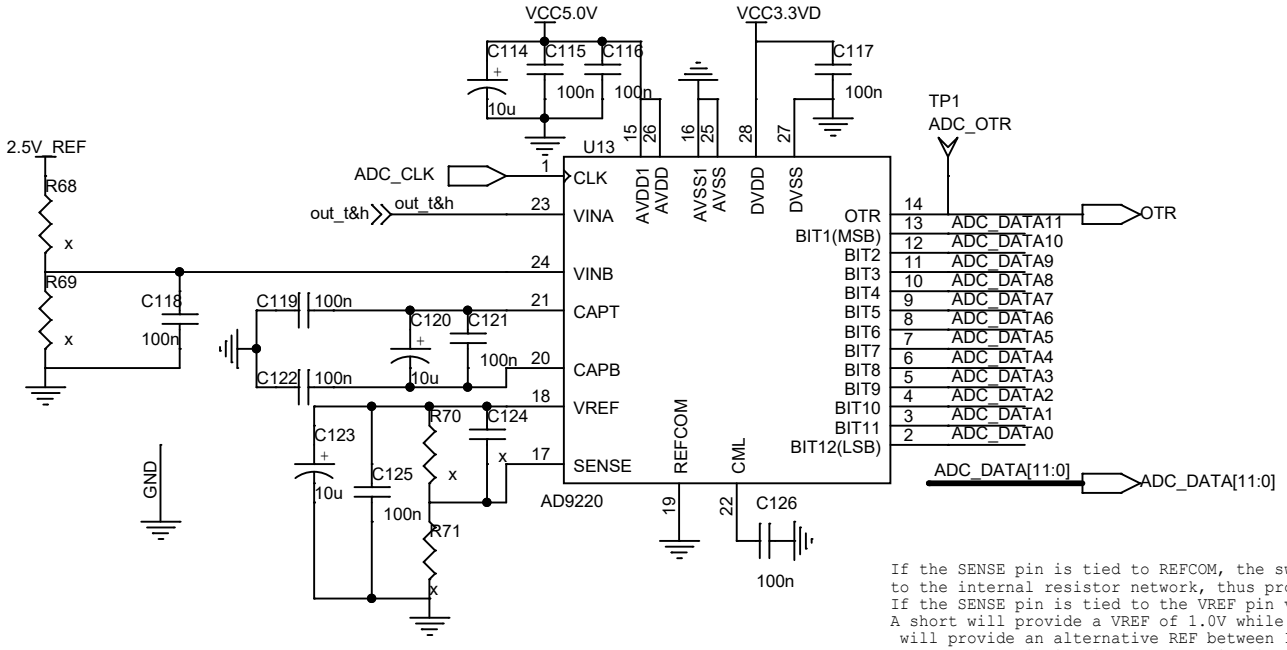

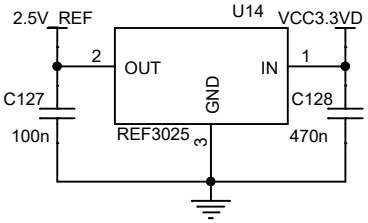

If the SENSE pin is tied to REFCOM, the switch is connected
to the internal resistor network, thus providing a VREF of 2.5V
If the SENSE pin is tied to the VREF pin via a short or resistor.
A short will provide a VREF of 1.0V while an external resistor
will provide an alternative REF between 1.0 and 2.5V.
If the SENSE pin is tied to AVDD, it will disabling the reference amplifier
allows the VREF pin to be driven by an external voltage reference
VREF = (1+R1/R2)

Title: **SDHCAL DIF**		
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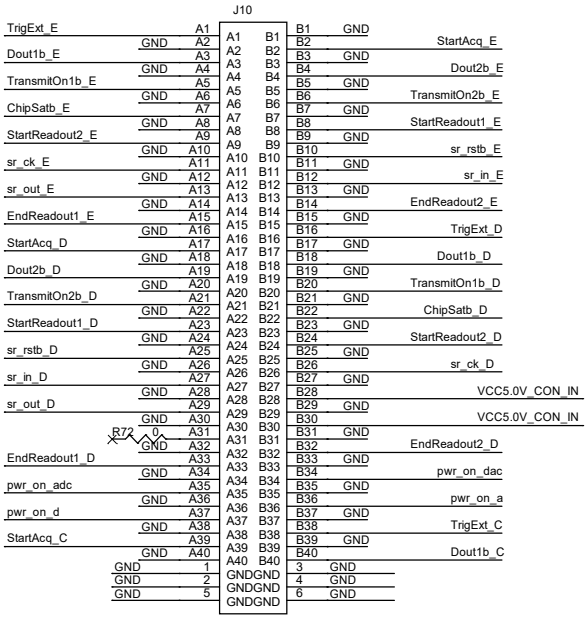
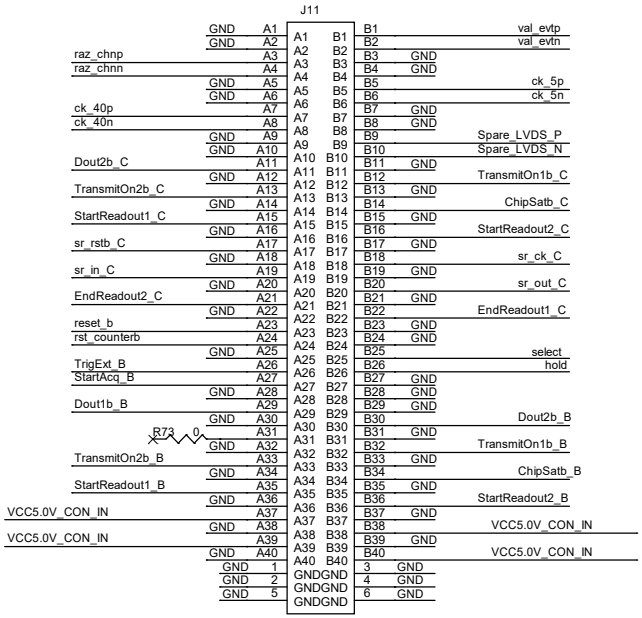
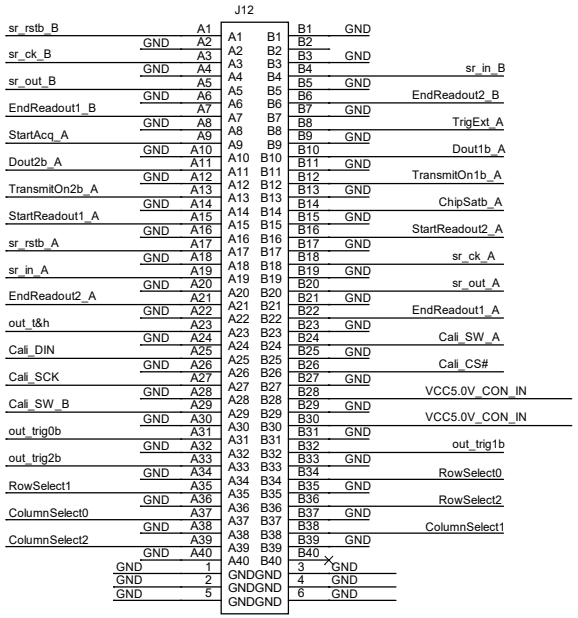
The B pins is forward to the innerside of board



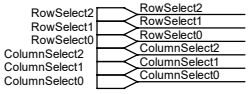




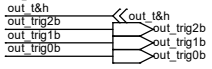
! ! ! **Warnning: The male connector and female connector has different footprint and package.**
The A1 pin of male connector is connected to the A1 pin of female connector, B1(male) connect to B1(female) ...
Note that this is different from ECal system but the signal connection is the same.

Female connector ERNI154744 on FEB
Male connector ERNI 154767 on DIF

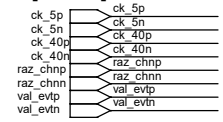
Row and Column select:
6 pins



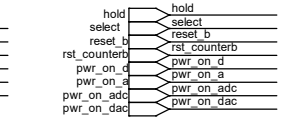
Test signal:
4 pins



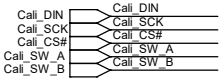
LVDS signals:
5 pairs 10pins

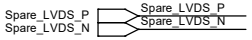


Common control signal:
8 pins

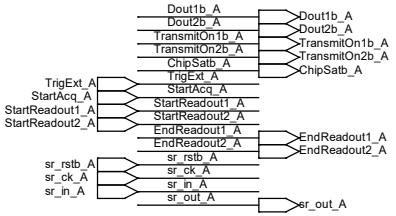


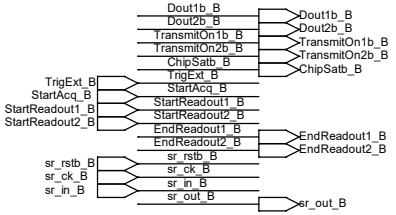
Calibration control:
5 pins

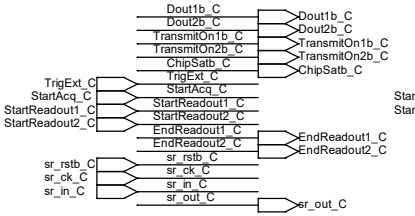


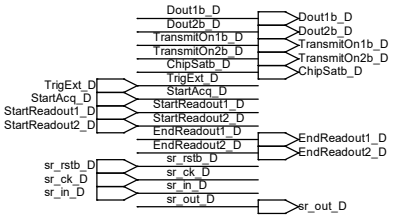


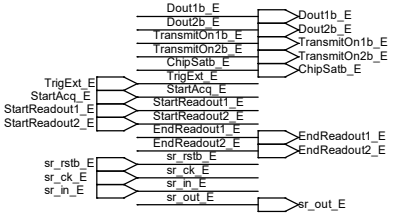
Independent control signals for each chain:
15*5 = 75 pins

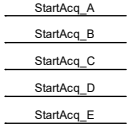




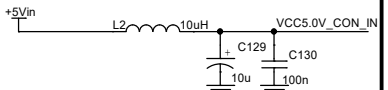


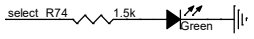






Power for FEB





Title	SDHCal DIF	
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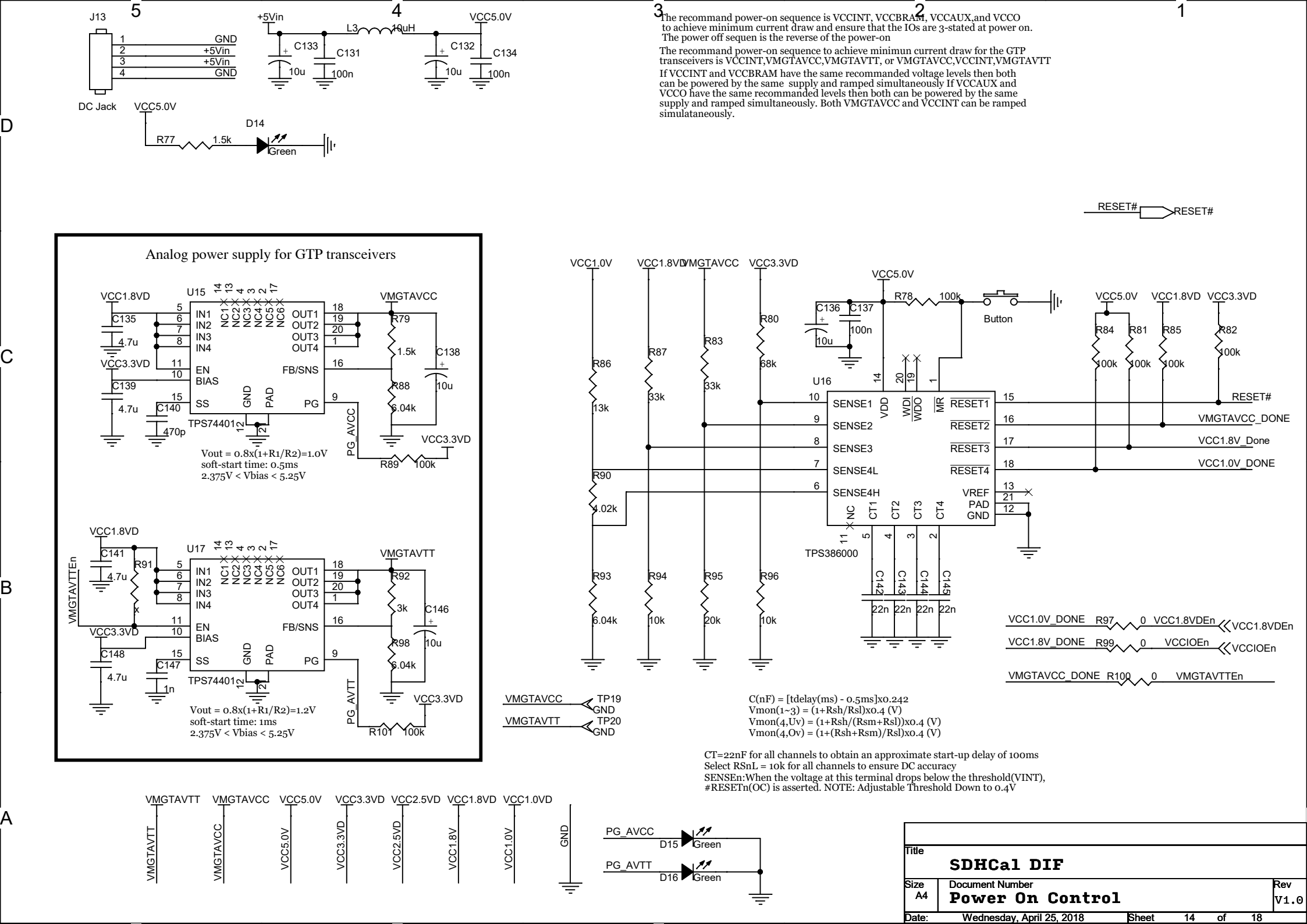
J13
GND
+5Vin
+5Vin
GND
DC Jack
VCC5.0V
D14
R77
1.5k
Green
+5Vin
L3
10uH
C133
C131
C132
C134
10u
100n
VCC5.0V
The recommand power-on sequence is VCCINT, VCCBRAM, VCCAUX,and VCCO to achieve minimum current draw and ensure that the IOs are 3-stated at power on. The power off sequen is the reverse of the power-on
The recommand power-on sequence to achieve minimun current draw for the GTP transceivers is VCCINT,VMGTAVCC,VMGTAVTT, or VMGTAVCC,VCCINT,VMGTAVTT
If VCCINT and VCCBRAM have the same recommanded voltage levels then both can be powered by the same supply and ramped simultaneously If VCCAUX and VCCO have the same recommanded levels then both can be powered by the same supply and ramped simultaneously. Both VMGTAVCC and VCCINT can be ramped simulataneously.
RESET#
RESET#
Analog power supply for GTP transceivers
VCC1.8VD
U15
TPS74401
VMGTAVCC
C135
4.7u
VCC3.3VD
C139
4.7u
C140
470p
R79
1.5k
C138
10u
R88
6.04k
R89
100k
VCC3.3VD
PG_AVCC
Vout = 0.8x(1+R1/R2)=1.0V
soft-start time: 0.5ms
2.375V < Vbias < 5.25V
VCC1.8VD
U17
TPS74401
VMGTAVTT
VMGTAVTTEn
C141
4.7u
R91
x
VCC3.3VD
C148
4.7u
C147
1n
R92
3k
C146
10u
R98
6.04k
R101
100k
VCC3.3VD
PG_AVTT
Vout = 0.8x(1+R1/R2)=1.2V
soft-start time: 1ms
2.375V < Vbias < 5.25V
VCC1.0V
VCC1.8VD
VMGTAVCC
VCC3.3VD
R86
13k
R87
33k
R83
33k
R80
68k
R90
4.02k
R93
6.04k
R94
10k
R95
20k
R96
10k
VCC5.0V
R78
100k
Button
C136
10u
C137
100n
U16
TPS386000
SENSE1
SENSE2
SENSE3
SENSE4L
SENSE4H
VDD
WDI
WDO
MR
RESET1
RESET2
RESET3
RESET4
VREF
PAD
GND
NC
CT1
CT2
CT3
CT4
C142
C143
C144
C145
22n
22n
22n
22n
VCC5.0V
VCC1.8VD
VCC3.3VD
R84
R81
R85
R82
100k
RESET#
VMGTAVCC_DONE
VCC1.8V_Done
VCC1.0V_DONE
VCC1.0V_DONE R97 0 VCC1.8VDEn
VCC1.8VDEn
VCC1.8V_DONE R99 0 VCCIOEn
VCCIOEn
VMGTAVCC_DONE R100 0 VMGTAVTTEn
VMGTAVCC TP19 GND
VMGTAVTT TP20 GND
C(nF) = [tdelay(ms) - 0.5ms]x0.242
Vmon(1~3) = (1+Rsh/Rsl)x0.4 (V)
Vmon(4,Uv) = (1+Rsh/(Rsm+Rsl))x0.4 (V)
Vmon(4,Ov) = (1+(Rsh+Rsm)/Rsl)x0.4 (V)
CT=22nF for all channels to obtain an approximate start-up delay of 100ms
Select RSnL = 10k for all channels to ensure DC accuracy
SENSEn:When the voltage at this terminal drops below the threshold(VINT), #RESETn(OC) is asserted. NOTE: Adjustable Threshold Down to 0.4V
VMGTAVTT
VMGTAVCC
VCC5.0V
VCC3.3VD
VCC2.5VD
VCC1.8V
VCC1.0V
GND
PG_AVCC
D15
Green
PG_AVTT
D16
Green
Title
SDHCal DIF
Size
A4
Document Number
Power On Control
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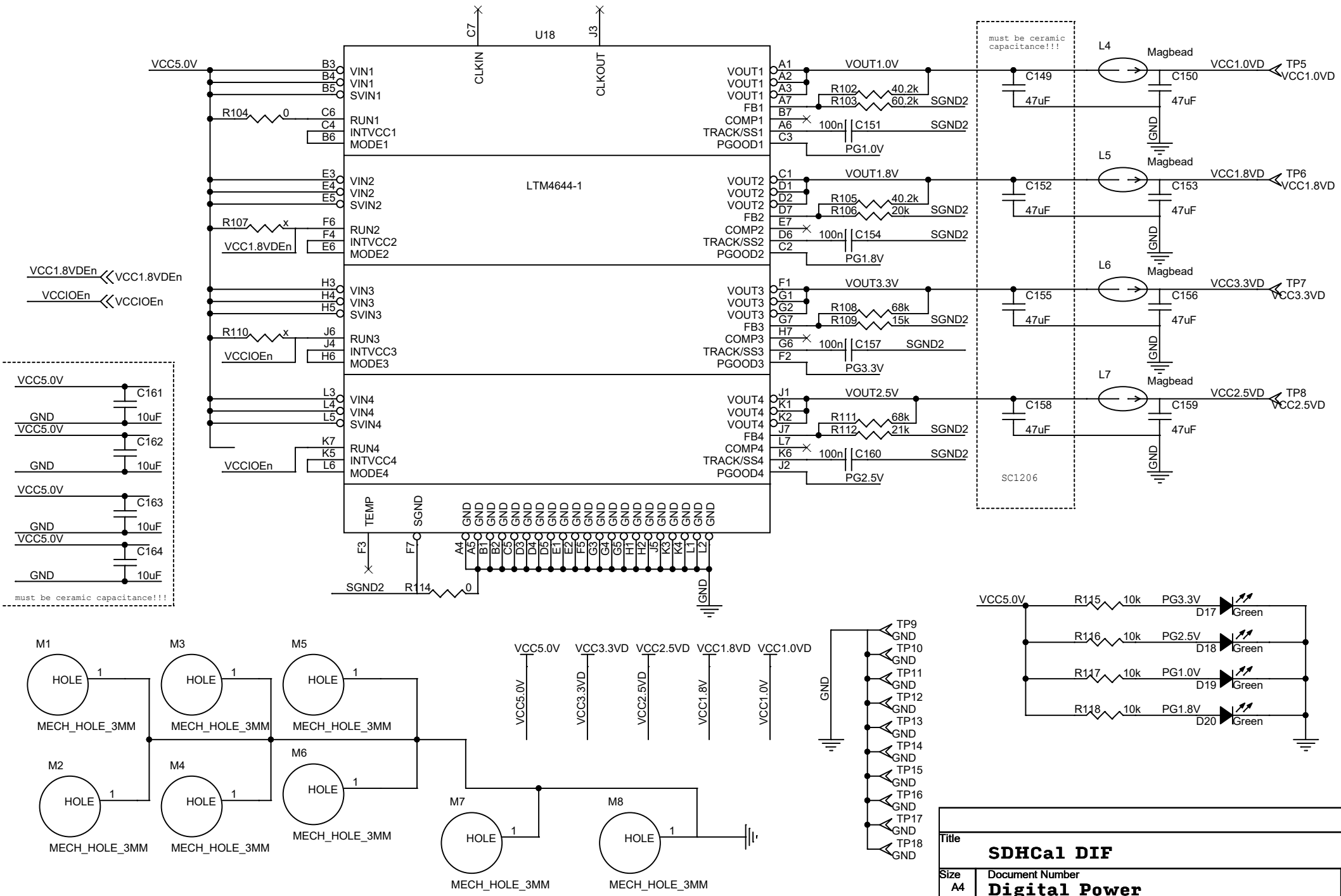
U18
LTM4644-1
C7
CLKIN
J3
CLKOUT
VCC5.0V
VIN1
VIN2
VIN3
VIN4
SVIN1
SVIN2
SVIN3
SVIN4
RUN1
RUN2
RUN3
RUN4
INTVCC1
INTVCC2
INTVCC3
INTVCC4
MODE1
MODE2
MODE3
MODE4
R104 0
R107 x
R110 x
R102 40.2k
R103 60.2k
R105 40.2k
R106 20k
R108 68k
R109 15k
R111 68k
R112 21k
VOUT1.0V
VOUT1.8V
VOUT3.3V
VOUT2.5V
FB1
FB2
FB3
FB4
COMP1
COMP2
COMP3
COMP4
TRACK/SS1
TRACK/SS2
TRACK/SS3
TRACK/SS4
100n C151 SGND2
100n C154 SGND2
100n C157 SGND2
100n C160 SGND2
PG1.0V
PG1.8V
PG3.3V
PG2.5V
PGOOD1
PGOOD2
PGOOD3
PGOOD4
TEMP
SGND
SGND2
R114 0
must be ceramic capacitance!!!
C149 47uF
C150 47uF
C152 47uF
C153 47uF
C155 47uF
C156 47uF
C158 47uF
C159 47uF
L4 Magbead
L5 Magbead
L6 Magbead
L7 Magbead
VCC1.0VD
VCC1.8VD
VCC3.3VD
VCC2.5VD
TP5 VCC1.0VD
TP6 VCC1.8VD
TP7 VCC3.3VD
TP8 VCC2.5VD
SC1206
VCC1.8VDEn
VCCIOEn
C161 10uF
C162 10uF
C163 10uF
C164 10uF
must be ceramic capacitance!!!
M1 HOLE MECH_HOLE_3MM
M2 HOLE MECH_HOLE_3MM
M3 HOLE MECH_HOLE_3MM
M4 HOLE MECH_HOLE_3MM
M5 HOLE MECH_HOLE_3MM
M6 HOLE MECH_HOLE_3MM
M7 HOLE MECH_HOLE_3MM
M8 HOLE MECH_HOLE_3MM
VCC5.0V VCC3.3VD VCC2.5VD VCC1.8VD VCC1.0VD
GND
TP9 GND
TP10 GND
TP11 GND
TP12 GND
TP13 GND
TP14 GND
TP15 GND
TP16 GND
TP17 GND
TP18 GND
R115 10k PG3.3V D17 Green
R116 10k PG2.5V D18 Green
R117 10k PG1.0V D19 Green
R118 10k PG1.8V D20 Green
Title
SDHCal DIF
Size A4
Document Number
Digital Power
Rev V1.0
Date: Thursday, April 26, 2018
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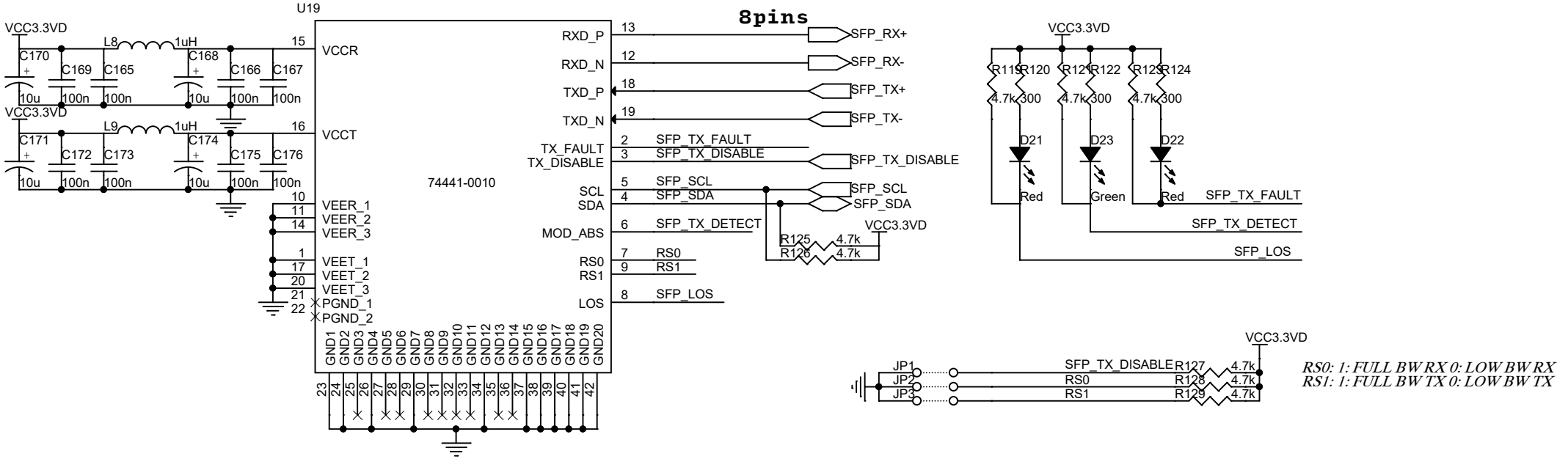

pin 9在sfp中应该连地，在sfp+中可以作为选择速度的管脚接高。但此处应该直接连接地。

Electronic 74441-0010

Cage: 74754-0101

TX Fault is an open collector/drain output, which should be pulled up with a 4.7K~10Kohm resistor on the host board. Pull up voltage between 2.0V and VccT, R+0.3V. When high, output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.
TX disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7k~10 K ohm resistor. Its states are:
Low (0 ~0.8V): Transmitter on
(>0.8, < 2.0V): Undefined
High (2.0 ~3.465V): Transmitter Disabled
Open:Transmitter Disabled

Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7K~10K ohm resistor on the host board. The pull-up voltage shall be VccT or VccR
Mod-Def0 is grounded by the module to indicate that the module is present
Mod-Def1 is the clock line of 2 wire serial interface for serial ID
Mod-Def2 is the data line of 2 wire serial interface for serial ID

Rate Select(I): is used to control the receiver bandwidth for compatibility with multiple data rates. If implemented, the input will be internally pulled down with > 30k?resistor. The input states are:
Low/Open,Reduced Bandwidth;High,full Bandwidth
LOS:high indicates the received optical power is below the worst-case receiver sensitivity Low indicates normal operation

VccR and VccT are the receiver and transmitter power supplys.
They are defined as 3.3V,5% at the SFP connector pin

Title: **SDHCal DIF**		
Size: A4	Document Number: **SFP**	Rev: V1.0
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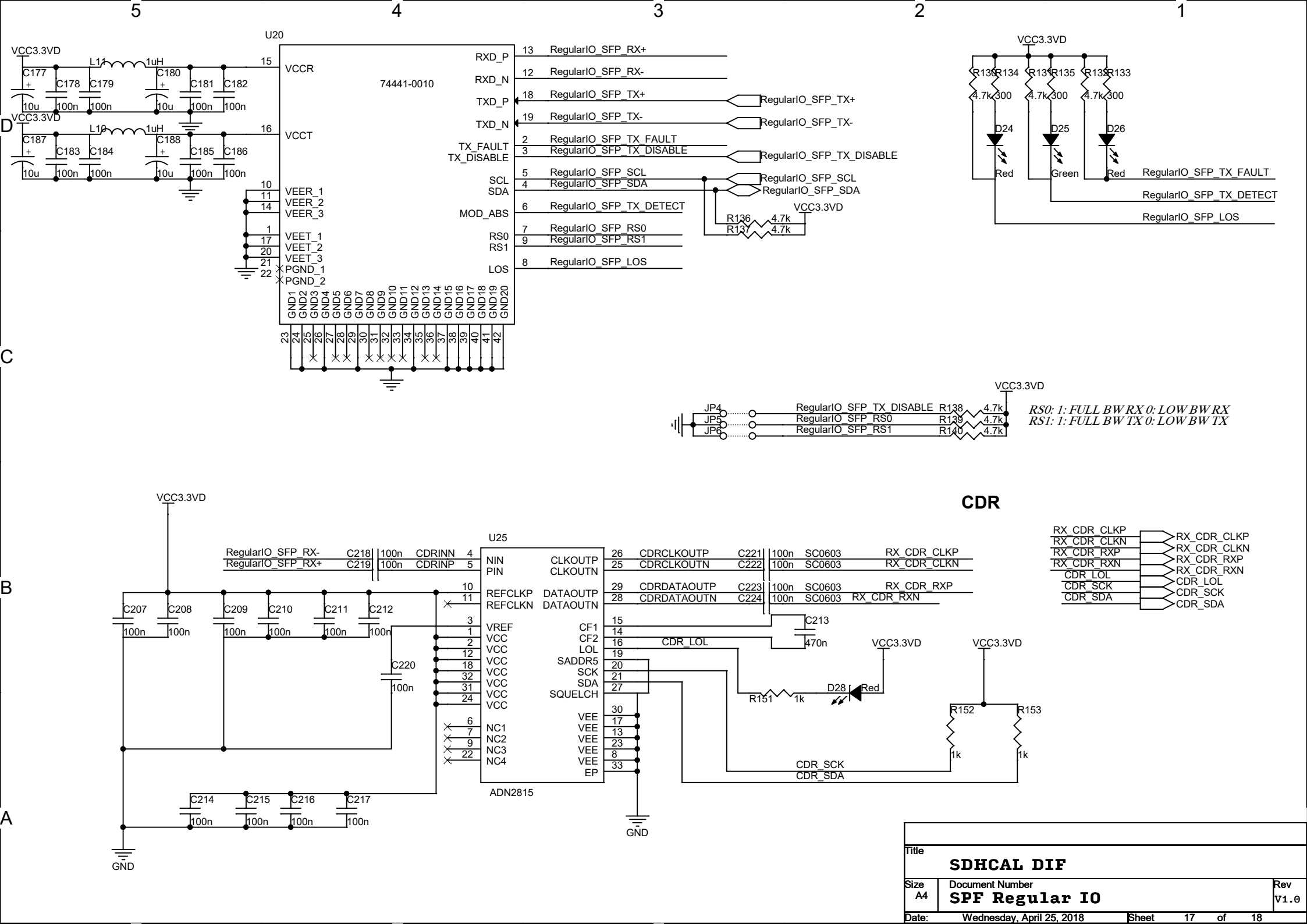

Title	SDHCAL DIF	
Size A4	Document Number SPF Regular IO	Rev V1.0
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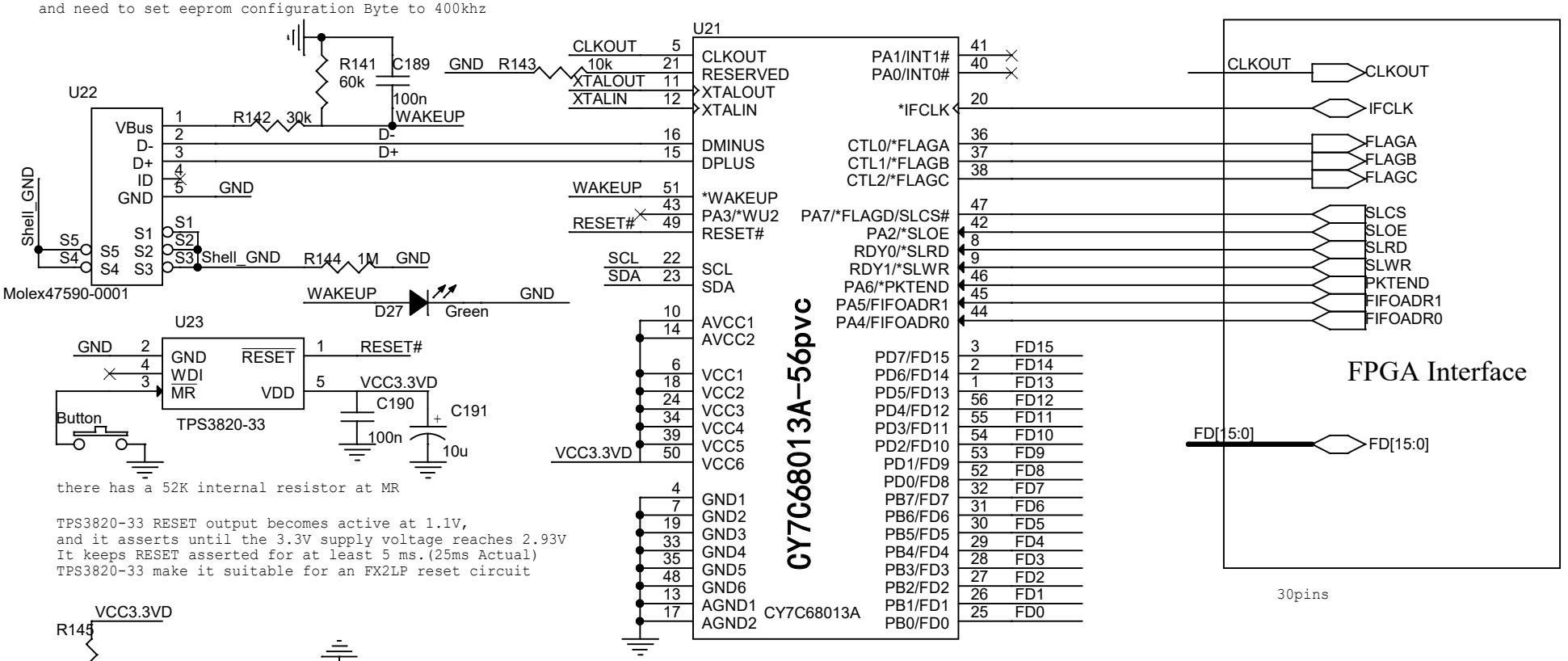
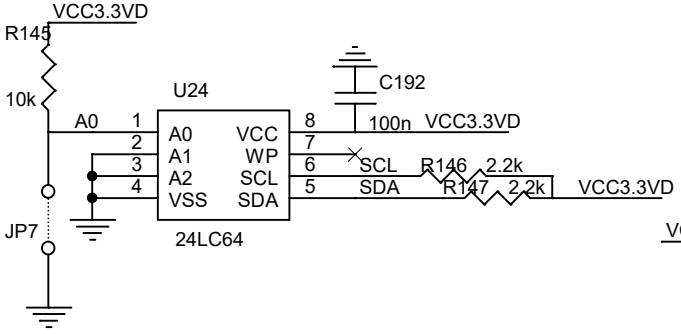
USB2.0 Slave FIFO mode

FX2LP into a low-power(sleep) state until VBUS is reapplied
and need to set eeprom configuration Byte to 400khz



there has a 52K internal resistor at MR

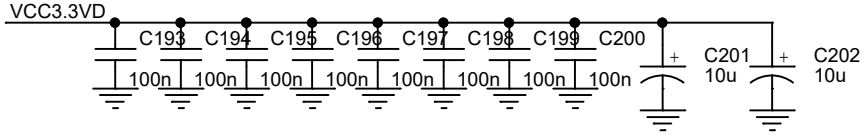
TPS3820-33 RESET output becomes active at 1.1V,
and it asserts until the 3.3V supply voltage reaches 2.93V
It keeps RESET asserted for at least 5 ms.(25ms Actual)
TPS3820-33 make it suitable for an FX2LP reset circuit



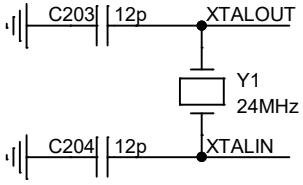
Note: CLKOUT pin should be connected to a FPGA's dedicated clock input pin

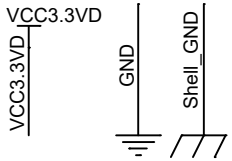
Note: IFCLK should not connected to a FPGA's input-only pin

Power decoupling



EEPROM should be write protect,but it is not necessary





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