Presentation of the front-end “ROC” chips readout for ECAL and HCAL ILC calorimeters

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Abstract

The OMEGA group at LAL has designed 3 chips for the ILC calorimeters. Two are dedicated to the hadronic calorimeters (SPIROC for the analog one and HARDROC for the digital one) and the third for the electromagnetic calorimeter (SKIROC).
These front-end ASICs must ensure a data format uniformity in all the calorimeters to allow a standardised detector interface board (DIF). The main requirement for data transfer is the minimization of power dissipation as all chips are embedded inside the detector. Data lines must also be minimized as the detector front-end boards need to be abuttable to reach a length of several meters. The readout system is based on the token ring protocol and all critical data lines are doubled for redundancy. The readout and the management of these 3 chips are explained in detail in section 2 and 4.
The section 3 of this paper is dedicated to the Power On Digital (POD) module which is necessary to manage the 40 MHz and 5 MHz clocks during the readout and thus allows to fulfil the 10-25 µW per channel requirement.

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1 Introduction to “ROC” chips family for CALICE/EUDET

1.1 SKIROC for the ECAL

SKIROC (Silicon Kalorimeter ReadOut Chip) has been designed to read-out the upcoming generation of Si-W calorimeter [1] matching the future International Linear Collider (ILC) requirements. The SKIROC2 chip handles 64 channels with a 15 depth analog memory. The digital part integrates a 4K bytes memory to handle the converted charge and time from the internal ADC. A snapshot of the layout is displayed in figure 1.

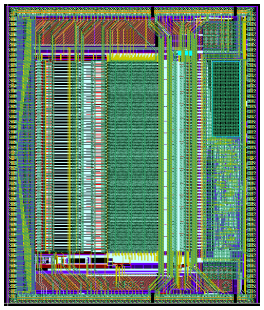

Figure 1: SKIROC2 chip layout

1.2 SPIROC for the AHCAL

SPIROC (Silicon Photomultiplier Integrated ReadOut Chip) is a 36 channels dedicated front-end electronics [2] for an ILC prototype of an Analog Hadronic CALorimeter (AHCAL) equipped with Silicon photomultiplier readout. Each channel integrates a 16 depth analog memory. This Switched Capacitor Array (SCA) is controlled by the digital part [3] built around 2 memories of 2K bytes. A picture of the layout is shown in figure 2.

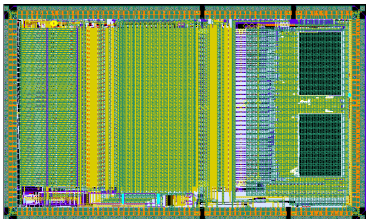

Figure 2: SPIROC2 chip layout

1.3 HARDROC for the DHCAL

HARDROC (HAdronic Rpc Detector ReadOut Chip) is the front end chip [4] designed for the readout of the RPC or Micromegas foreseen to equip the Digital Hadronic CALorimeter (DHCAL) of the future ILC. HARDROC readout is a semi-digital readout which integrates 5 0.5K bytes memories to store 127 events. These memories can be seen on the right side of the layout below in figure 3.

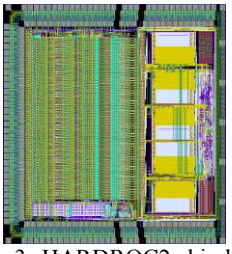

Figure 3: HARDROC2 chip layout

2 Digital readout and ILC phases

2.1 ILC phases

The future ILC is made of 1 ms short trains with bunch to bunch separation of 300 ns interrupted by 200 ms long empty intervals (figure 4). This beam structure allows to perform the acquisition and memorization of the events (acquisition phase) when the beam trains are colliding and to convert and output the data during the inter bunch breaks (conversion and readout phases).
In this paper, power considerations will be treated only from the digital point of view (section 3) but these ILC phases will also be interesting for the power management of the internal analog cells in the chips. For example, preamplifiers and shapers can be shut down during the conversion and readout as there are only useful during the acquisition. Besides, to meet power budget, the power pulsing mode has been generalised.

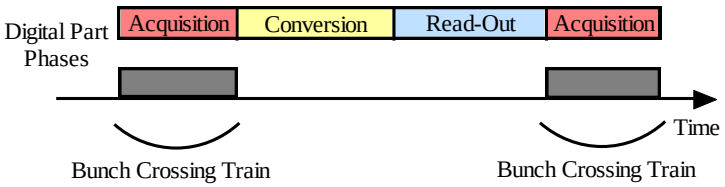

Figure 4: ILC timing requirements

2.2 Similarity between ILC phases and digital part

Due to the machine beam structure, the digital part is guided by different phases. These phases are sent to the ASIC through command boards (DAQ, DIF, and CCC) [5] using digital signals of the CALICE DAQ.
Depending on the chip, there are 2 or 3 phases: the analog to digital conversion phase is only needed for the chips where events are stored in an analog way (in an analog memory). This is the case for SPIROC and SKIROC chips. On the contrary, HARDROC stores every discriminated signal directly into an integrated digital memory, so no conversion is needed. All the chips integrate an acquisition phase to memorize events and a readout phase to empty the memory. The general digital structure of a chip is shown in figure 5.

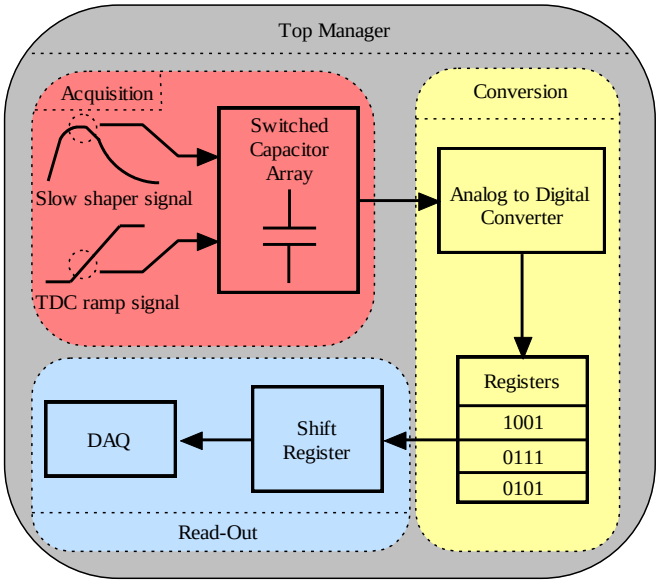

Figure 5: High level working

2.3 Global sequencing and general timings

The readout system is based on a token ring to allow a whole bunch of ASICs to be read out by one output line, using the same protocol (in fact 2 lines for reliability). The digital signals of these ASICs are open collector and can be daisy chained to limit to a bare minimum the number of the output lines on the detector where the chips are embedded.
The global sequencing is made around 3 signals coming from the DAQ: *StartAcquisition*, *StartConversionb* and *StartReadout* [6].
As the acquisition and conversion phases are active at the same time for all the ASICs, these signals are generated by the DAQ and distributed in parallel to all the ASICs. Conversely, as the readout must be sequential to limit the number of output lines, the associated signals go from one ASIC to the next one.
In response to these 3 signals, the ASICs answer with 2 signals. The first one, *ChipSat*, is common to all the ASICs: it consists of a wired OR of each ASIC's local *ChipSat*. If its rising edge occurred during acquisition, it tells the DIF when one or more ASICs are full (figure 6), otherwise it notifies the DIF when the conversion could start (figure 7). On its falling edge, it informs when the internal analog to digital conversion is finished.
The second one is the daisy chain *EndReadout* which starts the readout of the following chip in the chain. The global sequencing is different whether the chip is full during the acquisition (figure 6) or not (figure 7).

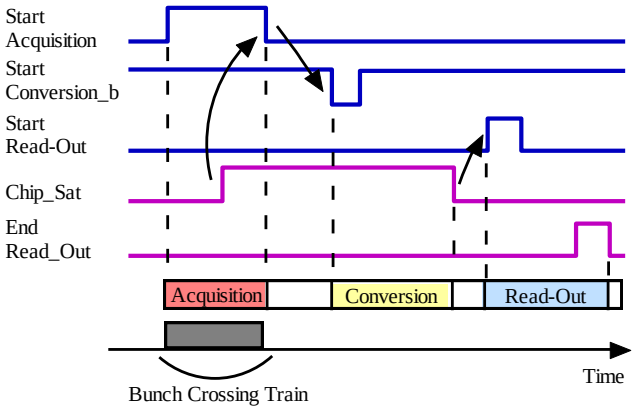

Figure 6: Global sequencing with chip full during acquisition

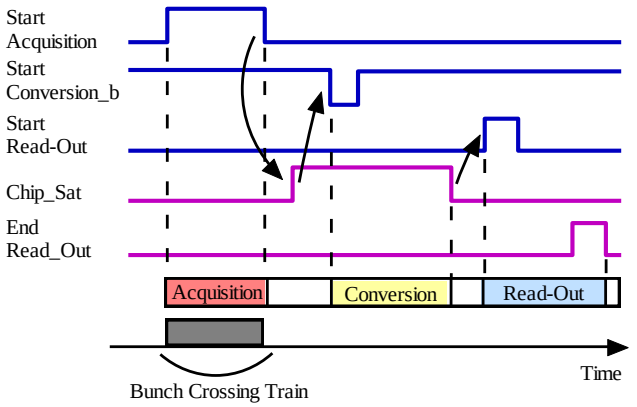

Figure 7: Global sequencing with chip not full during acquisition

The maximum duration of each phase of the sequence are given in the table 1 below. For each cycle of 200 ms, an ASIC should be powered during only 10 ms (5% of cycle) which stands for the worst case (i.e. ASIC full). To minimize the power consumption, the ASICs should be powered during this time only. This is the purpose of the Power On Digital (POD) module described in next section.

Table 1: ASIC timings

Phase	Duration	Comments
Acquisition	1 ms	Bunch crossing train duration
Conversion	4 ms	Worst case (SKIROC2 chip)
Readout	5 ms	5 MHz readout clock

3 Power On Digital (POD) module

In this entire section, timings diagrams were made using a *FastClock* of 40 MHz and a *SlowClock* of 5 MHz as typical values. For other frequencies, timings can be calculated by using the given multiples of clock ticks.

3.1 Block diagram

The POD module has been design to meet the ILC power budget which is lower than 25 µW per channel. In a first approach, its behaviour can be described as a "clock-gating" controller: it allows to start or stop clocks depending on the sequencing of the 3 phases.
In addition, it also handles the management of the LVDS receiver by switching off its bias current when it is not used. Its block diagram is visible in figure 8.

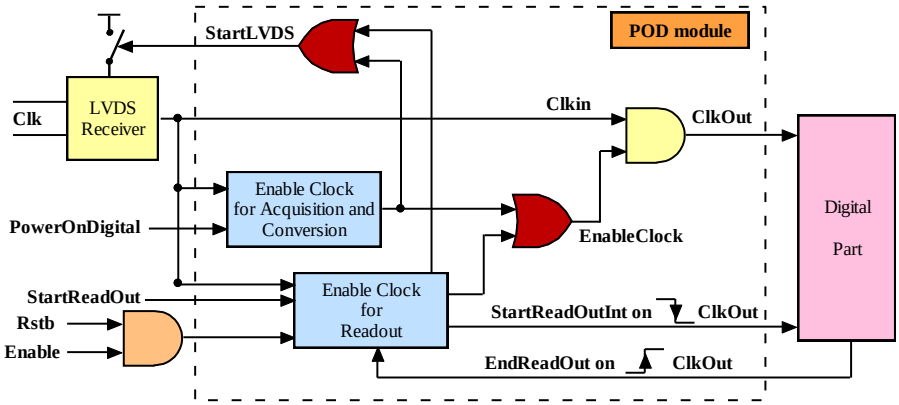

Figure 8: Block diagram

The POD module is divided in 3 parts. One is activated by the *PowerOnDigital* signal coming from the DAQ during the common phases (acquisition and conversion). The second one is set during the readout by the daisy chain token signal: *StartReadout*. The last one is used to handle the LVDS receiver bias.

3.2 Detailed working

The timing diagram given below (figure 9) represents the complete sequence driven by the DAQ. It shows the 3 sequences and how they are controlled. The "clock stopped" zones correspond to phases where clocks are not needed: as mentioned above, it represents at least 95% of the cycle time. In these zones, clocks are stopped and LVDS receivers are switched off in order to save power.

As a general rule, for each phase, LVDS receivers are switched ON asynchronously, then clocks are enabled and stopped synchronously.

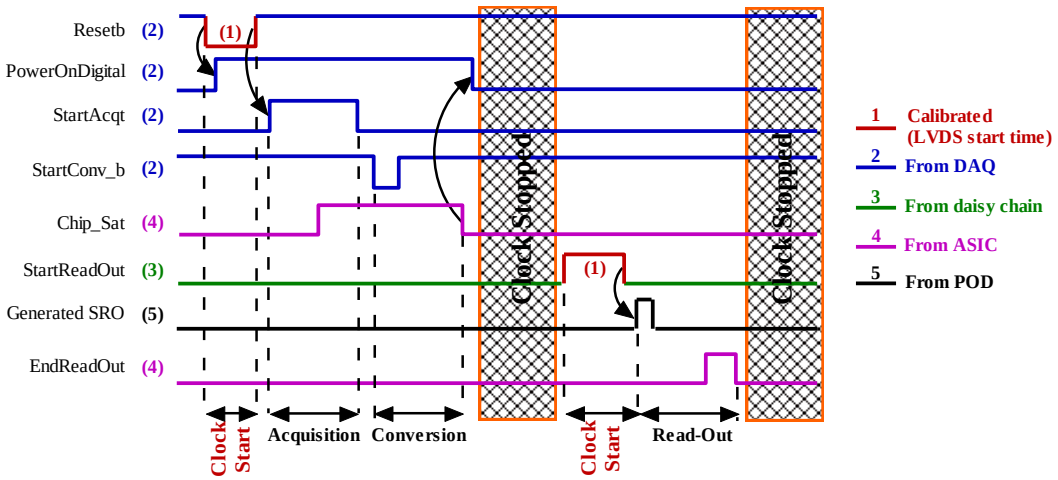

Figure 9: Detailed working

3.2.1 Acquisition phase

As the acquisition phase is common to all the ASICs, the management of the clocks is made by the DAQ through the POD: the global signal involved is *PowerOnDigital*. This signal is set during the reset state before each acquisition. As pointed out above, it will start the LVDS receivers and consequently the clocks. When clocks are established, the reset signal can be released. This can be done after a fixed latency equal to the LVDS receiver start-up time. As a consequence, the reset state is always longer than this wakeup time (see figure 10).

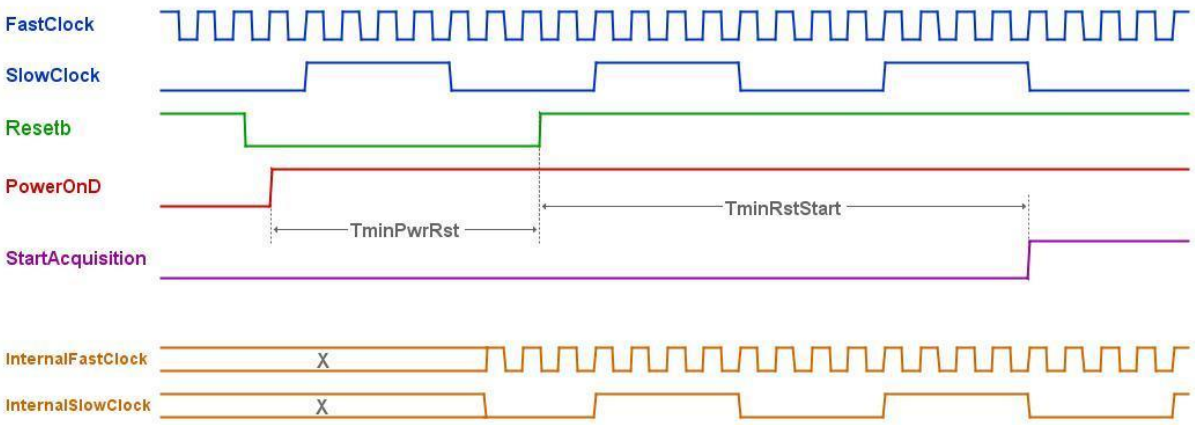

Figure 10: Beginning of acquisition chronogram

The timing corresponding to figure 10 are given below in table 2.

Table 2: Beginning of acquisition timings

Name	Min Duration	Comments
TminPwrRst	200 ns	Time to wake up clock LVDS receivers
TminRstStart	1 µs	4 SlowClock ticks + 4 FastClock ticks (internal management)

3.2.2 Conversion phase

The conversion phase is identical to the previous one because it's a common one managed by the DAQ through the POD. From the point of view of the DAQ, only a *StartAcquisitionb*

signal (negative pulse) should be generated to start this phase. Then, the DAQ waits for the end of the analog to digital conversion by probing the *ChipSat* signal in order to release the *PowerOnD* signal (figure 11). This action stops the clocks synchronously and switches off the LVDS receivers.

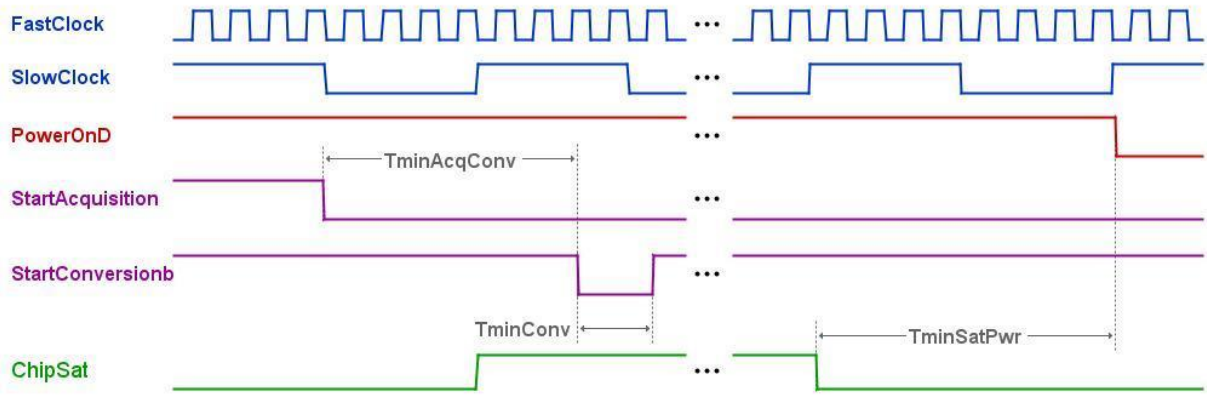

Figure 11: Stop of acquisition and conversion chronogram

The timing corresponding to figure 11 are given below in table 3.

Table 3: Beginning of acquisition timings

Name	Min Duration	Comments
TminAcqConv	1 µs	4 SlowClock ticks + 4 FastClock ticks (internal management)
TminConv	50 ns	2 FastClock ticks (internal management)
TminSatPwr	1 µs	4 SlowClock ticks + 4 FastClock ticks (internal management)

3.2.3 Readout phase

As this phase is managed by the daisy chain, the global *PowerOnD* signal can not be used. This signal is replaced by the daisy chained ones: *EndReadout/StartReadout*. The calibrated *StartReadout* signal stands for a local *PowerOnD* and starts LVDS receivers and clocks. At the end of the readout cycle, the chip generates an *EndReadout* signal which will be used by the following chip in the daisy chain to start its own readout (figure 12).

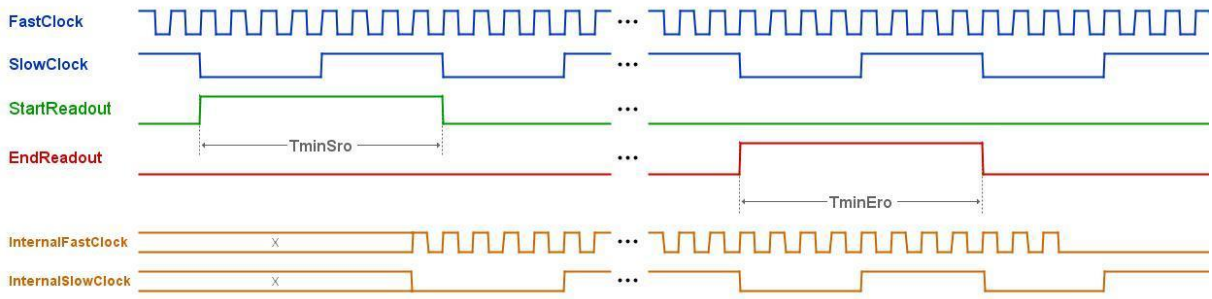

Figure 12: Readout sequence chronogram

The timing corresponding to figure 12 are given below in table 4.

Table 4: Start/End readout signals timings

Name	Min Duration	Comments
TminSro	400 ns	Time to wake up clock LVDS receivers
TminEro	400 ns	Time to wake up clock LVDS receivers of next chip

4 Data readout and memory mapping

4.1 Readout structure

In the chosen structure, all the ASICs are daisy chained: this structure allows to limit the number of lines between ASICs and from/to the DAQ (DIF). Moreover a common serial link is used to transmit data from the ASIC to the DAQ. This link is composed of 2 lines:

- *DataOut* line: data serial link
- *TransmitOn* line: serial link active

As this link is shared by all the ASICs, an open collector bus has been implemented for these 2 lines. This common structure has been integrated in all the "ROC" family chips.

4.2 Memory mapping

The memory mapping of each "ROC" chips are given below (figures 13, 14 and 15). These mappings stand for a maximum number of triggers acquired: chips are full. If not, the number of data sent to the DAQ is reduced. So, the readout frame can be easily determined by looking at these mappings.

As a general rule, the readout frame starts with the MSB bit of the higher address and then stops with the LSB bit of the lower address. Moreover, each address is sent from MSB to LSB bit.

HARDROC chips are able to acquire 127 events on 2 bits for 64 channels. Then, the maximum number of stored data is 20320 bits (figure 13).

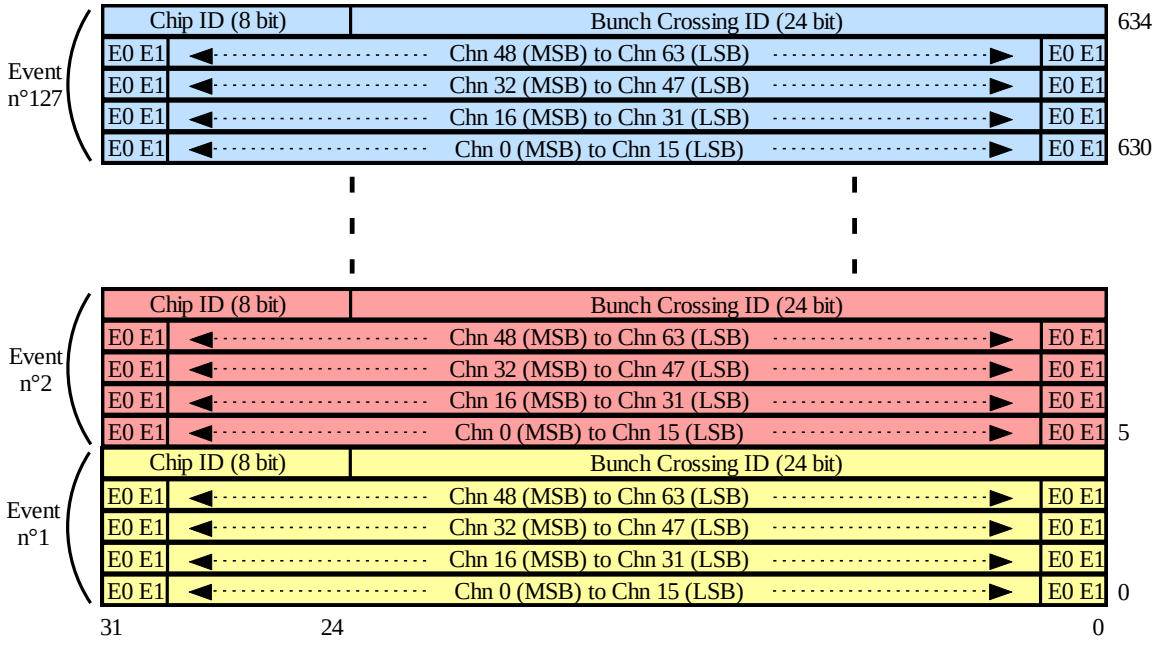

Figure 13: HARDROC memory mapping

SPIROC chips are able to acquire 16 events on 36 channels. As the ADC resolution is 12-bits for charge and time, the maximum number of stored data is 18704 bits (figure 14).

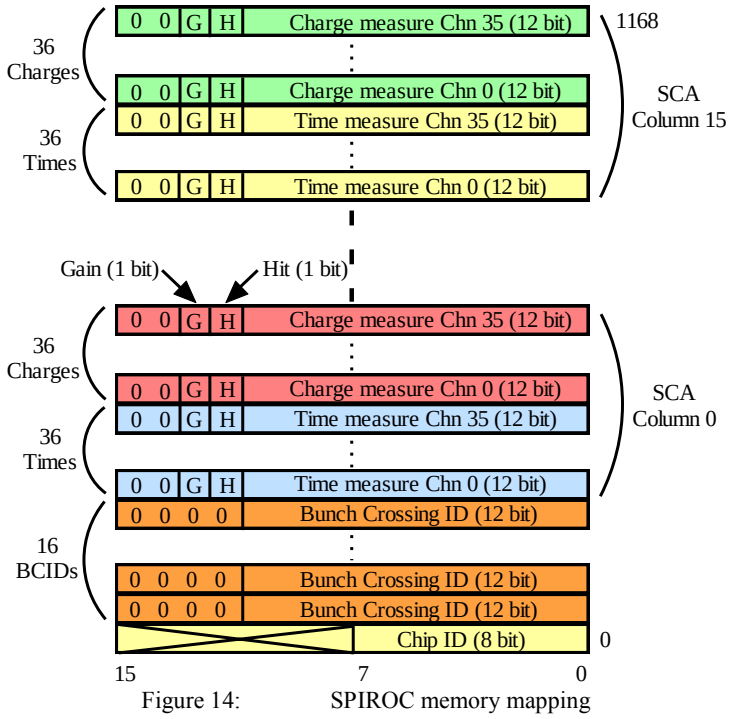

Figure 14: SPIROC memory mapping

SKIROC chips are able to acquire 15 events on 64 channels. The ADC resolution is the same as SPIROC chips so the maximum number of stored data is 30976 bits (figure 15).

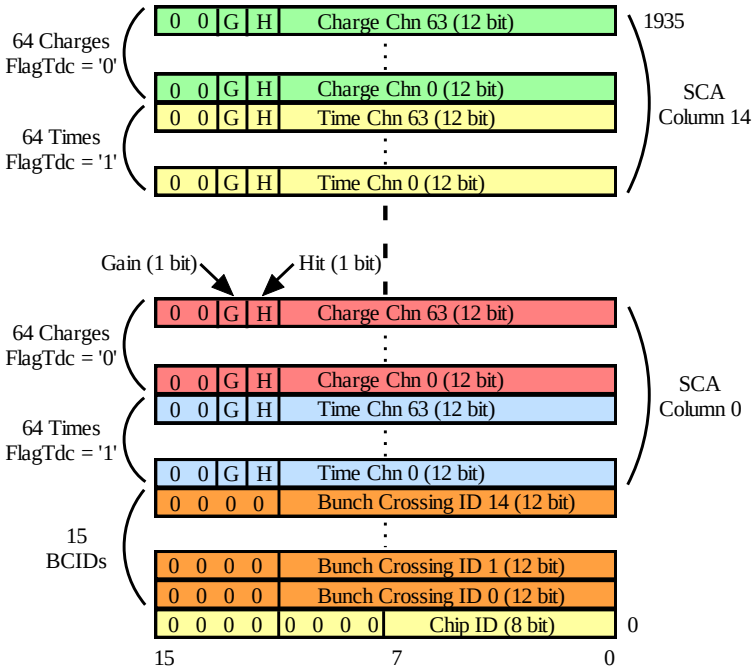

Figure 15: SKIROC2 chip memory mapping

4.3 Readout duration

Assuming the memory mapping given above and the worst case (chips are full), we can extract the total readout duration for each chip. This is given below in table 5.

Table 5: Readout duration

Chip	Readout clock	Number of bits	Total readout duration
HARDROC	5 MHz	20320	4064 µs
SPIROC	5 MHz	18704	3740.8 µs
SKIROC2	5 MHz	30976	6195.2 µs

On the figure 16, we can see a possible integration of 144 ASICs on a PCB (IPNL laboratory).

Figure 16: HARDROC integration on slab @ IPNL

5 Conclusion

The readout and the management of these different chips have been standardized to ease their use. This readout protocol has been validated by the DHCAL detector prototypes. Moreover, analog and digital modules (ADC, Bandgap, memory management, etc.) have been reused from chip to chip to reduce development time.

Acknowledgement

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References

[1] Fleury J. et al, "SKIROC: A front-end chip to read out the imaging silicon-tungsten calorimeter for ILC", IEEE NSS-MIC Conference record 2007, vol. 3, pp. 1847-1850

[2] Raux L. et al., "SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out", IEEE NSS-MIC Conference record 2007, vol. 3, pp. 1857-1860

[3] Dulucq F. et al., "Digital part of SiPM Integrated Read-Out Chip ASIC for ILC hadronic calorimeter", TWEPP 2007 conference proceedings, pp.428-431

[4] Seguin-Moreau N. et al., "HARDROC, Readout chip of the Digital Hadronic Calorimeter of ILC", TWEPP 2009 conference proceedings, pp. 122-126

[5] Wing M. et al., "Calorimeter DAQ status", EUDET-Memo-2009-27

[6] Dulucq F. et al., "Presentation of the "ROC" Chips Readout", TWEPP 2009 conference proceedings, pp.491-494