MICROROC is dedicated chip for GEM/MICROMEGAS. MICROROC(pin pin compatible with HR2b) is based on HR2b same back-end, same readout format, same pinout, only the preamplifier is changing Dynamic range 1fC~500fC



The GEM detector is designed as 37cm*37cm, and its effictive area is 30cm*30cm. Each Microroc ASIC has 64 readout channels. That is to say some of Microrocs cannot be full used and the unused pin should tied to GND via a capacitor. The ESD protection is necessary as there might be spark in the GEM.

SUHCAL FEB

SDHCal FEB Version: 1.0

Design Tools: Cadence 16.6 Finish Date: 2017/08/23

Engineer: Yu Wang

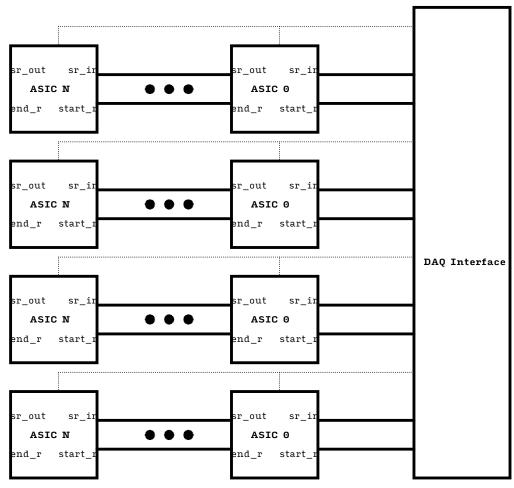
Company: USTC

Tips: If there is gibberish, please install the 'Input' font, 'Romantic' font and 'Celestina' font.

Note: All the Title and Document Number is Input, blod, size 10. Rev is Input, size 6. All the comments is Input, blue size 6

Note: All the unsolder package should value x(Not X)

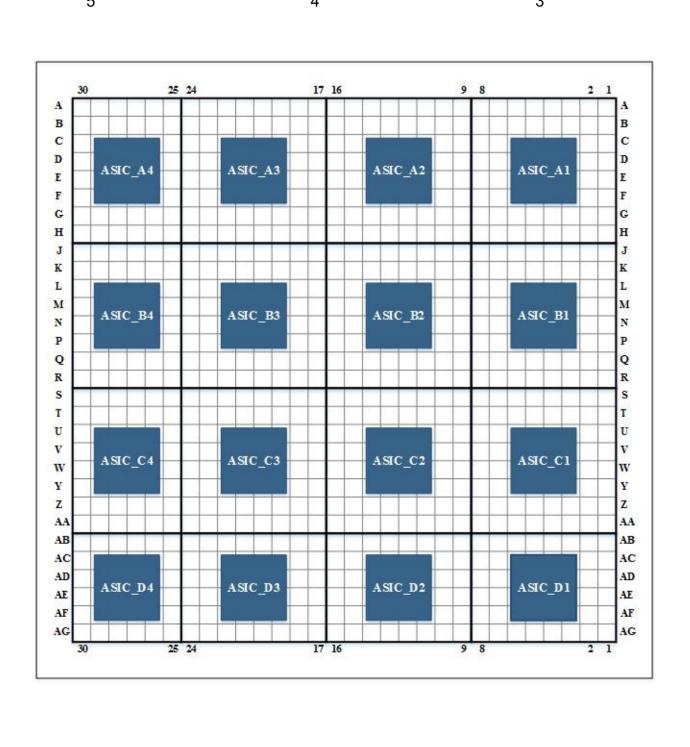
Capacitor: F(Not f)



There are 3 kinds of control signals 1. Daisy chain signals: sr_in, sr_out, start_readout, end_readout
2. Independent signal for each chain: Dout1b, Dout2b, TransmitOn1b,
TransmitOn2b, ChipSatb, TrigExt, StartAcq, StartReadout1, StartReadout2, sr_rstb,
sr_ck, sr_in, EndReadout1, EndReadout2, sr_out
3. Common signals for all chains: 4 LVDS signals, power on signals, reset_b, rst_counterb, select, hold, out_trigger0~2b

FPGA LVDS driver can handle directly many ASICs (6-10) for sure. But if there is more ASICs, you should use more than 1 dedicated LVDS drivers. In this design, M-LVDS buffer is used





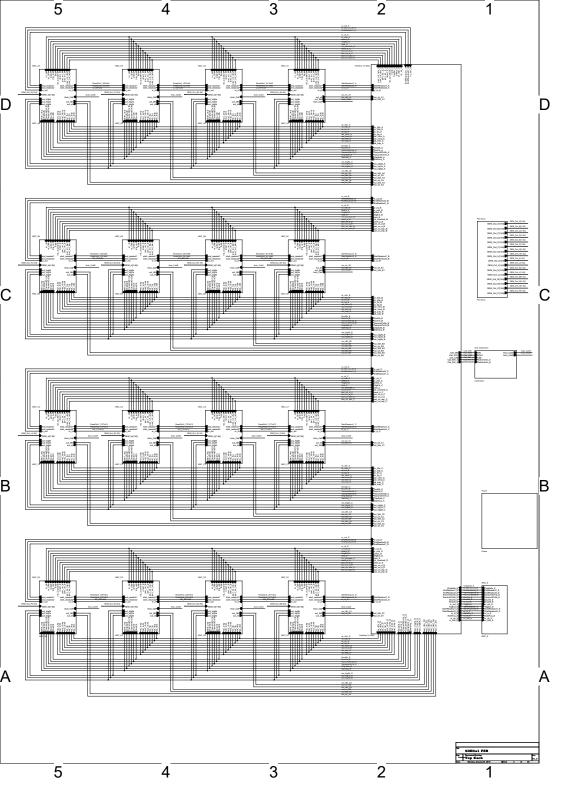
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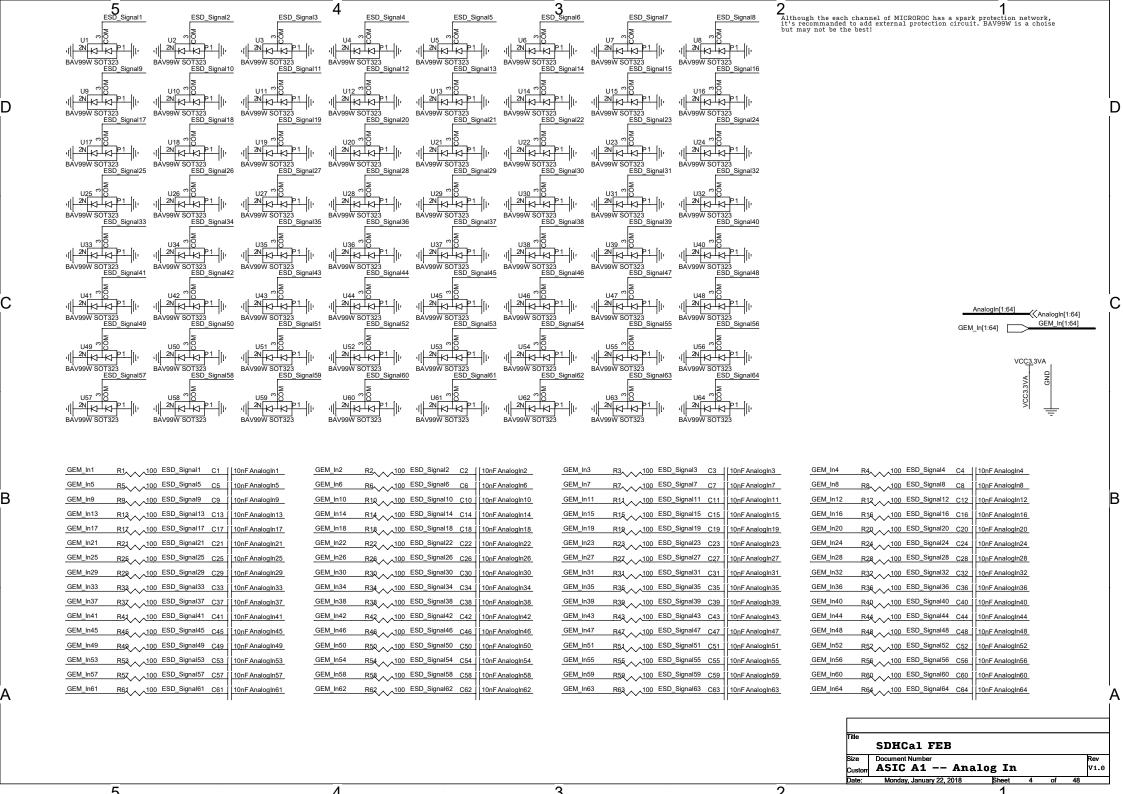
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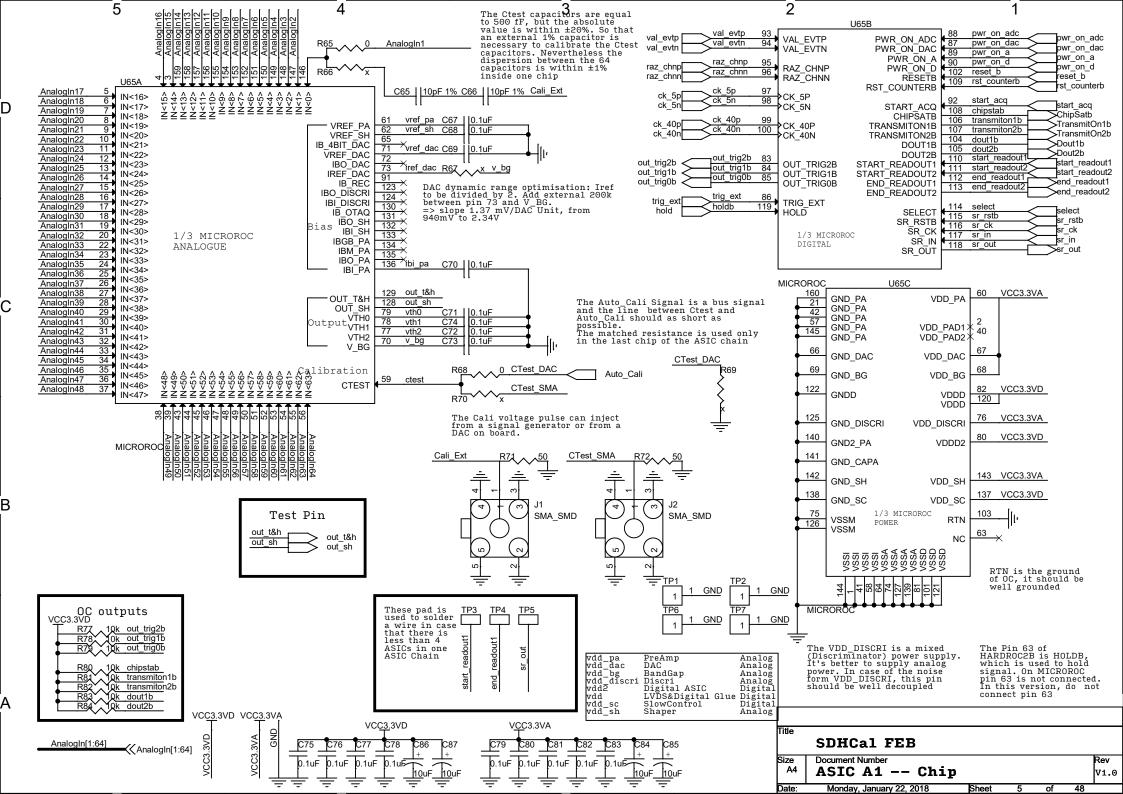
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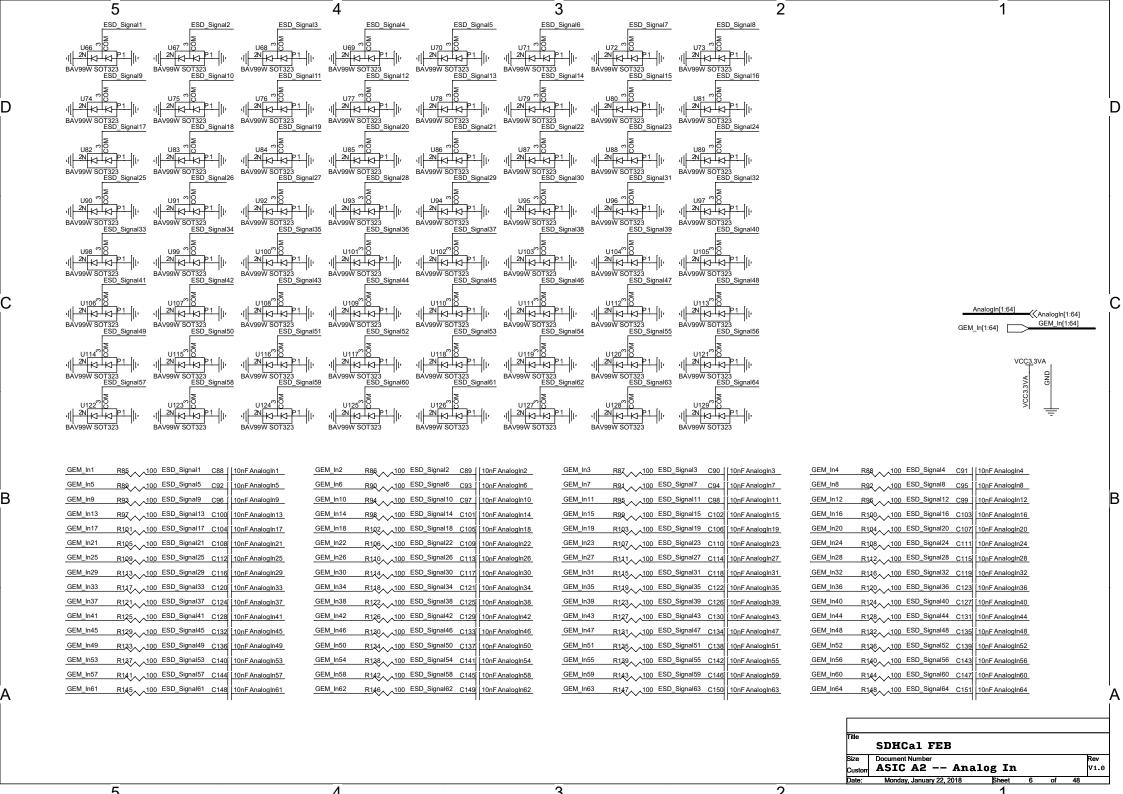
A4 Design Structure

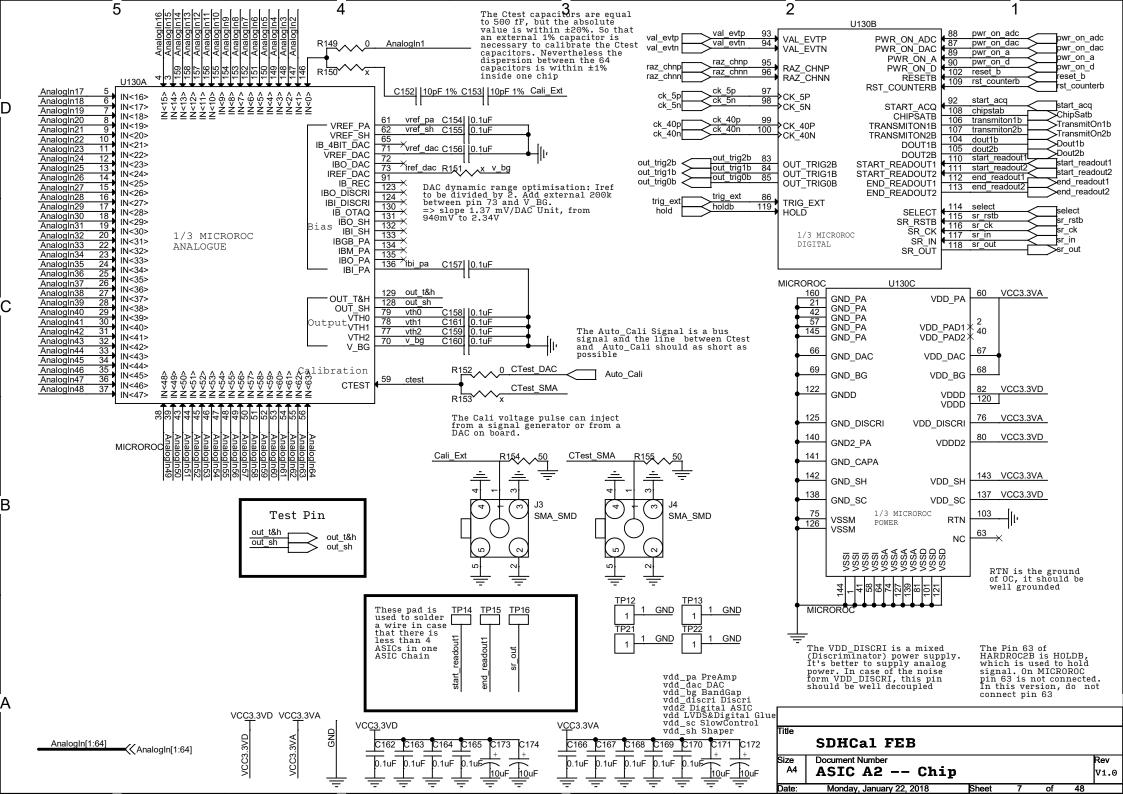
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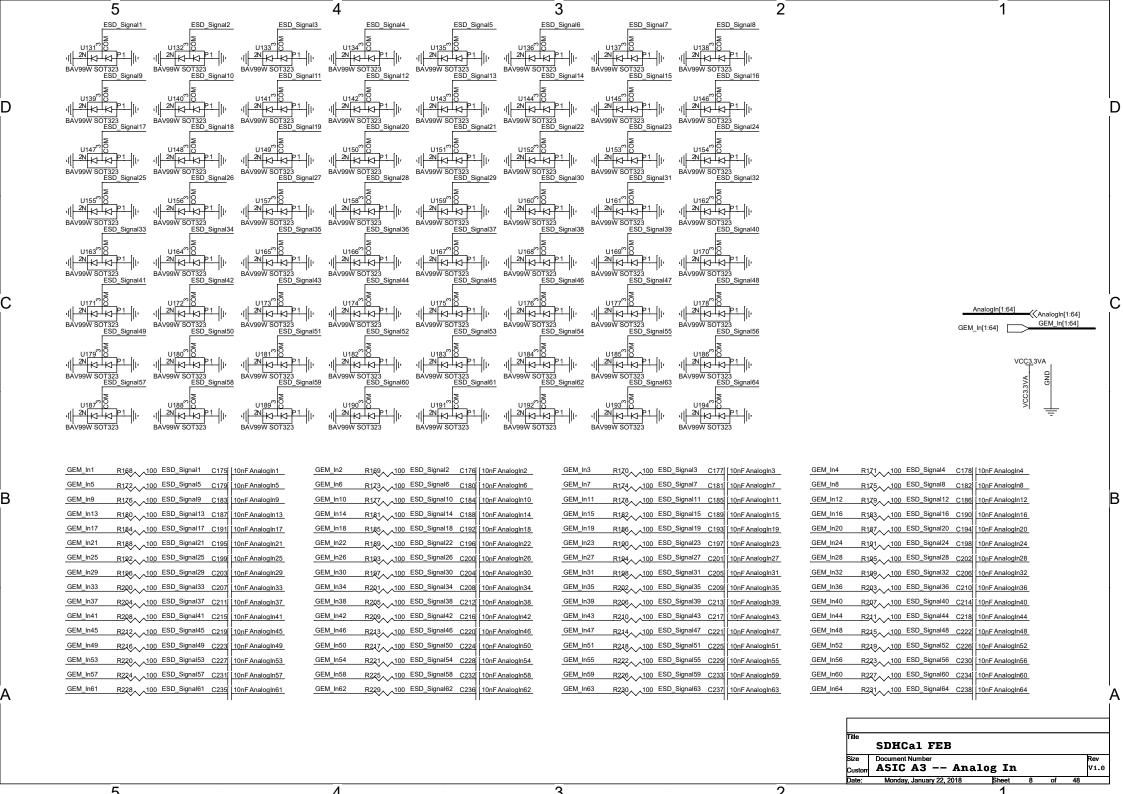


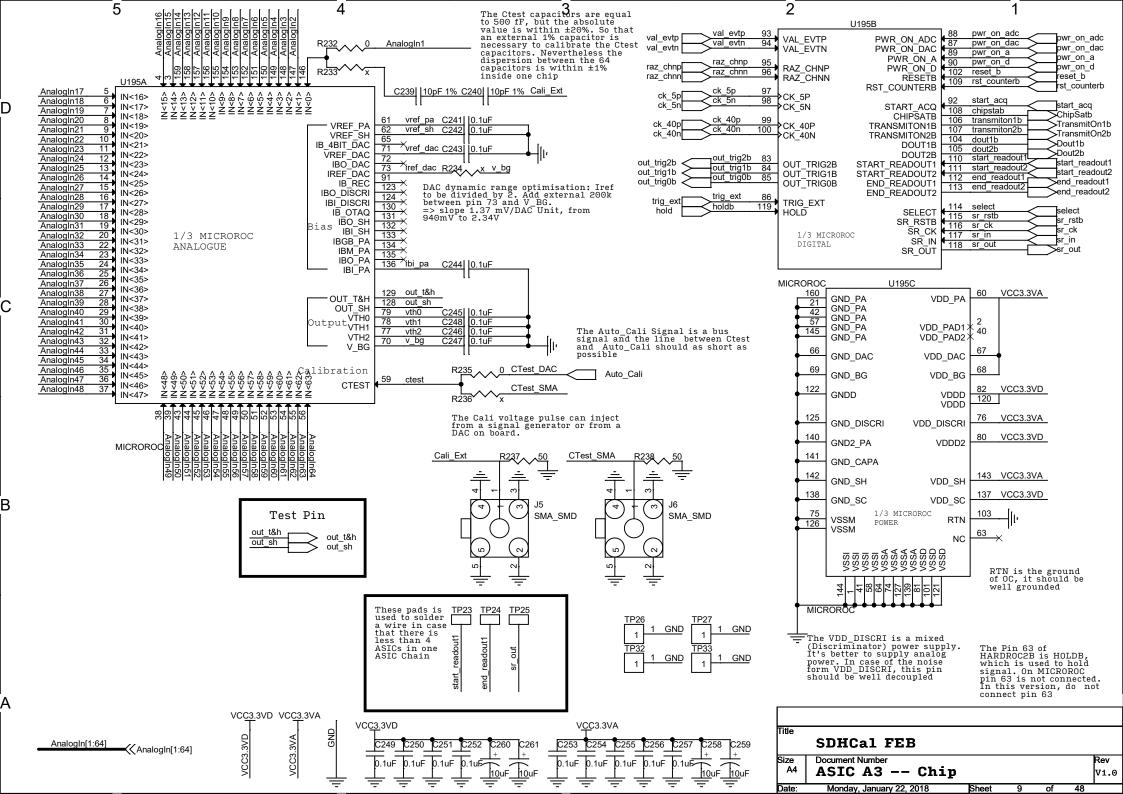


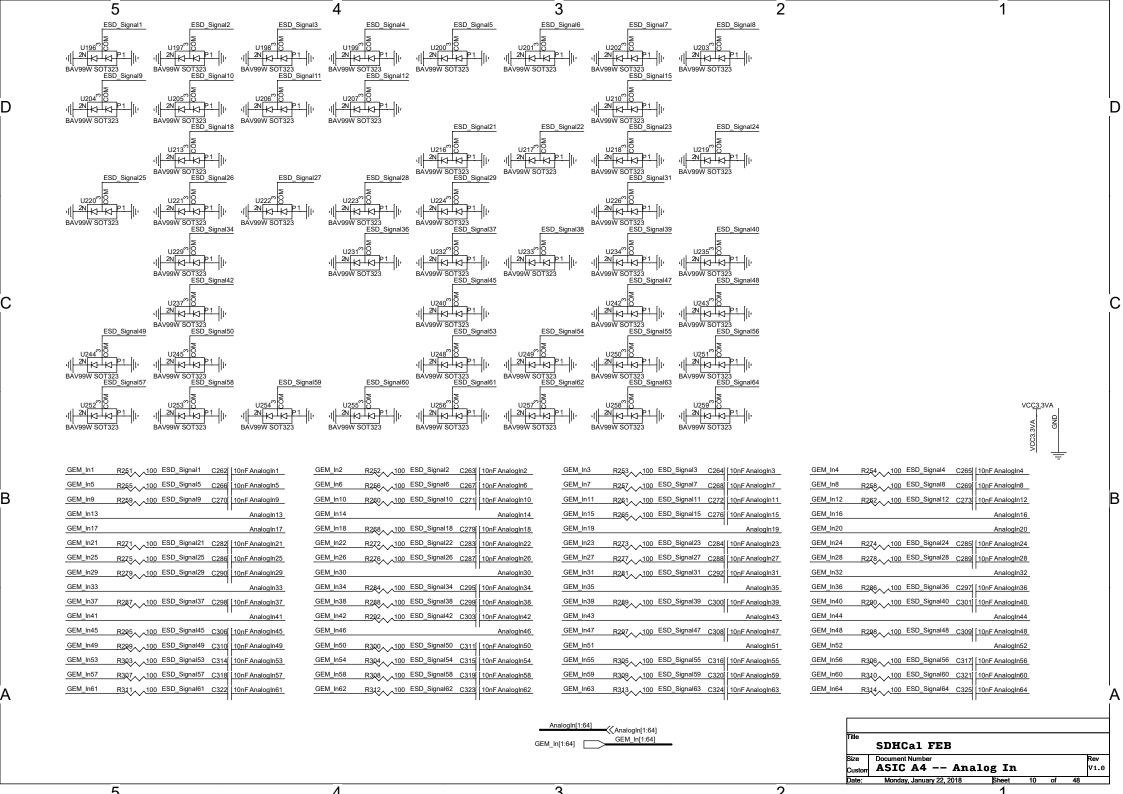


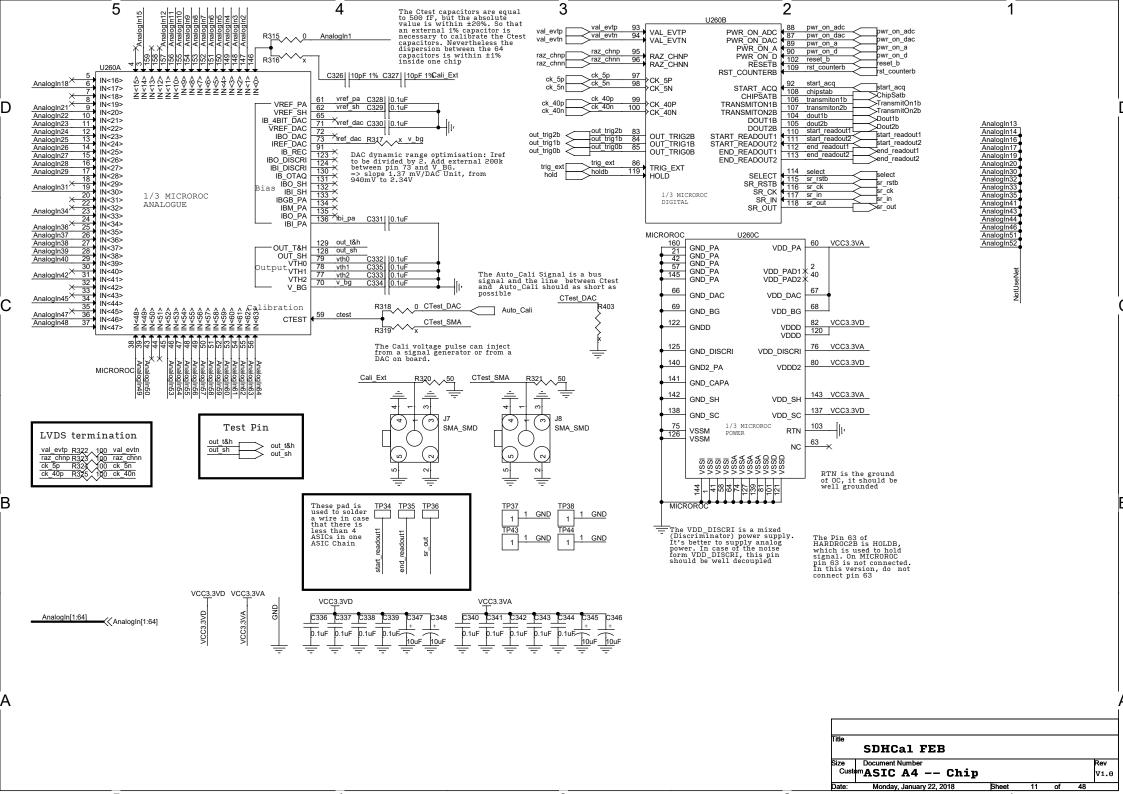


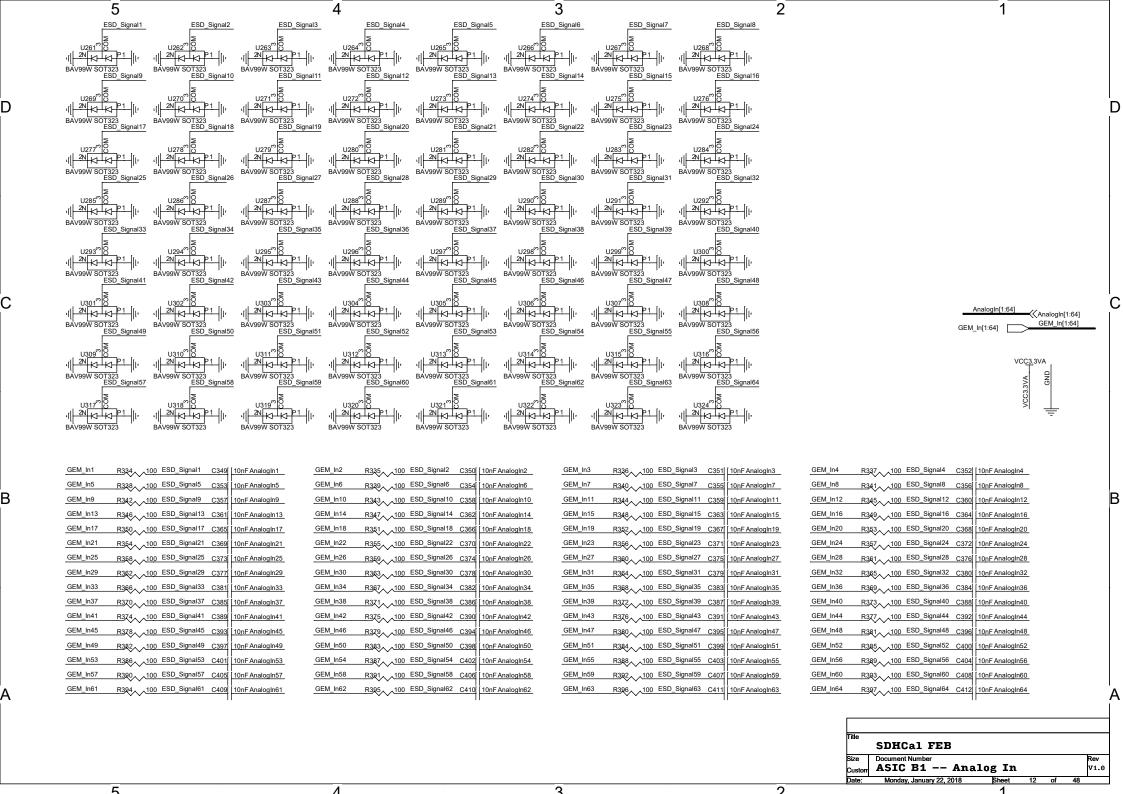


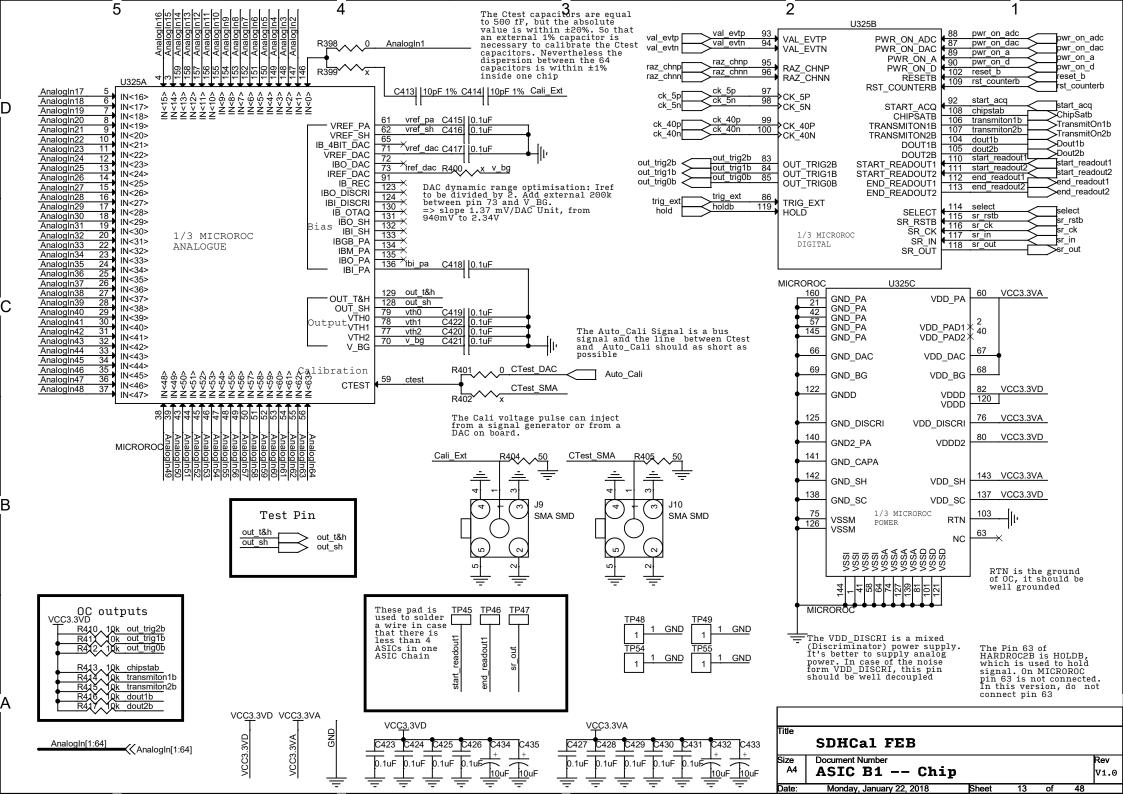


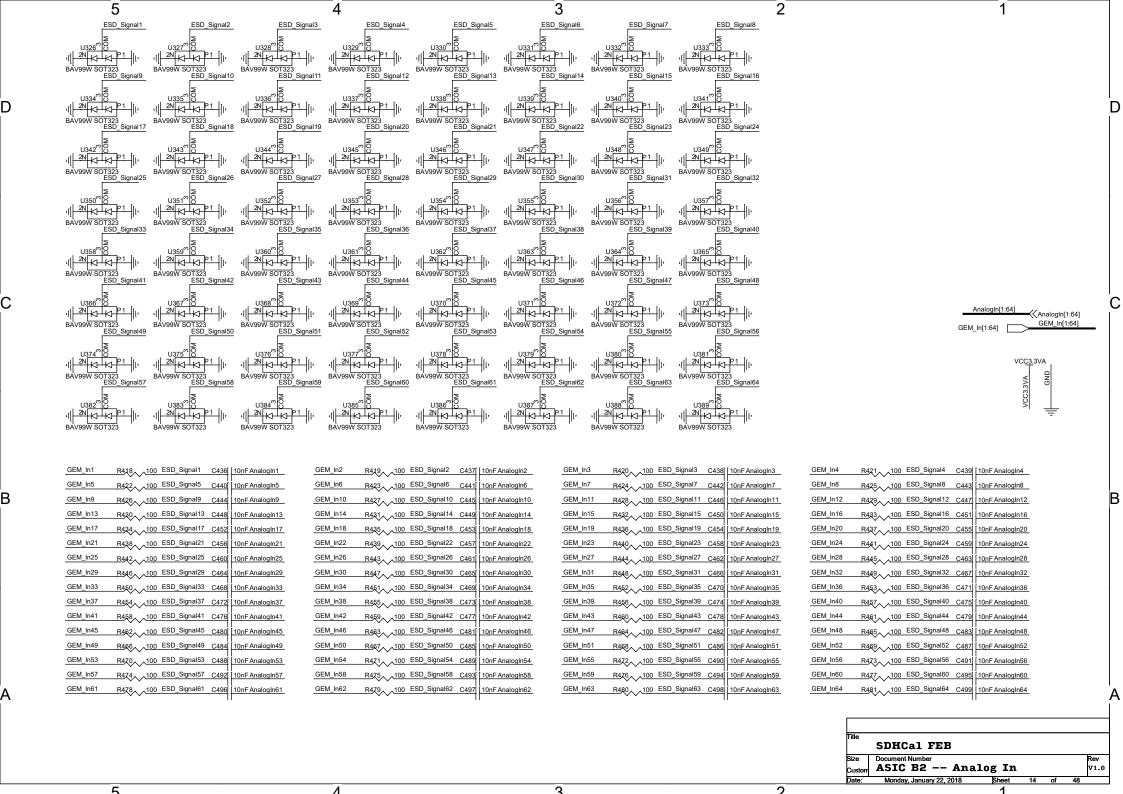


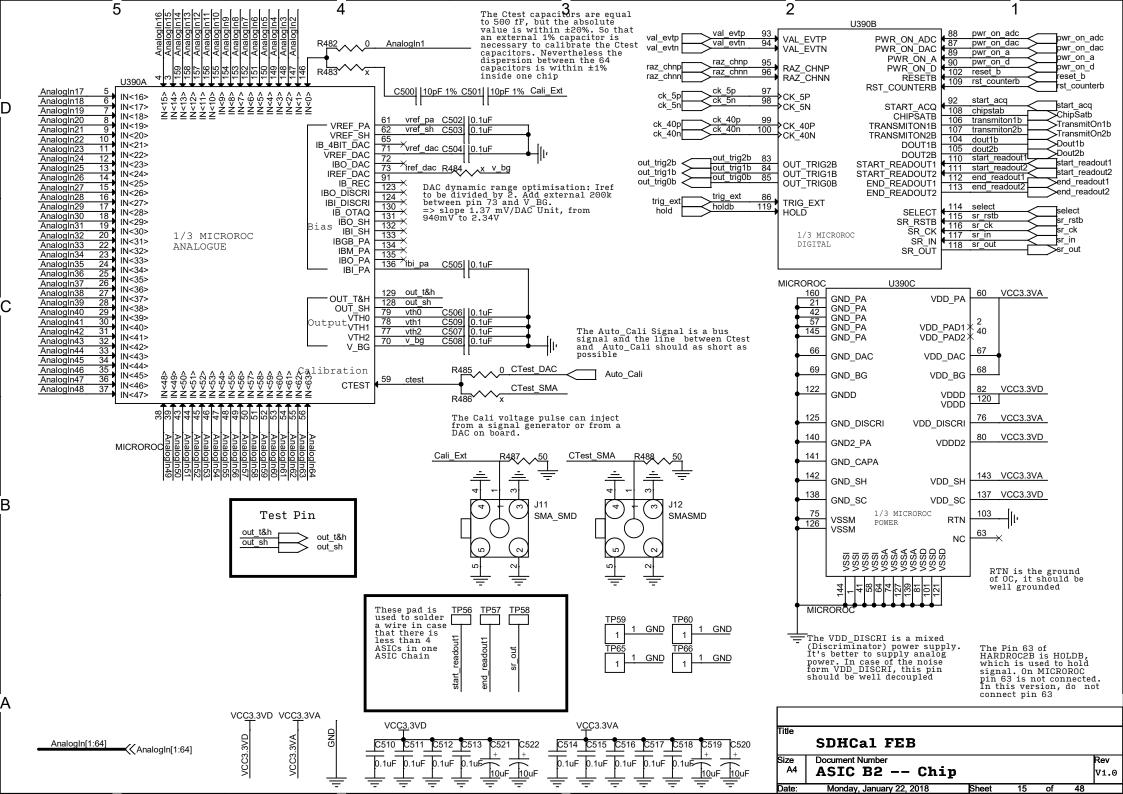


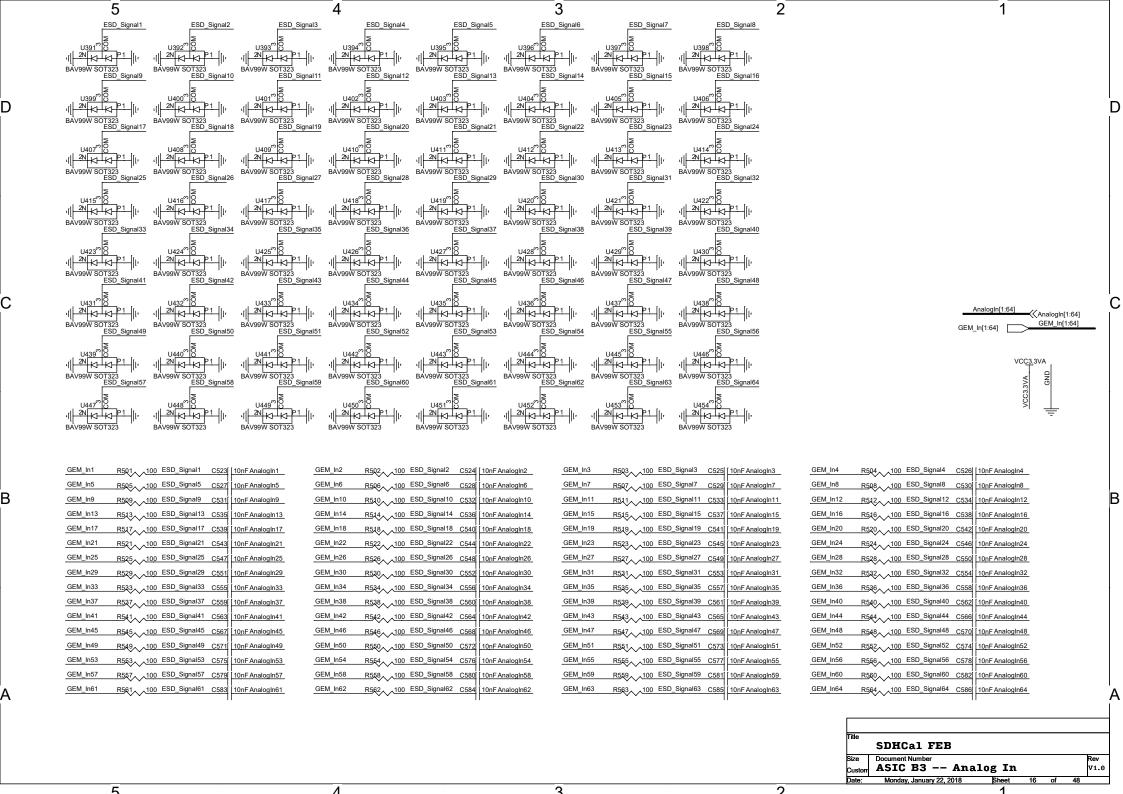


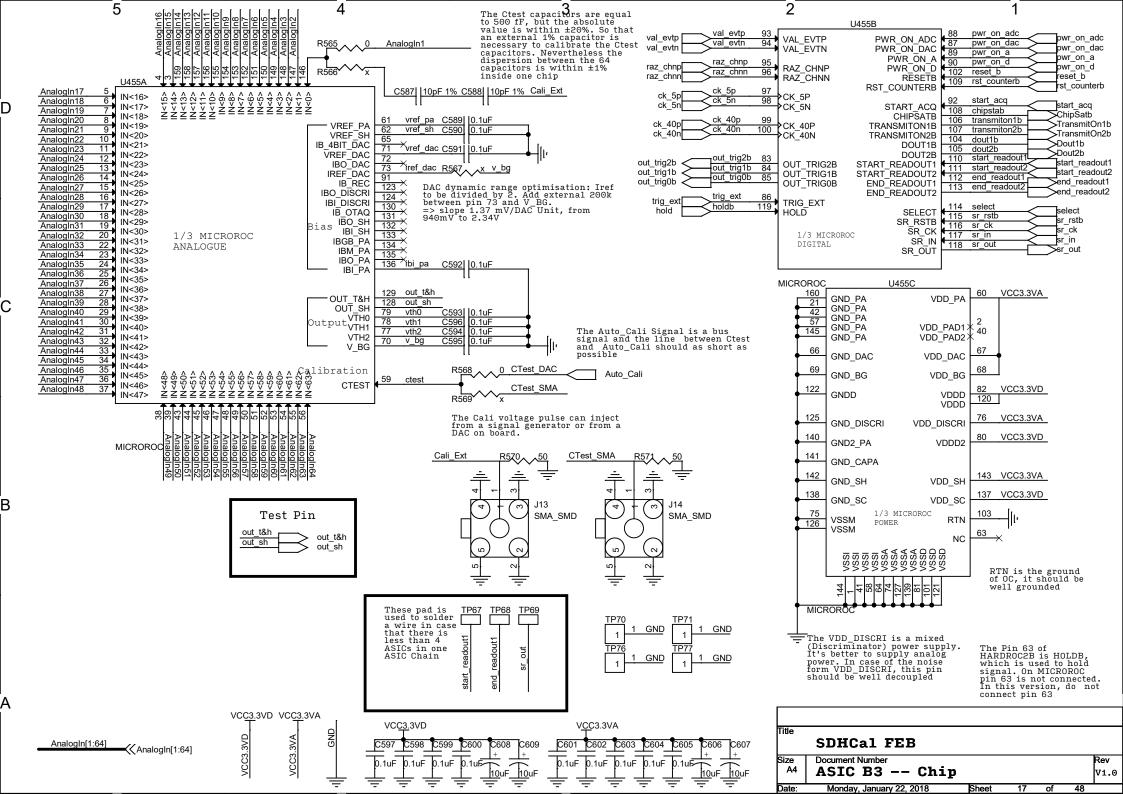


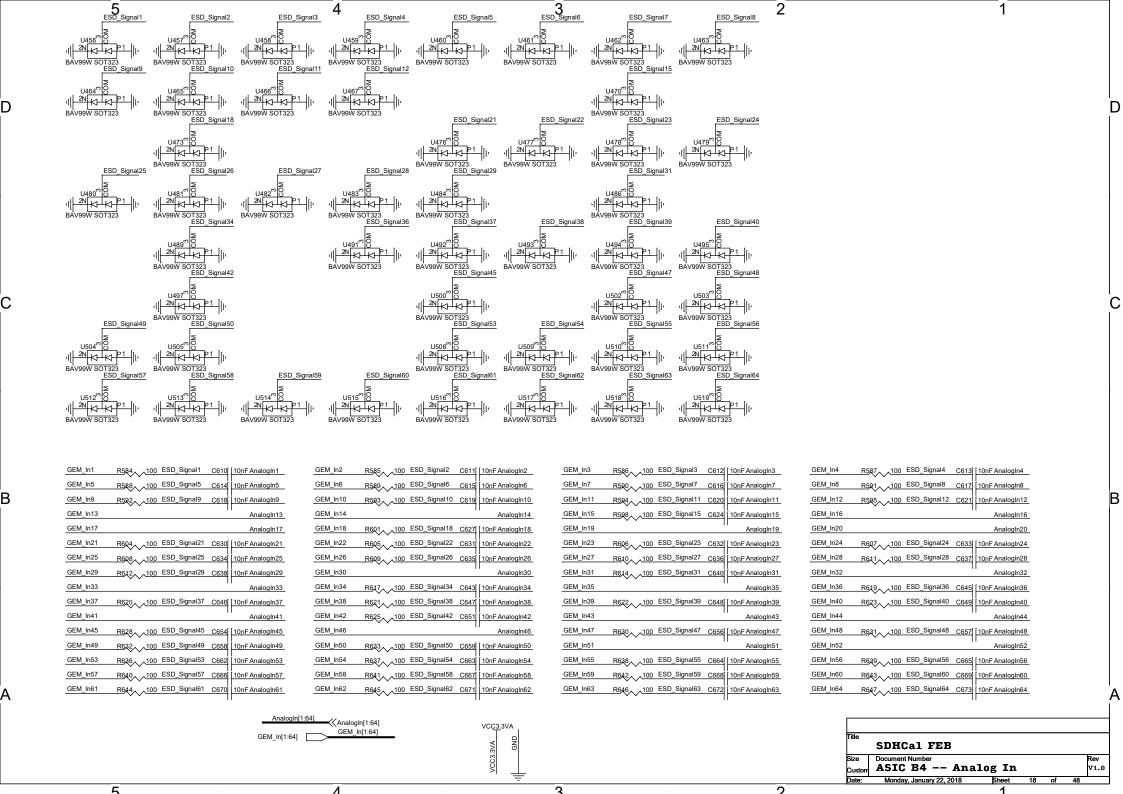


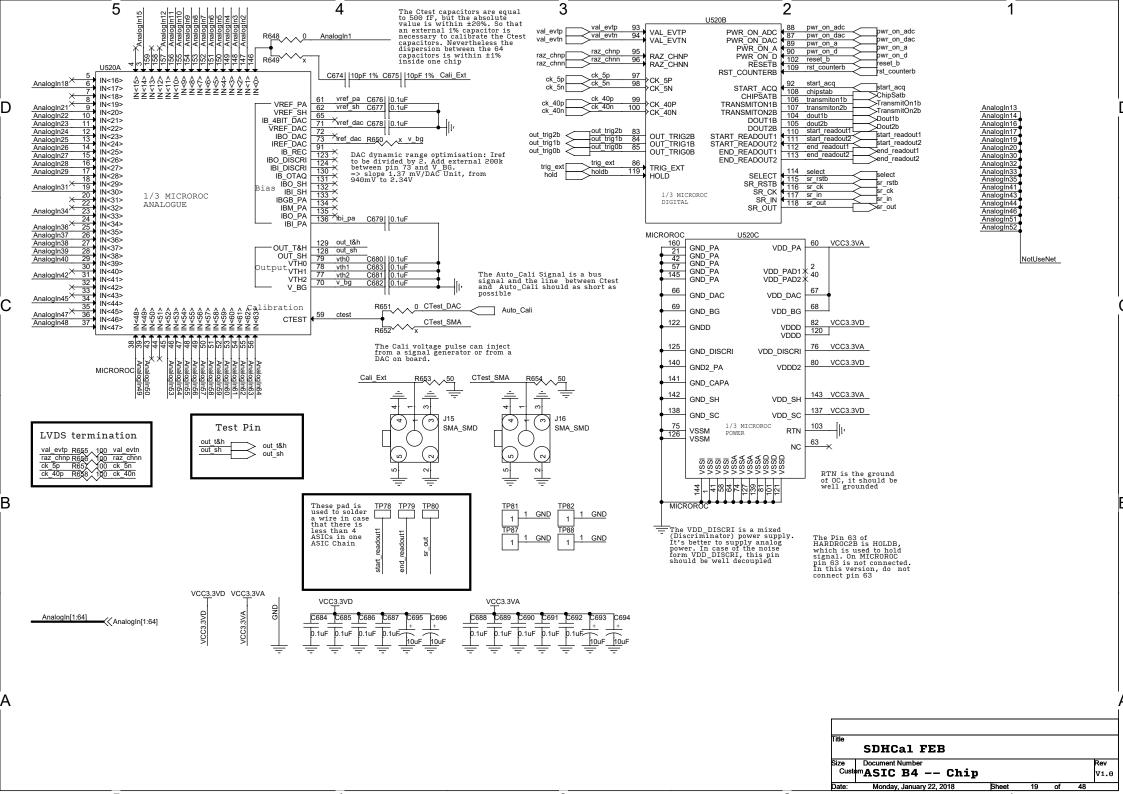


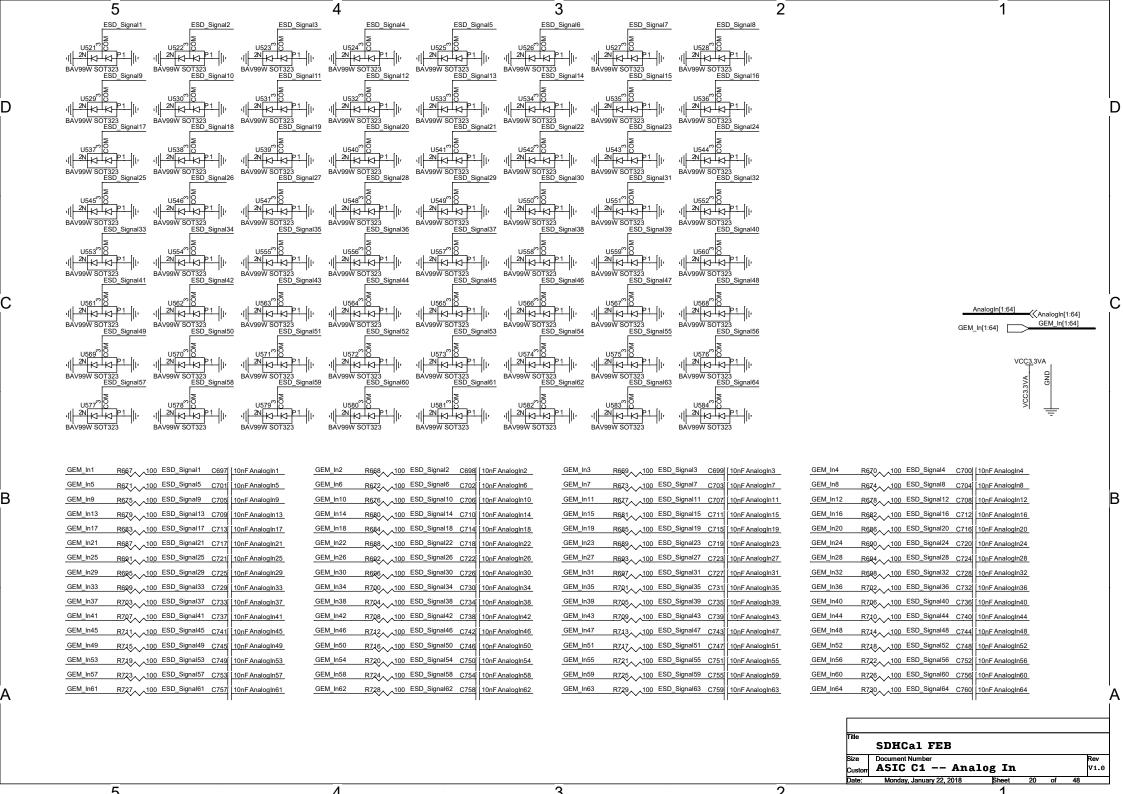


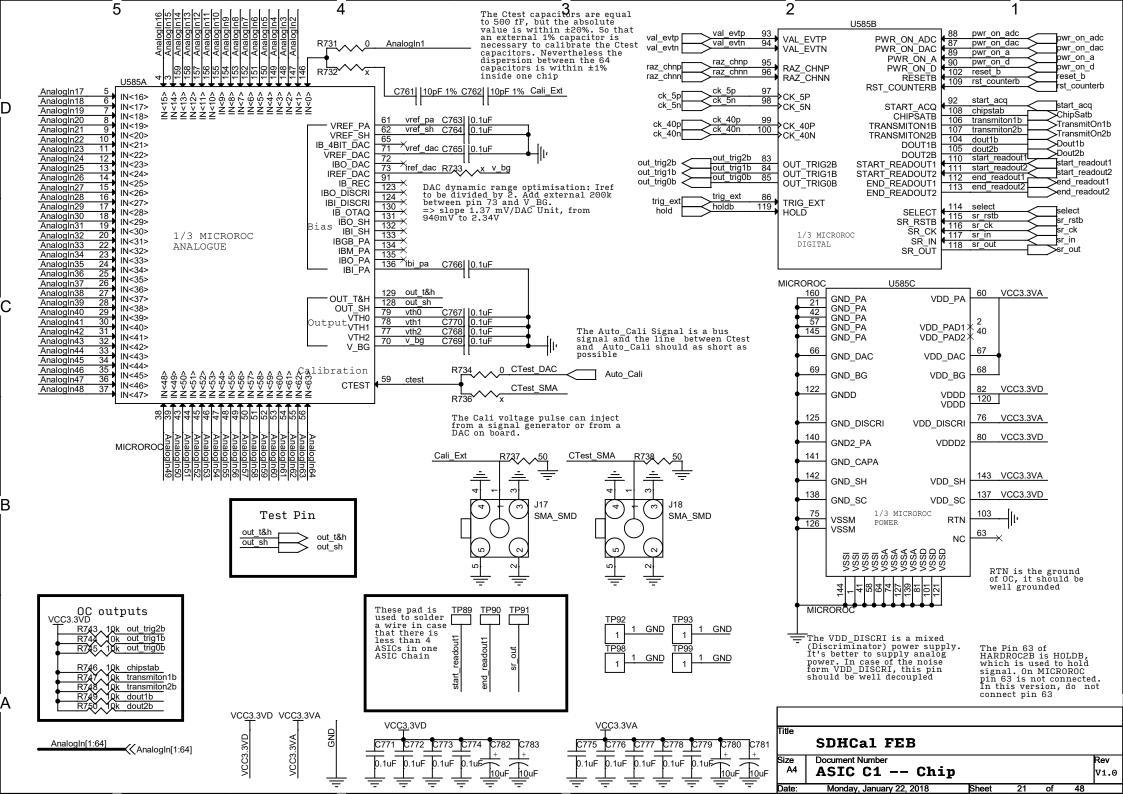


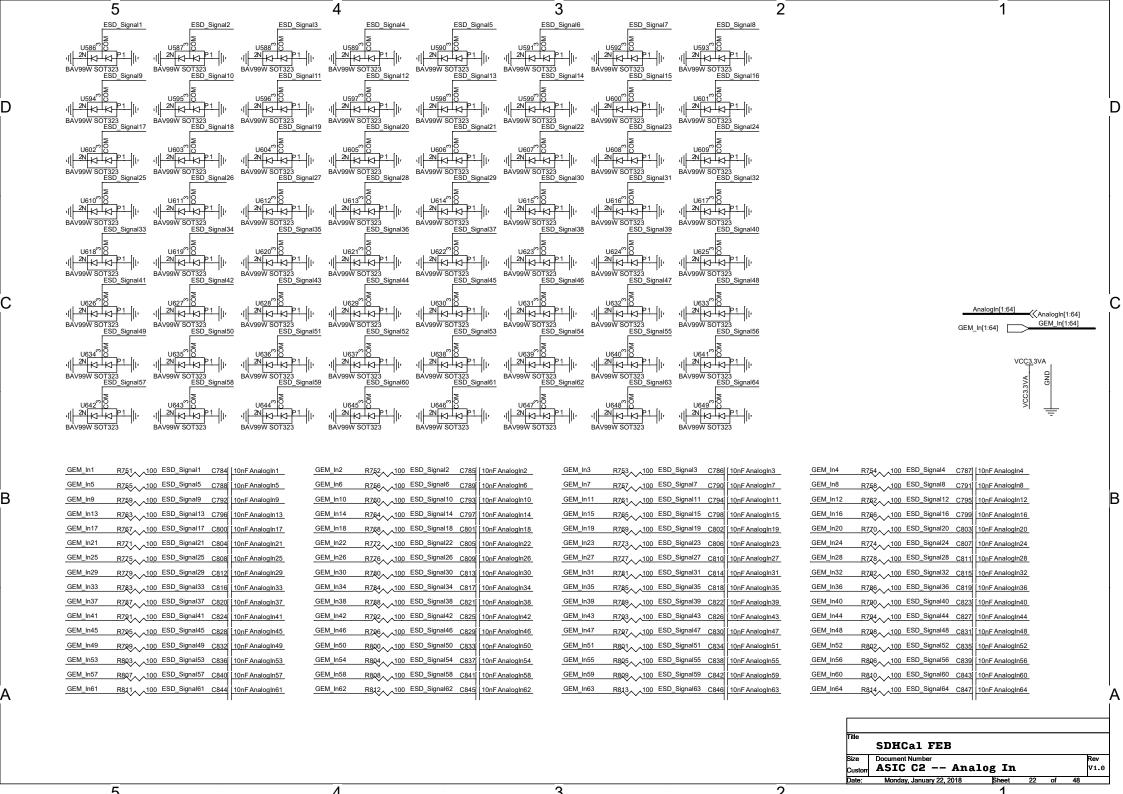


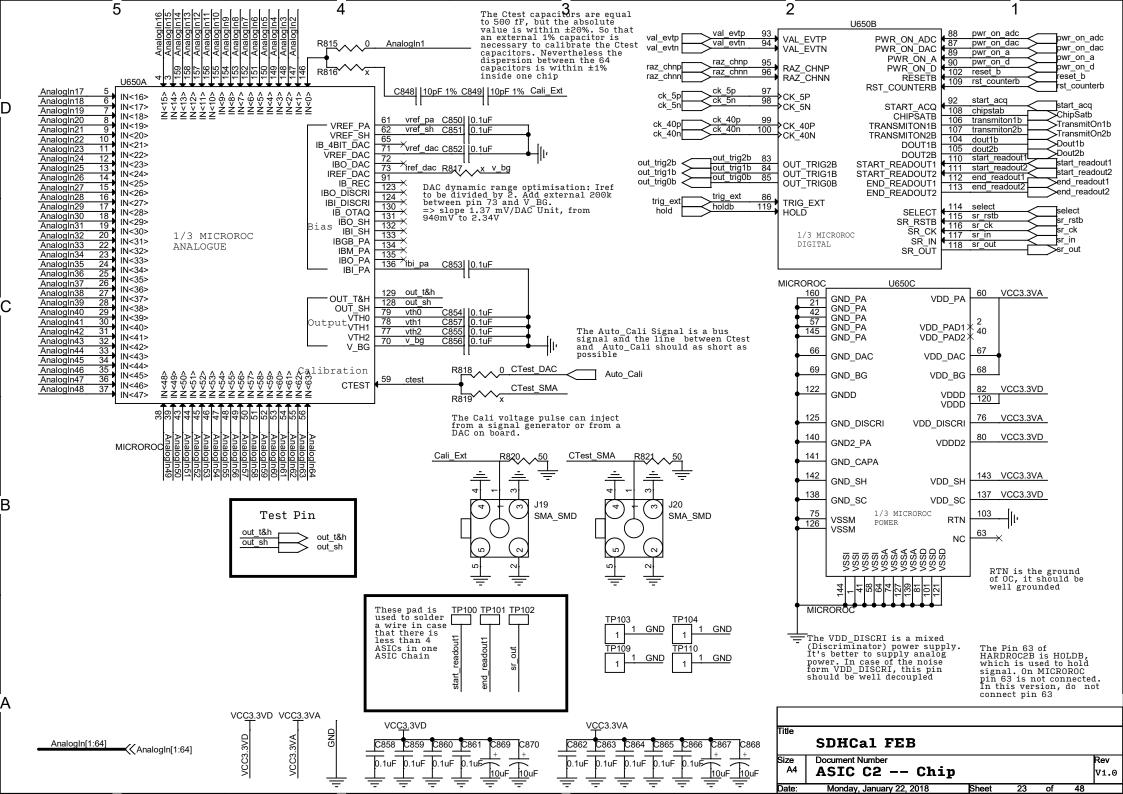


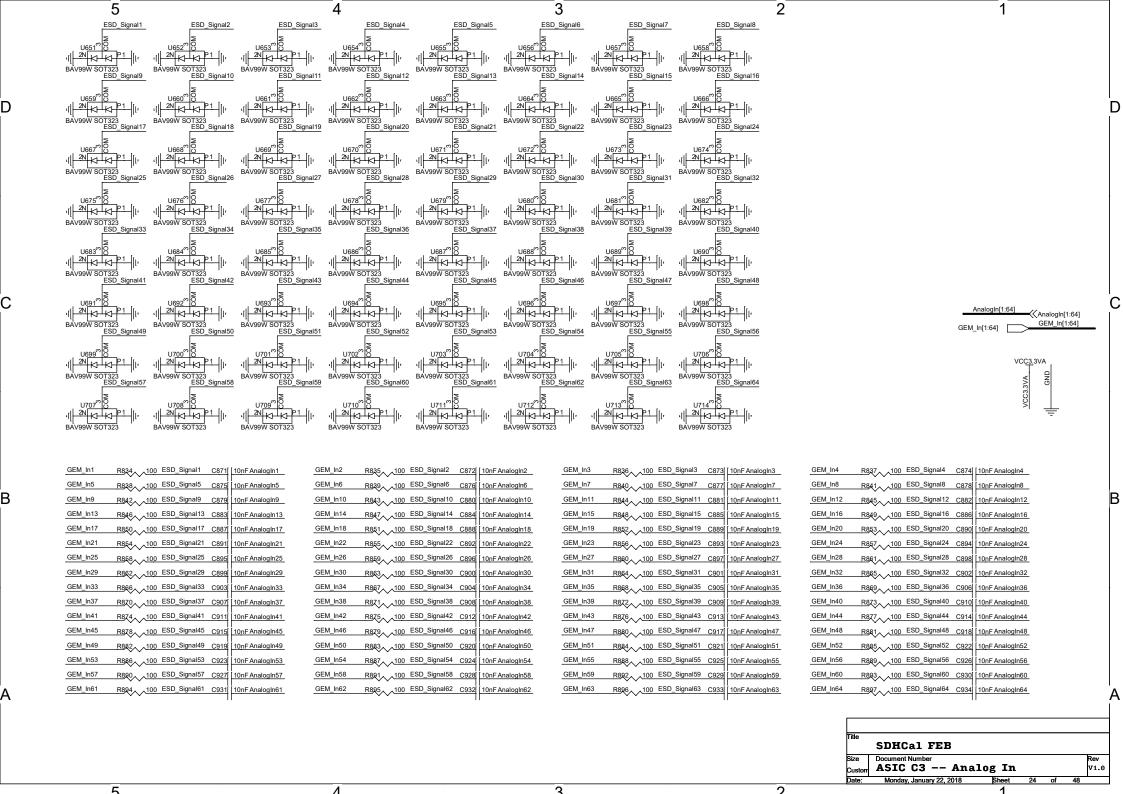


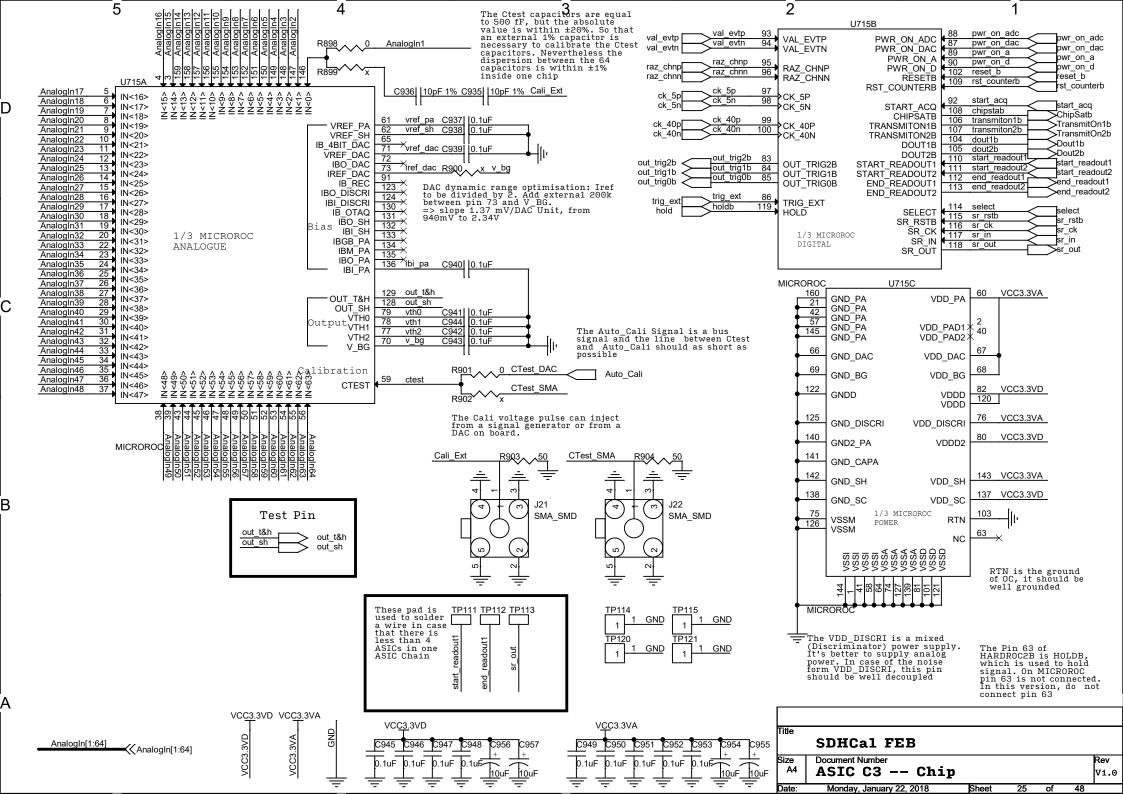


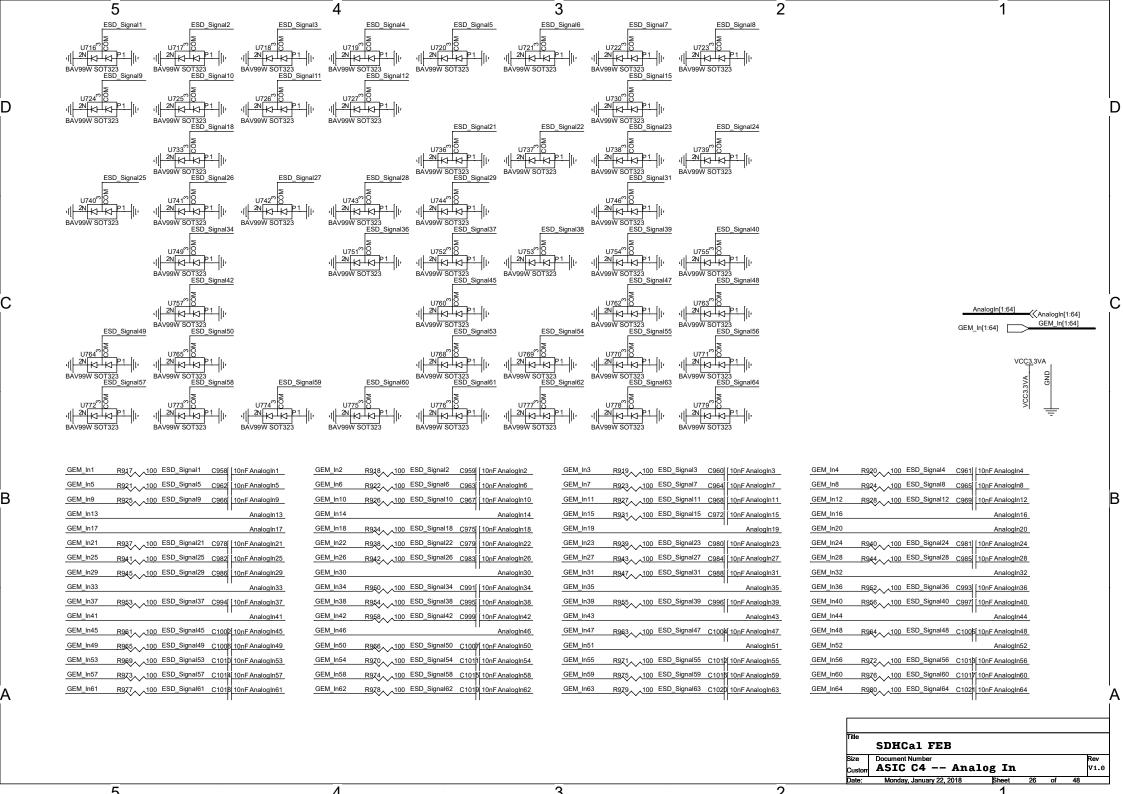


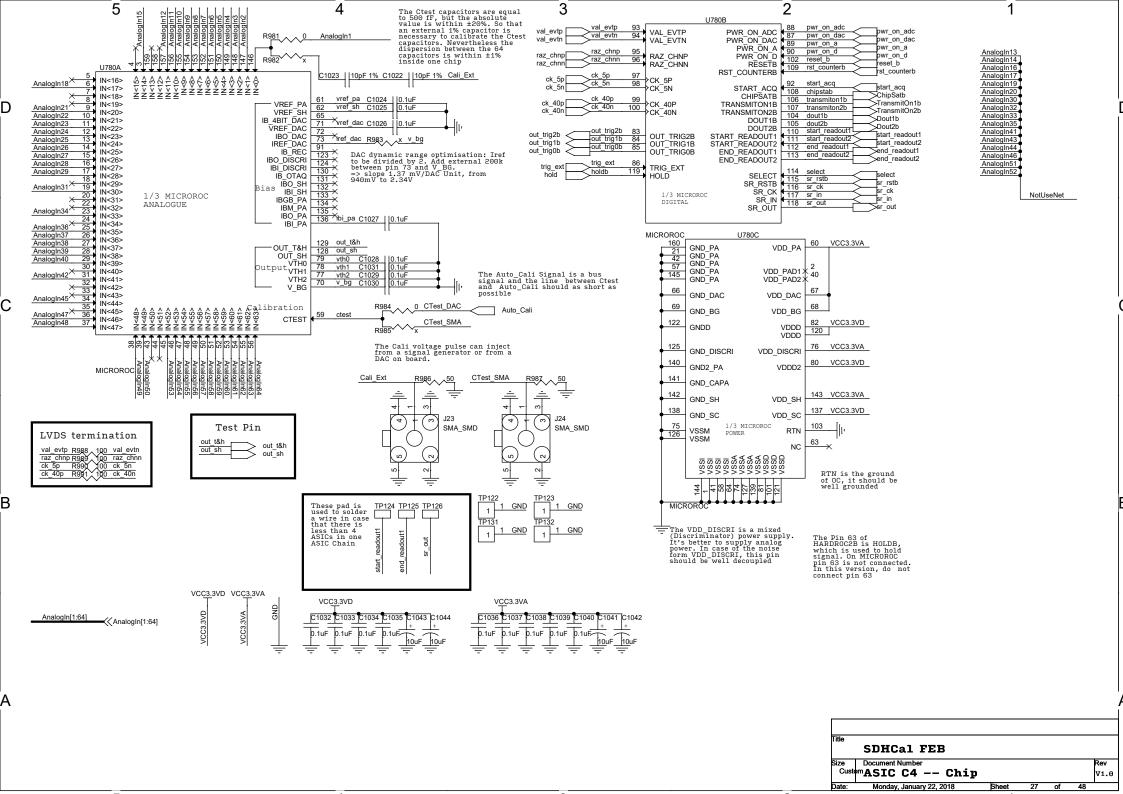


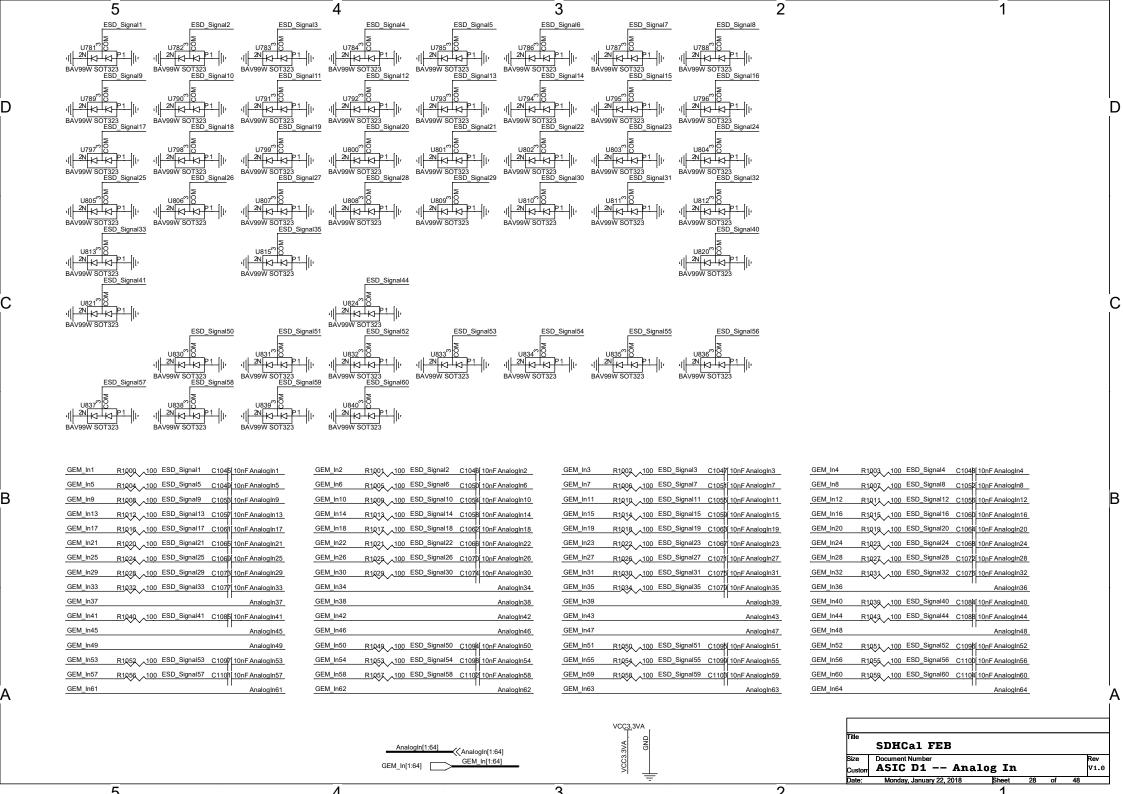


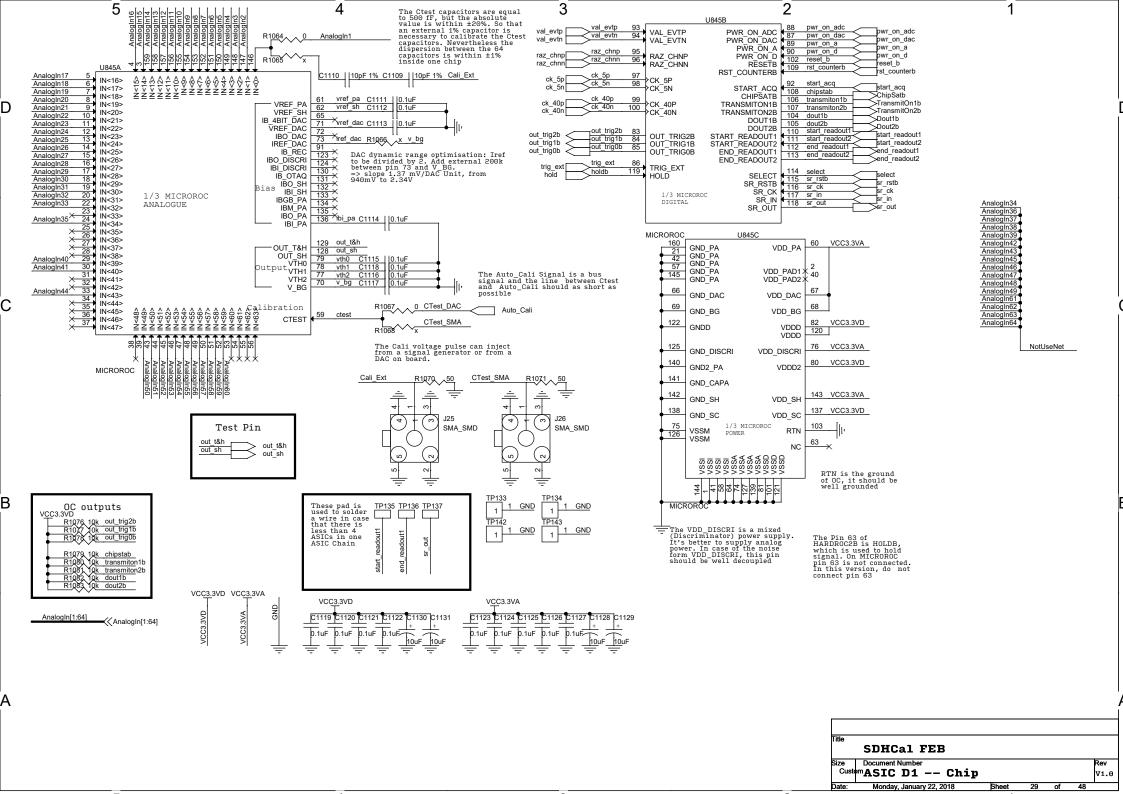


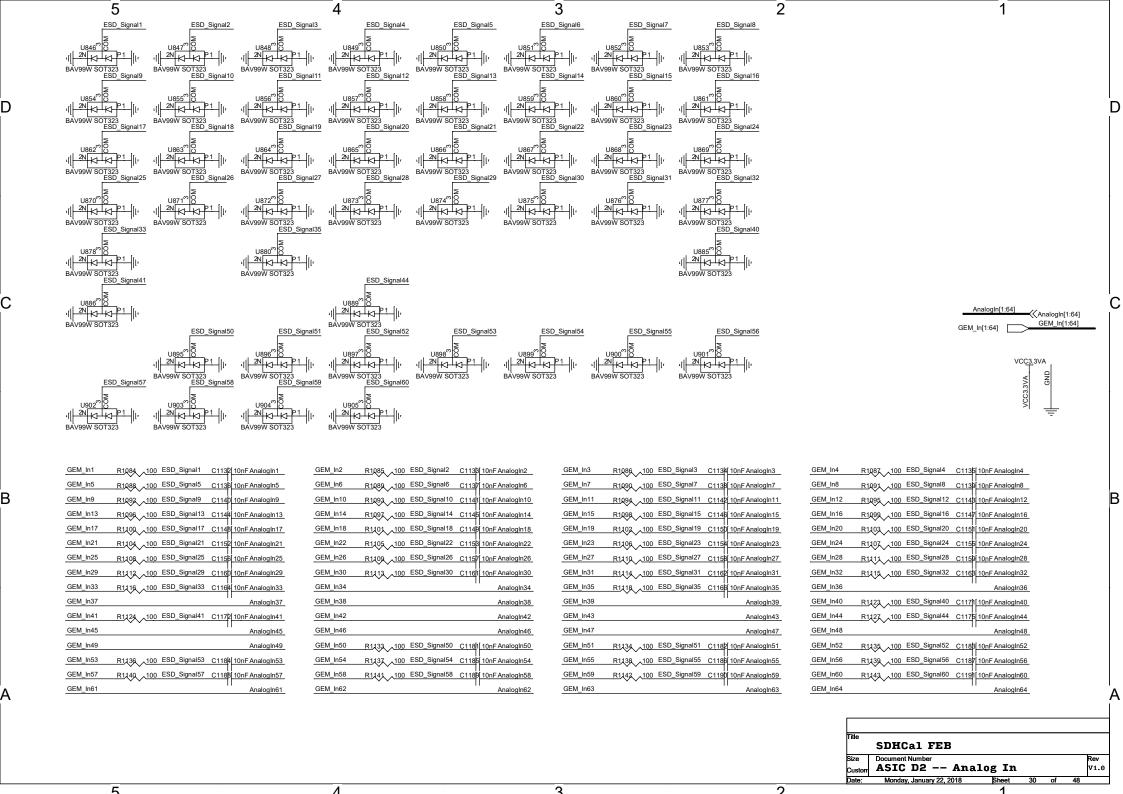


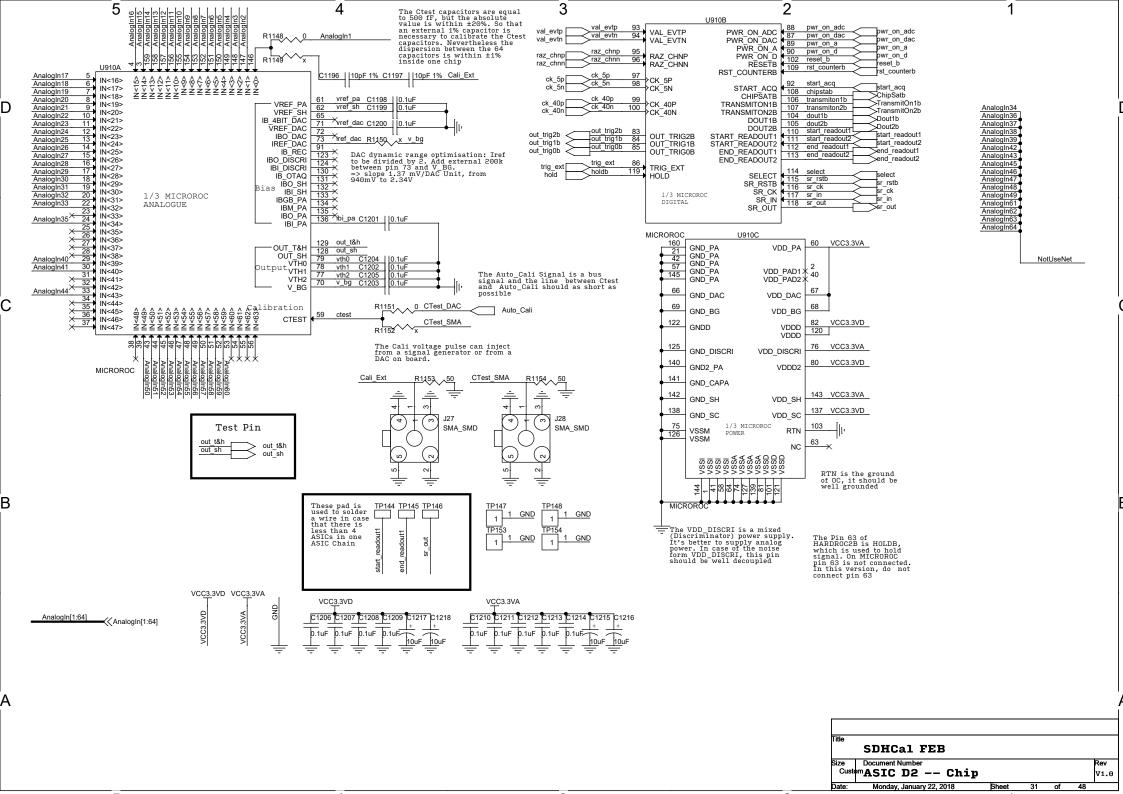


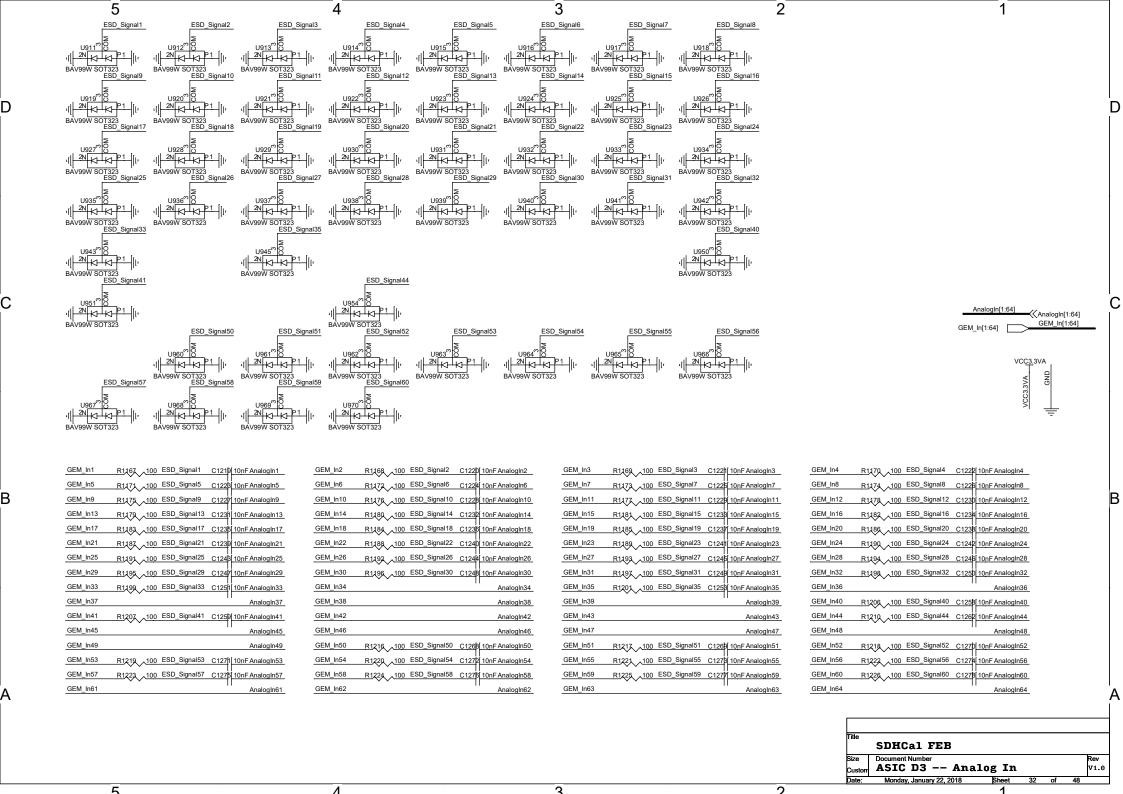


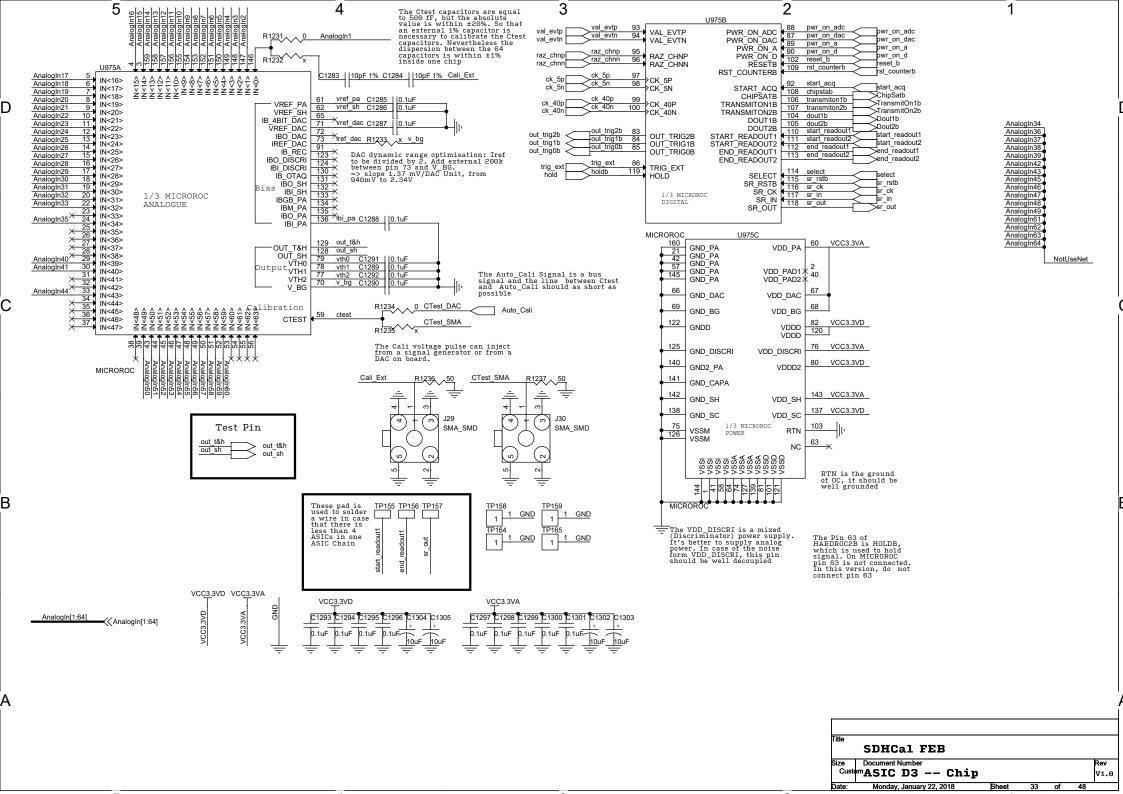


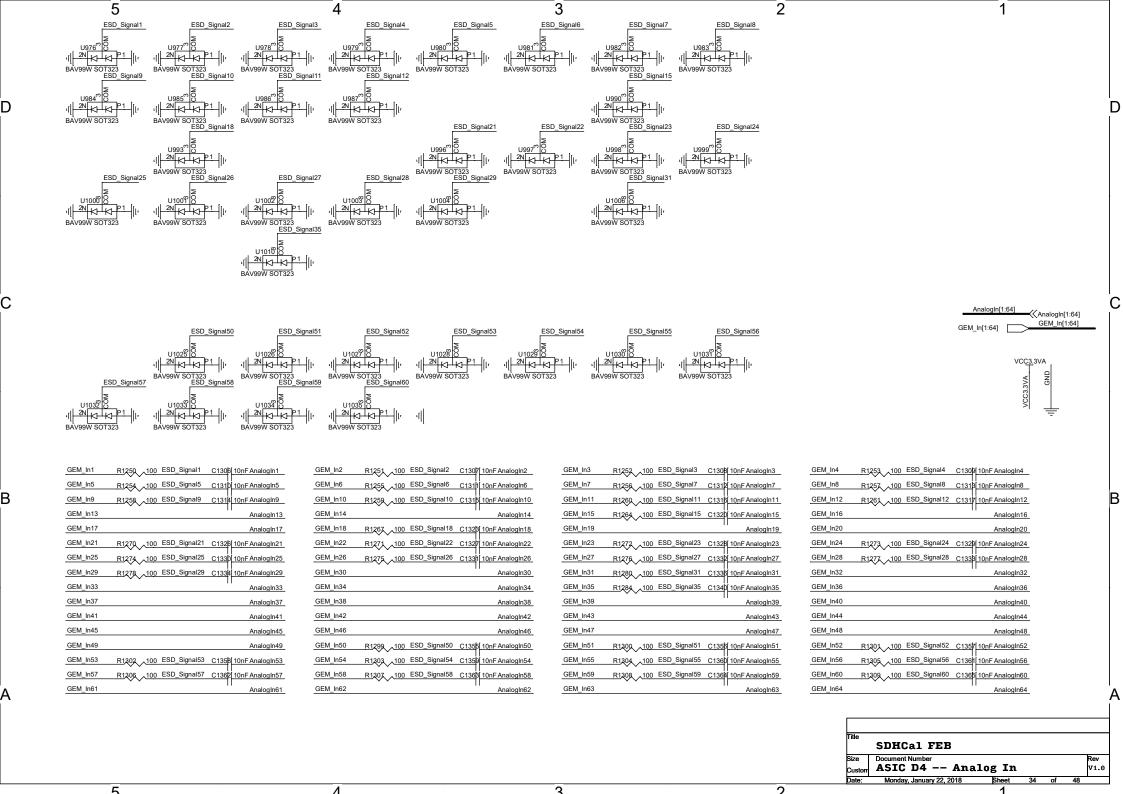


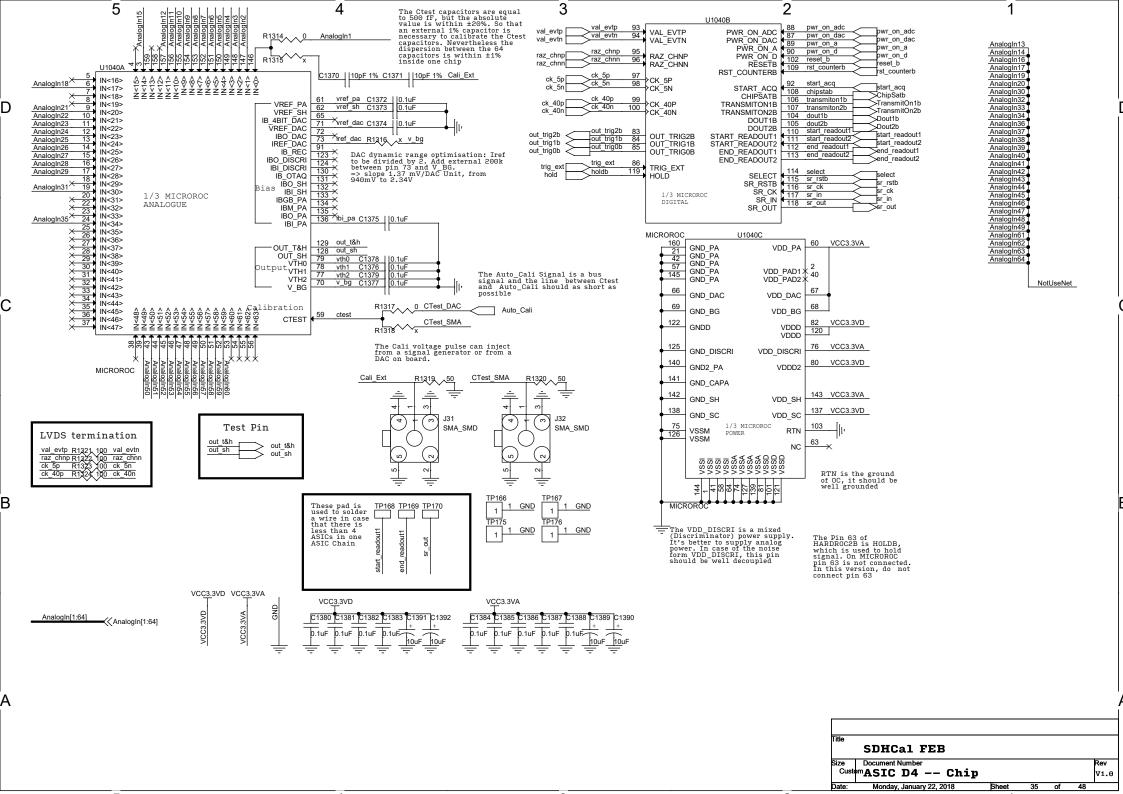


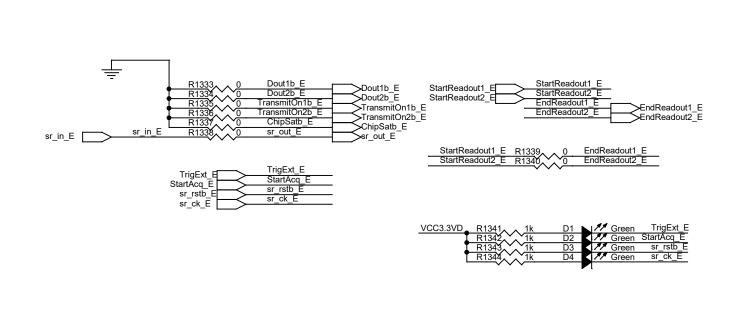




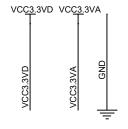






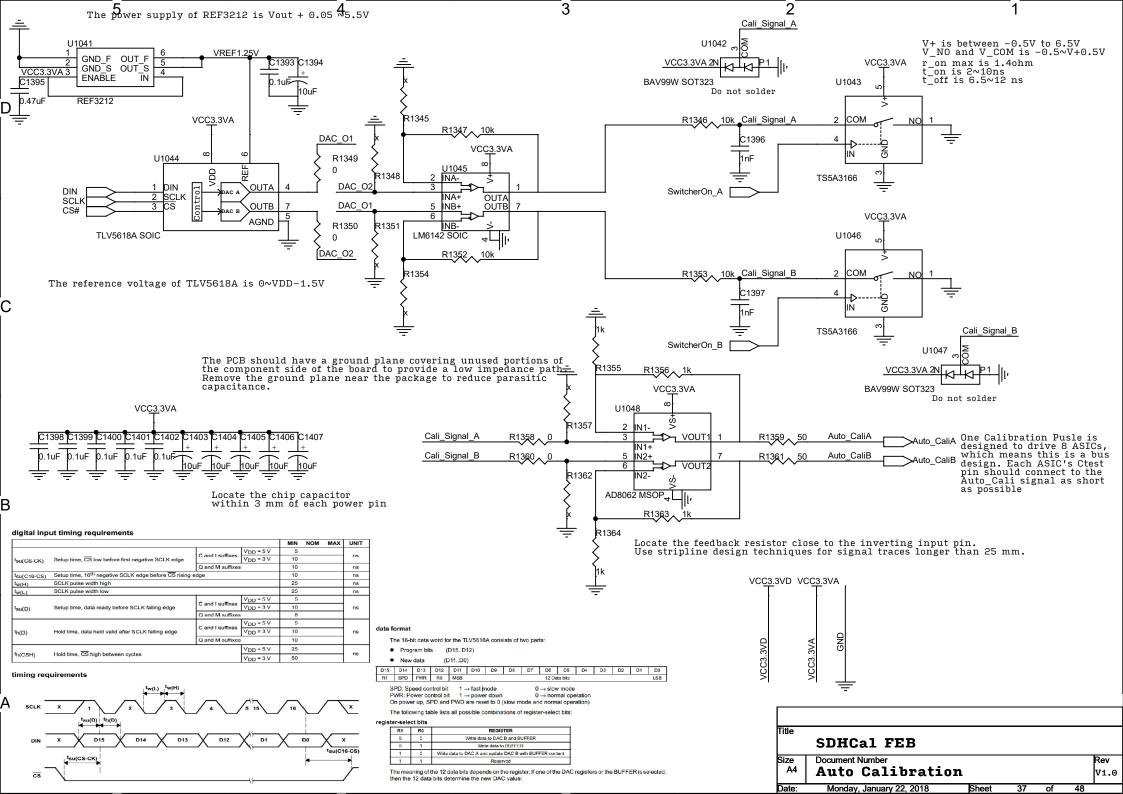


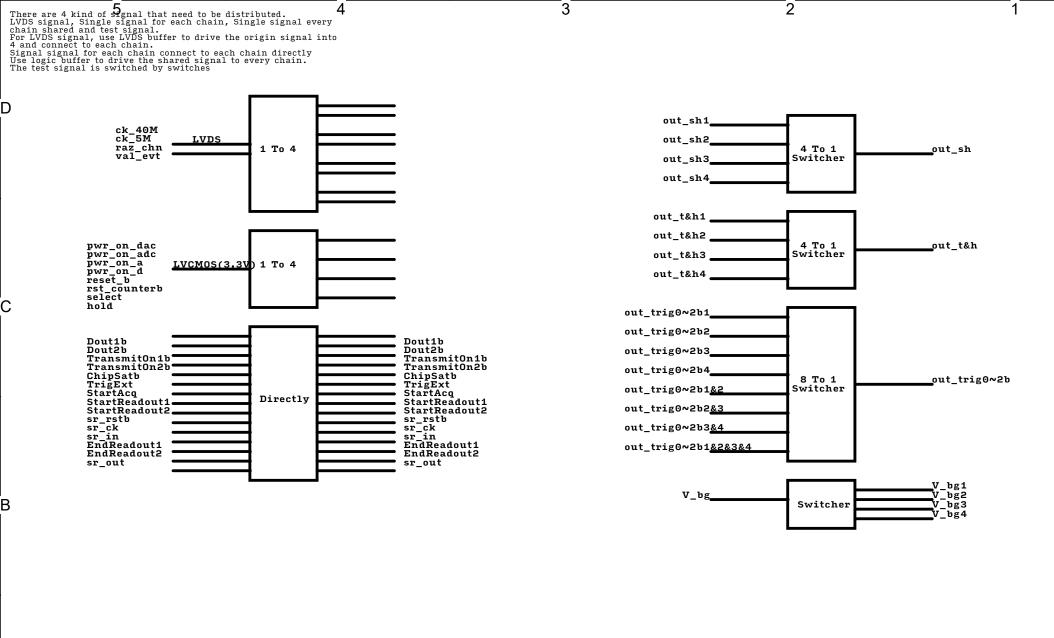
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SDHCal FEB

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