SKIROC

SOFTWARE & TEST BOARD USER GUIDE

Version: 18 August 2014

Abstract

SKIROC is a 64-channel front end ASIC dedicated to the read-out of Silicon PIN diodes.

This guide explains how to install & use the test board for SKIROC and how to operate with the associated software.

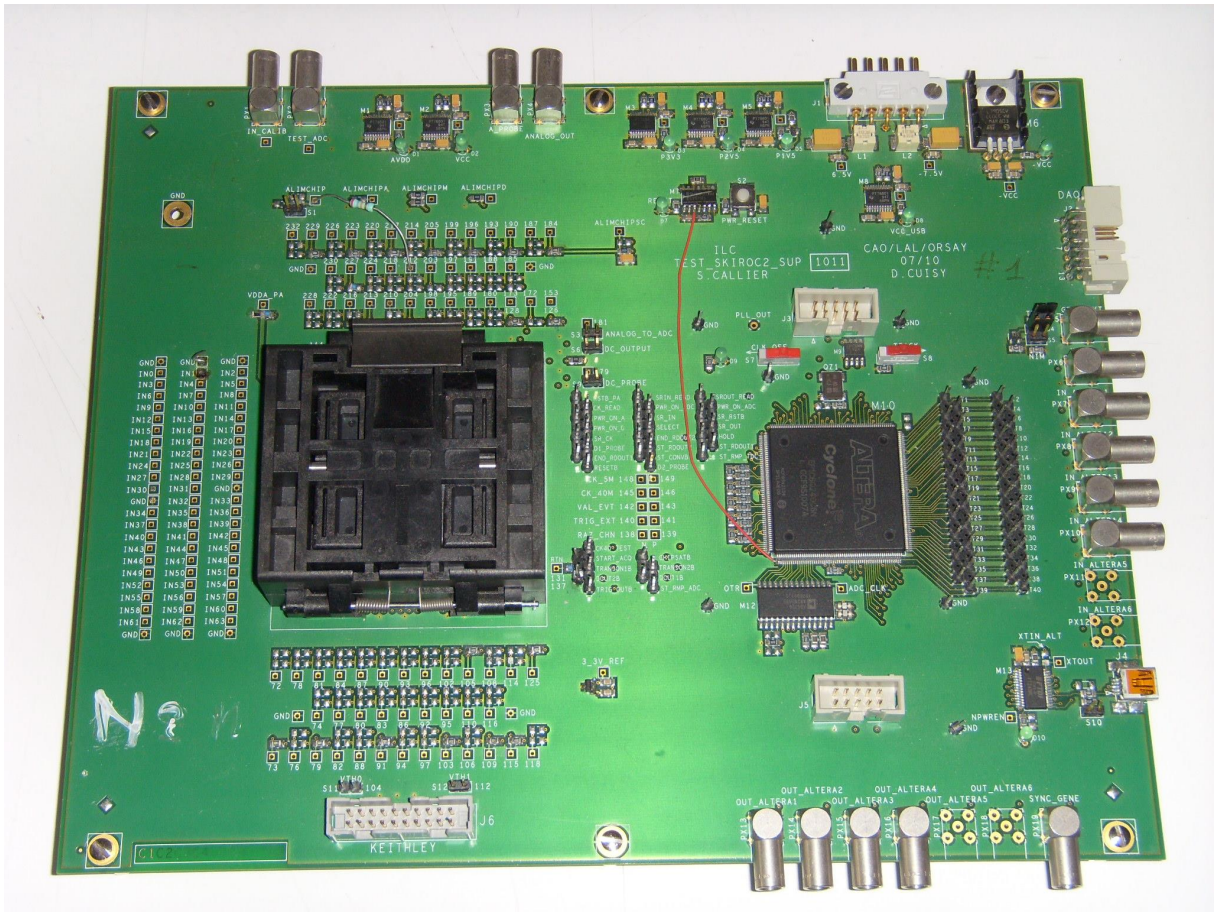


Table of content

1. Installation & Test of the Test Board

1.1. Pre requisites

The use of this PCB requires:

- A computer (windows OS) with USB connection
- A USB-A to mini-USB cable
- LabVIEW software version **2010** or later (*note that only **32-bit** version is supported*)
- A dual-output power supply (delivering 400mA for positive supply ***+6V*** and 100mA for negative supply ***-7V***)

1.2. Installation guide

Before connecting the board and running the LABVIEW software, the user has to follow some steps:

1. The user has to create the following folder : **C:\DATA\DRIVERS\FTDI**
2. He/she has to download the driver of the **FT245B**[1] and unzip the file inside this folder.
3. He/she has to install in few steps the **LAL_USB** [2] package (software setup application). This will also install the **Test245** software and add a shortcut on the desktop.
4. He/she has to power and connect the test board to his/her computer through the USB cable, and then the computer will ask for the test board driver. The user has just to indicate the folder in which he/she unzipped the file previously mentioned: **C:\DATA\DRIVERS\FTDI.**
5. During the LabVIEW installation, the user has to install the **NI VISA** software.
6. Then, he/she has to install the **NI IVI Compliance Package (ICP)**[3].
7. He/she has to install the **Keithley 2000 Driver (IVI version)**[4] for LabVIEW. Note: This tool is needed even if the user does not use this material.
8. He/she has to install the **Agilent E3631A (IVI version)**[5] for LabVIEW. Note: This tool is needed even if the user does not use this material.
9. He/she has to launch **National Instrument Measurement & Automation Explorer**, select in the **Tools** menu, **NI-VISA**, then **VISA options**, and in **passport**, he/she has to enable **NI-VISA Tulip**.
10. He/she has to launch the program **Test245**: This will check if the USB device (the test board) is well recognised. *This program has to be run prior using the LabVIEW software if the test board power supply has been switched off.*

[1] Available at http://www.ftdichip.com/Drivers/D2XX.htm
[2] Available at http://lalusb.free.fr/software.html
[3] Available at http://www.ni.com/ivi/ivi_prod.htm
[4] Available at http://www.ni.com/devzone/idnet
[5] Available at http://www.ni.com/devzone/idnet

Figure 1 show results when a test board has been found. Device Description and Serial Number are displayed and surrounded by a red circle. Serial Number parameter has to be provided to the LabView software for a proper functioning.

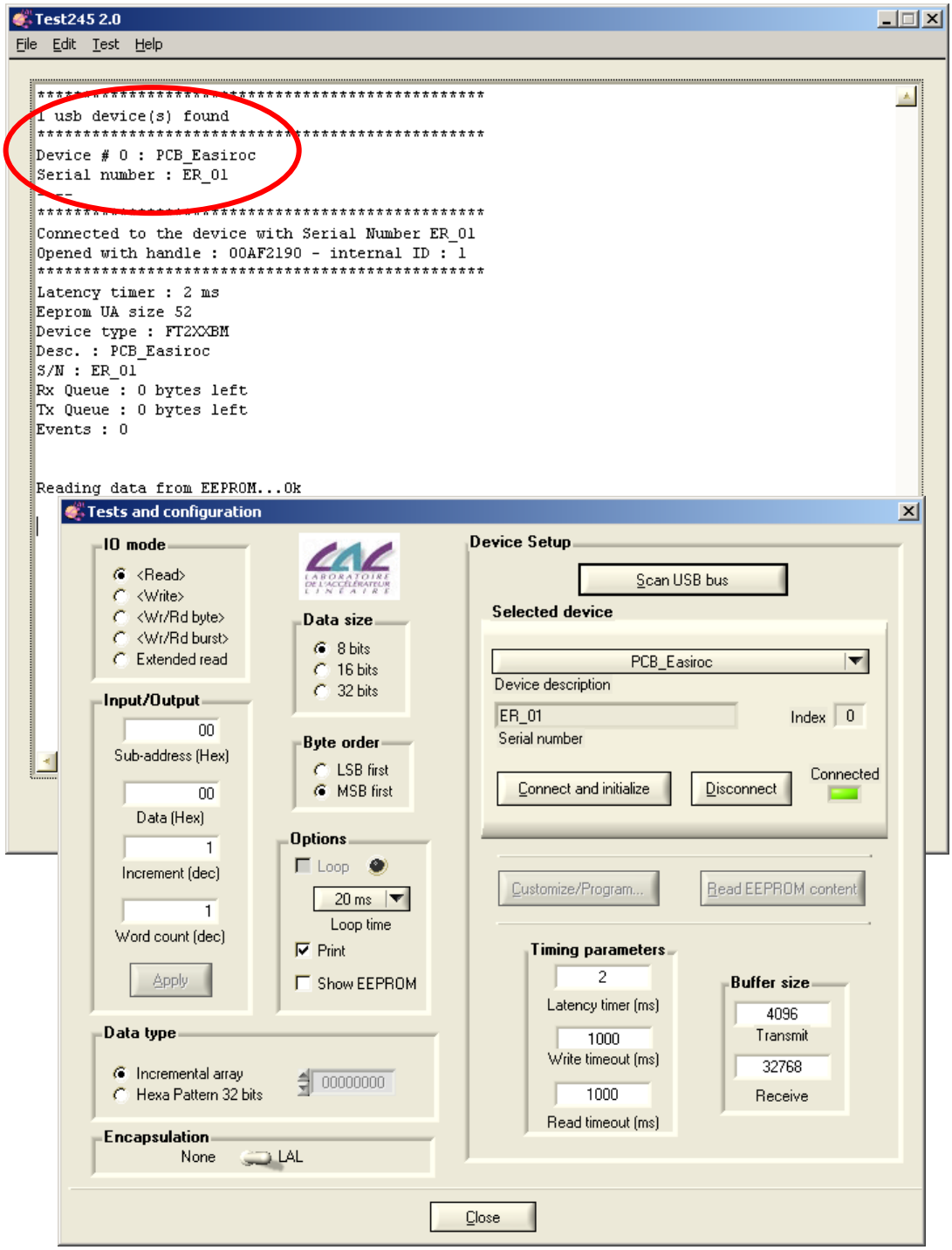
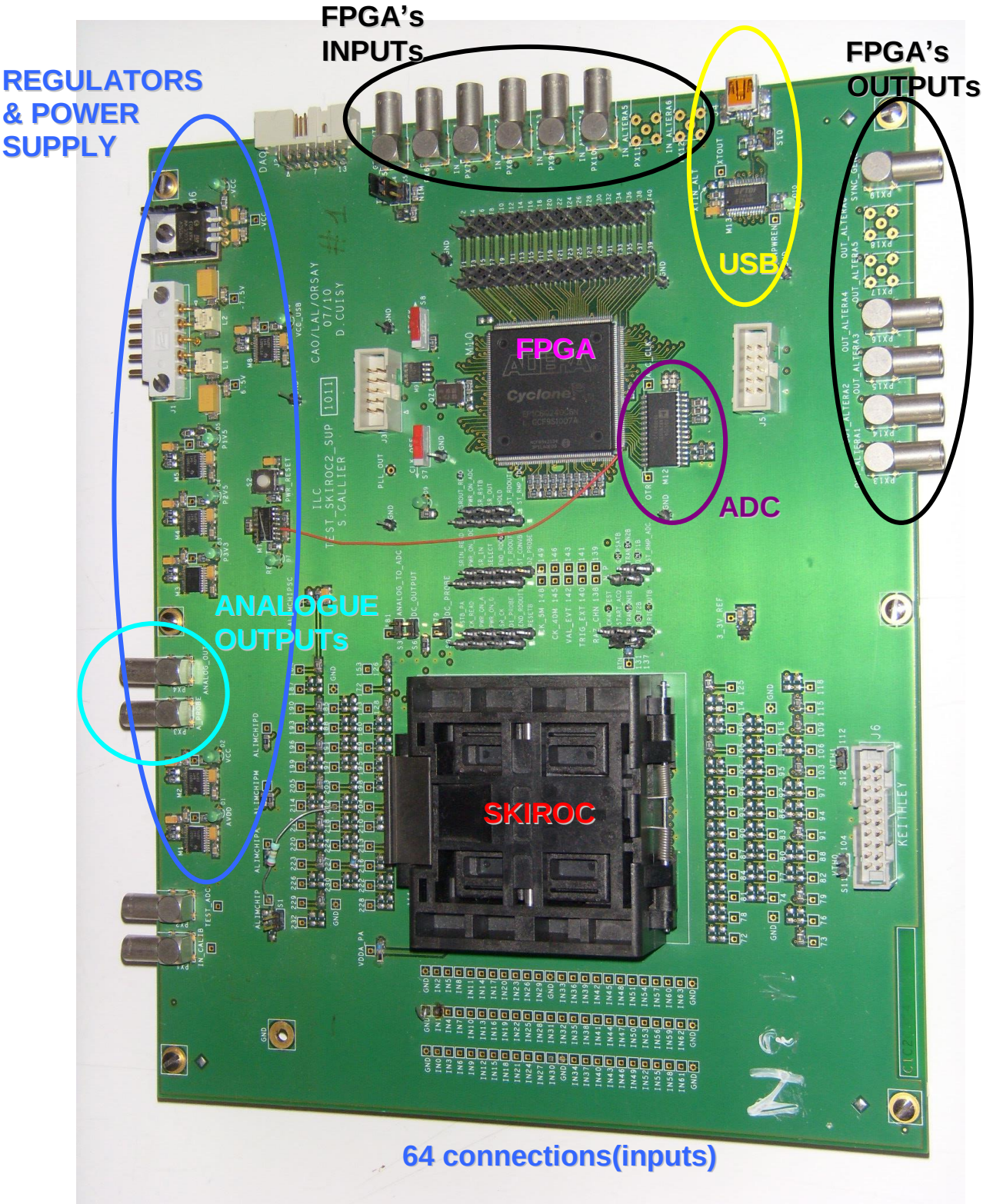


Figure 1 - Test 245 window and prompt when the test board has been found

2. PCB presentation

The test board you have in hands has mainly been developed to allow characterization and debug of the ASIC SKIROC. Some features were added on the PCB or in the firmware/software to allow its use with real detector or within an experiment. This versatility is nicely convenient, and as schematics of the PCB, the firmware and software sources are provided, users can modify anything to fit its own requirements.



- The PCB allow easy access to each SKIROC's pin, as all analogues pins are connected to "square" holes (where pin number is written on the silkscreen layer) and as all digitals I/Os are connected to probes between the ASIC and the FPGA.
- Many test points are also connected to the FPGA, outputting digital internal nodes.
- The OR64 trigger signal output is available on LEMO connectors
- 2 analogue buffers provide ASIC's analogue output and analogue probe output on LEMO connectors.
- External ADC is on-board, allowing ASIC internal and external data acquisitions.

Note that SKIROC power consumption can be monitored on connector S1 as a 1 ohm resistor is set is serial mode on the power line.

3. The Software

Once you have successfully executed the **Test245** software, get the Serial Number and provide it to the SKIROC Software. When this software is launched, the number of devices detected is displayed, and no error should occur, meaning that the installation has been successfully achieved.

If crash occurs, restart the procedure and check both USB cable and Power Supply. Ensure too that a 40MHz clock is well provided to the FPGA by checking the status of the LED (D9). Whenever no light is emitted, remove the on-board switch (S7) from the "CLK OFF" position.

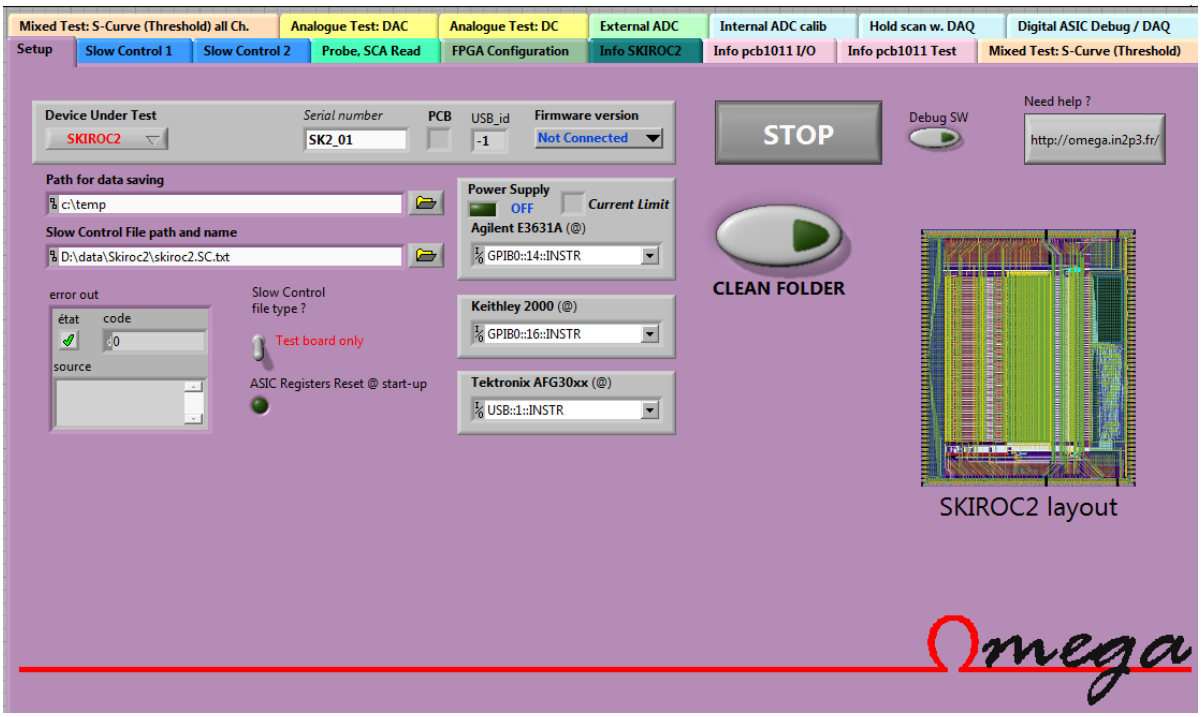


Figure 2 - Setup entry cells (Inputs: white boxes, Outputs: grey boxes)

Note that the Firmware Version is automatically detected by the software. When bugs are discovered, either the firmware or the software (or both) is (are) corrected. Please visit our website http://omega.in2p3.fr , in the download centre area, to check the available updates. If update of the software is very simple (only download and replace the old one), the update of

the firmware requires an external bundle. Indeed update is performed by an ALTERA "USB Blaster™" connected to the connector "Serial Active" (for definitive programming) or "JTAG" (for temporary update, until power supply is shut down).

3.1. Informative pages

To avoid the need of many papers, datasheets, applications notes and so on, 3 front pages have no function but to provide useful information concerning the chip pinout and the PCB, its connectors and tests points.

Figure 3 - Chip informations page

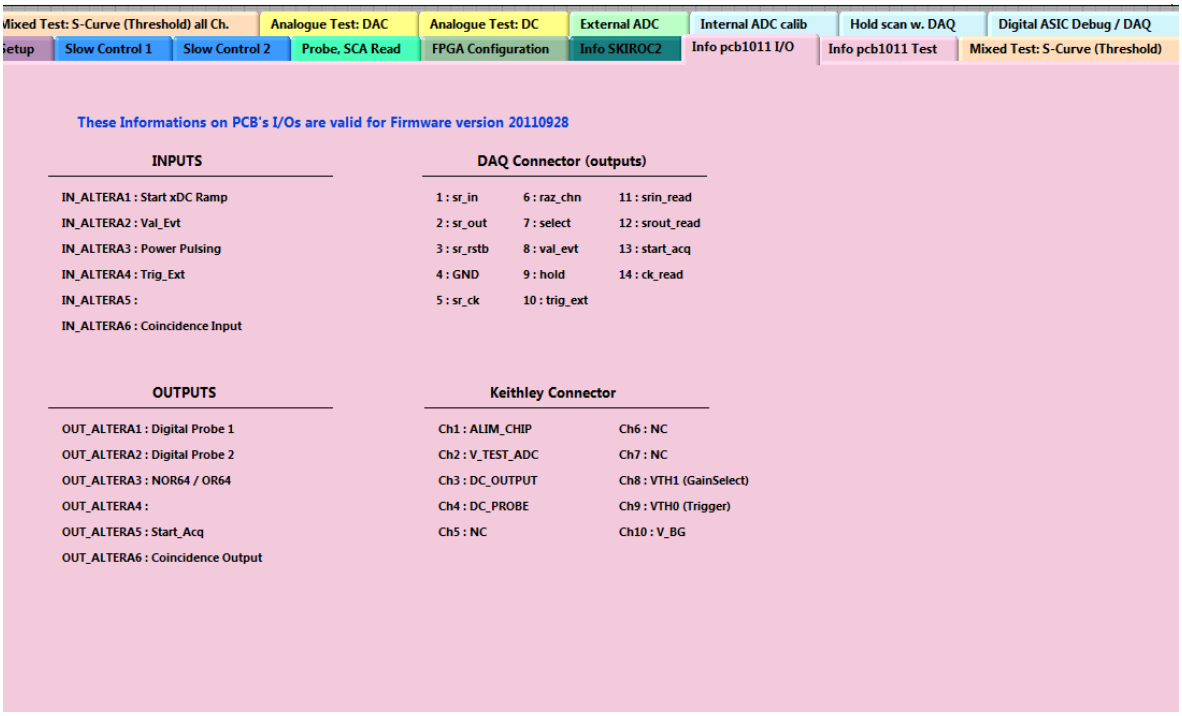


Figure 4 - PCB information page [connectors + FPGA I/O]

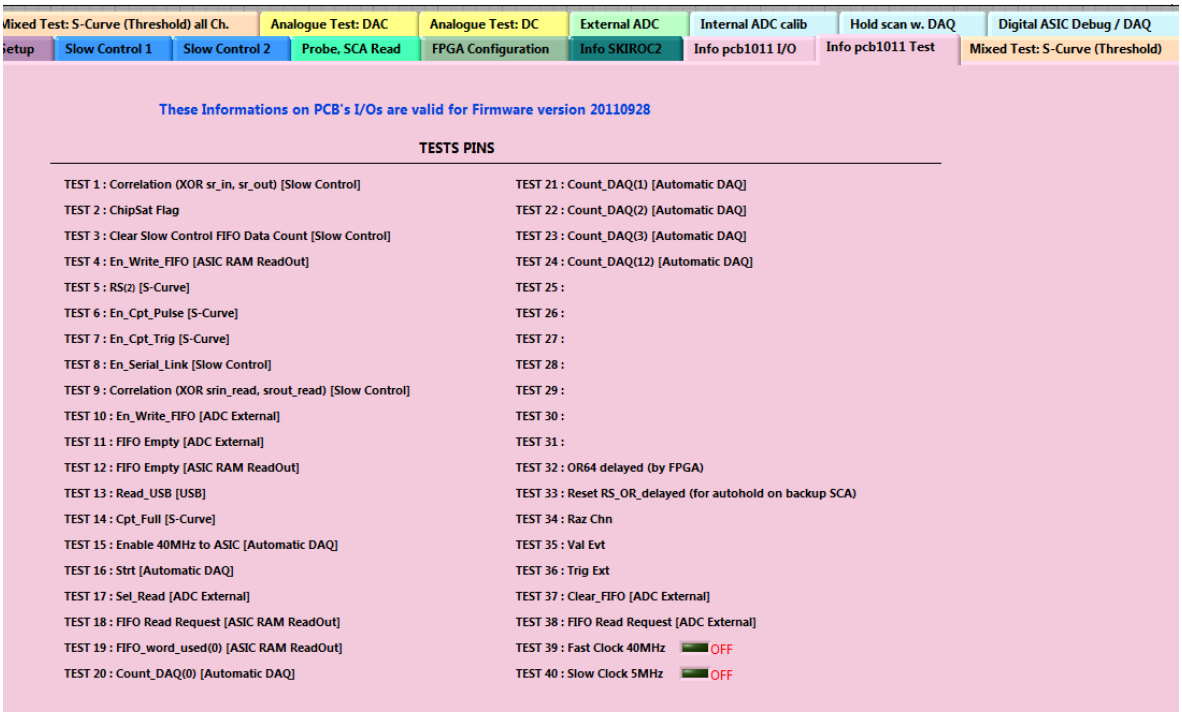


Figure 5 - PCB information page [connectors + FPGA I/O + Test points]

3.2. The slow control pages

All the slow control parameters of the SKIROC are displayed on these 2 pages, allowing tuning & tests of different settings.

To program the ASIC, just click on the "Transmit Slow Control" button. A front page indicator displays the status of this SC register and should be green after a "Transmit SC" command. This SC register can be reset by the "Reset Slow Control" order.

The settings of the front pages can be saved in a text format file thanks to "Save -> File Slow Control" button, and reloaded from this file by the "File -> Load Slow Control" command. This is very helpful as there are more than 600 slow control bits! Note that the path & name for this file has to be provided in the cell of the setup entry. Refer to the datasheet to know the meaning of every individual bit!

Depending only on the Slow Control configuration (preamplifiers, fast shapers, 10-bit DACs and discriminators mask) and on the Pwr_On, Val_Evt & Raz_Chn commands, the triggers should be immediately available on the OR64 output after the transfer of the slow control.

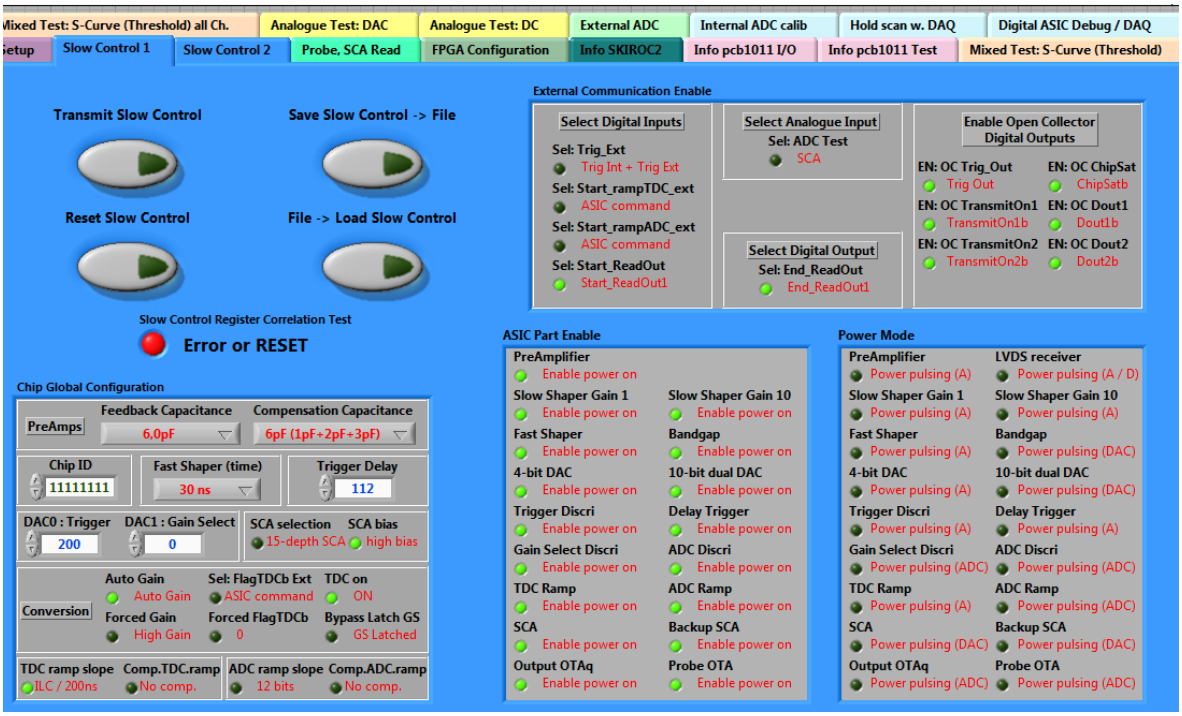


Figure 6 - Slow Control page (1)

On "Slow Control (2)" page, some settings are individual for each channel (Test Capacitance & Trigger). A 3-position cursor allows forcing all these control bits active or inactive. For these 2 cases, no matter is the status of the LED inside the box shown close to the cursor. Only the third position (in the middle) takes care of the bits position inside the associated box.

For the 4-bit DAC Adjustment, the 3-position cursor allow to either have an individual value for each channel, or have a common value for all channel, or have only one channel which has a different value of all other channels.

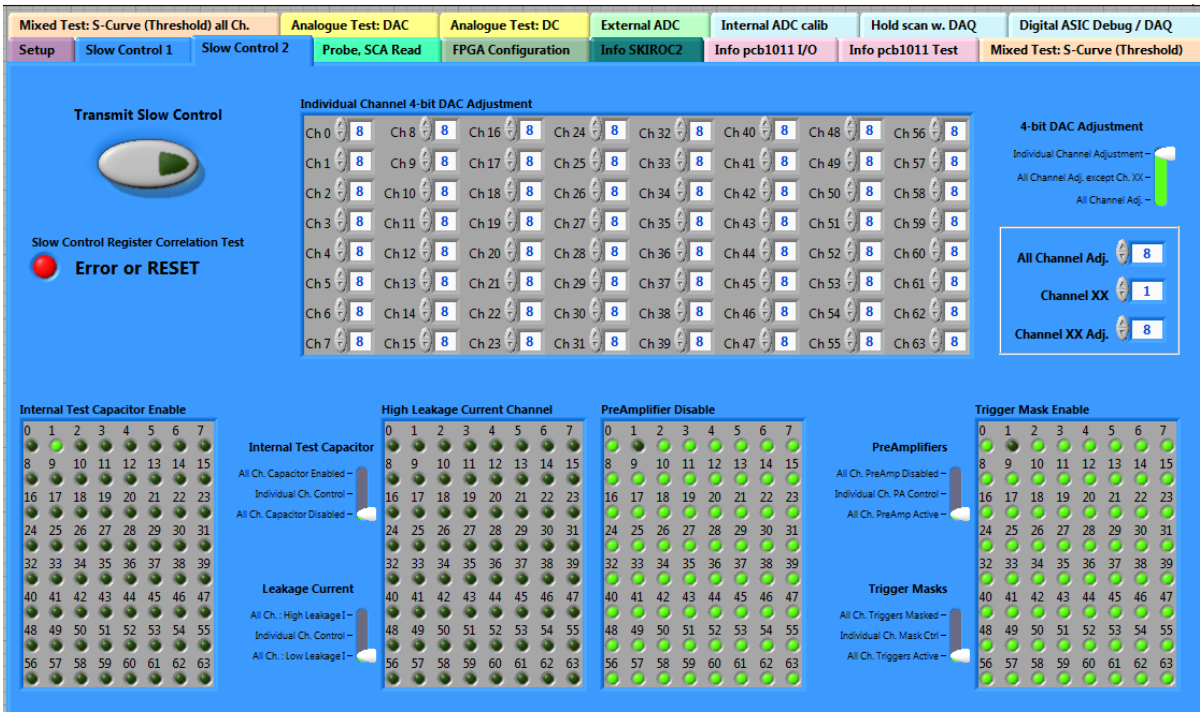


Figure 7 - Slow Control page (2)

Note on the Slow Control configuration / bits meaning:

The *ASIC Part Enable* bits allow to shut down any unused stage of the device.

The *Power Mode* bits can/should be left ON, except if user needs to power down the stages to save power during dead time.

The DAC Threshold and the shaping time can be changed in the *Chip Global Configuration*, as well as the data to be digitized/converted (data to digitized is displayed on the "SCA Read" page when using analogue output and on "Digital ASIC/DAQ" page when using digital output). This choice is made thanks to the "SCA selection" SC bit (15-depth SCA uses internal ADC providing digital data, whereas Backup SCA allow analogue output use. To control the data to be digitized/converted, please refer to the datasheet's "Analogue Output/Converted data" Table.

The *External Communication Enable* is focused on the I/Os used by the ASIC. Most of the settings can be left as default values are for both analogue display and digital readout of the ASIC.

Refer to the datasheet to know the effects of all of the "Slow Control" bits.

Note that LabView allows choosing the start-up values, which is achieved by the "Make Current Values Default" command in the Edition/Tools/Execution Menu. You can save your preferred values thanks to this feature. The Load/Save option is preferred to this method.

3.3. The SCA read page & The Probe page

The “Probe register” is used for debug only, and allow monitoring of analogue and digital ASIC internal signals. Some probe signals (written in blue) require a channel number to be specified, while the one in purple need the column number too.

Note that the reset is common for both SCA Read register and Probe register.

The “Read Register” is a shift register which allow outputting sequentially the analogue hold data from the Analogue Memory (SCA) to pins 181 (also buffered on LEMO connector and DC level monitored on S6). This register is controlled manually by the 4 buttons (Transmit SCA read, next ch. SCA Read, previous ch. SCA Read and reset SCA Read register) on this page or automatically by the software during acquisition using external ADC.

When analogue output is selected (Backup SCA in SC page), the shaper output is directly displayed on the analogue output of the chip, thus once a channel is selected, no other command is requested (exception made of the hold/track command).

A hold signal has to be provided to the board at the maximum signal of the charge, and the switch S8 has to be set on the “HOLD” mode, otherwise, no hold is performed on the analogue memory. The “TRACK” mode is only useful for debug. Note that display shown using that mode does not indicate the maximum value of the charge, as internal buffers have low biasing current for saving power consumption and thus slow down the signal displayed. The choice of the Hold signal is made on the “FPGA Configuration” page (either OR64 of the triggers which is delayed by a tuneable delay, or external hold signal of the hold connector).

Note that in order to see the Triggers from the chip, AutoDAQ has to be disabled if no acquisition is performed, as the “Val_Evt” signal is set to low in AutoDAQ mode (except during acquisition).

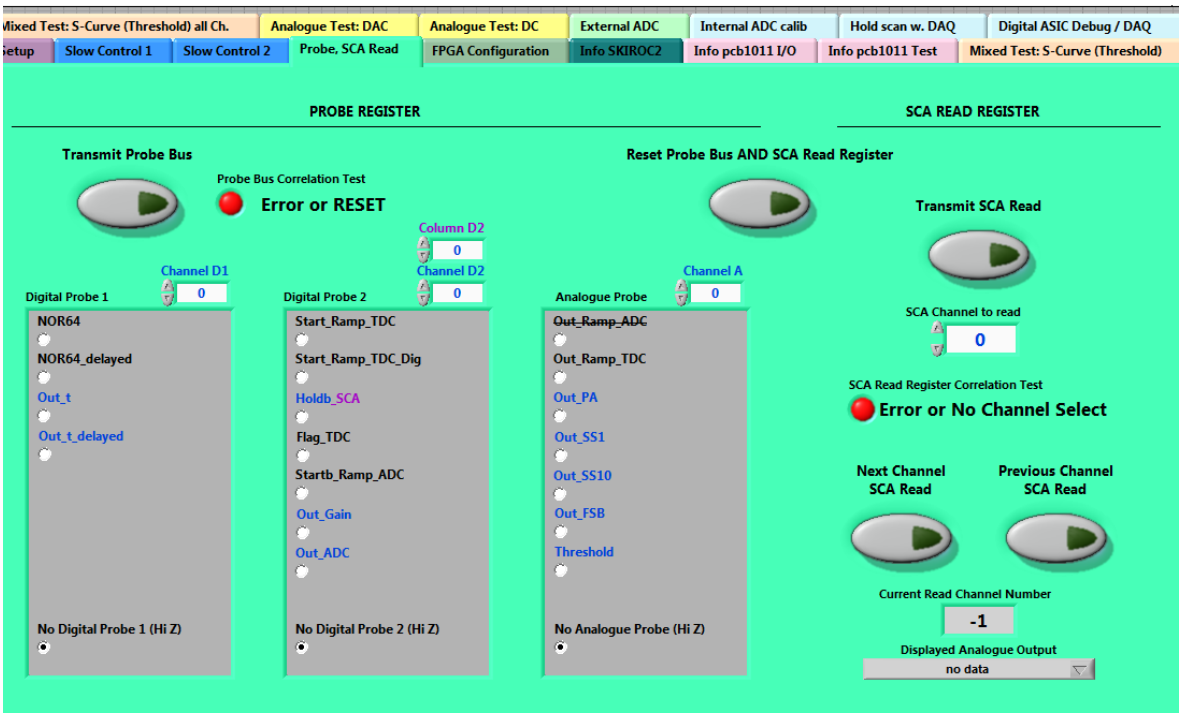


Figure 8 - Read and Probe page

3.4. The FPGA configuration page

This page is mainly used for the configuration of the board.

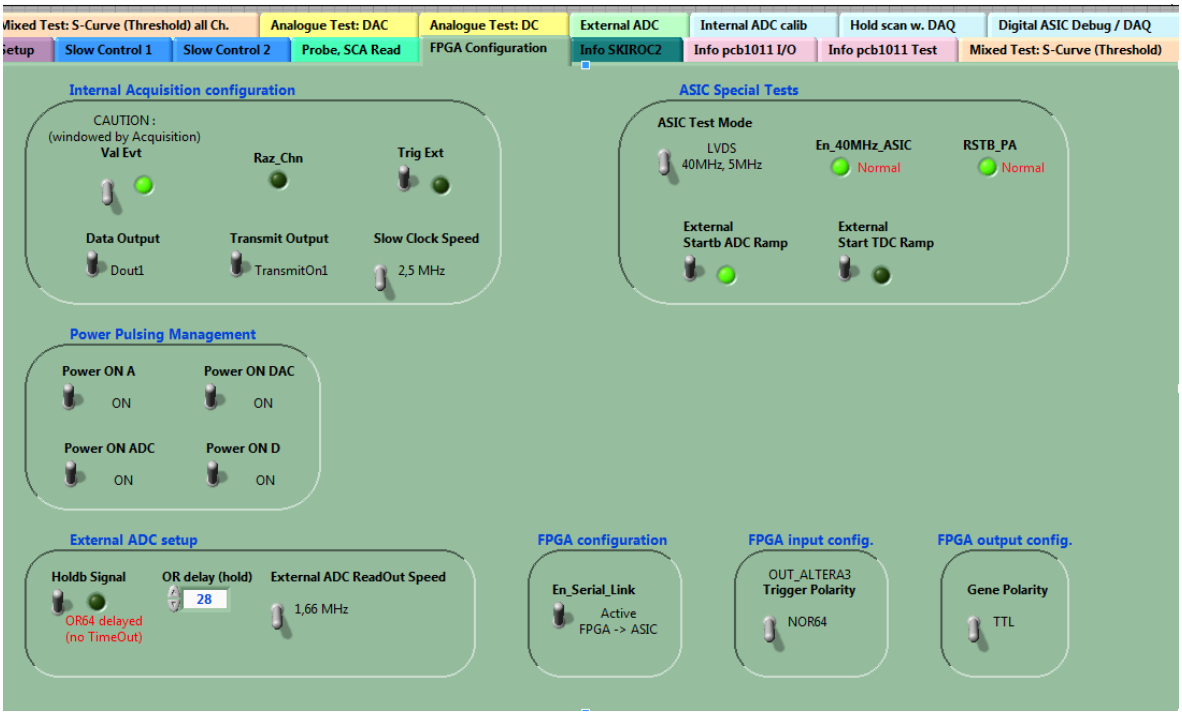


Figure 9 - FPGA configuration page

On this page, the ASIC configuration depending on pin signals can be changed. The settings for some signal is displayed by a LED, a green LED on the front page corresponding to a logic “1”/ON (example: “Val_Evt” or “Raz_Chn”).

When the switch of the Power_ON bit is set to “ON”, the PWR_ON pin of the ASIC is set to logic 1. Otherwise, when this bit is set to “Low/In_altera3”, data presented to the PWR_ON pin is the same as data provided to IN_ALTERA3 LEMO connector. If nothing is connected, the PWR_ON pin is tied to logic 0.

3.5. The Digital ASIC page

This page is useful to perform digital acquisitions using the digital part of the ASIC. Two modes are available. In AutoDAQ case, the user has to specify the clock used by the ASIC, which will be used as time tagging reference. It can be either the FPGA internal one (5 or 2.5MHz) or external clock provided by the user (low down to 5kHz and up to 5MHz). In that case, the user can control the phase of the injected charge with respect to the clock.

The chip has to be well configured in order to acquire date with the digital part: in the Slow control, be sure that the settings are well configured (Masks, Threshold).

A “manual” Data Acquisition system can be used (ie. “Automatic DAQ” is not selected). Each buttons are available for step-by-step control of the digital part of the ASIC. Refer to SKIROC datasheet to understand the full working mode of the ASIC. Basically, when the

acquisition is started, if triggers occur, analogue data are stored in the Analogue memory; a digitization sequence is then needed, followed by the ReadOut of digital RAM of the ASIC.

An automated DAQ is available. When using this mode, the user needs to provide the number of acquisitions and then start the test sequence! Note that it is recommended to erase previous data before taking a huge amount of data, as LabVIEW is slowing with respect to the number of files written on the Hard Disk Drive. Digitized data are displayed in the software (raw data, decoded data and an histogram is plotted –which requires to specify a channel number and a column value) and saved to files.

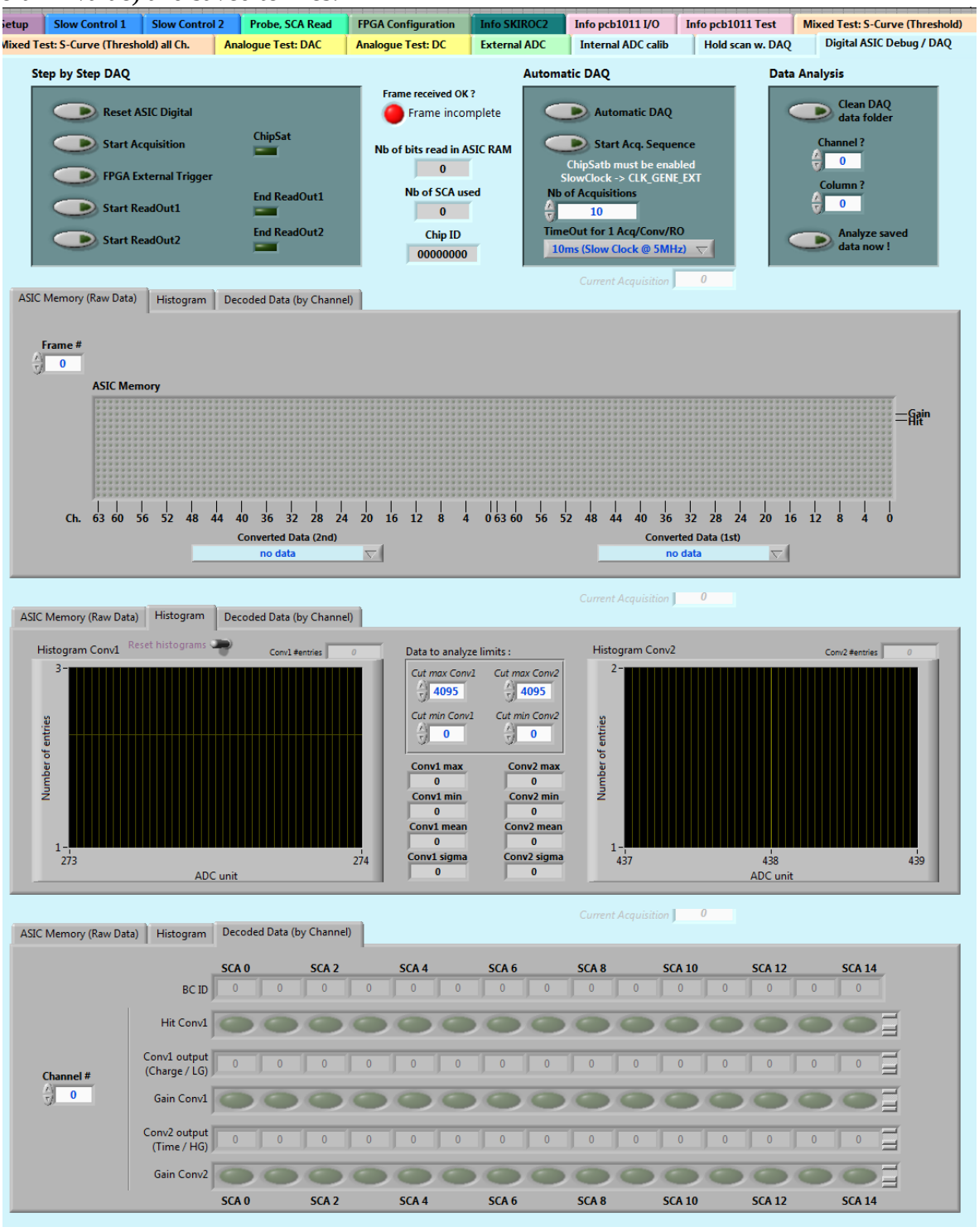


Figure 10 – Digital ASIC page

3.6. Hold Scan page

This chip performs the energy measurement of the particles which crosses the Silicon Detector. As the signal corresponding to the energy is filtered by a shaper, it is important to have a good precision on the sampled signal. Using a pulser as emulation of the injected charge and the OR64 as hold command for this sampling command, the software can perform a step-by-step scan to reconstruct the shape of the signal.

As the delay is done using FPGA internal PLL clock (40MHz), the step is 2.5ns. The user has to specify the step, the minimum and maximum of the delay on the OR64 as hold signal.

This test requires that the AutoDAQ is fully working and analyses one channel and one column specified.

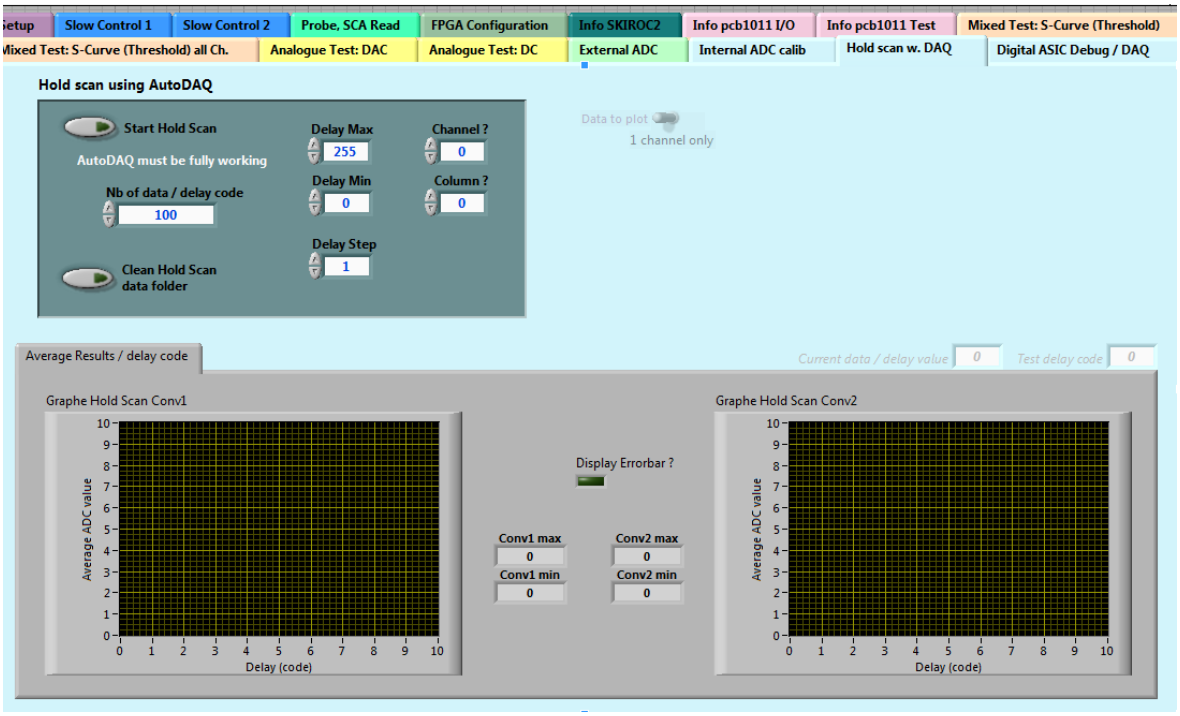


Figure 11 – Hold Scan page

3.7. Internal ADC calibration

Using an external power supply Agilent E3631 controlled by GPIB, the internal ADC can be calibrated. As the chip embeds a Wilkinson ADC, all channels are sampled and digitized at the same time. Thus, injecting a DC voltage on the pin 183 (in_adc_ext) and setting the SC bit to “select ADC test” instead of “SCA” (in the External Communication Enable, will bypass the entire analog front-end to directly provide this DC voltage to the internal ADC.

This test requires that the AutoDAQ is properly working. As the steps of each ADC bin is about 500µV, this test can be quite long, and it is recommended to start it before a long away time!

3.8. The S-curve tests

The trigger efficiency is a very important measurement. The trigger efficiency versus DAC value has been automated in this software. Note that for this test, the NOR64 must be selected on the Digital Probe 1.

The "Single Custom Test" does not change any slow control parameter (no trigger masked, no injector Capacitance enabled/disabled) except made, of course, of the DAC value! Triggers occurring while performing this test are due to any channel, depending on your slow control setup. As this test will not perform a loop on all channels, it is a quite fast test. Final result of this test is displayed on the top right graph. 3 small grey boxes allow a live monitoring of number of pulse injected and of triggers counted by the FPGA, as well as the current DAC value.

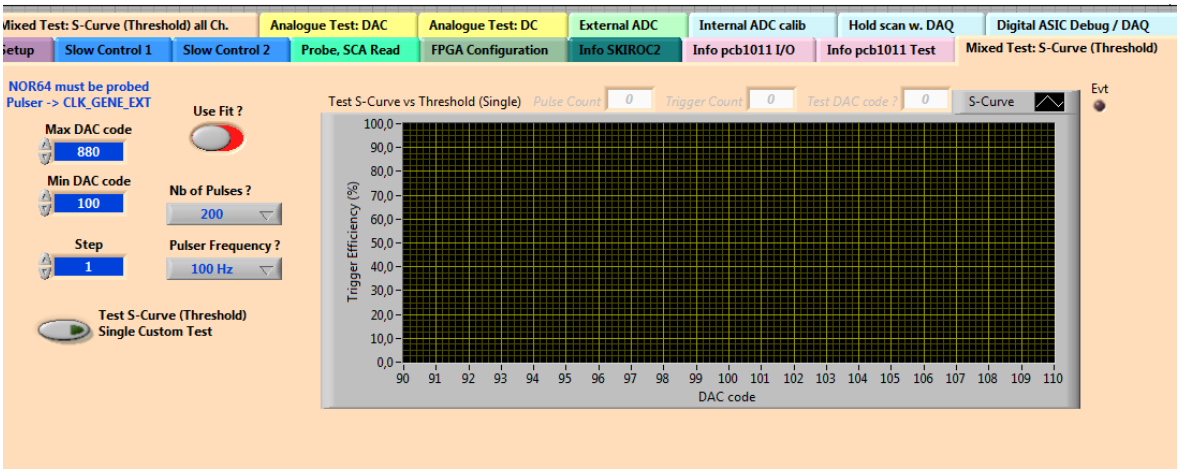


Figure 12 - S-curve page (single)

The "Fully Automated Test" takes over the setting specified in the slow control to test trigger efficiency channel-by-channel. Injection capacitance and trigger & PreAmps (if requested as "Mask other Channels"/"Mute other channels" green LEDs) are activated for the channel under test. Results of last channel tested are shown on the bottom left graph. After the 64-turn loop is achieved, the final result is nicely plotted on the top right graph, using different colours to distinguish each channel. The 50% trigger efficiency is displayed below.

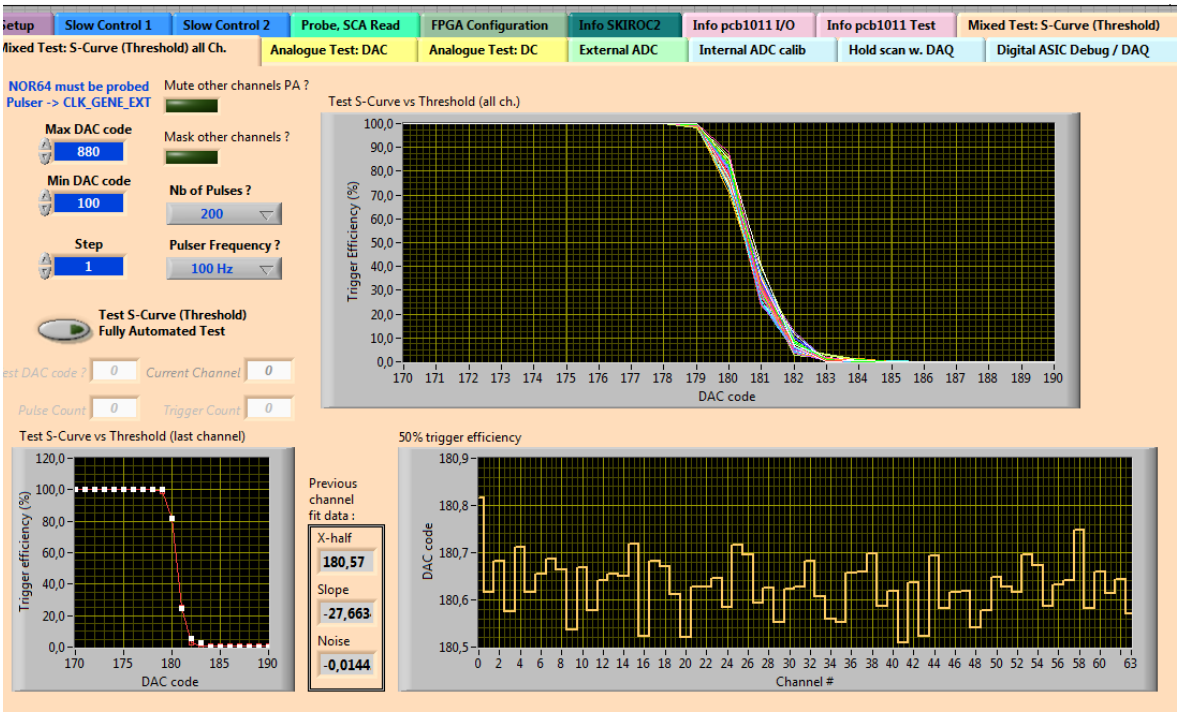


Figure 13 - S-curve page (automated)

Of course, all data are saved in files for off-line use. Number of pulses to be injected and injector frequency have to be specified. Minimum, maximum and step values can be tuned. A reference clock has to be provided on the CLK_GENE_EXT connector. This signal is driven by the following rule: Injected charge has to occur more or less at the same time as the rising edge of this clock (Refer to Figure 14). Moreover, En_count_T (a signal which is available on a test pin), has also to be synchronous with this signal.

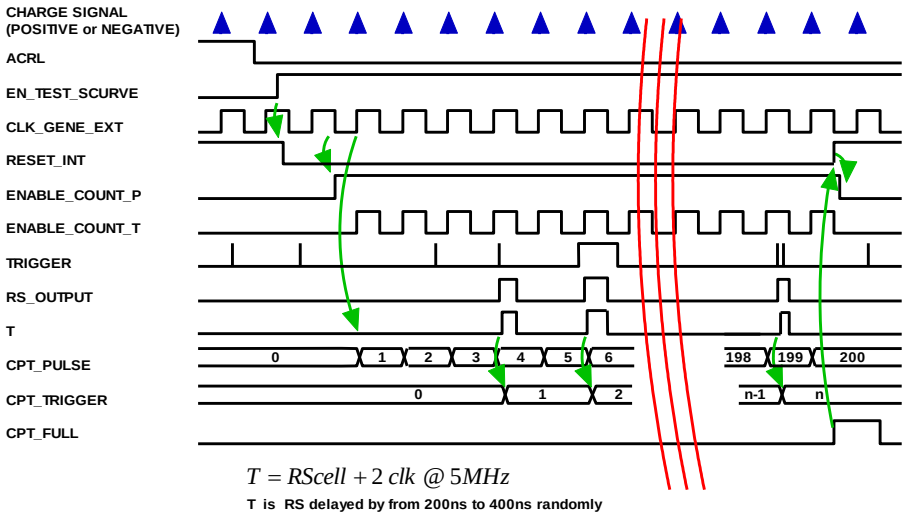


Figure 14 - S-curve test working mode

The specified Pulser frequency must be higher or equal to the injected frequency; otherwise some pulses could be missed. This is the case if the Pulse counter displayed does not reach the specified value.

3.9. The DAC(s) characterization

The software allows performing a linearity scan on the Threshold DAC and on the Gain Select DAC. Data acquisition of the measured voltage has been developed using a Keithley 2000 DMM. GPIB address of this tool has to be provided in the adequate white box, as well as the address where data will be saved.

Maximum DAC tested value has to be provided. Note that name of the saved files are clearly distinctive and no confusion in the resulting files can be seen.

When a linearity scan is performed on the Threshold DAC / Gain Select DAC, analogue data is available respectively on S11 / S12.

Results compute automatically the fit and provide the linear fit parameters, the INL, the DNL and plot the residuals.

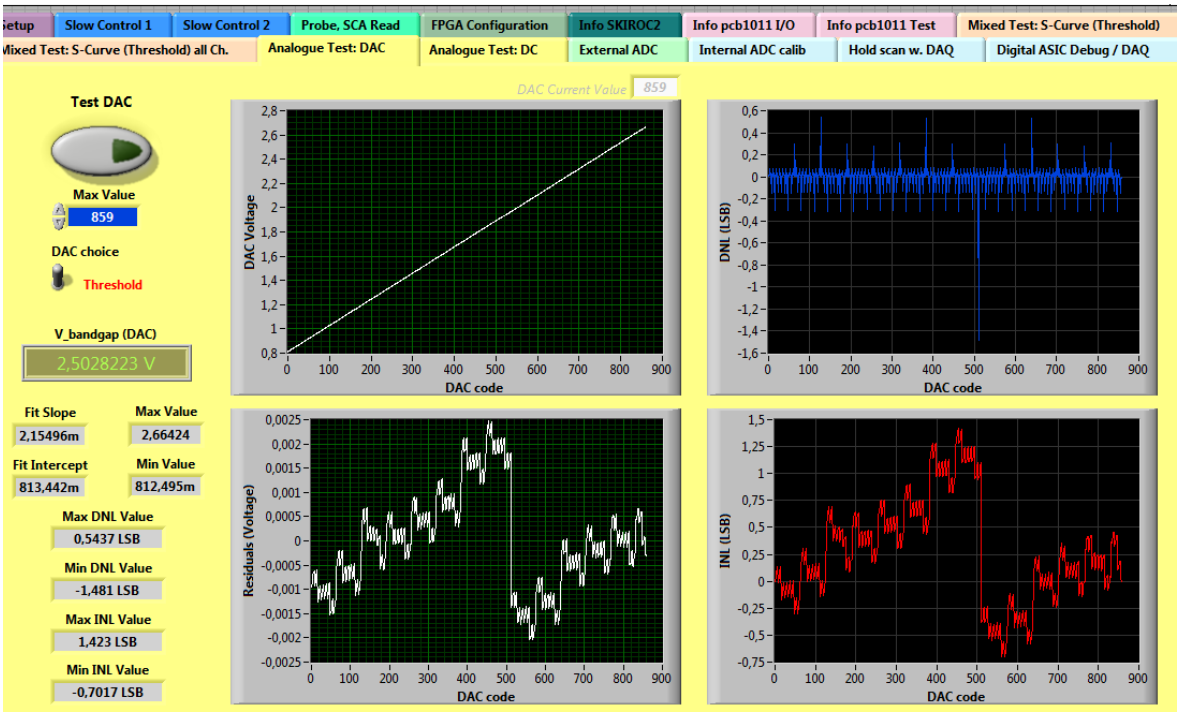


Figure 15 - DAC linearity test

3.10. The DC tests

Using the same Keithley 2000 DMM, but requiring additionally the scanner module plugged to the dedicated connector on the PCB, this software allows performing basic DC tests on any analogue point of the ASIC using the “Test DC” button., in order to check the behaviour from channel 0 to channel 63 (dispersion between channels).

The “Check DC” button provides a quick measurement on all the voltages displayed on the dedicated connector of the board.

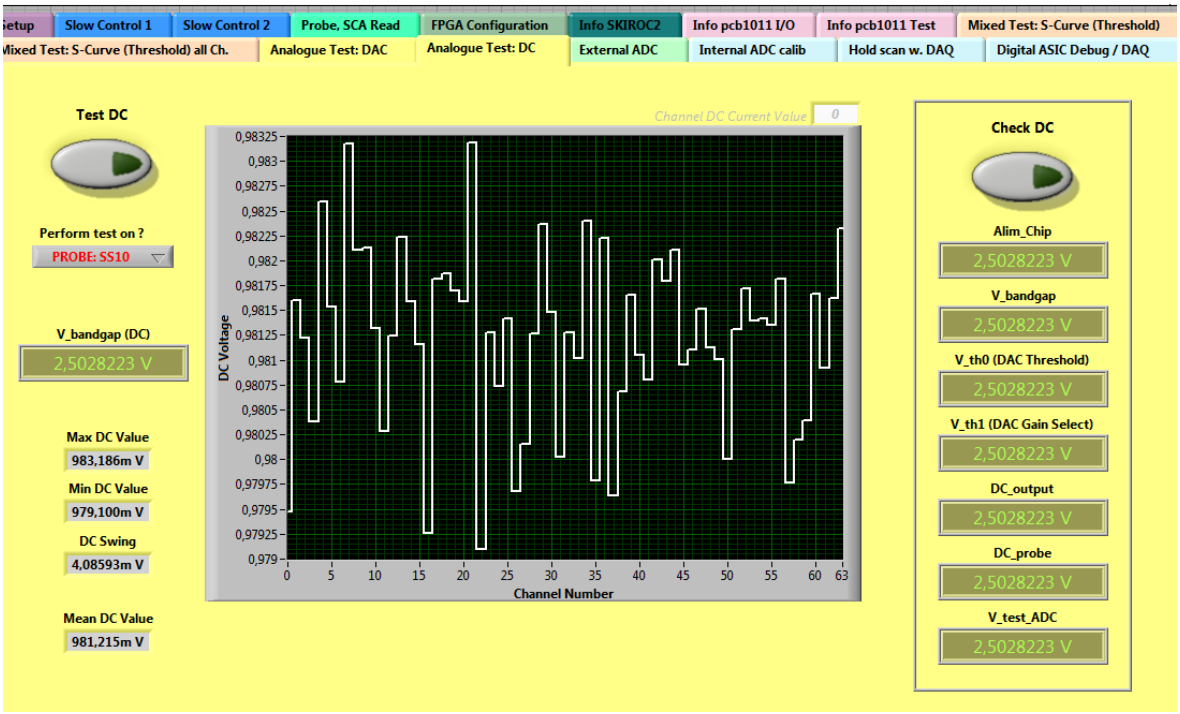


Figure 16 - DC tests

3.11. External ADC acquisition

The External ADC configuration is changed on the FPGA page, a switch allow to choose either the hold command from the HOLD connector or the OR64 delayed by the delay written in the box close to.

This tool is “experiment oriented” test. Indeed, all the other tests are only useful for the characterisation of the SKIROC chip, whereas this one allow acquiring data, with a detector connected to the board for physics analysis.

SKIROC has one analogue outputs, which is digitized using a robust ADC (AD9220 from Analog Devices). Result of live acquisition is shown on the top and right part of the page: for each channel, the converted value is displayed. The “Out of The Range” (OTR) signal is not monitored but saved in the file. However, this should never occur, as data coming from the chip are within the dynamic range of the external ADC. Note that jumper S3 has to be shorted to make link between ASIC output and ADC input.

The histogram shown on the bottom left plots the data of the specified channel in the Channel to analyse box (Ext ADC Channel to analyse?).

This test is not very fast, and it is recommended to clean the folder where the files are saved before each acquisition as the more files they are, the slower LabVIEW is to write the results.

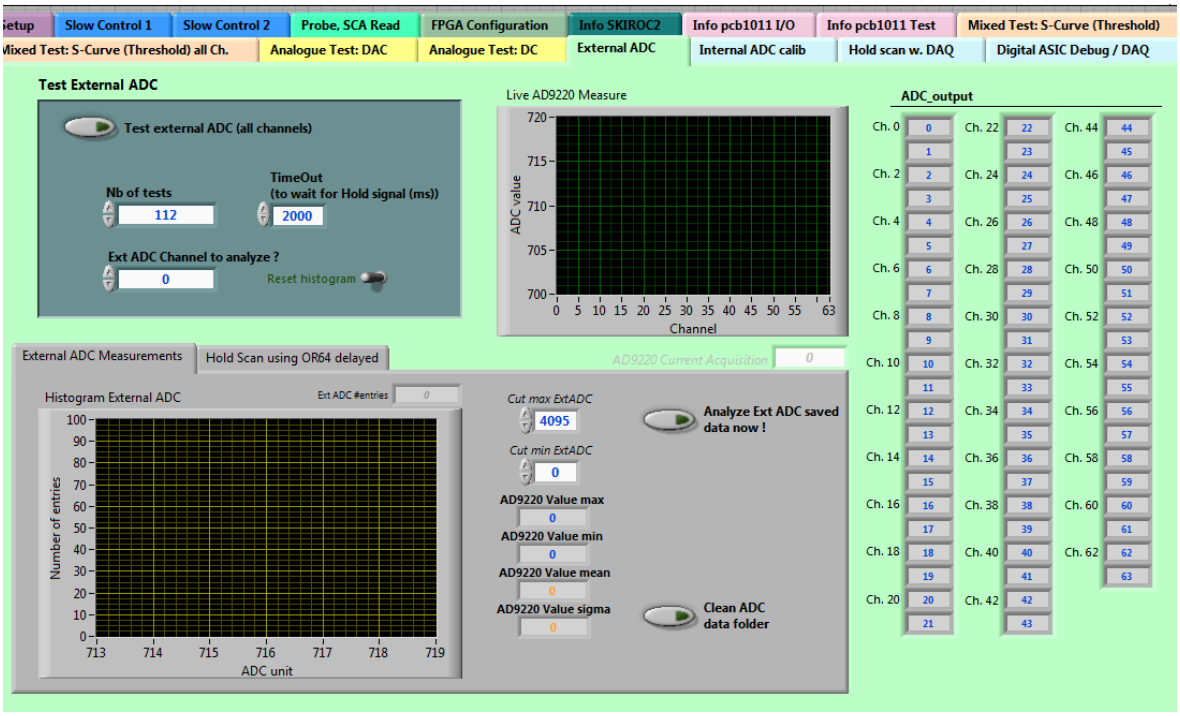


Figure 17 – External ADC test

Note that a “hold scan” (delay scan of the OR64 as sampling command) is provided and can be used by this External ADC.

After launching the test (by clicking on the "Test External ADC)" command), FPGA will wait for the specified time. If a hold command is provided, then the automate will start the following sequence: reset of the read register(if enabled in external ADC configuration page, recommended), then set the channel 0 on the output, then digitize it, then switch to channel 1, then convert it, and so on until last channel (channel 63). Digital data are sampled by the FPGA and saved to a build-in FIFO.

Note that the hold command must be provided. This signal can either come from the LEMO connector called HOLD or be provided by a delayed OR64 Trigger signal or be supplied by a delayed coincidence trigger signal. The hold command should fit with the maximum value of the analogue charge (corresponding to the peaking time).

On the screenshot below, analogue output is displayed in yellow, and digitized data in the software fit well with the data on the scope. In this case, channel 0 received a injected charge.

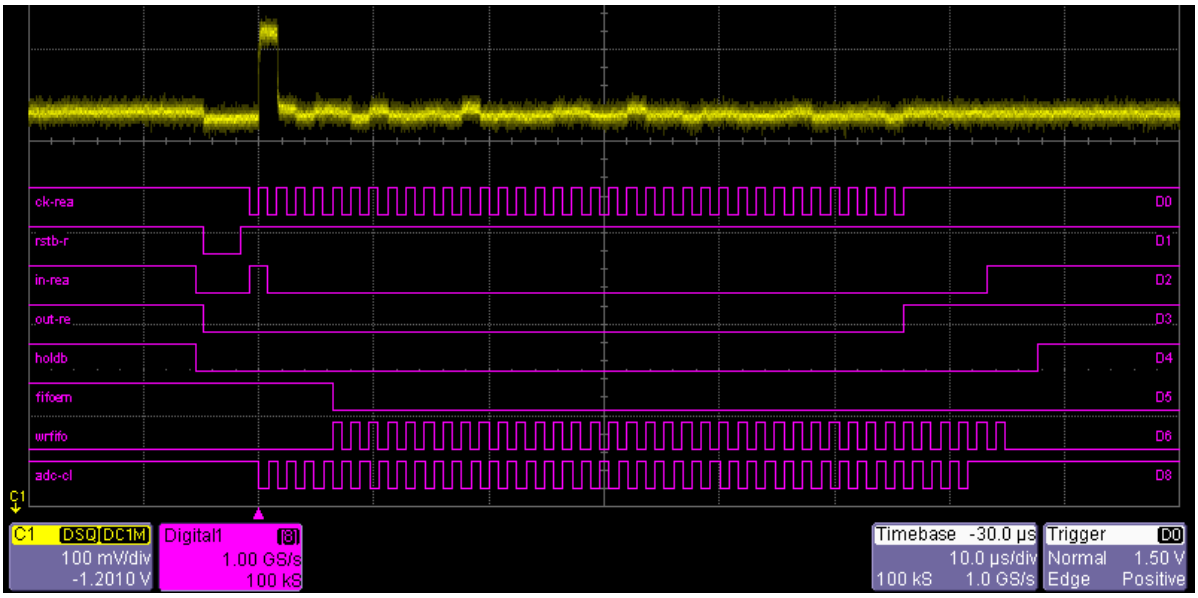


Figure 18 - Scope screenshot of an External ADC acquisition

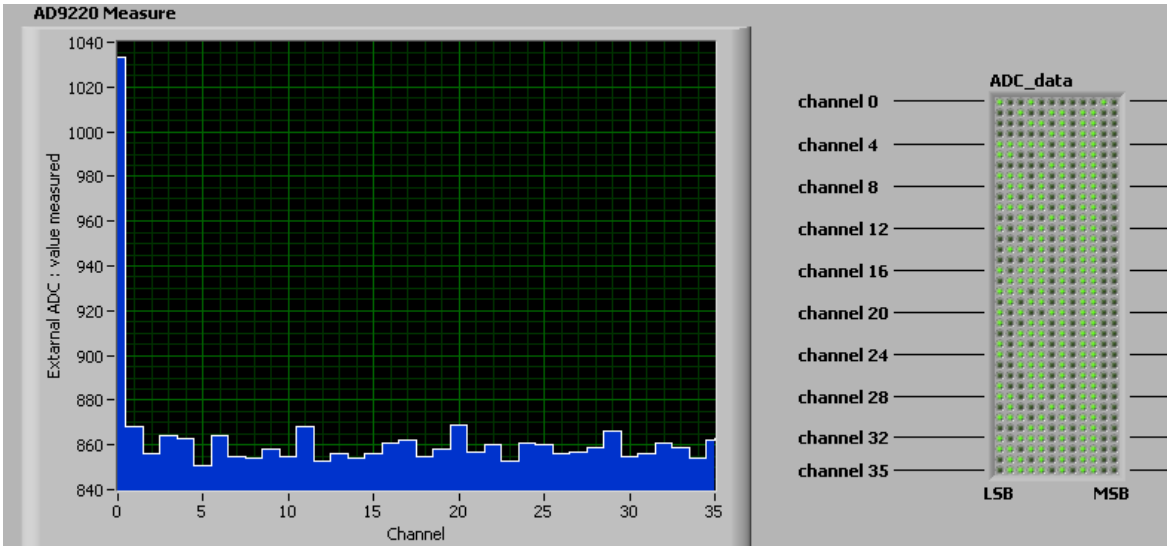


Figure 19 - LabView page corresponding to the acquisition above

Annex A: Testboard's FPGA Internal Registers

Skiroc2 Test Board ALTERA Registers

LSB							MSB
WORD 0							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
sel_val_evt	Raz_Chn	Val_Evt_LV	sel_trig_ext	en_serial_link		test_chk_read	test_chk_sr
Select Data to send to (ASIC) Val_Evt : '0' Lemo Conn. In_altera2, '1' Val_Evt_LV	'1' : Noise Trigger, clear last event	'1' : Valid Event	Select Data to send to (ASIC) Trig_Ext : '0' Lemo Conn. In_altera4, '1' Alt_trig_ext	'1' : Enable sr_ck, sr_in, ck_read, srin_read. '0' all Hi Z		'1' : SCA Read Correlation Test query	'1' : SR Register Correlation Test query
WORD 1							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
ADC readout speed	StartCycle (config)	resetb	trig_out_polarity	rstb_pa	select		sr_rstb
'0' : 1,66MHz '1' : 416kHz	'↑' : Start Data (Slow Control, SCA Read or Probe) Shift	'0' : Altera Output / ASIC input : ASIC Digital part Reset	Out_altera3 provides trigger output : '1' : OR64, '0' NOR64	'0' : Altera Output / ASIC input : PreAmps Reset	'1' : Select Probe Register '0' Select Slow Control		'0' : Altera Output / ASIC input : Slow Control Register Chain Reset (when select=0) / Probe and Read Register Chain Reset (when select=1)
WORD 2							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
StartAcq	Start_ReadOut2	Start_ReadOut1	Alt_trig_ext	DAQ_mode	Test mode	start_rampb_adc_ext	start_ramp_tdc_ext
'1' :Altera Output / ASIC input : Enable Acquisition	'1' : Altera Output / ASIC input : Start ReadOut Signal	'1' : Altera Output / ASIC input : Start ReadOut Signal	Data send to ASIC trig_ext if Sel_trig_ext = '1'	'0' manual DAQ, '1' Auto DAQ	'0' standard mode, '1' Test mode		
WORD 3							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
sel_pwr_on_d	sel_pwr_on_a		sel_pwr_on_adc	sel_pwr_on_dac	En_Test_Scurve	resetb_Scurve	sclkspeed
Select Data to send to (ASIC) pwr_on_d : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	Select Data to send to (ASIC) pwr_on_a : '0' LOW / Lemo Conn. In_altera3, '1' HIGH		Select Data to send to (ASIC) pwr_on_adc : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	Select Data to send to (ASIC) pwr_on_dac : '0' LOW / Lemo Conn. In_altera3, '1' HIGH	'1' : Enable Scurve Tests	'0' : Reset Counters for Scurve Tests	Slow Clock (5MHz) Speed : '0' 10MHZ, '1' 5MHz
WORD 4							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
		ChipSatb	End_ReadOut1	End_ReadOut2		chksum_read	chksum_sr
						SCA Read Correlation Test Result	SR Register Test Result
WORD 5							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
40MHz_ASIC	sel_ramp_adc	gene_polarity	Nb_scurve_0	Nb_Scurve_1	sel_Dout	sel_Transmit	ADC mode
'1' : Enable 40MHz Clock to ASIC '0': no Clock	Select Data to send to (ASIC) start_rampb_ADC_ext : '0' LOW / Lemo Conn. In_altera1, '1' word_2[6]	Select CLK_GENE_EXT [TTL] or not(CLK_GENE_EXT) [NIM]	Set the number of Pulses for Scurve tests: '0' => 200 pulses '1' => 1000 pulses '2' => 10000 pulses '3' => 50000 pulses		'1' : Dout1b '0' Dout2b	'1' : TransmitOn1b '0' TransmitOn2b	'0' none, '1' Test_internal_ADC
WORD 6							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
en_test_40M	sel_ramp_tdc	en_test_5M	sel_OR2hold	EN_TimeOut			debug_mode
'1' : Allow Fast clock on test pin 39. '0' : no data	Select Data to send to (ASIC) start_ramp_TDC_ext : '0' LOW / Lemo Conn. In_altera1, '1' word_2[7]	'1' : Allow Slow clock on test pin 40. '0' : no data	'1' : Select OR64 delayed as hold command. '0' : select HOLD connector.	'1' : Enable TimeOut for latched OR64delayed.			'1' : allow to send 1 clk tick on SR_CK or CK_READ
WORD 7							
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7

Adress 8	Scurve Pulse Counter (8-bit) LSB
Adress 9	Scurve Trigger Counter (8-bit) LSB
Adress 10	SR (Slow Control (select=1) and Probe (select=0)) Register
Adress 11	
Adress 12	SCA Read register
Adress 13	ReadOut FIFO empty & 0 & 0 & 0 & Word Used in ReadOut FIFO [11..8]
Adress 14	Word used in ReadOut FIFO [7..0]
Adress 15	ReadOut FIFO (8-bit)
Adress 16	
Adress 17	
Adress 18	Scurve Pulse Counter (8-bit) MSB
Adress 19	Scurve Trigger Counter (8-bit) MSB
Adress 20	StartADC ReadOut & 0 & 0 & ADC OTR & ADC ReadOut [12..9]
Adress 21	ADC ReadOut [8..1]
Adress 22	ADC FIFO1 Empty & ADC FIFO2 Empty & 0 & 0 & 0 & 0 & 0 & 0 & 0
Adress 23	Start_DAQ_Sequence & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
Adress 24	
Adress 30	0 & 0 & Delay for OR64 -> hold signal [5..0]
Adress 100	Firmware version

Annex B: Firmware of the PCB (Top level only)