# GEM-based HCAL

As HCAL sensitive elements, it must fulfill the requirements of high efficiency, high rate capability, homogeneity and compactness. Micro Pattern Gaseous Detectors (MPGD), in particular Gas Electron Multiplier (GEM), have been widely used in high energy experiments like COMPASS. With the development of GEM production technology, the maximum size of GEM foil should be increasing, and a GEM foil with an area of 60cm\*120cm has been produced by CERN in 2011. GEM detector can offer a high position resolution of few 10s of μm and provide flexible configurations, which allows small anode pads for high granularity that meets need for the CEPC calorimeters. It is fast with only a few nano-second rise time, and also has a short recovery time that makes GEM detector a higher rate capability compared to other detectors. It is robust against occasional discharges, and operate at a relatively low voltage across the amplification layer with a stable high gain while using ArCO2 as the working gas. Considered the properties mentioned-above and cost, a large area GEM detector could be attractive for a DHCAL sensitive detector.

A double layer GEM detector using self-stretching technique (as shown in fig.1) could be one of the candidates, it consists of 3 mm drift gap, 1 mm transfer gap and 1 mm induction gap, as shown in fig.2. The ionization signal from charged tracks passing through the drift section of the active layer is amplified by the double GEM foil. The amplified charge is collected at the anode layer with pads at zero volts. To keep HCAL as compact as possible, total thickness of the double layer GEM detector including readout electronics has to be minimized. The readout electronics could be integrated into the double GEM detector, and the board assembly will utilize a mechanical structure made of 4 mm absorber-stainless steel plate. The other consideration is to change the structure of GEM detector. μRWELL, a new structure gaseous detector, has characteristics in common either with GEM or Micromegas, as shown in Fig.3. Compared to GEM and micromegas, the μRWELL detector is extremely compact, and it does not require mechanical support while allowing large area covering.

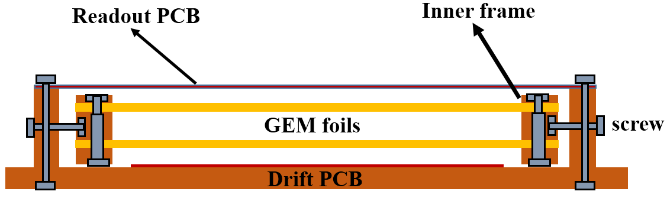


Fig.1 Self-stretching technique (from CERN)

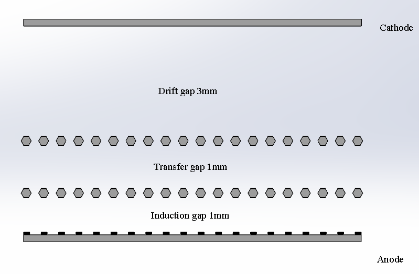


Fig.2 Structure of the double GEM detector

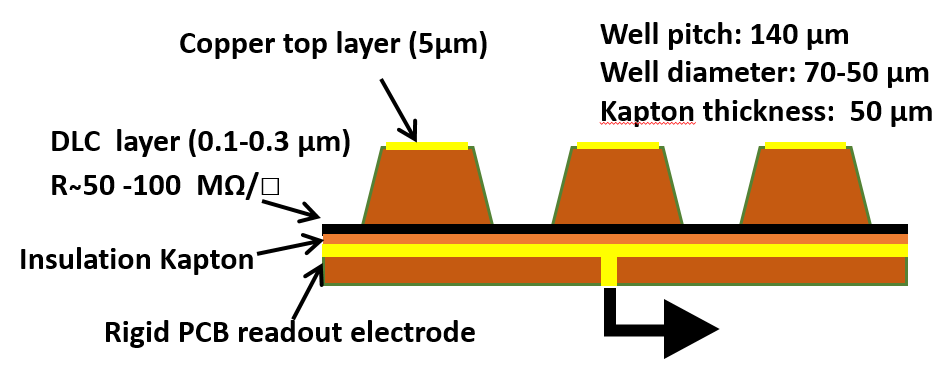


Fig.3 Structure of μRWELL

For a large area GEM detector, the homogeneity is an important issue. Further study including optimization of detector working condition, the design of 50\*100cm2 double GEM detector and development of μRWELL is on the progress.

# Readout Electronics

## Readout ASIC

To read out the GEM-based SDHCAL, we chose an ASIC called MICROROC (MICRO-mesh gaseous structure Read-Out Chip), developed at IN2P3 by OMEGA/LAL and LAPP microelectronics groups. The MICROROC is a 64-channel mixed-signal integrated circuit based on 350nm SiGe technology. Each channel of the MICROROC chip is made of a very low noise fixed gain charge preamplifier optimized for a detector capacitance of 80 pF and able to handle a dynamic range from 1fC to 500fC, two different adjustable shapers (A high gain shaper for small signal and a low gain shaper for large signal), three comparators for tri-threshold readout and a random access memory used as a digital buffer. Other blocks, like 10-bit DAC, configuration register, bandgap voltage reference, LVDS receiver are shared by 64 channels. The package of MICROROC is TQFP (Thin Quad-Flat Package), which means the thickness is 1.4mm.

## Readout System Structure



Figure 1. Readout system structure

The readout system structure is developed on SRS (the Scalable Readout System), proposed by the RD51 Collaboration. Similar with SRS, our readout system contains 3 parts, a front-end board (FEB), a detector interface board (DIF) and a data acquisition card (DAQ). Figure 1 shows the structure of this system. The FEB (also called ASU-Active Sensor Unit) carries all the front-end ASIC, together with the readout plane of GEM detector. The DIF in charge of ASIC control and data connection, plugs to the FEB using high density connector. The DAQ card is designed to serve several DIF boards. It distributes the clock, command and trigger to different DIF and gather the data from DIF boards.

The FEB is the combination of readout pads of GEM detector and readout ASICs. In order to reduce the “dead-area”, the FEB is designed to use blind and buried via technology. Considering the signal integrity and costs, 8/10-layer PCB is a suitable choice. The thickness of this kind of PCB can be as thin as 1.2mm. This means contain the 1.4mm MICROROC, the total thickness of FEB can be made within 3mm. Limited by PCB manufacturing technology, a well-performance FEB can be made as large as 50cm × 50cm. If a 1m2 prototype is made, it necessary to combine 4 FEB into one detector layer.

The DIF controls the FEB and gather the data of ASIC and can be tailored to the particular front-end ASIC with the particular application, giving the users the freedom of choice for the front-end circuit. Just changing the ASIC and DIF, the same design can be used both in ECAL and HCAL. Considering the data rate and costs, the master device of DIF can be some low-cost FPGA and the communication interface to the DAQ can be both USB type C or fiber-optical.

The DAQ card accesses the command from a server and controls several DIF. The design goal of the DAQ card is a universal controller for both ECAL and HCAL. Once a mature DAQ card is finished, it can be in common use even if we change the front-end ASIC.

Besides the readout ASIC and card, the clock synchronization design is an important block of the system. There are two kinds of clock source in the readout system, local clock and global clock (Usually, this kind of clock may be hundreds or thousands of meters from calorimeters). The local clock goes through the PLL and low-skew fan-out chip to the DIF, then the DIF distribute the clock to the FEB for local synchronization. If a global clock source is used, it is necessary to module there clock to optical signal and distribute the clock through fiber-optical. Another circuit call Clock and Data Recover (CDR) is needed for clock rebuild. The rebuild clock is global synchronized and can be used as local clock in one DAQ card.

## Phase I Design of the Readout system

A “phase I” design is completed to verify this kinds of readout structure and to test the performance of the MICROROC chip. In this design we separate the front-end ASIC from the detector readout plane for single test the ASIC. It contains the readout array of the GEM detector, front-end ASIC board and DIF board. The structure of the design is shown in figure 2. The GEM detector is 30cm × 30cm, and the readout pad detector is 1cm2. To ensure signal integrity and low cross talk the readout plane is designed 8-layer PCB with 4 ground plane to separate the signal and shield. The pads signal is connector to the front-end ASIC board via soft-board made from kapton. The front-end ASIC board composed by 4 ASIC controlled in daisy chain. The DIF board controls the front-end ASIC board and transmit data to the upper monitor. The main controller of DIF is Xilinx A7 100T series, a low cost FPGA. The data can be readout via USB2.0 or fiber-optical or Giga-bit Ethernet. We also reserve an ADC on DIF for monitoring the analog test signal. Figure 3 shows the picture of these three board.



Figure 2. The diagram of the phase I design

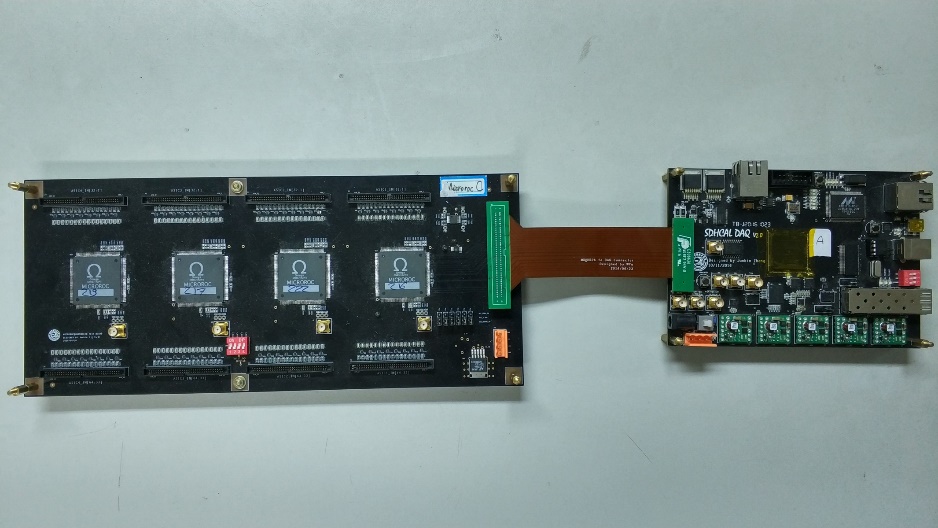
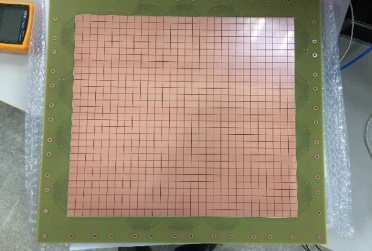


Figure 3. Picture the phase I design

We have done the test of this design. For all the ASIC channel, the maximum noise is 0.35fC, which means it beyonds the best performance of this ASIC distinguishing at least 2fC signal. The linear region of the high gain shaper is 0~140fC, and the low gain shaper is 0~500fC. All the result shows that this ASIC can work well with the detector and the readout scheme is effective.

## Next Stage Design

Since we have tested the MICROROC and the readout scheme, the next stage design is in progress. We design to mount the MICROROC chip on the back side of the readout plane, utilizing blind buried via technology. A 10-layer PCB with 3 ground plane and 2 power plane will ensure good signal integrity and low crosstalk. Considering the cost and performance, we choose 2 kinds of blind via (Layer1 - Layer2 and Layer9 - Layer10) and 1 kinds of buried via (Layer2 - Layer9). This board is the “real” FEB in the system structure. The design diagram is shown in figure 4. Besides FEB, the design of the DIF board is going on the same time. The DIF can plug to FEB directly or through a soft-board made from kapton. After the DIF design, we will consider the design of DAQ board. We can share the same DAQ board with ECal readout system. The DIF is connected to DAQ through USB type C wire or fiber-optical. Besides the SRS readout structure, a new system name FELIX is under research, which can made the whole system trig less readout.



Figure 4. Design scheme of next stage FEB