|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **RTL** | **Registers** | | | | | | | **Memory** | | | |
| **A** | **B** | **C** | **PC** | **IR** | **MAR** | **MBR** | **14 (K)** | **15 (L)** | **16 (M)** | **17 (N)** |
| Initial | - | ?? | ?? | ?? | 00 | 21 | ?? | ?? | 31 | F5 | 0E | 00 |
| LOAD M  (21) | MAR ← M  MBR ← M[MAR]  A ← MBR  PC ← PC + 2  IR ← M[PC] | **0E** | ?? | ?? | **02** | **10** | **16** | **0E** | 31 | F5 | 0E | 00 |
| MOV C, A  (10) | C ← A  PC ← PC + 2  IR ← M[PC] | 0E | ?? | 0E | **04** | **21** | 16 | 0E | 31 | F5 | 0E | 00 |
| LOAD L  (21) | MAR ← L  MBR ← M[MAR]  A ← MBR  PC ← PC + 2  IR ← M[PC] | **F5** | ?? | 0E | **06** | **10** | **15** | **F5** | 31 | F5 | 0E | 00 |
| MOV B, A  (10) | B ← A  PC ← PC + 2  IR ← M[PC] | F5 | **F5** | 0E | **08** | **21** | 15 | F5 | 31 | F5 | 0E | 00 |
| LOAD K  (21) | MAR ← K  MBR ← M[MAR]  A ← MBR  PC ← PC + 2  IR ← M[PC] | **31** | F5 | 0E | **0A** | **40** | **14** | **31** | 31 | F5 | 0E | 00 |
| ADD A, B  (40) | A ← A + B  PC ← PC + 2  IR ← M[PC] | **26** | F5 | 0E | **0C** | **50** | 14 | 31 | 31 | F5 | 0E | 00 |
| SUB A, C  (50) | A ← A - C  PC ← PC + 2  IR ← M[PC] | **18** | F5 | 0E | **0E** | **31** | 14 | 31 | 31 | F5 | 0E | 00 |
| STORE N  (31) | MAR ← N  MBR ← A  M[MAR] ← MBR  PC ← PC + 2  IR ← M[PC] | 18 | F5 | 0E | **10** | **??** | **17** | **18** | 31 | F5 | 0E | **18** |

For each instruction in the program, above, fill out the entire row of register and memory values after that instruction executes. Highlight in **bold** and/or red any values that have changed because of this current instruction.