EEE-2103: Electronic Devices and Circuits

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BJT Switching

Diode-connected BJT:

$I_E = I_C + I_B$

Total voltage drop across BJT → V_{BE} = 0.7 V

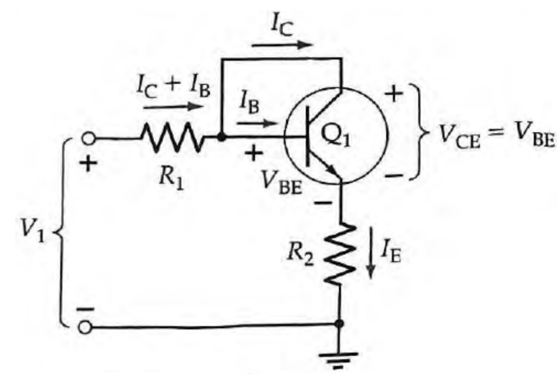
Charge carriers flow across forward-biased *BE* junction.

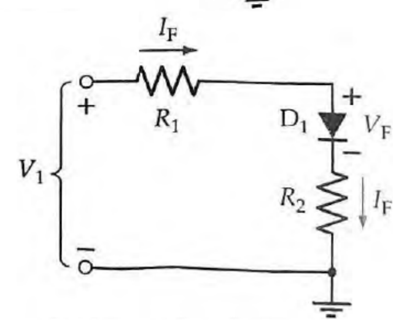
External *CB* voltage V_{CB} = 0 V

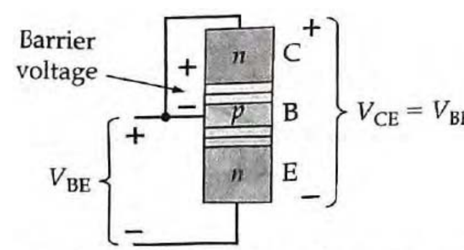
Barrier voltage at unbiased *BC* junction →

+ve on *n* side and –ve on *p* side.

pulls minority charge carriers from base into collector.







BJT Switching

BJT saturation:

Switching circuit →

input = pulse waveform to base

$V_i = 0$ →

$I_B = 0, I_C = 0, V_{CE} = V_{CC} - I_C R_2 = V_{CC}$

$V_i = +\text{ve}$ →

I_B is made large so that $I_C R_2 \approx V_{CC}$

$V_{CE} \approx V_{CC} - I_C R_2 \approx 0$

CB junction = forward-biased = 0.7 V

carriers from emitter are repelled from CB junction

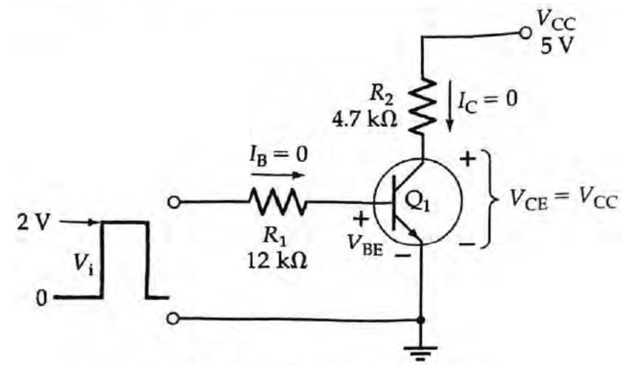
$I_C = 0$ →

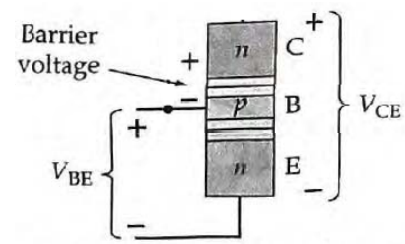
$V_{R2} = 0$

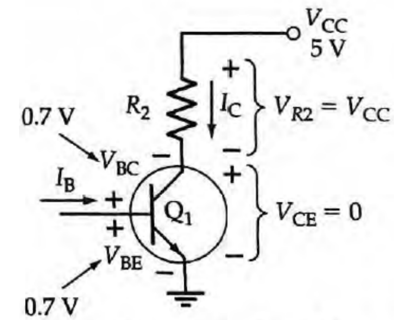
CE junction is not forward-biased

I_C flows but not large →

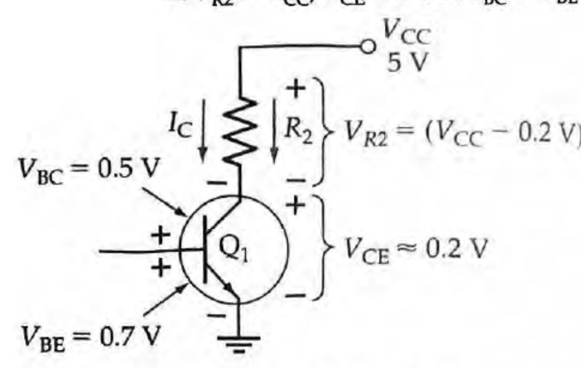
$V_{CE} \neq 0$







If $V_{R2} = V_{CC}$, $V_{CE} = 0$ and $V_{BC} = V_{BE}$



When Q_1 is saturated $V_{CE} \approx 0.2$ V

BJT Switching

BJT saturation:

$V_{CE} \neq 0 \rightarrow$

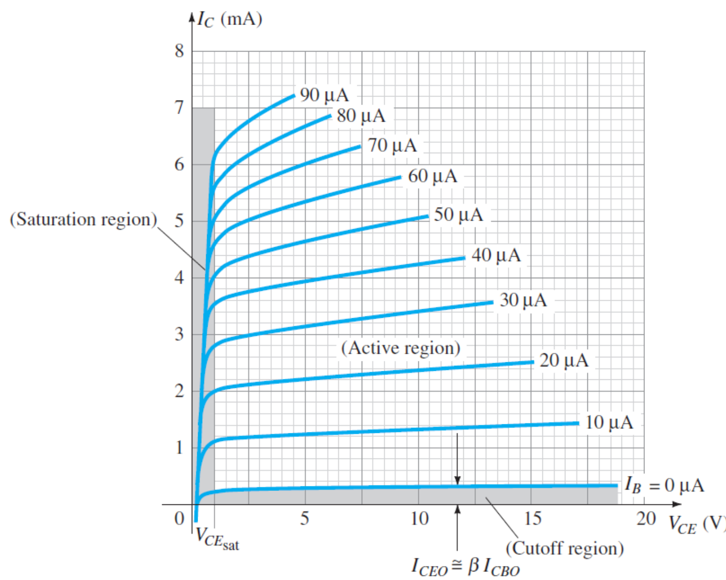
I_C flows when

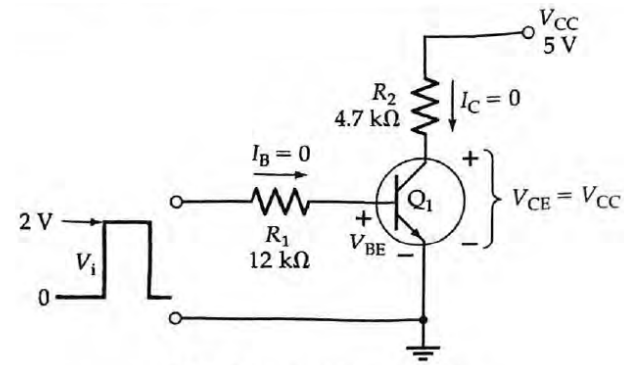
$V_{CB} = 0$

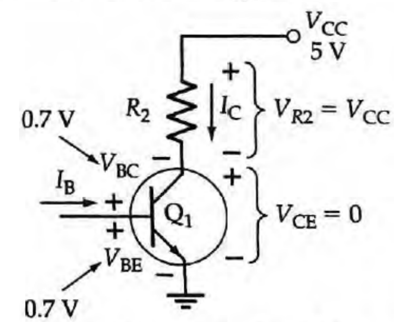
CB junction is partially forward-biased

$V_{BC} \approx 0.5$ V $\rightarrow$ $V_{CE} \approx 0.2$ V $= V_{CE(sat)}$

Small I_B controls larger I_C $\rightarrow$ switch BJT between OFF and ON.







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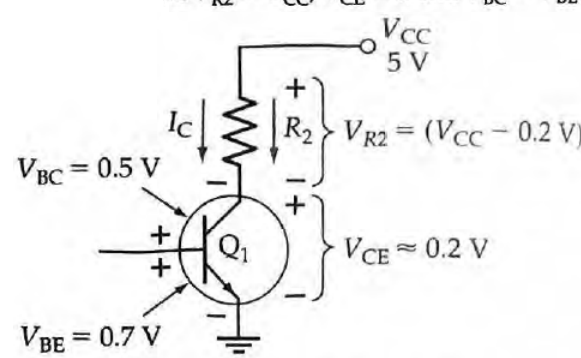


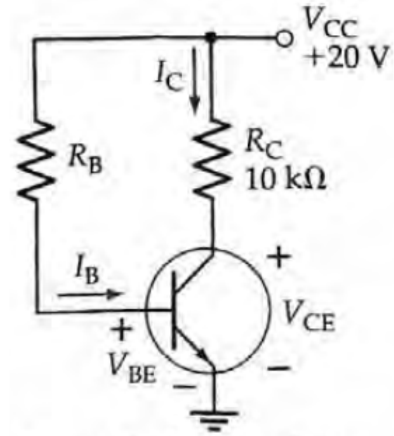
When Q_1 is saturated $V_{CE} \approx 0.2$ V

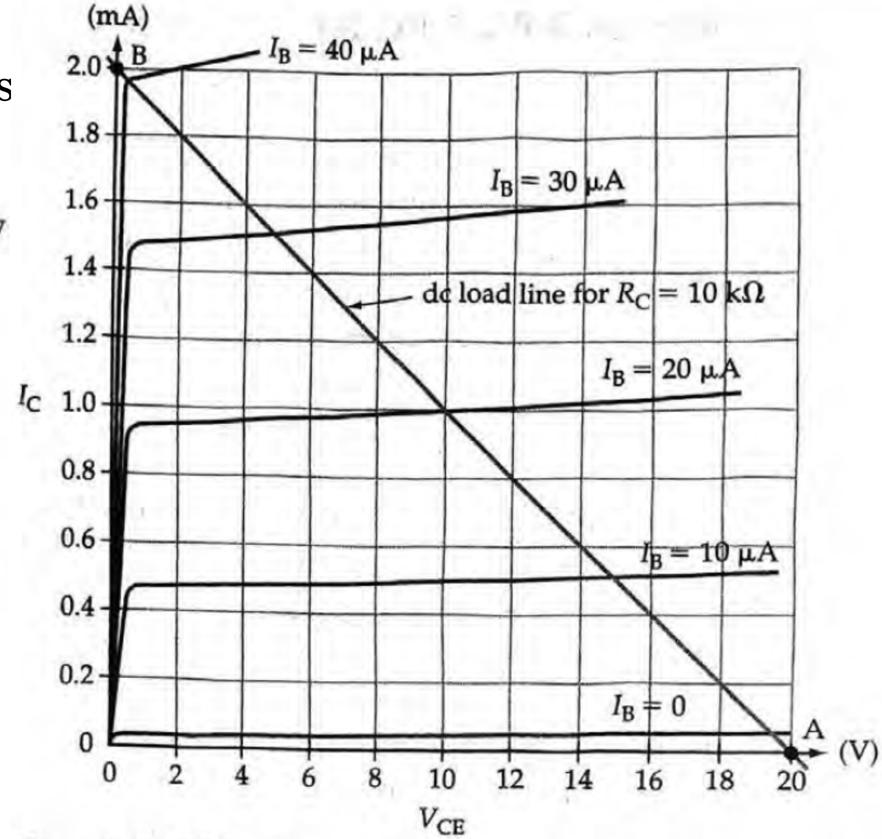
DC Load Line and Bias Point

DC load line:
Straight line drawn on transistor output characteristics
Shows all corresponding levels of I_C and V_{CE} for ckt.

$V_{BE} = 0 \rightarrow I_C = 0$
$V_{CE} = V_{CC} - I_C R_C$
$= 20 - (0 \times 10 \times 10^3) = 20$ V
Point $A = (20, 0)$

Assume $I_C = 2$ mA $\rightarrow$
$V_{CE} = 20 - (2 \times 10^{-3} \times 10 \times 10^3) = 0$ V
Point $B = (0, 2)$





DC Load Line and Bias Point

DC load line:

$I_C = 0 \rightarrow$

$V_{CE} = V_{CC} - I_C R_C$

$\quad = 20 - (0 \times 10 \times 10^3) = 20\text{ V}$

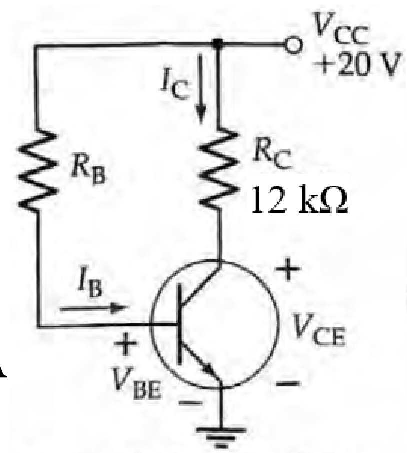
Point A = (20, 0)

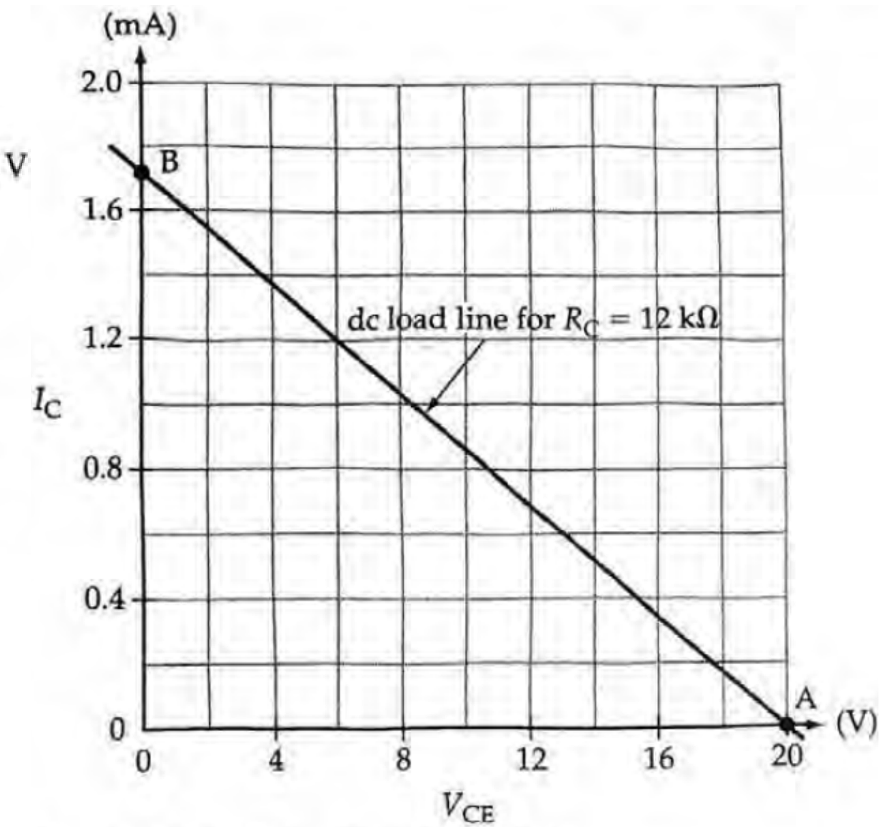
$V_{CE} = 0\text{ V} \rightarrow$

$0 = V_{CC} - I_C R_C$

$I_C = V_{CC}/R_C = 20/10 \times 10^3 = 1.7\text{ mA}$

Point B = (0, 1.7)

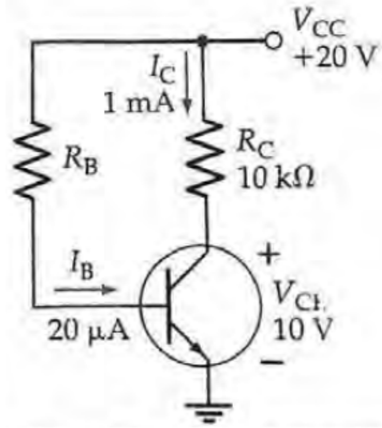


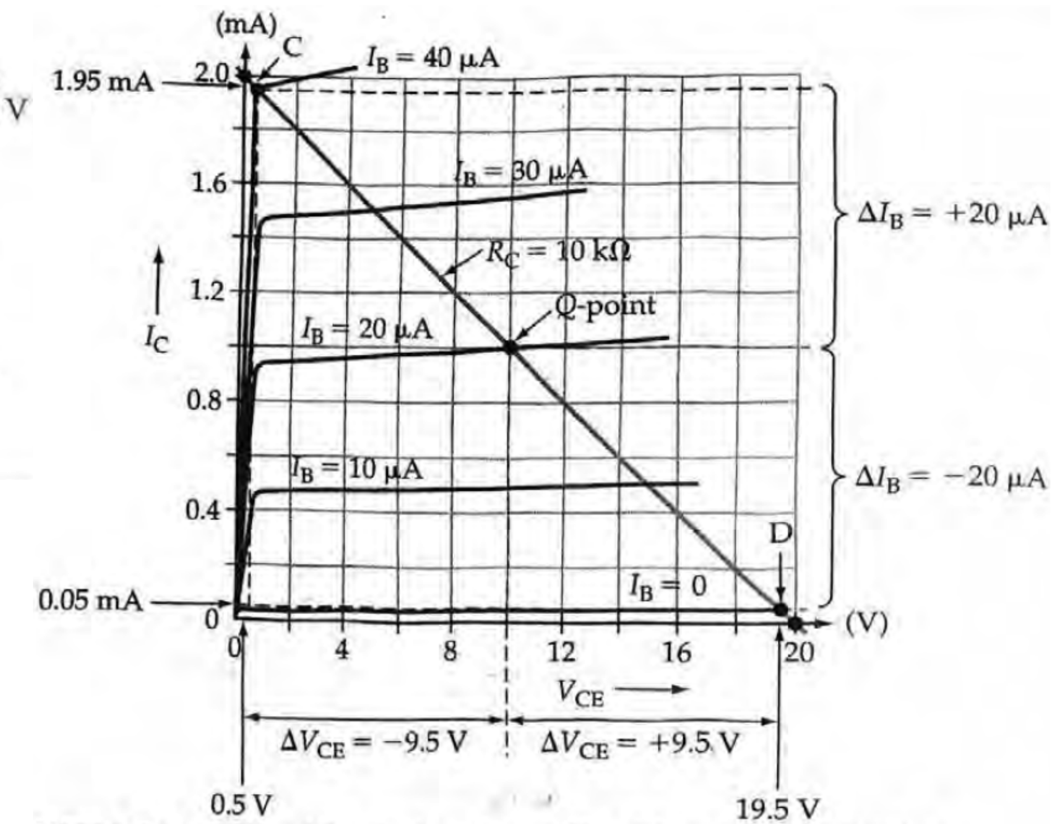


DC Load Line and Bias Point

DC bias point (Q-point):
dc bias point = quiescent point = Q-point = dc operating point =
Identifies I_C and V_{CE} when I_B = 0

Bias conditions →
Identified by Q-point
I_B = 20 μA
I_C = 1 mA
V_{CE} = 10 V





I_B = 40 μA →

I_C = 1.95 mA, V_{CE} = 0.5 V
ΔV_{CE} = 10 – 0.5 = 9.5 V

I_B = 0 μA →

I_C = 0.05 mA, V_{CE} = 19.5 V
ΔV_{CE} = 19.5 – 10 = 9.5 V

ΔI_B = ±20 μA → ΔV_{CE} = ±9.5 V

ΔI_B = ±10 μA → ΔI_C = ±0.5 mA, ΔV_{CE} = ±5 V

DC Load Line and Bias Point

DC bias point (Q-point):

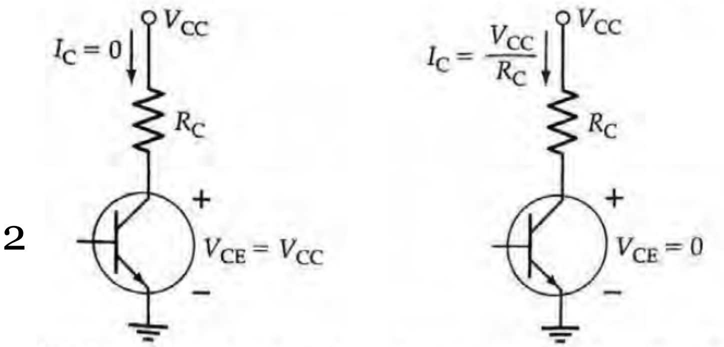
Maximum possible ΔV_{CE} → $\Delta I_C = 0 \sim V_{CC}/R_C$

$\Delta V_{CE} = V_{CC} \sim 0$

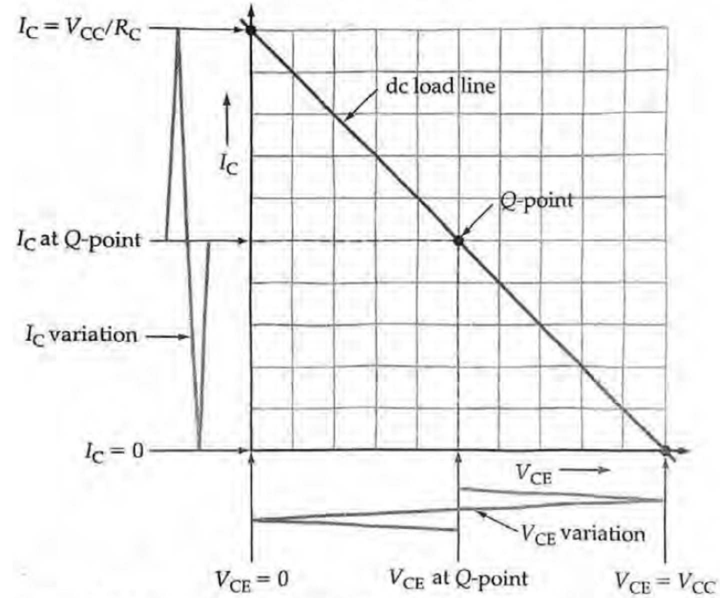
Q-point at center of load line → Max possible $\Delta V_{CE} = \pm V_{CC}/2$

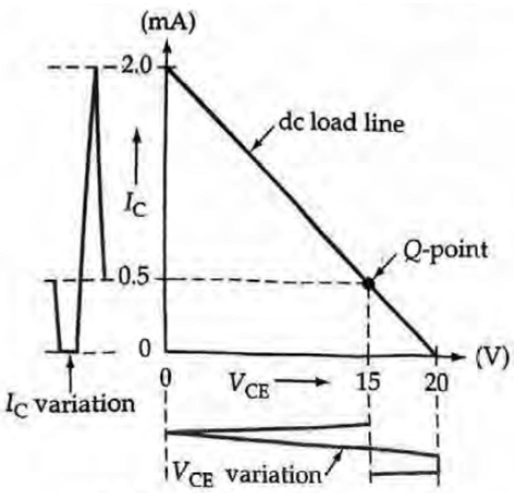
When used as amplifier →

output voltage swing must be symmetrical

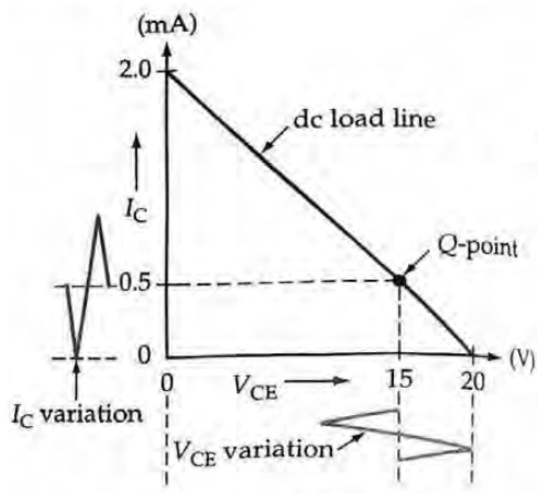


(a) $V_{CE} \approx V_{CC}$ when $I_C = 0$ (b) $V_{CE} \approx 0$ when $I_C = V_{CC}/R_C$





(a) Assymmetrical V_{CE} swing



(b) Symmetrical V_{CE} swing