EEE-2103: Electronic Devices and Circuits

Dept. of Computer Science and Engineering
University of Dhaka

Prof. Sazzad M.S. Imran, PhD
Dept. of Electrical and Electronic Engineering
sazzadmsi.webnode.com

DC Load Line and Bias Point

Promble-21:

The transistor circuit in Fig. 21(a) has the collector characteristics shown in Fig. 21(b). Determine the circuit *Q*-point and estimate the maximum symmetrical output voltage swing. Note that V_{CC} = 18 V, R_C = 2.2 kΩ, and I_B = 40 μA.

$I_C = 0 \rightarrow$

$V_{CE} = V_{CC} - I_C R_C = V_{CC} - 0 = 18$ V

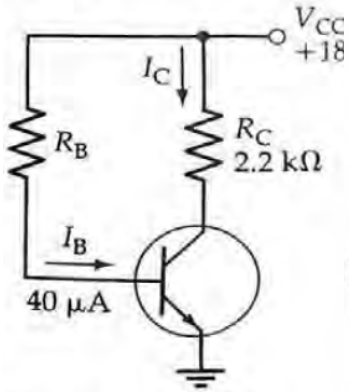
Point A = (18, 0)

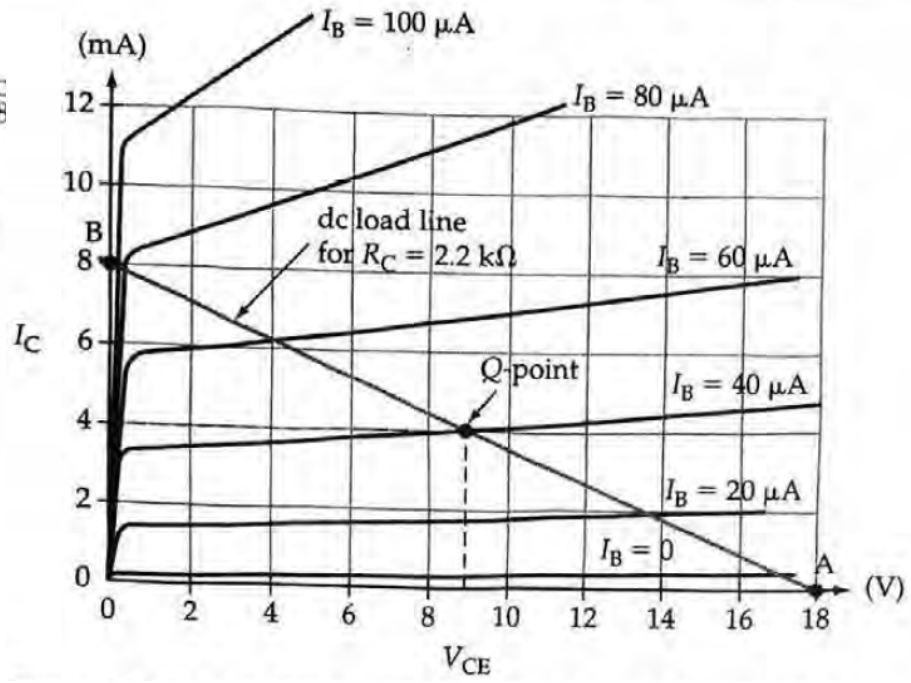
$V_{CE} = 0$ V →

$0 = V_{CC} - I_C R_C$

$I_C = V_{CC}/R_C = 18/2.2\times10^3 \approx 8.2$ mA

Point B = (0, 8.2)





Q-point is at intersection of load line and I_B = 40 μA

DC bias conditions are →

$I_C \approx 4.1$ mA and $V_{CE} \approx 9$V

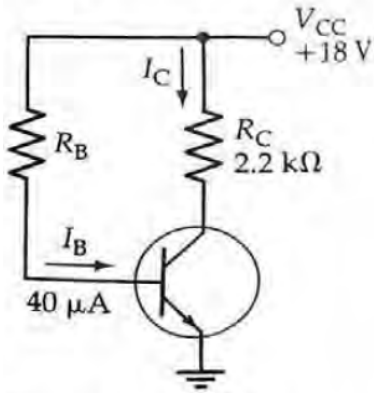
Max symmetrical output voltage swing, $\Delta V_{CE} \approx \pm 9$ V

DC Load Line and Bias Point

Effect of R_E →

DC load = R_E

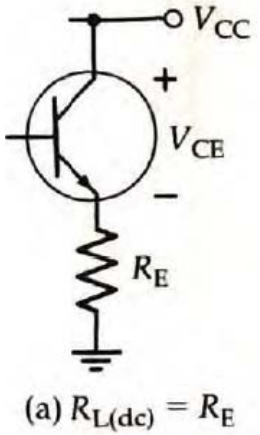
$V_{CE} = V_{CC} - I_E R_E$ $[I_C \approx I_E]$



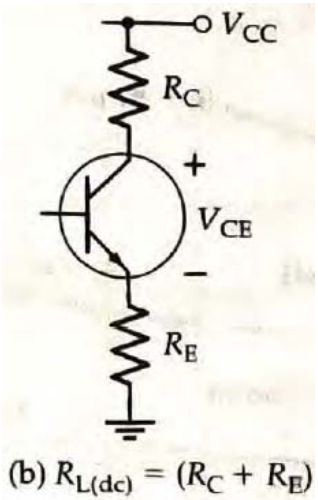
Effect of R_C and R_E →

DC load = $R_C + R_E$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$



(a) $R_{L(dc)} = R_E$



(b) $R_{L(dc)} = (R_C + R_E)$

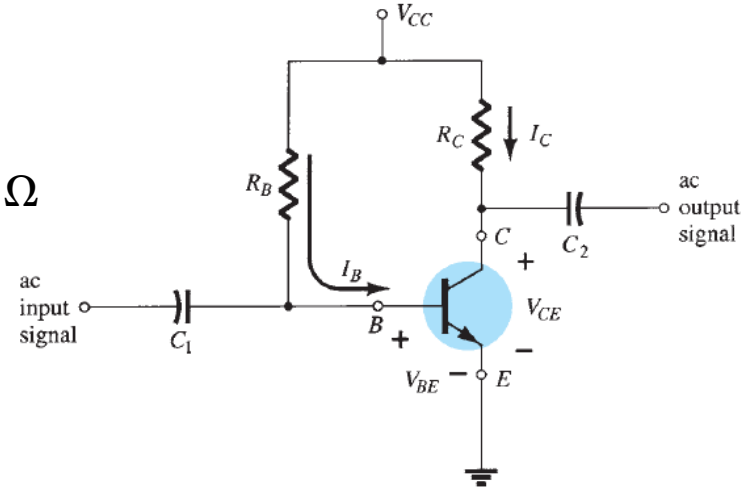
Fixed Bias Configuration

For dc analysis →

network can be isolated from ac levels

replacing capacitors with open-circuit

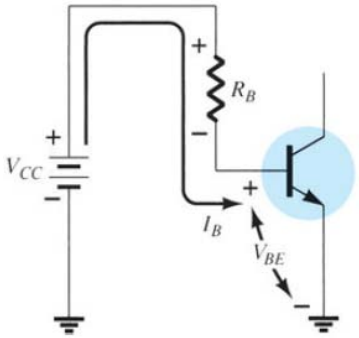
for dc, $f = 0$ Hz, and $X_C = 1/(2\pi fC) = 1/(2\pi(0)C) = \infty\ \Omega$



BE loop →

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

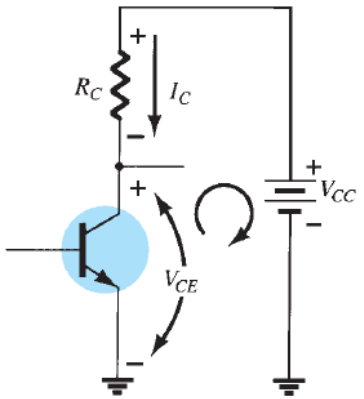


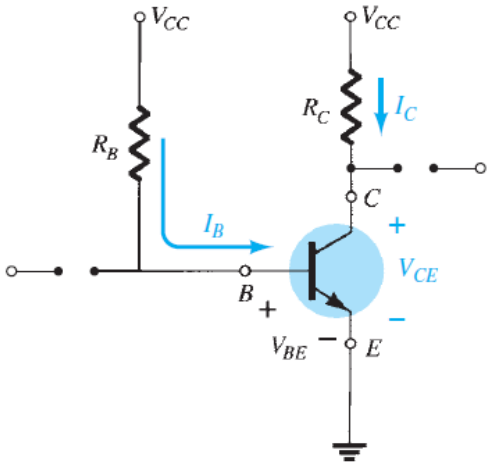
CE loop →

$$I_C = \beta I_B$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$



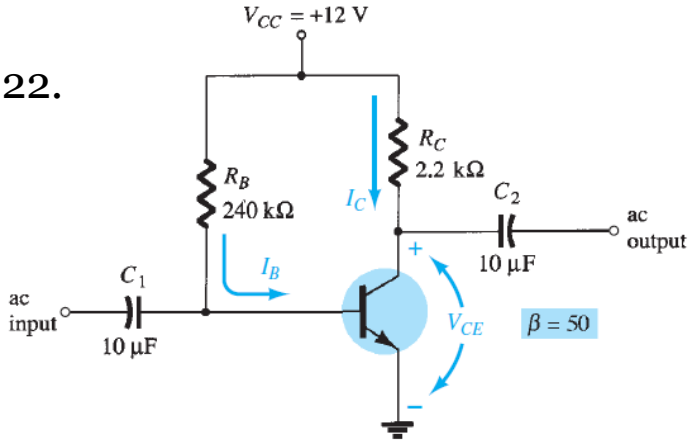


Fixed Bias Configuration

Problem-22:

Determine the following for the fixed-bias configuration of Fig. 22.

a) I_{BQ} and I_{CQ}. b) V_{CEQ}.
c) V_B and V_C. d) V_{BC}.



a) $I_{BQ} = \frac{V_{CC}-V_{BE}}{R_B} = \frac{12-0.7}{240\times10^3} = 47.08\ \mu A$

$I_{CQ} = \beta I_{BQ} = (50)(47.08\times10^{-6}) = 2.35\ mA$

b) $V_{CEQ} = V_{CC} - I_C R_C = 12\ V - (2.35\times10^{-3})(2.2\times10^3) = 6.83\ V$

c) $V_B = V_{BE} = 0.7\ V$
$V_C = V_{CE} = 6.83\ V$

d) $V_{BC} = V_B - V_C = 0.7 - 6.83 = -6.13\ V$

Fixed Bias Configuration

Transistor saturation:

saturation = levels have reached their maximum values.

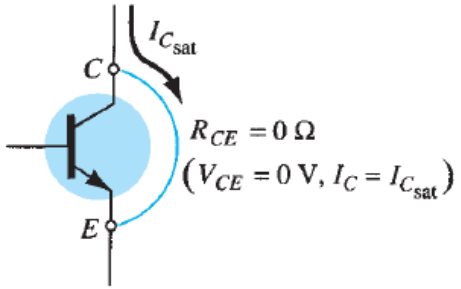
transistor saturation region =

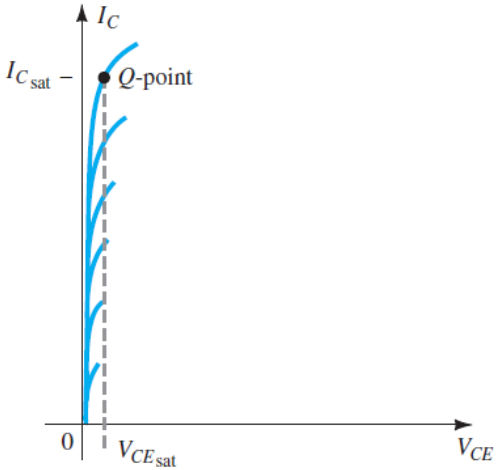
current is maximum for particular design.

characteristic curves join.

$V_{CE} <= V_{CEsat} \approx 0$ V

$R_{CE} = V_{CE}/I_C = 0/I_{Csat} = 0\ \Omega$





Saturation conditions are normally avoided →

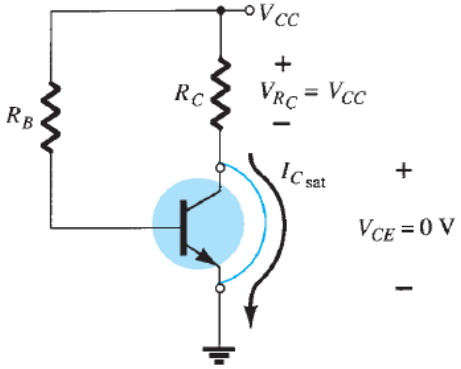
BC junction is no longer reverse-biased

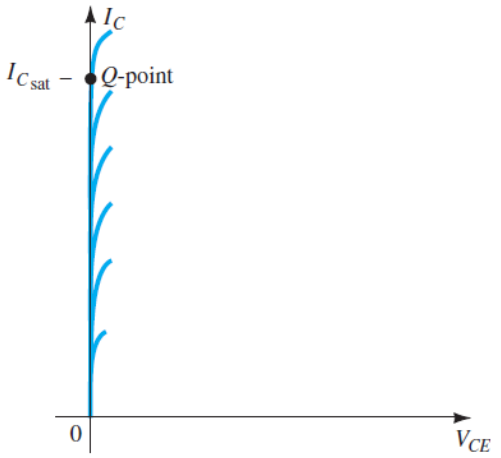
output amplified signal will be distorted.

Set $V_{CE} = 0$ V.

$I_{Csat} = V_{CC}/R_C$

Keep $I_C < I_{Csat}$ if we expect linear amplification.





Fixed Bias Configuration

Load line analysis:

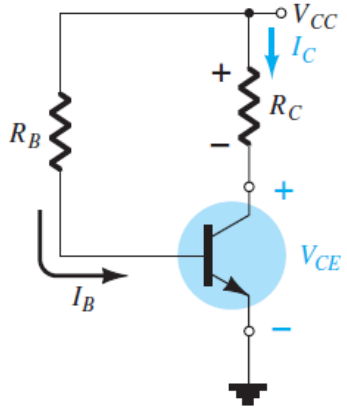
Output equation →

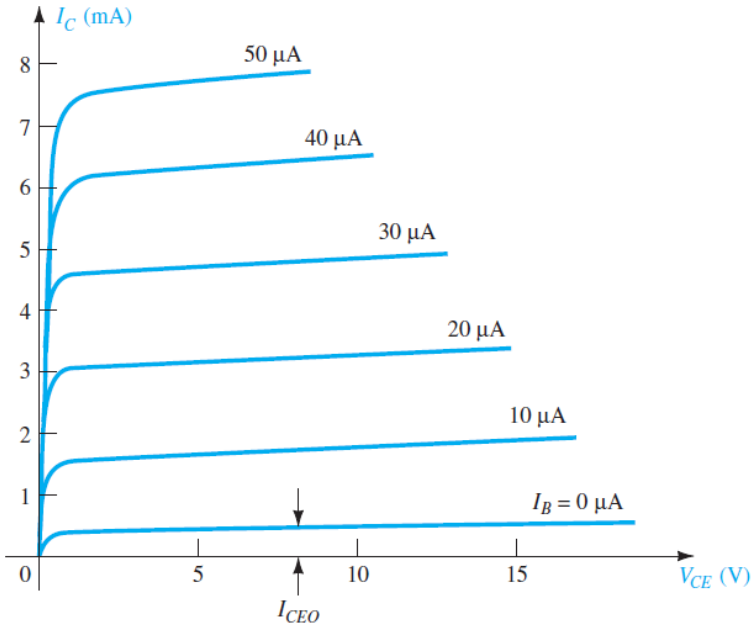
$$V_{CEQ} = V_{CC} - I_C R_C$$

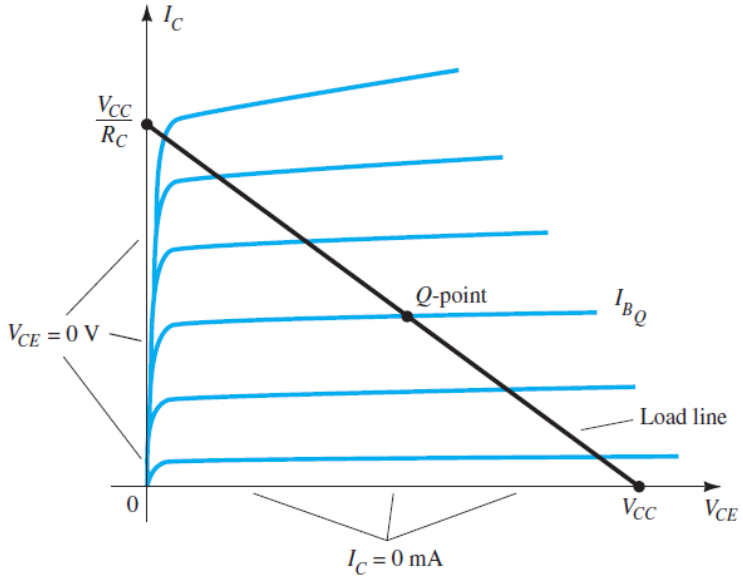
I_C = o mA → $V_{CE} = V_{CC} - (o)R_C = V_{CC}$

V_{CE} = o V → o = $V_{CC} - I_C R_C$

$$I_C = V_{CC}/R_C$$



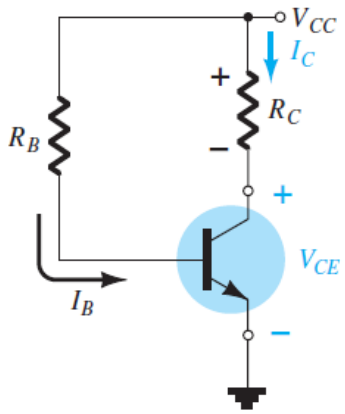


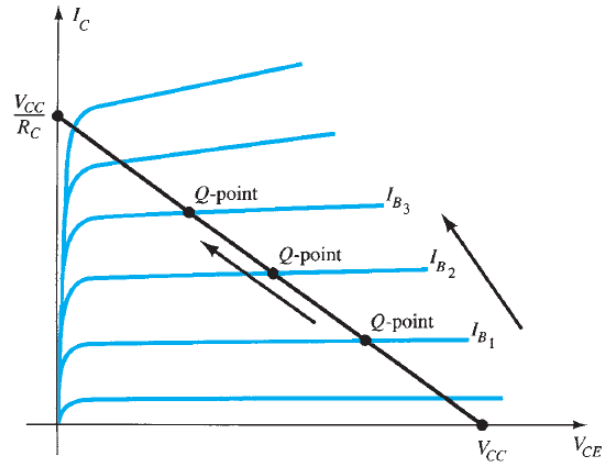


Fixed Bias Configuration

Load line analysis:

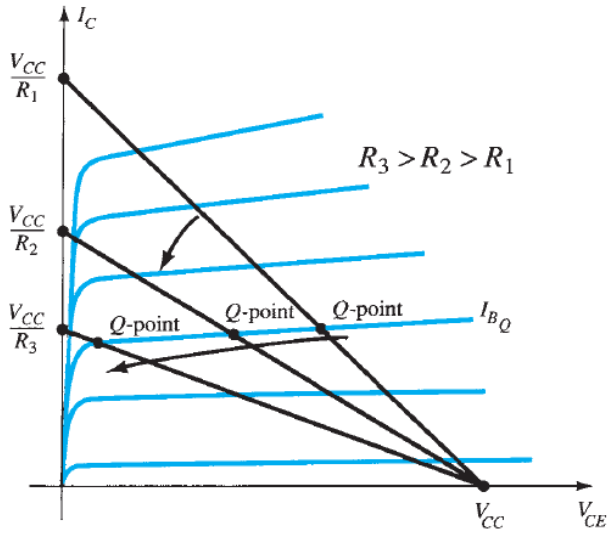
If I_B is changed by varying R_B →





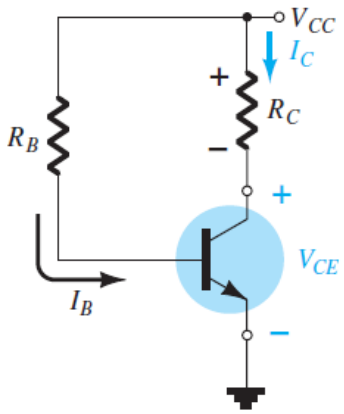
If V_{CC} is held fixed and R_C increased →

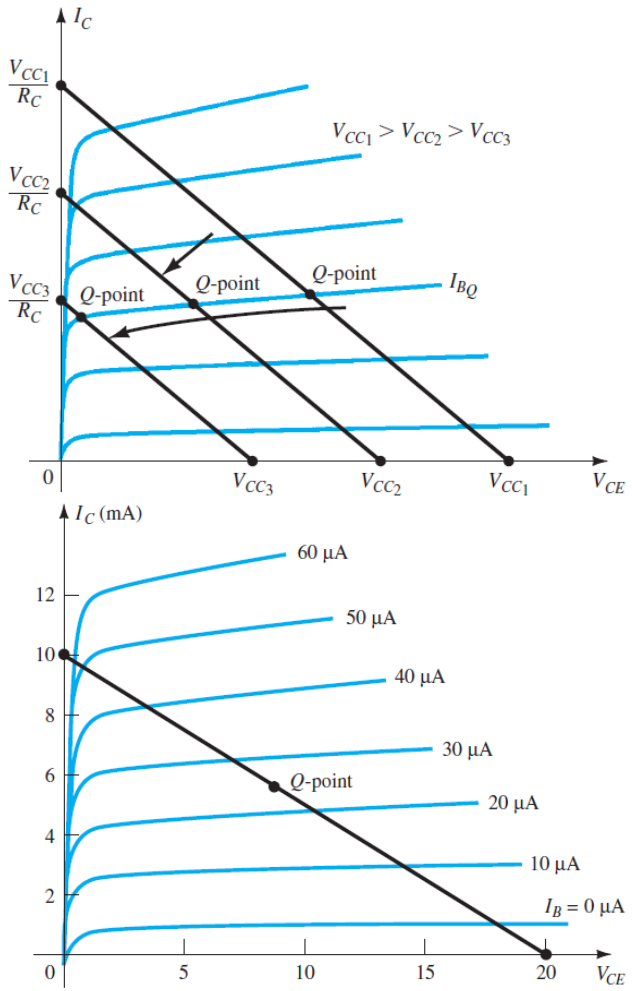
If I_B is held fixed →



Fixed Bias Configuration

Load line analysis:
If R_C is fixed and V_{CC} decreased →





Problem-23:
Given the load line of Fig. 23 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

$V_{CE} = V_{CC} = 20$ V at $I_C = 0$ mA

$I_C = V_{CC}/R_C$ at $V_{CE} = 0$ V
$R_C = V_{CC}/I_C = 20/10\times10^{-3} = 2$ kΩ

$I_B = (V_{CC} - V_{BE})/R_B$
$R_B = (V_{CC} - V_{BE})/I_B = (20 - 0.7)/25\times10^{-6} = 772$ kΩ