EEE-2103: Electronic Devices and Circuits

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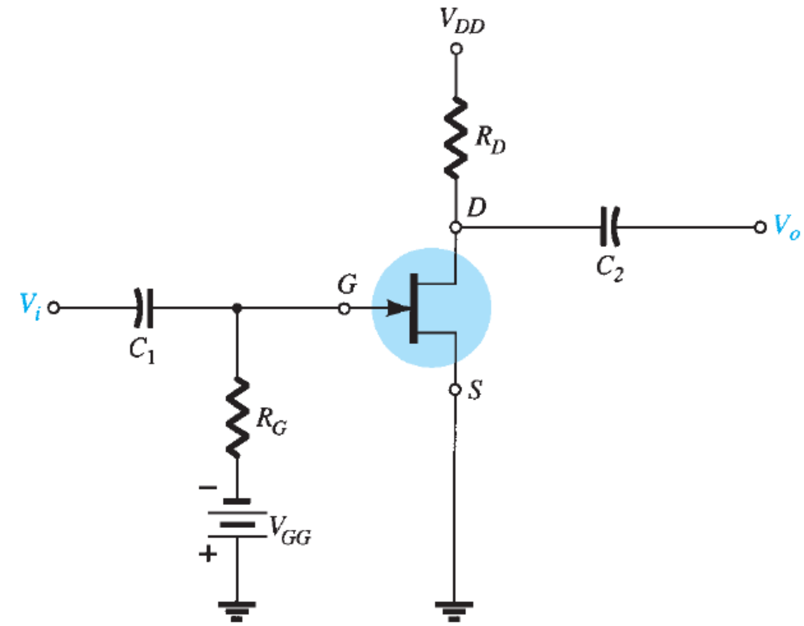
Fixed-Bias Configuration of JFET

Coupling capacitors → open circuits for dc analysis and short circuits for ac analysis.



R_G → to ensure that V_i appears at input for ac analysis.

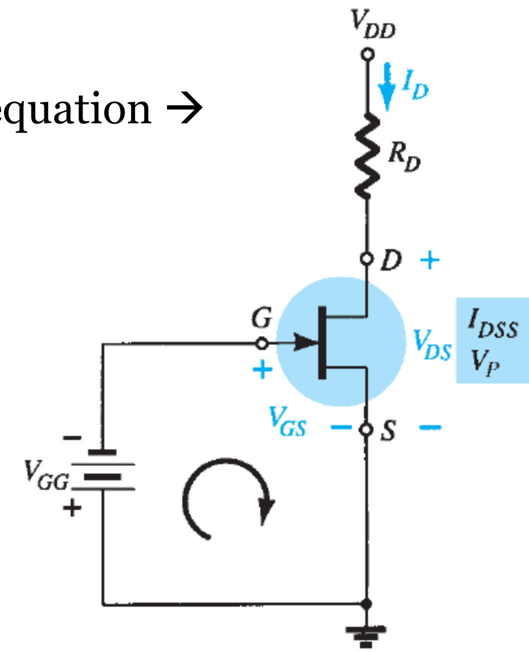
For dc analysis → $I_G \approx 0$ A

$V_{RG} = I_G R_G = (0)R_G = 0$ V

V_{GS} = -V_{GG}

I_D is controlled by Shockley's equation →

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Fixed-Bias Configuration of JFET

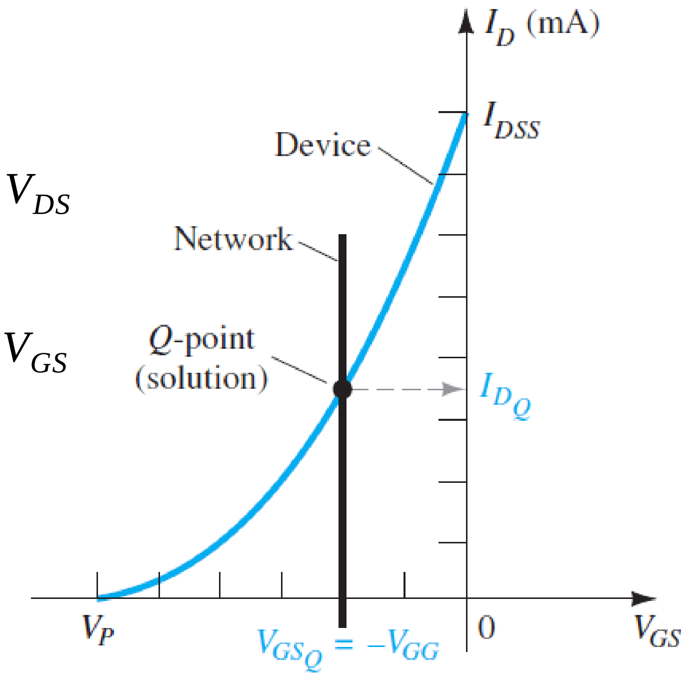
Quiescent or operating point → $V_{GS} = -V_{GG}$

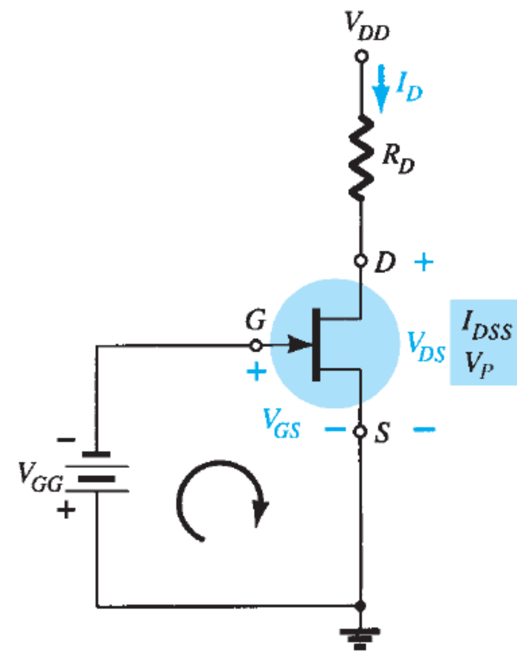
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$+V_{DS} + I_D R_D - V_{DD} = 0$
$V_{DS} = V_{DD} - I_D R_D$

$V_S = 0\text{ V}$
$V_{DS} = V_D - V_S$
$V_D = V_{DS} + V_S = V_{DS} + 0\text{ V} = V_{DS}$

$V_{GS} = V_G - V_S$
$V_G = V_{GS} + V_S = V_{GS} + 0\text{ V} = V_{GS}$





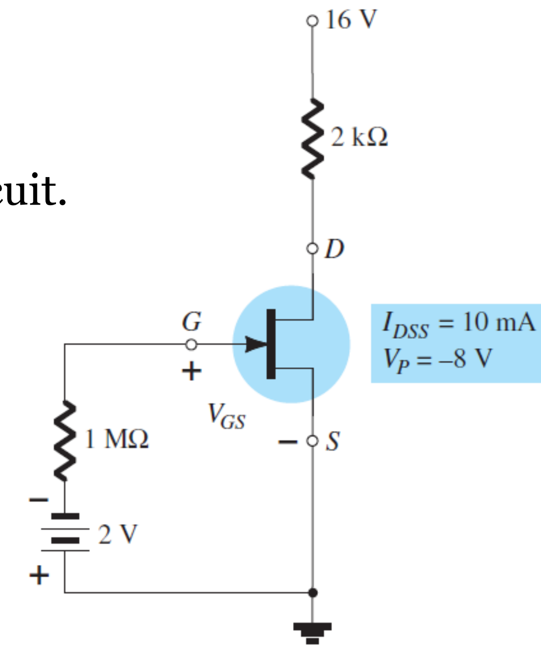
Fixed-Bias Configuration of JFET

Problem-38:

Determine the following for the network of Fig. 38.

a) V_{GSQ}. b) I_{DQ}. c) V_{DS}. d) V_D. e) V_G. f) V_S.

Draw the resulting Shockley curve and show the Q-point of biased circuit.



a) V_{GSQ} = -V_{GG} = -2 V

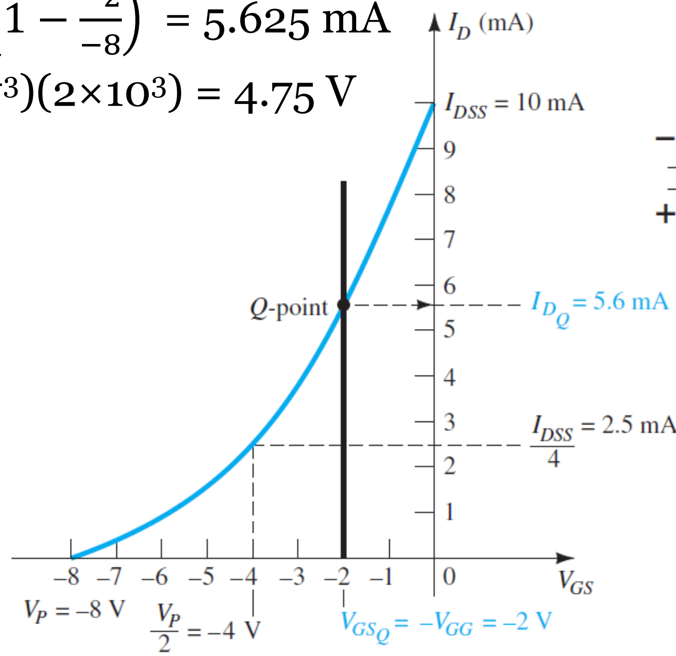
b) $I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{-2}{-8}\right)^2$ = 5.625 mA

c) $V_{DS} = V_{DD} - I_D R_D$ = 16 – (5.625×10^{-3})(2×10^{3}) = 4.75 V

d) $V_D = V_{DS}$ = 4.75 V

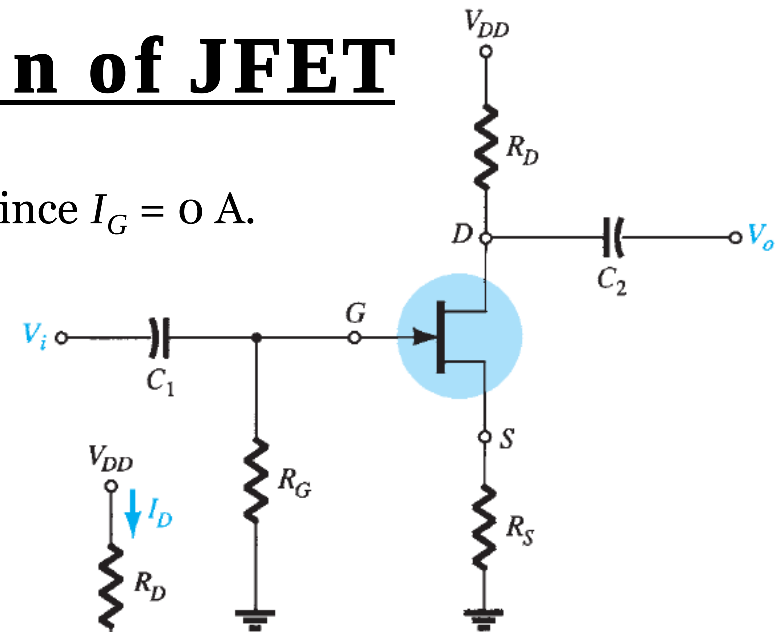
e) $V_G = V_{GS}$ = -2 V

f) V_S = 0 V



Self-Bias Configuration of JFET

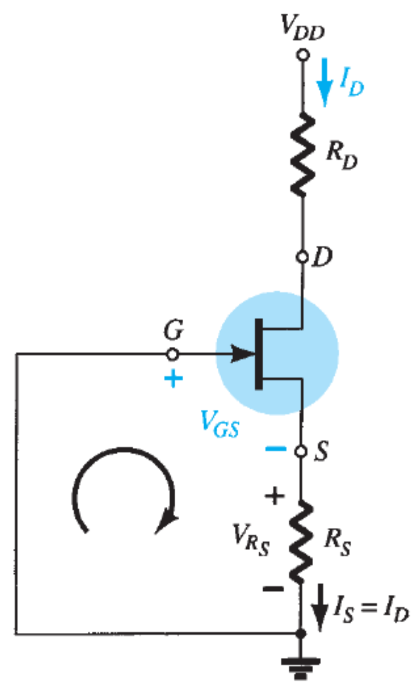
dc analysis → capacitors are replaced by open circuits
R_G is replaced by short-circuit equivalent since I_G = 0 A.



$I_S = I_D$
$V_{RS} = I_D R_S$

$-V_{GS} - V_{RS} = 0$
$V_{GS} = -V_{RS} = -I_D R_S$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$
$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

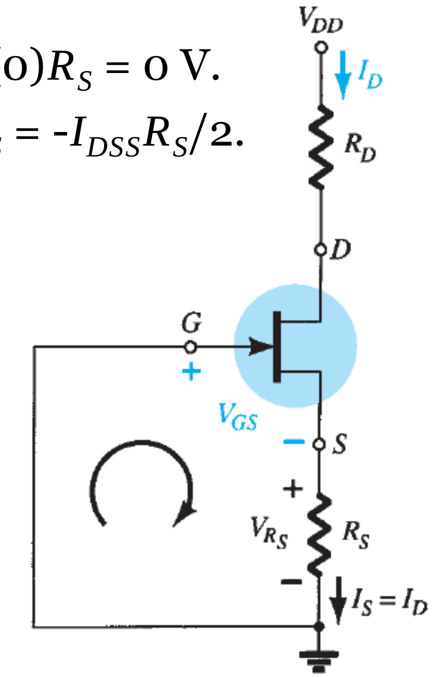


Self-Bias Configuration of JFET

Quiescent or operating point →

1^{st} point → I_D = 0 A, $V_{GS} = -I_D R_S = (0)R_S = 0$ V.

2^{nd} point → $I_D = I_{DSS}/2$, $V_{GS} = -I_D R_S = -I_{DSS} R_S/2$.



$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$

$V_{DS} = V_{DD} - V_{RS} - V_{RD} = V_{DD} - I_S R_S - I_D R_D$

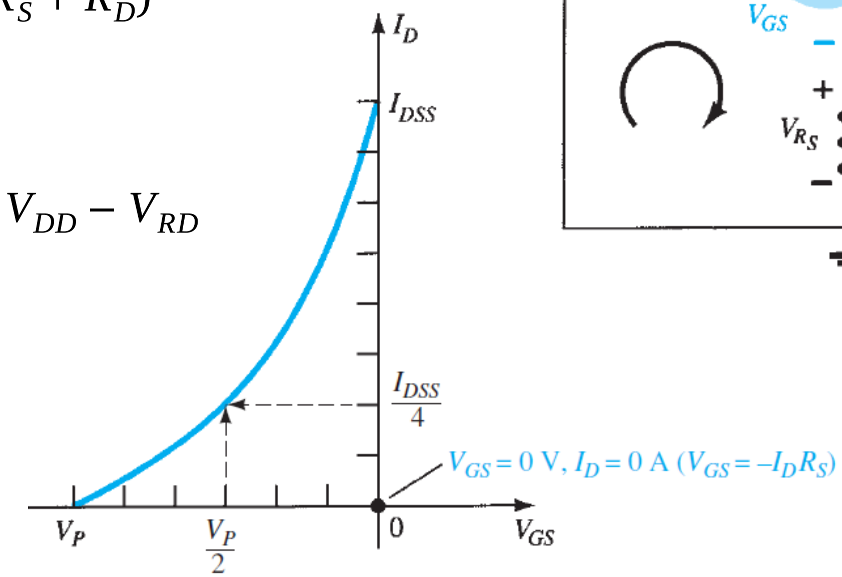
$I_D = I_S$

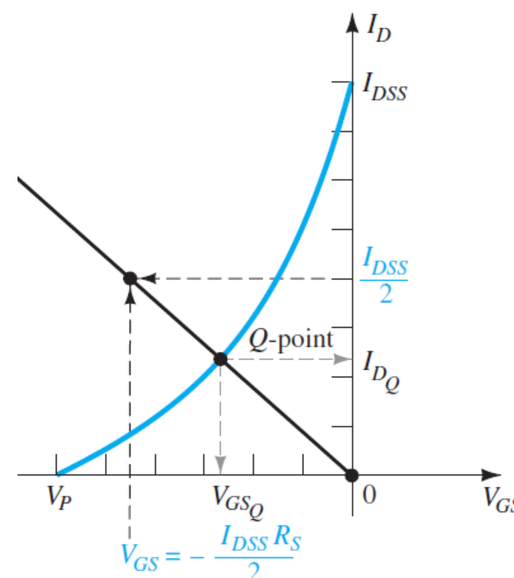
$V_{DS} = V_{DD} - I_D(R_S + R_D)$

$V_S = I_D R_S$

$V_G = 0$ V

$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$





Self-Bias Configuration of JFET

Problem-39:

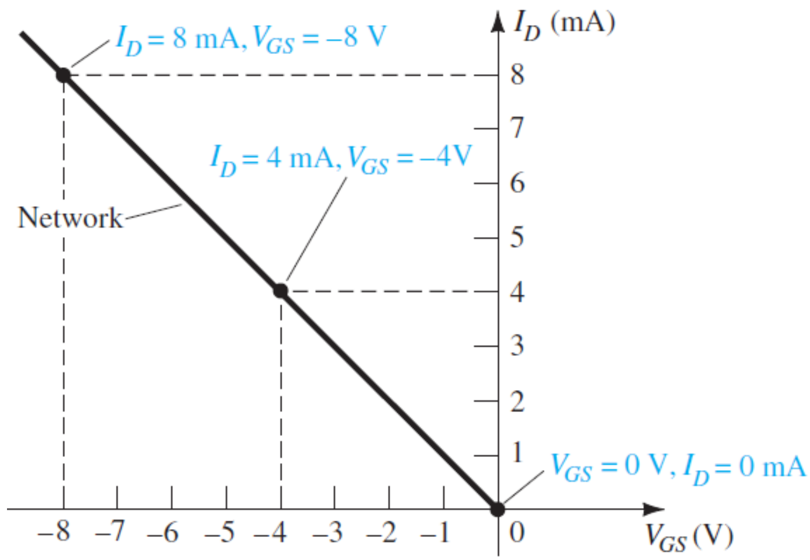
Determine the following for the network of Fig. 39.

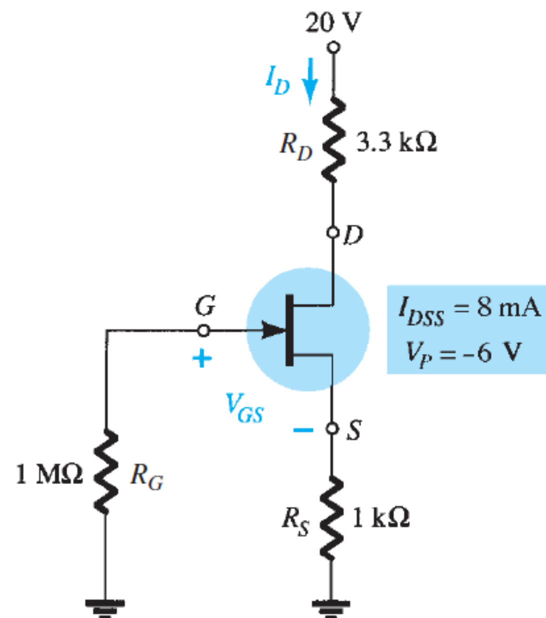
a) V_{GSQ}. b) I_{DQ}. c) V_{DS}. d) V_S. e) V_G. f) V_D.

a) $V_{GS} = -I_D R_S$

Choosing I_D = 4 mA, $V_{GS} = -(4\times10^{-3})(1\times10^{3}) = -4$ V

Choosing I_D = 8 mA, $V_{GS} = -(8\times10^{-3})(1\times10^{3}) = -8$ V

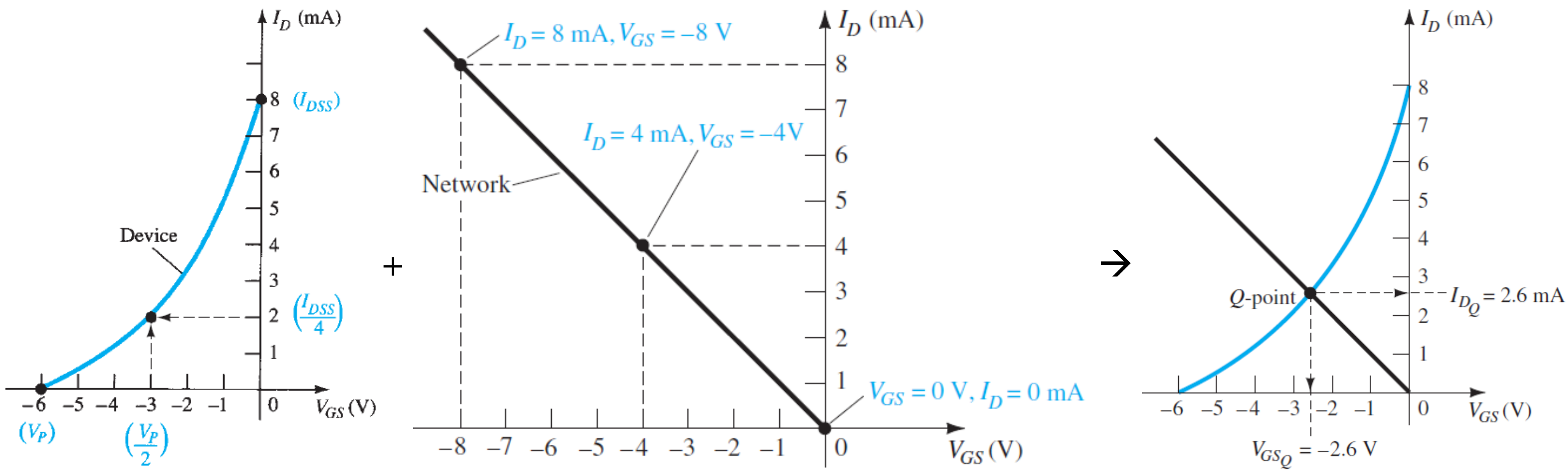




<u>Self-Bias Configuration of JFET</u>

<u>Problem-39:</u>

a) Choosing $V_{GS} = V_P/2 = -3$ V, $I_D = I_{DSS}/4 = 8/4 = 2$ mA



$V_{GSQ} = 2.6$ V

b) $I_{DQ} = 2.6$ mA

Self-Bias Configuration of JFET

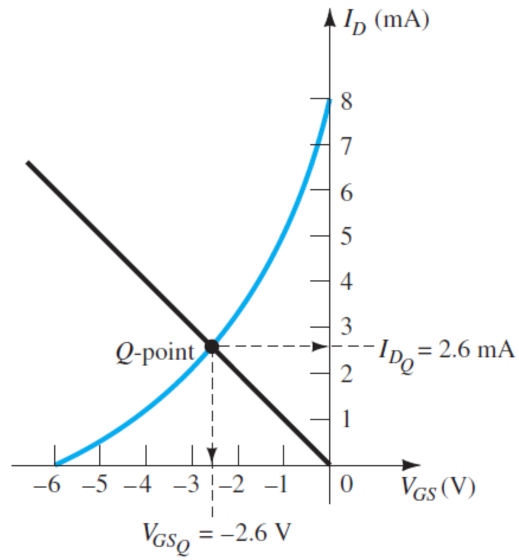
Problem-39:

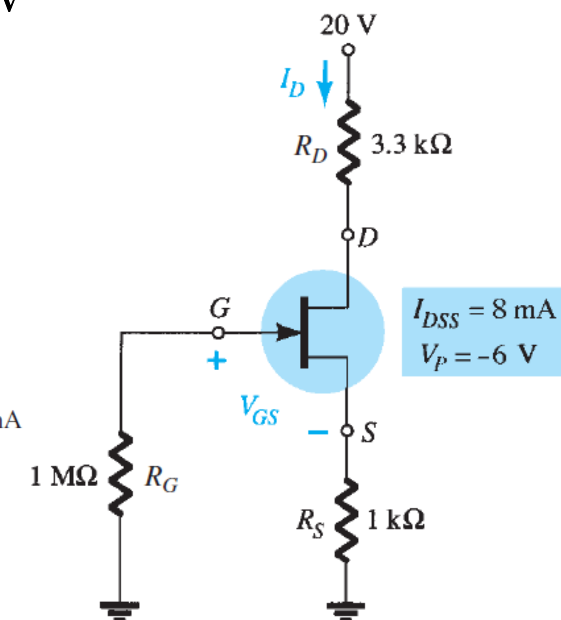
c) $V_{DS} = V_{DD} - I_D(R_S + R_D) = 20 - (2.6\times10^{-3})(1\times10^{3} + 3.3\times10^{3}) = 8.82$ V

d) $V_S = I_D R_S = (2.6\times10^{-3})(1\times10^{3}) = 2.6$ V

e) $V_G = 0$ V

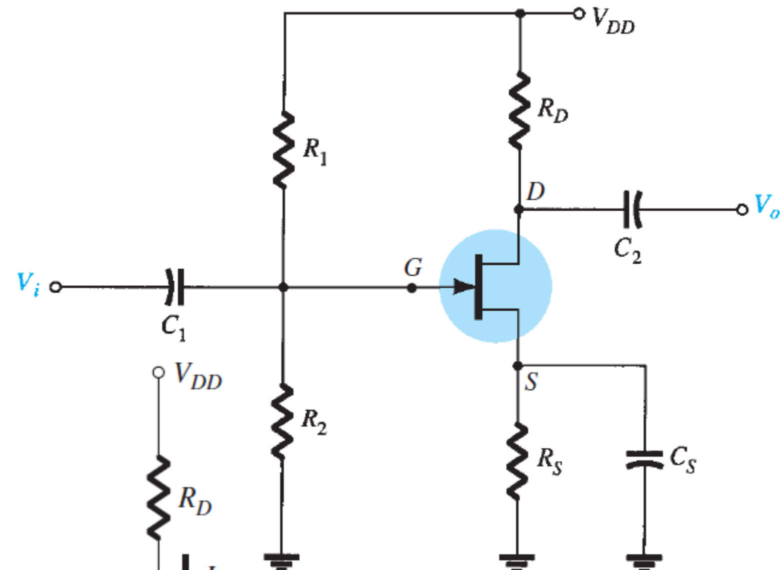
f) $V_D = V_{DS} + V_S = 8.82 + 2.6 = 11.42$ V





Voltage-Divider Biasing of JFET

Coupling capacitors → open circuits for dc analysis and short circuits for ac analysis.



$I_G = 0$ A, $I_{R1} = I_{R2}$, $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

Applying Kirchhoff's voltage law

$$V_G - V_{GS} - V_{RS} = 0$$
$$V_{GS} = V_G - V_{RS}$$

Substituting $V_{RS} = I_S R_S = I_D R_S$,

$$V_{GS} = V_G - I_D R_S$$

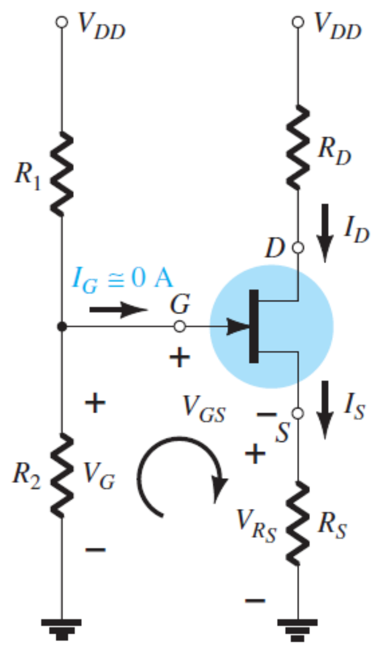
1st point → $I_D = 0$ mA

$V_{GS} = V_G - I_D R_S = V_G - (0)R_S = V_G$

2nd point → $V_{GS} = 0$ V

$V_{GS} = V_G - I_D R_S = 0$ V

$I_D = V_G / R_S$

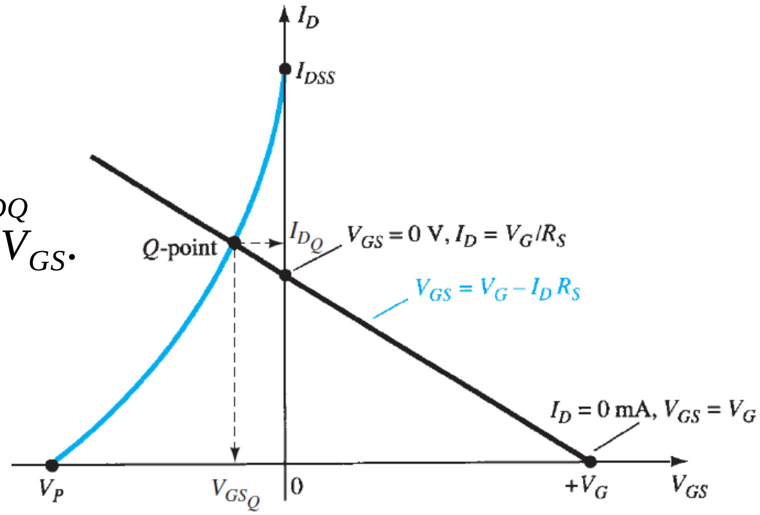


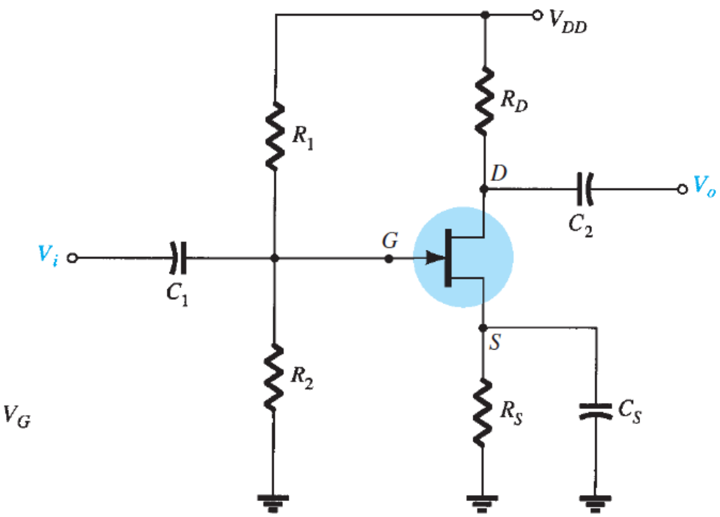
Voltage-Divider Biasing of JFET

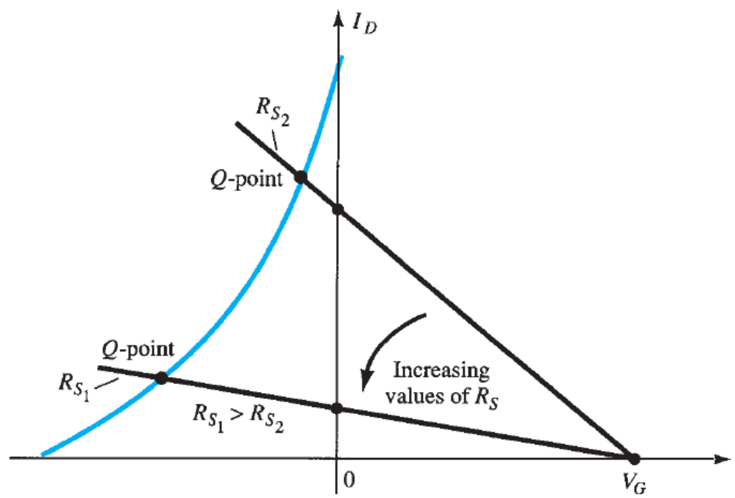
$I_D = 0\text{ mA}, V_{GS} = V_G$
$V_{GS} = 0\text{ V}, I_D = V_G/R_S$

R_S increases → lower I_{DQ}
decline V_{GS}.

$V_{DS} = V_{DD} - I_D(R_D + R_S)$
$V_D = V_{DD} - I_D R_D$
$V_S = I_D R_S$
$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$





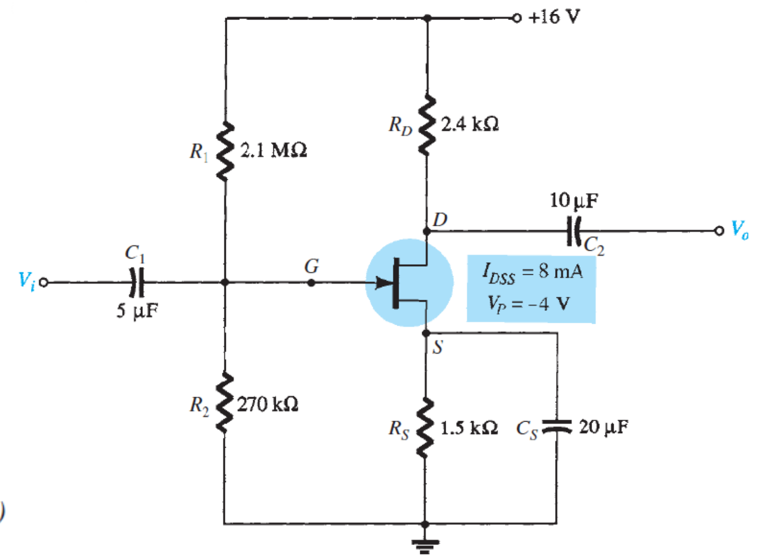


Voltage-Divider Biasing of JFET

Problem-40:

Determine the following for the network of Fig. 40.

a) I_{DQ} and V_{GSQ}.   b) V_D.   c) V_S.   d) V_{DS}.   e) V_{DG}.



a) For transfer characteristics,

$I_D = I_{DSS}/4 = 8/4 = 2$ mA,

$V_{GS} = V_P/2 = -4/2 = -2$ V.

$$V_G = \frac{R_2 V_{DD}}{R_1+R_2} = \frac{(270\times10^3)(16)}{2.1\times10^6+0.27\times10^3} = 1.82 \text{ V}$$

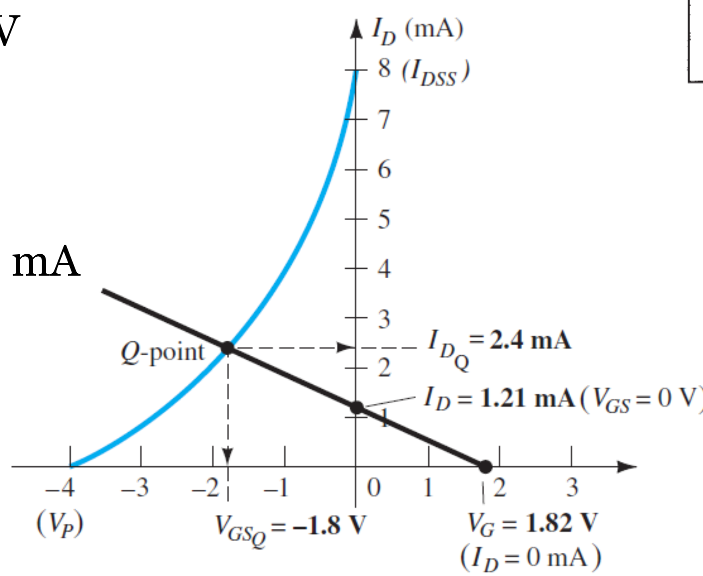
$V_{GS} = V_G - I_D R_S = 1.82 - I_D(1.5\times10^3)$

$I_D = 0$ mA, $V_{GS} = +1.82$ V

$V_{GS} = 0$ V, $I_D = 1.82/(1.5\times10^3) = 1.21$ mA

$I_{DQ} = 2.4$ mA

$V_{GSQ} = -1.8$ V



Voltage-Divider Biasing of JFET

Problem-40:

b) $V_D = V_{DD} - I_D R_D = 16 - (2.4\times10^{-3})(2.4\times10^{3}) = 10.24\text{ V}$

c) $V_S = I_D R_S = (2.4\times10^{-3})(1.5\times10^{3}) = 3.6\text{ V}$

d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16 - (2.4\times10^{-3})(2.4\times10^{3} + 1.5\times10^{3}) = 6.64\text{ V}$

e) $V_{DG} = V_D - V_G = 10.24 - 1.82 = 8.42\text{ V}$