EEE-2103: Electronic Devices and Circuits

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Voltage Divider Bias Configuration

Approximate analysis:

$R_i = (\beta + 1)R_E \approx \beta R_E$

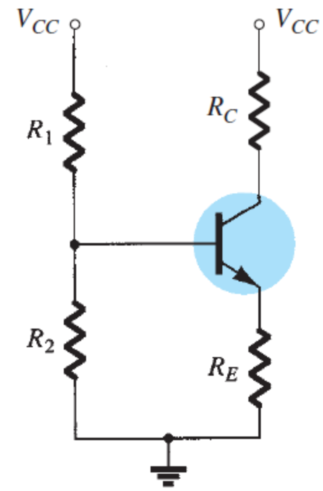
If $R_i >> R_2 \rightarrow I_B << I_2$

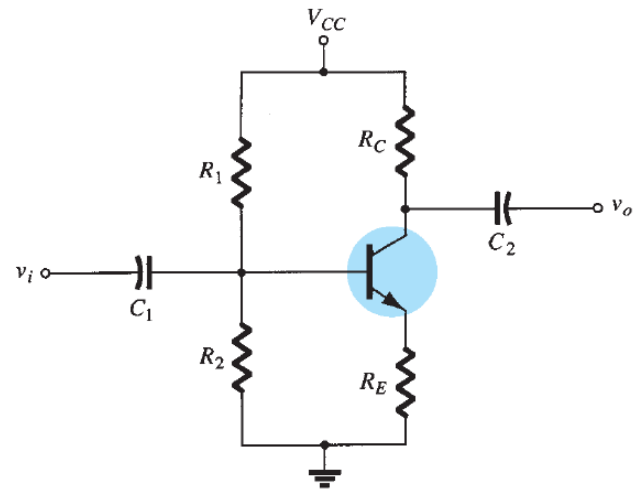
$I_2 \approx I_1$

$I_B \approx 0$ A compared to I_1 or I_2

$I_1 = I_2$

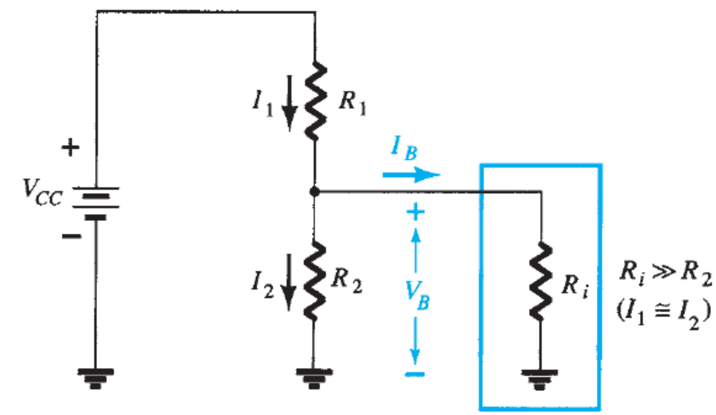
$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$





Approximate approach can be applied with high degree of accuracy if

$\beta R_E \geq 10 R_2$



$V_E = V_B - V_{BE}$

$I_E = V_E / R_E$

$I_{CQ} \approx I_E$

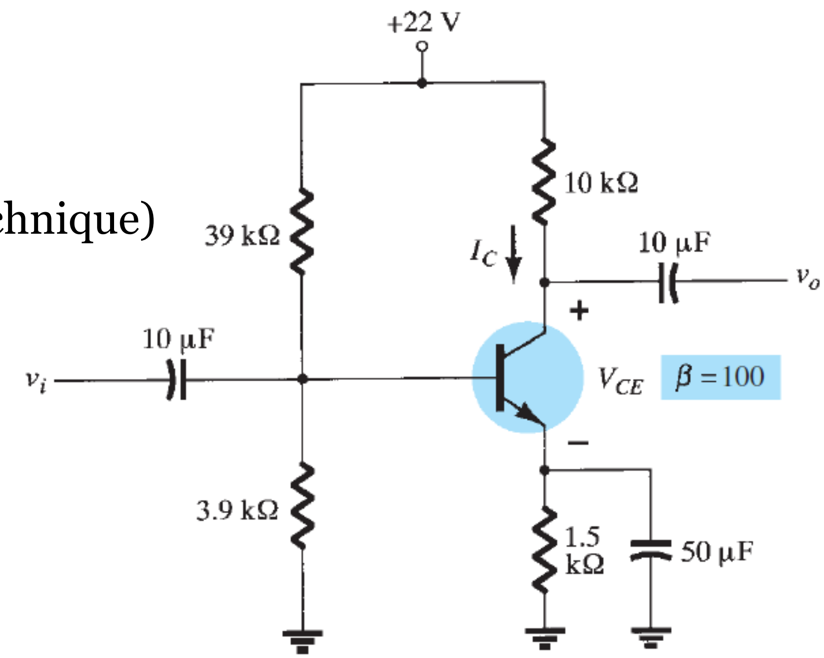
$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$

Voltage Divider Bias Configuration

Problem-27:

Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Fig. 27 using the approximate technique.



$\beta R_E \geq 10R_2$

$(100)(1.5\times10^3) \geq 10(3.9\times10^3)$

$150\ \text{k}\Omega \geq 39\ \text{k}\Omega$ (satisfied, so we can use approximate technique)

$V_B = \frac{R_2 V_{CC}}{R_1+R_2} = \frac{(3.9\times10^3)(22)}{39\times10^3+3.9\times10^3} = 2\ \text{V}$

$V_E = V_B - V_{BE} = 2 - 0.7 = 1.3\ \text{V}$

$I_{CQ} \approx I_E = V_E/R_E = 1.3/(1.5\times10^3) = 0.867\ \text{mA}$

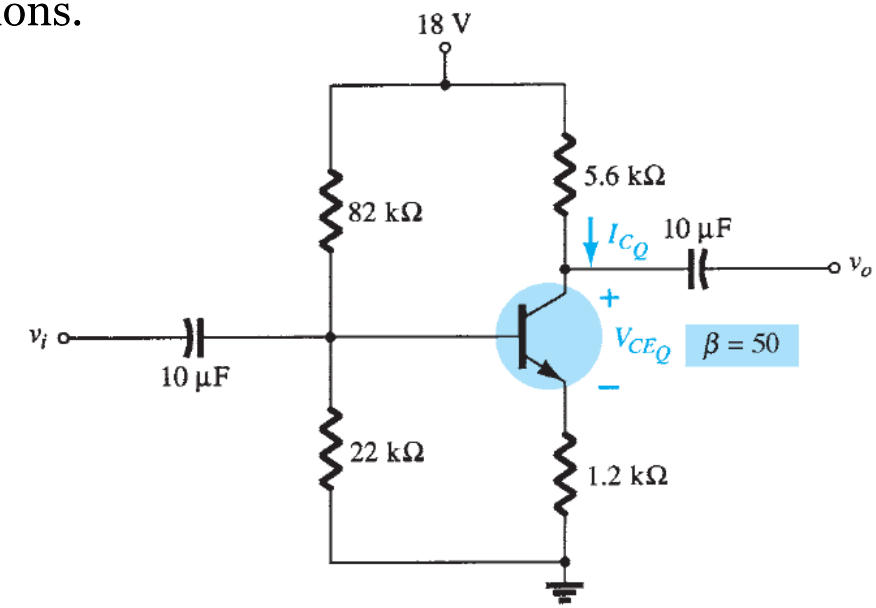
$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$

$= 22 - (0.867\times10^{-3})(10\times10^3 + 1.5\times10^3)$

$= 12.03\ \text{V}$

Voltage Divider Bias Configuration

Problem-28:
Determine the levels of I_{CQ} and V_{CEQ} for the voltage-divider configuration of Fig. 28 using the exact and approximate techniques and compare solutions.



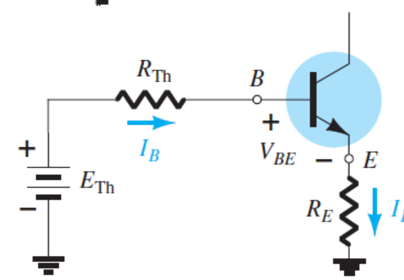
Exact analysis:

$$R_{Th} = R_1 \parallel R_2 = \frac{(82\times10^3)(22\times10^3)}{82\times10^3+22\times10^3} = 17.35\ \text{k}\Omega$$

$$E_{Th} = V_{R2} = \frac{R_2 V_{CC}}{R_1+R_2} = \frac{(22\times10^3)(18)}{82\times10^3+22\times10^3} = 3.81\ \text{V}$$

$$I_B = \frac{E_{Th}-V_{BE}}{R_{Th}+(\beta+1)R_E} = \frac{3-0.7}{17\times10^3+(51)(1.2\times10^3)} = 39.6\ \mu\text{A}$$

$I_{CQ} = \beta I_{BQ} = (50)(39.6\times10^{-6}) = 1.98$ mA
$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$
$= 18 - (1.98\times10^{-3})(5.6\times10^3 + 1.2\times10^3) = 4.54$ V



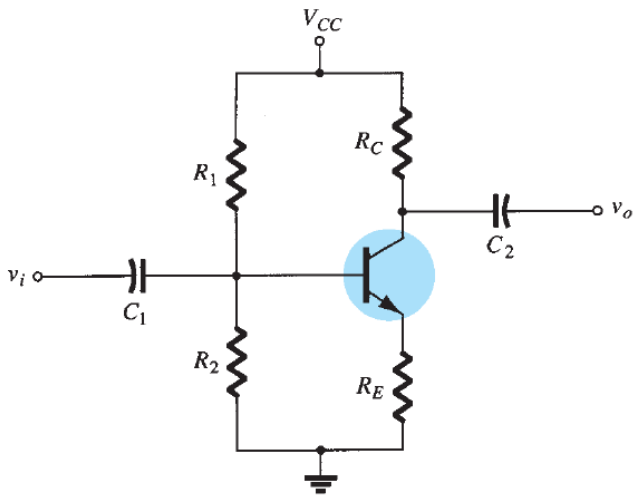
Approximate analysis:
$\beta R_E \geq 10R_2$
$(50)(1.2\times10^3) \geq 10(22\times10^3)$
$60\ \text{k}\Omega \ngeq 39\ \text{k}\Omega$ (not satisfied, so we cannot use approximate technique)

Voltage Divider Bias Configuration

Transistor saturation:

$V_{CE} = 0$ in $V_{CEQ} = V_{CC} - I_C(R_C + R_E)$

$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C+R_E}$



Load-line analysis:

$I_C = 0$ in $V_{CE} = V_{CC} - I_C(R_C + R_E)$

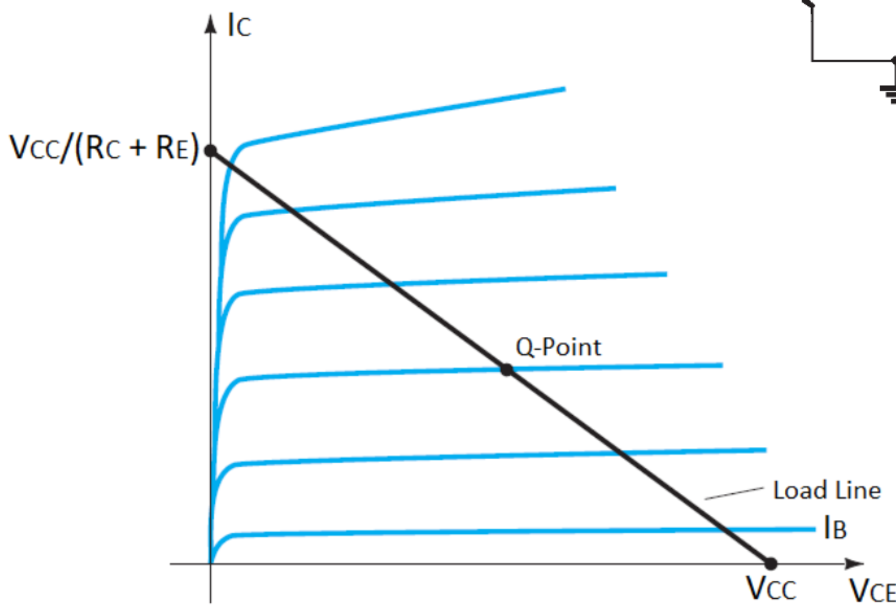
$V_{CE} = V_{CC}$

Point $A = (V_{CC}, 0)$

$V_{CE} = 0$ in $V_{CE} = V_{CC} - I_C(R_C + R_E)$

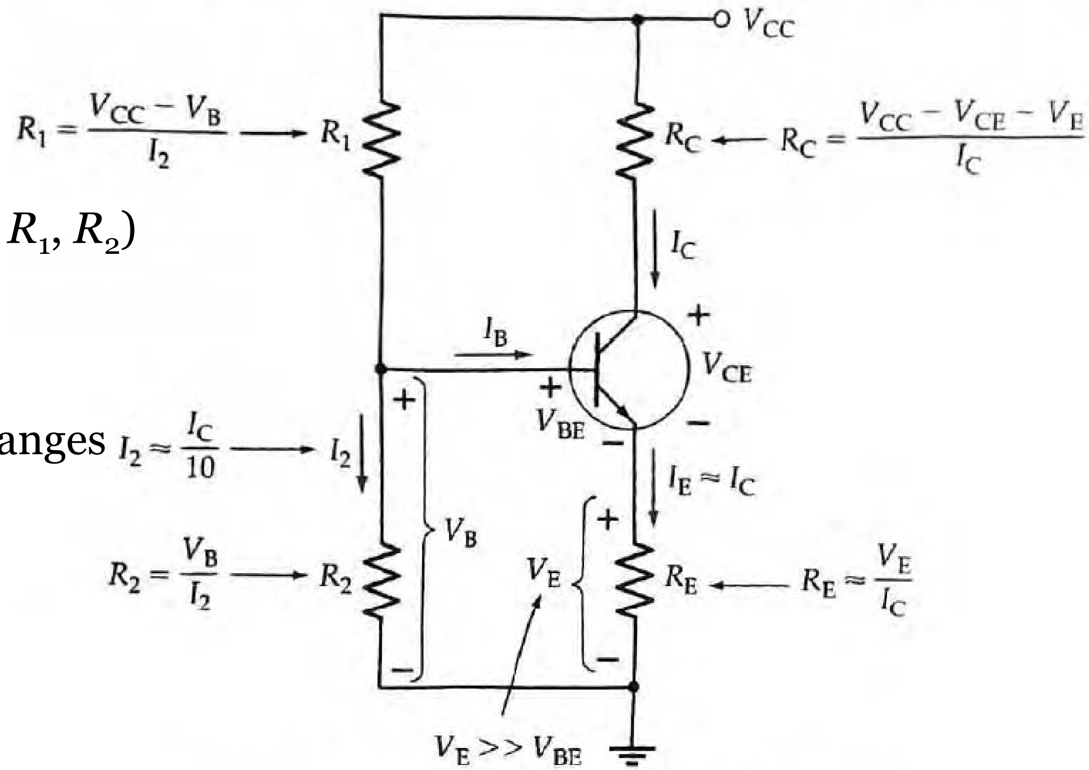
$I_C = \frac{V_{CC}}{R_C+R_E}$

Point $B = (0, V_{CC}/(R_C + R_E))$



Bias Circuit Design

Design → Specification of supply voltage
Required levels of I_C and V_{CE}
Required voltage and current across each resistor
Resistor values are calculated by Ohm's law.



<u>Voltage divider bias circuit design:</u>

$I_2 >> I_B$ → V_B stable
unaffected by h_{FE}
low input impedance (low R_1, R_2)

Rule of thumb: $I_2 = I_C/10$
large R_1, R_2 + ($I_2 > I_B$)

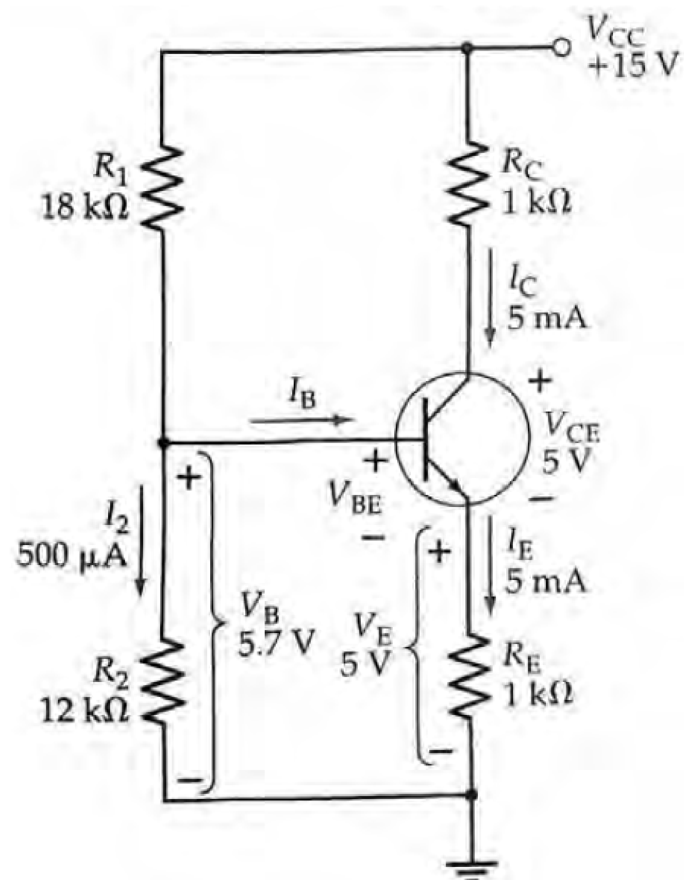
$V_E >> V_{BE}$ → minimizes effect of V_{BE} changes

Rule of thumb: $V_E = 5$ V if $V_{CC} \geq 10$ V
$V_E = 3$ V if $V_{CC} < 10$ V

Bias Circuit Design

Problem-29:

Design the voltage divider bias circuit to have $V_{CE} = V_E = 5$ V and $I_C = 5$ mA when the supply voltage is 15 V. Assume the transistor h_{FE} is 100.



$R_E = V_E/I_E \approx V_E/I_C = 5/(5\times10^{-3}) = 1$ kΩ

$R_C = \frac{V_{CC}-V_{CE}-V_E}{I_C} = \frac{15-5-5}{5\times10^{-3}} = 1$ kΩ

$I_2 = I_C/10 = 5\times10^{-3}/10 = 500$ µA

$V_B = V_E + V_{BE} = 5 + 0.7 = 5.7$ V

$R_2 = V_B/I_2 = 5.7/500\times10^{-6}$

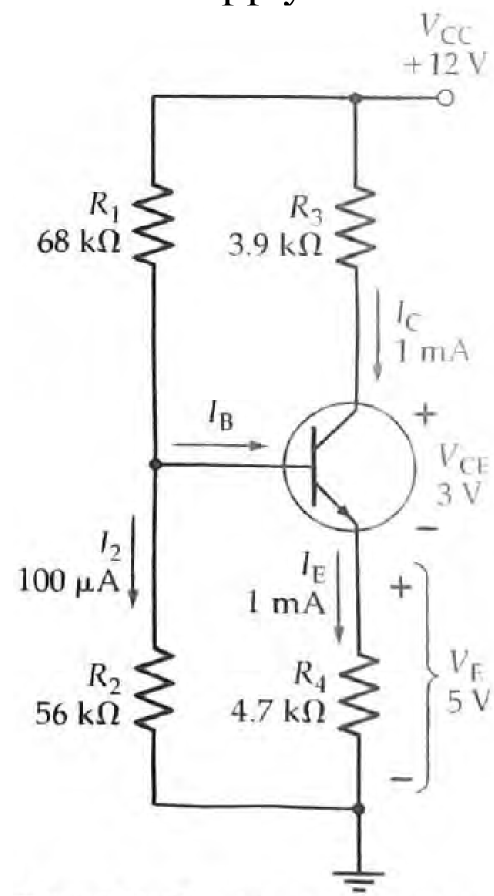
$= 11.4$ kΩ (use 12 kΩ standard value)

$R_1 = \frac{V_{CC}-V_B}{I_2} = \frac{15-5.7}{500\times10^{-6}} = 18.6$ kΩ (use 18 kΩ standard value)

Bias Circuit Design

Problem-30:

Design the voltage divider bias circuit in Fig. 30 to operate from a 12 V supply. The bias conditions are to be V_{CE} = 3 V, V_E = 5 V, and I_C = 1 mA.



$R_4 = V_E/I_E \approx V_E/I_C = 5/(1\times10^{-3}) = 5$ kΩ (use 4.7 kΩ standard value)

With I_C = 1 mA and R_4 = 4.7 kΩ

$$V_E = I_C R_4 = 1\times10^{-3}\times4.7\times10^3 = 4.7\text{ V}$$

$$V_C = V_E + V_{CE} = 4.7 + 3 = 7.7\text{ V}$$

$V_{R3} = V_{CC} - V_C = 12 - 7.7 = 4.3$ V

$R_3 = V_{R3}/I_C = 4.3/1\times10^{-3} = 4.3$ kΩ

(use 3.9 kΩ standard value to reduce V_{R3} and increase V_{CE})

$V_B = V_E + V_{BE} = 4.7 + 0.7 = 5.4$ V

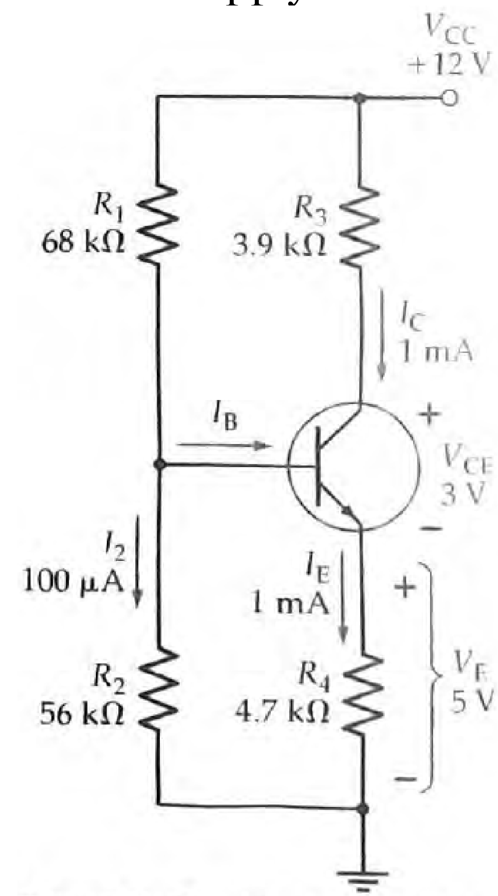
$I_2 = I_C/10 = 1\times10^{-3}/10 = 100$ µA

$R_2 = V_B/I_2 = 5.4/100\times10^{-6} = 54.4$ kΩ (use 56 kΩ standard value)

Bias Circuit Design

Problem-30:

Design the voltage divider bias circuit in Fig. 30 to operate from a 12 V supply. The bias conditions are to be V_{CE} = 3 V, V_E = 5 V, and I_C = 1 mA.



With R_2 = 56 kΩ and V_B = 5.4 V

$$I_2 = V_B/R_2 = 5.4/56\times10^3 = 96.4\ \mu A$$

$$R_1 = \frac{V_{CC}-V_B}{I_2} = \frac{12-5.4}{96.4\times10^{-6}} = 68.5\ k\Omega \text{ (use 68 k}\Omega\text{ standard value)}$$