

**PAMUKKALE ÜNİVERSİTESİ**

**MÜHENDİSLİK FAKÜLTESİ**

**ELEKTRİK-ELEKTRONİK MÜHENDİSLİĞİ**

**EEEN 360 FPGA İLE SAYISAL TASARIM**

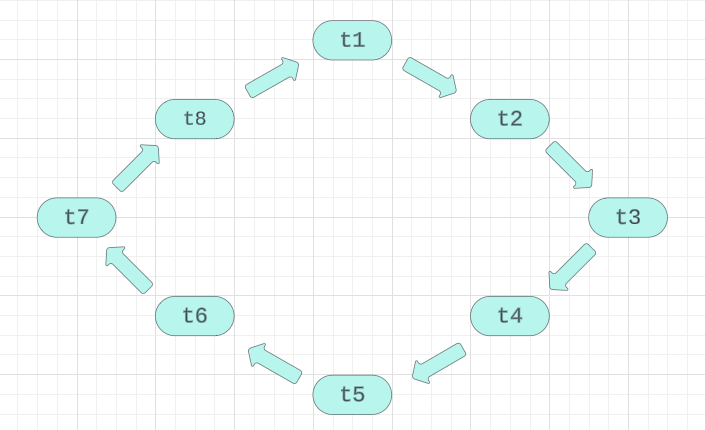
**BÖLÜM II VİZE SINAVI**

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**Diyagram:**



**Tablo:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | KI |  |  | DI |  |  | GI |  |  | BI |  |
|  | K | S | Y | K | S | Y | K | S | Y | K | S | Y |
| t1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| t2 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| t3 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| t4 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| t5 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| t6 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| t7 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| t8 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

**Işık Süreleri:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | KI |  |  | DI |  |  | GI |  |  | BI |  |
| K S Y | 30s | 6s | 24s | 46s | 6s | 8s | 44s | 6s | 10s | 48s | 6s | 6s |

**VHDL Kodları:**

library ieee;

use ieee.std\_Logic\_1164.all;

use ieee.numeric\_std.all;

entity TRI is

port(

--inputs

Clk : in std\_logic;

--outputs

KI : out unsigned (2 downto 0);

BI : out unsigned (2 downto 0);

DI : out unsigned (2 downto 0);

GI : out unsigned (2 downto 0));

end entity;

architecture Behavioral of TRI is

type durumlar is (t1,t2,t3,t4,t5,t6,t7,t8);

signal durum : durumlar := t1;

constant Clk\_freq : integer := 12000;

signal Cnt : integer range 0 to Clk\_freq\*60 := 0;

begin

process (Clk)is

begin

if rising\_edge(Clk) then

KI <= "000";

DI <= "000";

GI <= "000";

BI <= "000";

Cnt <= Cnt+1;

case durum is

when t1 =>

KI <= "010";

DI <= "100";

GI <= "100";

BI <= "010";

if Cnt = Clk\_freq\*3-1 then

Cnt <= 0;

durum <= t2;

end if;

when t2 =>

KI <= "001";

DI <= "100";

GI <= "100";

BI <= "100";

if Cnt = Clk\_freq\*24-1 then

Cnt <= 0;

durum <= t3;

end if;

when t3 =>

KI <= "010";

DI <= "010";

GI <= "100";

BI <= "100";

if Cnt = Clk\_freq\*3-1 then

Cnt <= 0;

durum <= t4;

end if;

When t4 =>

KI <= "100";

DI <= "001";

GI <= "100";

BI <= "100";

if Cnt = Clk\_freq\*8-1 then

Cnt <= 0;

durum <= t5;

end if;

When t5 =>

KI <= "100";

DI <= "010";

GI <= "010";

BI <= "100";

if Cnt = Clk\_freq\*3-1 then

Cnt <= 0;

durum <= t6;

end if;

When t6 =>

KI <= "100";

DI <= "100";

GI <= "001";

BI <= "100";

if Cnt = Clk\_freq\*10-1 then

Cnt <= 0;

durum <= t7;

end if;

When t7 =>

KI <= "100";

DI <= "100";

GI <= "010";

BI <= "010";

if Cnt = Clk\_freq\*3-1 then

Cnt <= 0;

durum <= t8;

end if;

When t8 =>

KI <= "100";

DI <= "100";

GI <= "100";

BI <= "001";

if Cnt = Clk\_freq\*6-1 then

Cnt <= 0;

durum <= t1;

end if;

end case;

end if;

end process;

end architecture;