Middle East Technical University - Department of Computer Engineering

CENG 232

Logic Design

2022-2023 Spring

Lab 2 Quiz

Quiz date: Sunday, April 30, 2023, 13:30
Duration 60 minutes

Logisim Part

You are expected to draw the circuits using the Logisim (CENG version) tool. **You may ask your questions using the chatbox of Zoom.**
The Logisim part consists of 2 questions. Labeling conventions are provided in each question section.

- Please implement each question in a different circ file.
- The circ file of the "4x12 Decoder" question should be named as **question1.circ**.
- The circ file of the "Demultiplexer" question should be named as **question2.circ**.

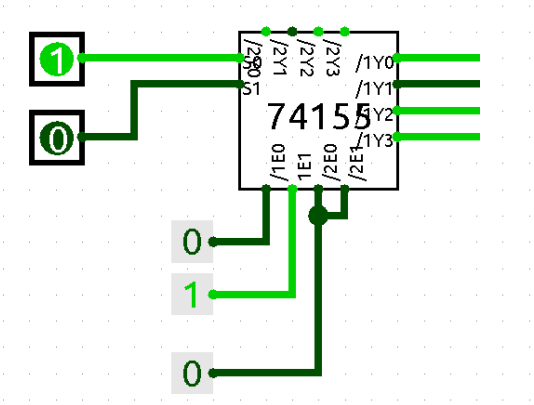
IC Pool

Only the following logic gates could be employed for the Logisim part.

- Constant Gate
- 74LS04 (NOT, Inverter)
- 74LS08 (AND)
- 74LS32 (OR)
- 74LS155 (2x4 Decoder)
- 74LS241 (3-state Buffer, Controlled Buffer)

Q1) 4x12 Decoder

Below a basic wiring scheme for operating a 2x4 decoder (74LS155) is given. 74LS155 accommodates two separate 2x4 decoders that share the input pins (S0, S1). For each decoder, there are two groups of enable pins: /1E0, 1E1 (for the first decoder) and /2E0, /2E1 (for the second one). So in order to activate the first decoder (whose outputs are labeled as /1Y0, /1Y1, /1Y2, /1Y3), the /1E0 pin should be set to 0 (because it is an active-low pin) and the 1E1 pin should set 1 (because it is an active-high pin). Similarly, to activate the second decoder (whose outputs are labeled as /2Y0, /2Y1, /2Y2, /2Y3), the /2E0 and /2E1 pins should be set to 0, 0, respectively. Both decoders deactivate (set to 0) their output pin which is determined via the input pins (and the other output pins are activated). When any of the enable pins of a decoder (2x4) is not set properly, it activates its all output pins (if you are planning to use a decoder, its enable pins should not be left unconnected, in other words, the enable pins should be connected to a logic signal (0 or 1)).
With the given information above, you are expected to implement a 4x12 decoder component by using 2x4 decoders (74LS155). The decoder (4x12) has 4 input pins (S0, S1, S2, S3), 1 enable pin (E), and 12 output pins (Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11). The following table describes the behavior of the decoder (4x12).



Inputs				Enable	Outputs											
S3	S2	S1	S0	E	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
X	X	X	X	0	1	1	1	1	1	1	1	1	1	1	1	1

When the enable pin (E) is low (0) all outputs are set to 1 no matter what the values of the input pins are. In the table, Xs denote don't-care values.

Labelling Specifications

- The input pins should be labeled as **S3, S2, S1, S0, E**.
- The output pins should be labelled as **Y11, Y10, Y9, Y8, Y7, Y6, Y5, Y4, Y3, Y2, Y1, Y0**.
- Label properties are case-sensitive. **Please be very careful at naming the labels correctly.**
- You will receive grade **penalty** unless labeling is done properly.

Note: For the evaluation, the other values that are not present in the table will not be tested for the input pins (e.g. the combination S3=1, S2=1, S1=0, S0=0 will not be tested).

Q2) Demultiplexer

A demultiplexer circuitry takes an input signal and transfers/directs it to a selected output (it reverses the operation of a multiplexer). It can be likened to a railway controller which connects a specific railway to different directions. You are expected to implement 1x4 demultiplexer consisting of 1 input pin (I0), 2 selector pins (S1, S0) and 4 output pins (O3, O2, O1, O0). (Hint: Using **Controlled Buffer** component (In Logisim Ceng232 Gates → Controlled Buffer) may simplify your design.)

Input	Selector		Output			
I0	S1	S0	O3	O2	O1	O0
A	0	0	0	0	0	A
A	0	1	0	0	A	0
A	1	0	0	A	0	0
A	1	1	A	0	0	0

Where A $\in \{0, 1\}$.

Labelling Specifications

- Your input pins should be labelled as **I0, S1, S0**.
- Your output pins should be labeled as O3, O2, O1, O0
- Label properties are case-sensitive. **Please be very careful at naming the labels correctly.**
- You will receive grade **penalty** unless labeling is done properly.

Cheating Policy

All the work should be individual and there is a zero-tolerance policy for cheating. See the course website for further information about the cheating policy.

References

CENG Logisim Version.