AMERICAN INTERNATIONAL
UNIVERSITY-BANGLADESH
Faculty of Science and Technology

Lab Report 8

Lab No: 8

Lab Title: **Construction of MOSFET Logic Gates**

Course Title: DIGITAL LOGIC AND CIRCUITS LAB

Course Code: EEE3102 **Section**: L

Semester: Summer 2021-22 Course Teacher: **NIRJHOR TAHMIDUR ROUF**

Date: 03-08-22

No	Name	ID	Program	Signature
01	Emon, Mehedi Hasan	19-41118-2	BSc in CSE	
02	Shojib, Kazi Ahsanul Haque	19-40051-1	BSc in CSE	
03	Rifat Ahmed	19-41107-2	BSc in CSE	
04	Md. Minhazul Hoque Chowdhury	20-43086-1	BSc in CSE	
05	S. M. Shadman Hossen	19-41526-3	BSc in EEE	

Experiment no: 8

Title: Construction of MOSFET Logic Gates

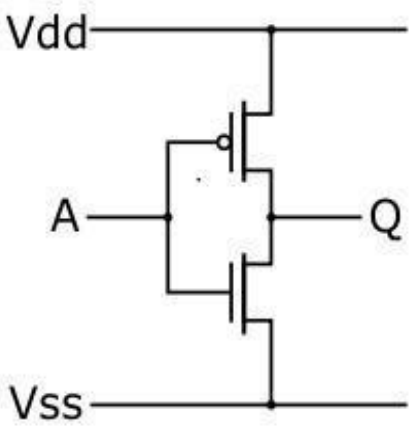
Introduction:

MOSFET:

The MOSFET transistor is a semiconductor component that is frequently used in electrical devices for switching and signal amplification. Due to its small size, a MOSFET is either a core or an integrated circuit that is designed and manufactured on a single chip. The field of switching in electronics has changed as a result of the invention of the MOSFET device.

CMOS

Complementary Metal Oxide Semiconductor is what the abbreviation CMOS means. The creation of integrated circuits using this technology is widespread today and it is one of the most well-liked technologies in the computer chip design business. This technique is used in today's computer memories, CPUs, and cell phones for several reasons. Both P channel and N channel semiconductor devices are used in this technique. A CMOS patent was given to Frank Wanlass in 1963. (3,356,858 USPTO). Another name for CMOS (sometimes known as COS-MOS) is complementary-symmetry metal-oxide semiconductor (or COS MOS). The term "complementary-symmetry" refers to the common practice of constructing CMOS logic functions using complementary and symmetrical pairings of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs).



CMOS inverter (NOT logic gate)

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

Some advantages of CMOS over TTL are:

• Because MOSFETs are voltage-controlled, rather than current-controlled, transistors, CMOS gate inputs consume far less current than TTL inputs.

• CMOS transistors are smaller in size and have lower power dissipation than NMOS transistors. • CMOS gates are able to function on a far wider range of power supply voltages than TTL: typically 3 to 15 volts compared to 4.75 to 5.25 volts for TTL.

In this experiment, we'll first take a look at a few NMOS-based logic circuit designs. The same logic circuits will then be implemented using CMOS in an effort to determine any potential design advantages over NMOS.

Theory and Methodology:

NMOS Inverter with Ohmic/ Resistive Load:

Considering an ideal scenario, when a HIGH (+5V) is applied to the input, the NMOS transistor turns ON and current flows from Vdd to ground; thus output voltage, Vo= 0V.
Similarly, if a LOW (0V) is applied to the input, the NMOS remains in its OFF state. As a result, the current from Vdd has no path to ground. The output voltage is +5V

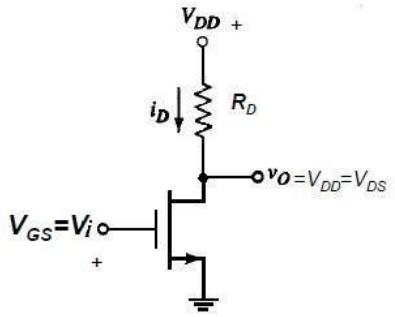


Fig.1: NMOS Inverter with Ohmic/Resistive Load

NMOS Inverter with NMOS Enhancement Transistor load:

One disadvantage of designing NMOS logic circuits with ohmic load is that even when the NMOS is OFF, there is static power dissipation due to the resistor. A better design is to use an enhancement-type NMOS as load. They are "*normally-off*" devices and it takes an applied voltage between gate and drain of the correct polarity to bias them *on*. Thus static power consumption is avoided

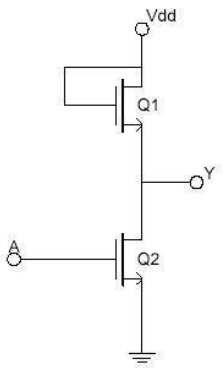


Fig.2 NMOS Inverter with NMOS Load

NMOS NAND Gate:

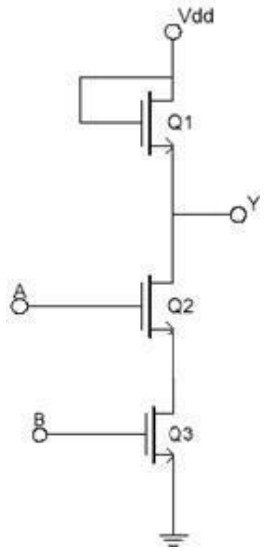


Fig.3 NMOS NAND Gate

NMOS NOR Gate:

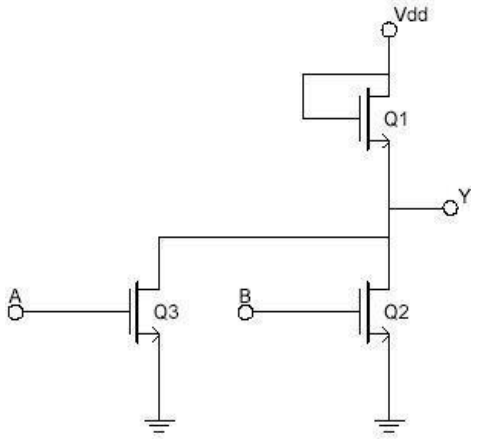


Fig.4 NMOS NOR Gate

CMOS Logic:

CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications.

CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When OFF, their resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

CMOS Inverter:

When the input is grounded (logic 0), the N-channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground. At the same time, the P-channel MOSFET is forward biased, so it has a channel enhanced within itself. This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the output up to +V (logic 1).

When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

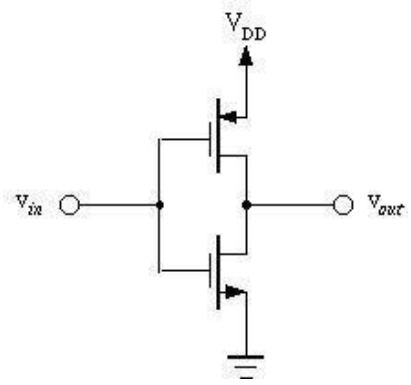


Fig.5 CMOS Inverter

CMOS NAND Gate:

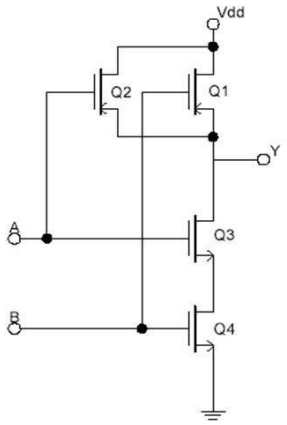


Fig.6 CMOS NAND Gate

CMOS NOR Gate:

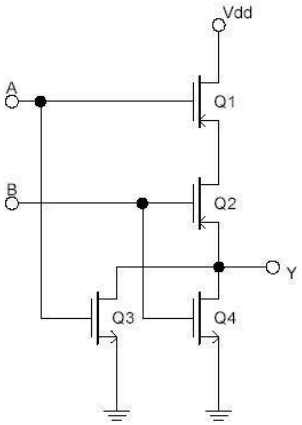
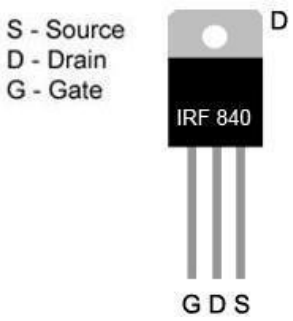


Fig.7 CMOS NOR Gate

MOSFET pin configuration:



Circuit Diagram/ Lab Work:

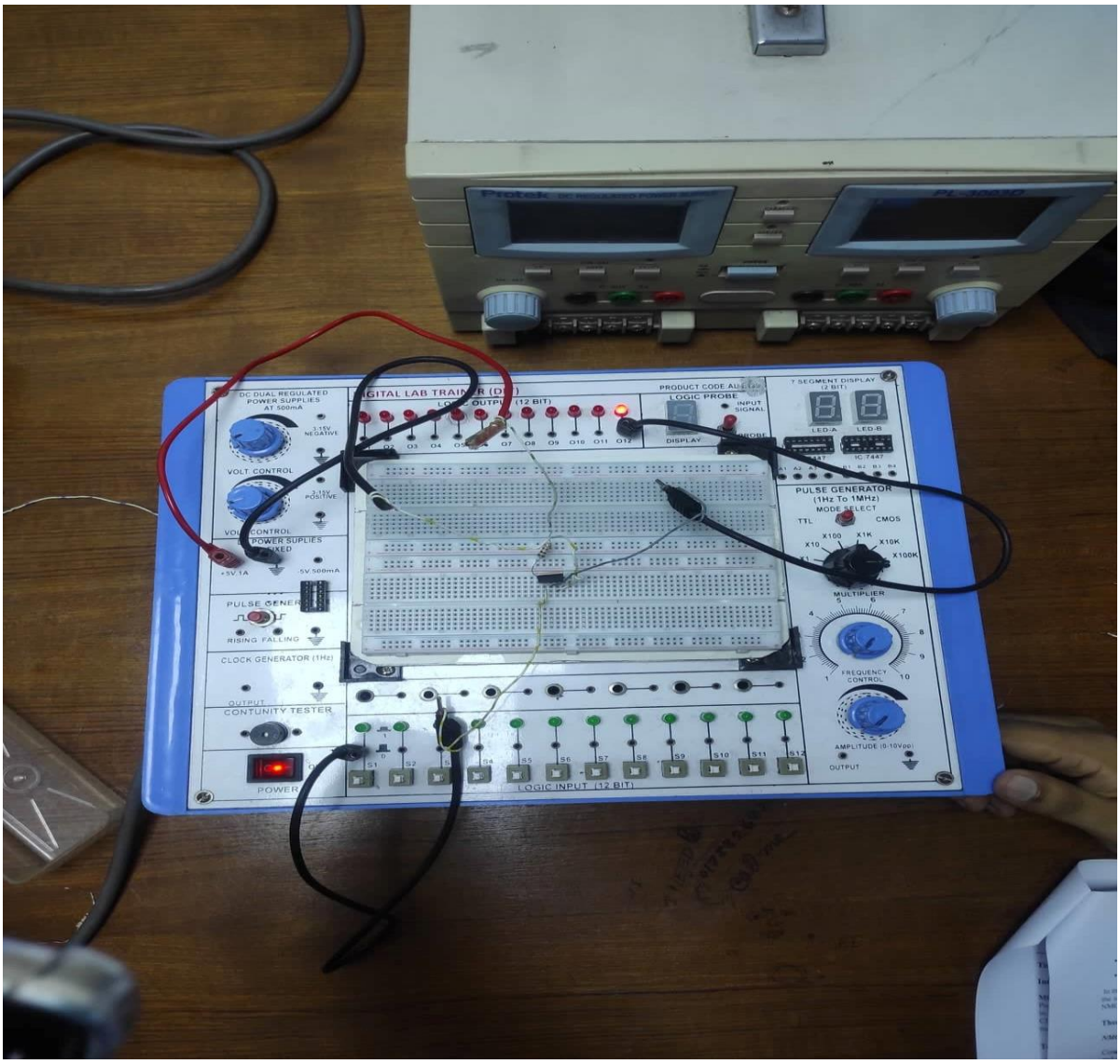
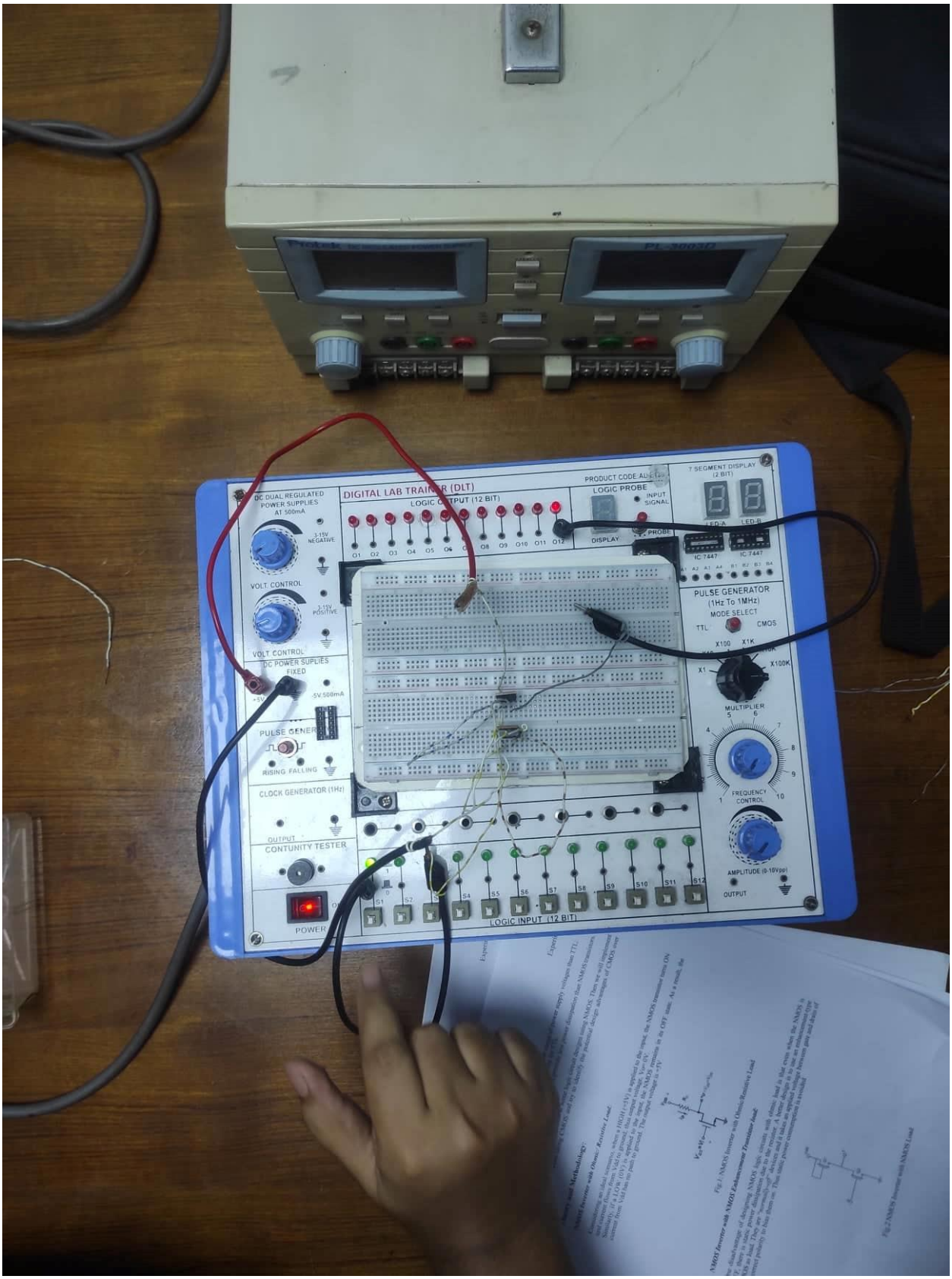


Fig1: NMOS Inverter with Ohmic Load


DIGITAL LAB TRAINER (DLT)
LOGIC PROBE
LOGIC OUTPUT (12 BIT)
LOGIC INPUT (12 BIT)
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CLOCK GENERATOR (1Hz)
CONTUNITY TESTER
VOLT CONTROL
DC POWER SUPLIES FIXED
7 SEGMENT DISPLAY (2 BIT)
IC 7447
POWER

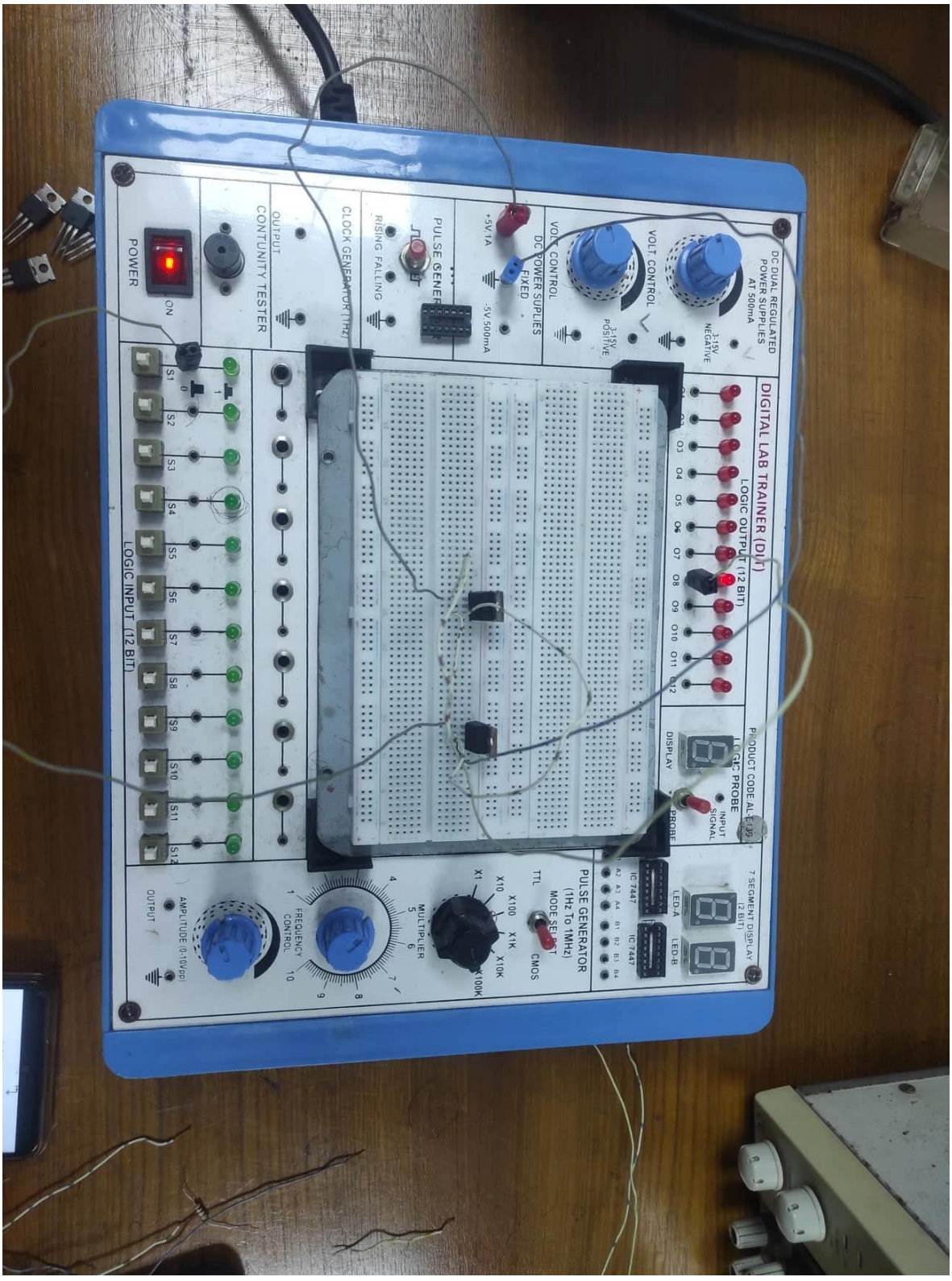


Fig2: NMOS Inverter with NMOS Load

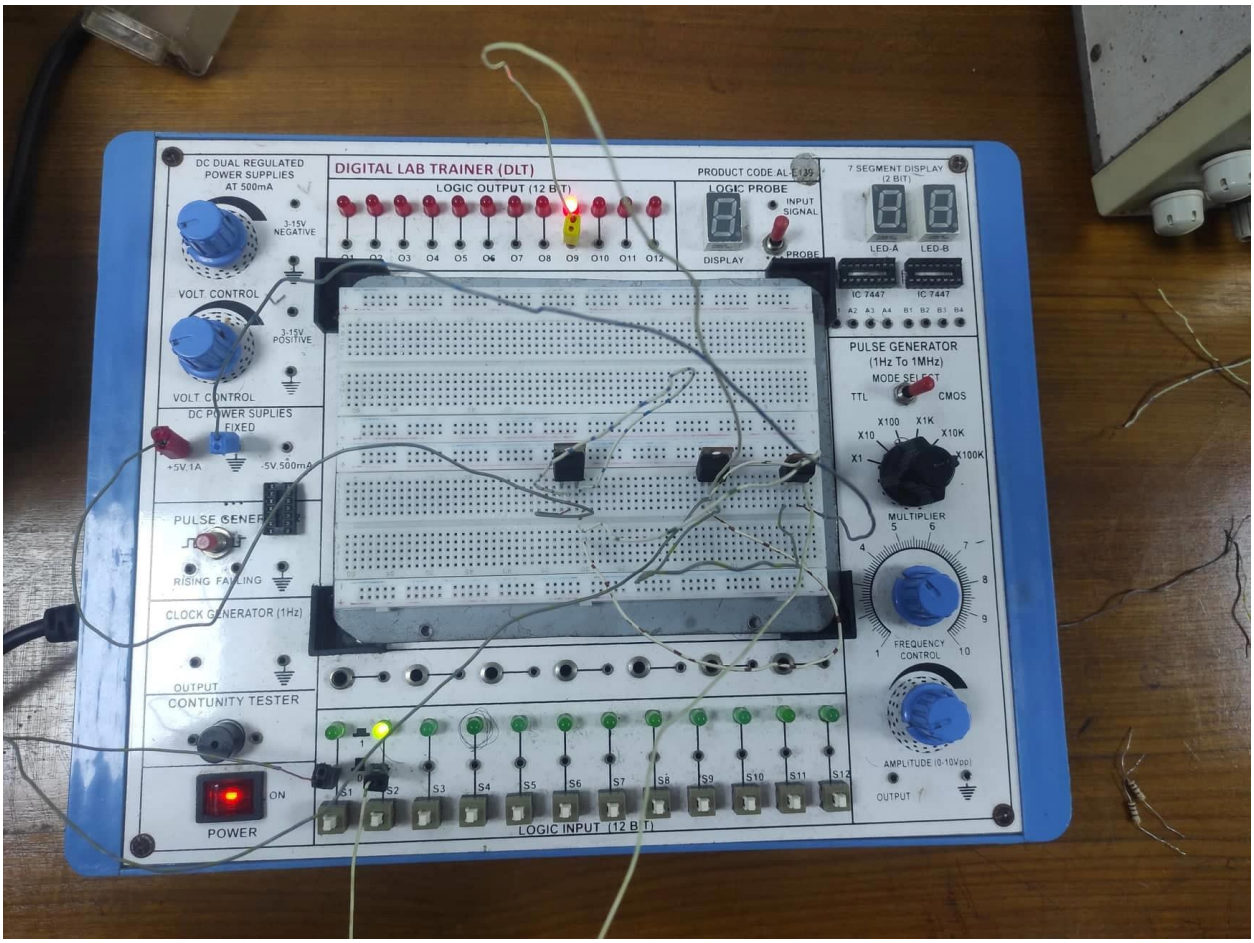
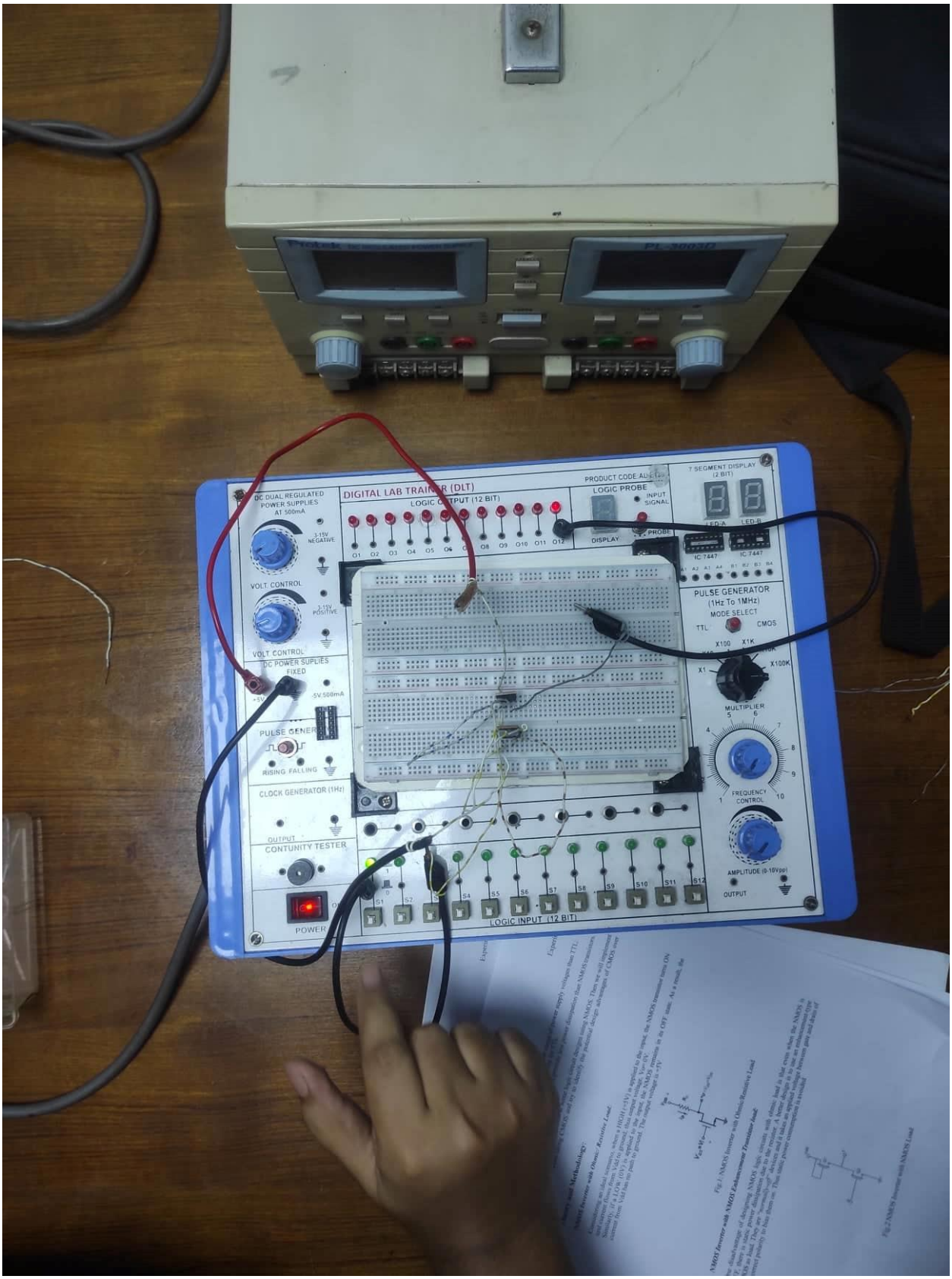


Fig.3 NMOS NAND Gate


DIGITAL LAB TRAINER (DLT)
LOGIC PROBE
LOGIC OUTPUT (12 BIT)
LOGIC INPUT (12 BIT)
PULSE GENERATOR
(1Hz To 1MHz)
MODE SELECT
TTL
CMOS
MULTIPLIER
FREQUENCY CONTROL
AMPLITUDE (0-10Vpp)
OUTPUT
CLOCK GENERATOR (1Hz)
CONTUNITY TESTER
VOLT CONTROL
DC POWER SUPLIES FIXED
7 SEGMENT DISPLAY (2 BIT)
IC 7447
POWER

Truth Table of NOT Gate and NAND Gate:

A	B	Y
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Truth Table Of NAND Gate

X	Y
0	**1**
1	**0**

Truth Table of NOT Gate

Results and Simulations:

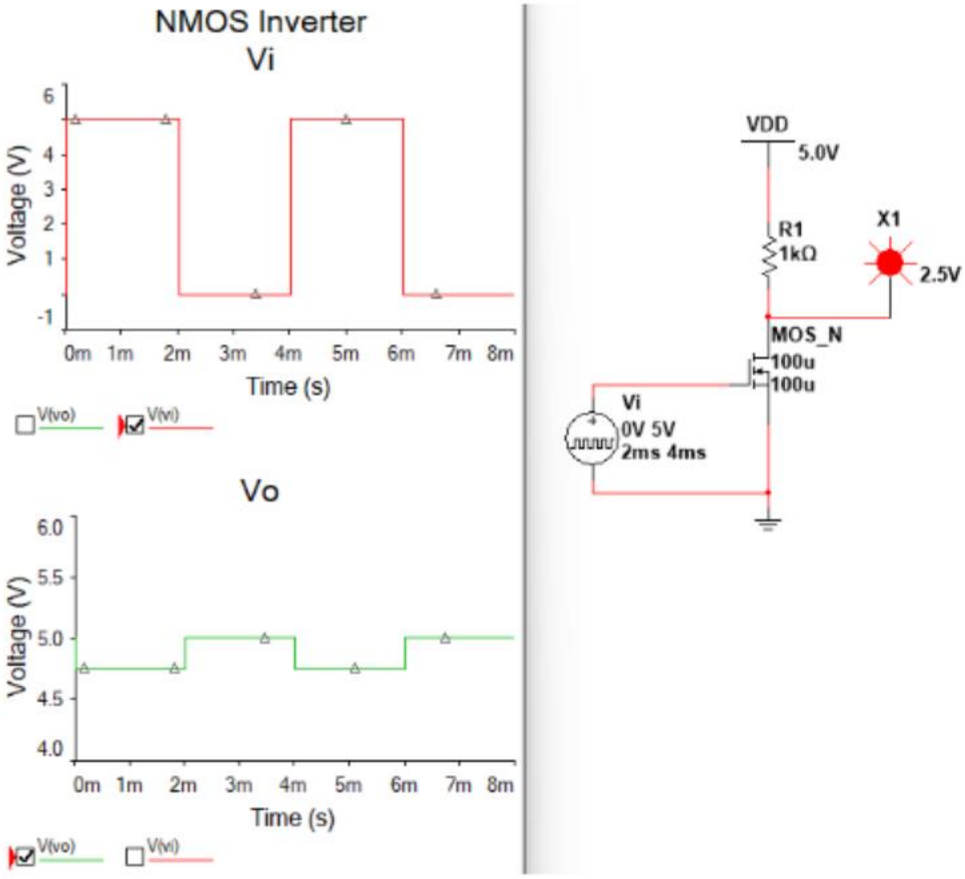


Figure: NMOS Inverter with
Ohmic/Resistive Load

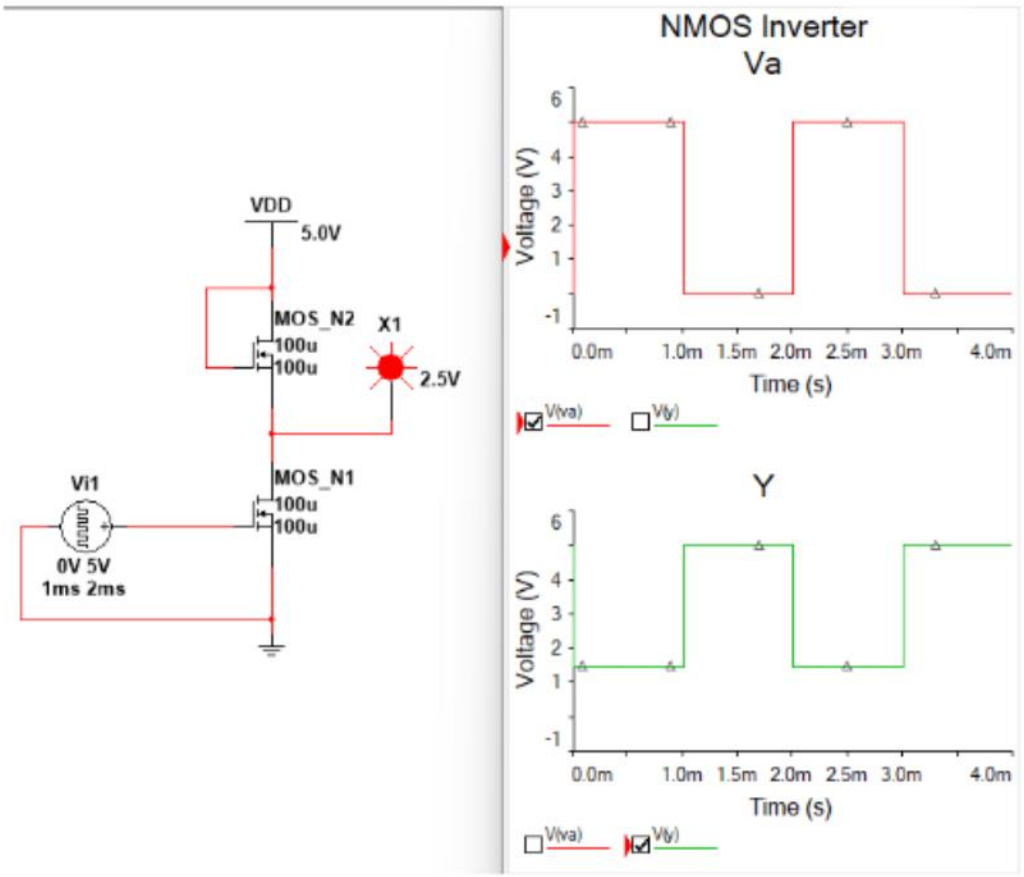


Figure: NMOS Inverter with NMOS Load

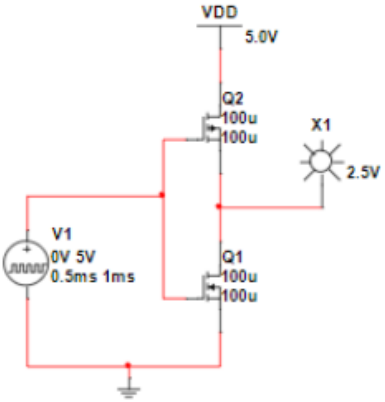


Fig: CMOS Inverter circuit diagram.

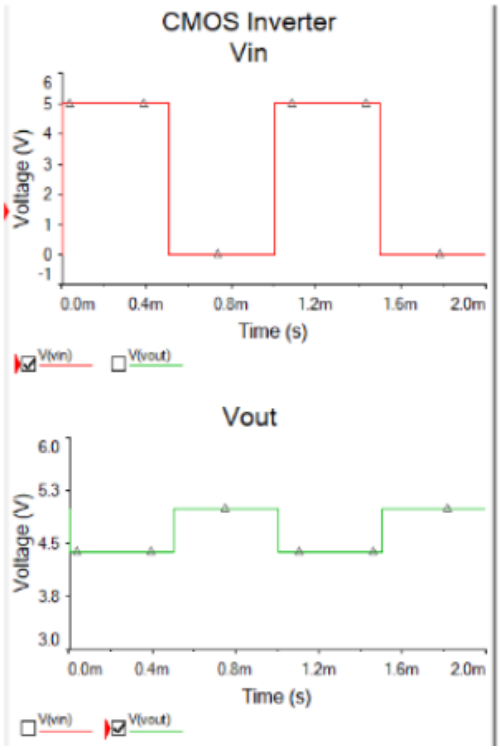


Figure: CMOS Inverter Transient Analysis

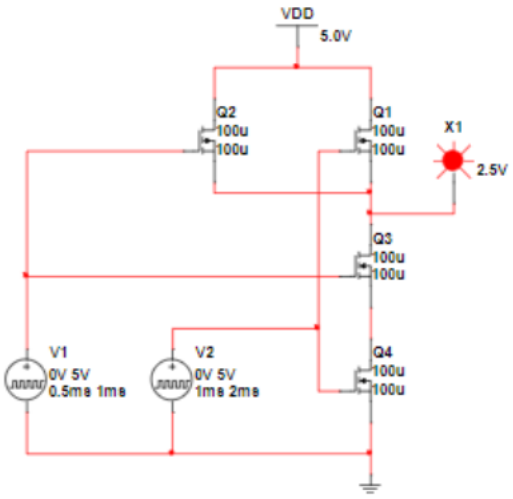


Figure: CMOS Nand Circuit Diagram

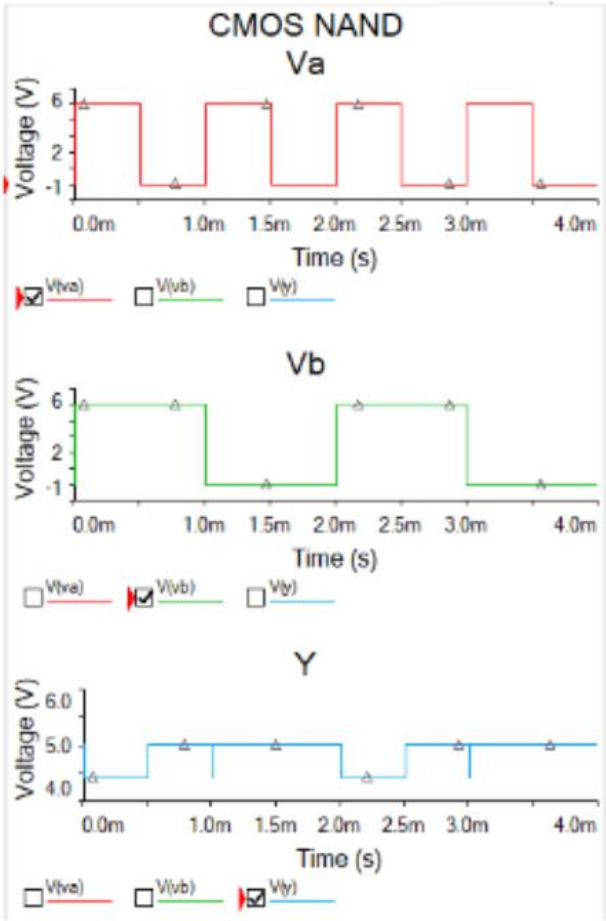


Figure: CMOS Nand Transient Analysis

Report Question Answers:

1. **For, each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?**

Ans: The experiment result did not match with the expected output because some of the circuit did not have the ohmic load.

Inverter: There were only two sorts of data available for inverter: logic 0 and logic 1. Logic 0 denotes a low voltage (0V), whereas Logic 1 denotes a high voltage (+5V). We can also observe from the results and simulation section that the findings are consistent with the ideal outputs that were predicted.

NAND Gate: As can be seen from the truth table section, we used four data sets for NAND Gate. In this case, logic 0 indicates that both inputs are low, while logic 1 implies that both inputs are high. One of the inputs is low and the other is high in logic 0/1 and logic 1/0, respectively. Similar to the Inverter, the NAND Gate's result was in line with expectations.

Discussion & Conclusion:

We created NOT and NAND gates in this experiment using MOSFETs, but it was difficult to tell which was CMOS and which was NMOS. We also observed dynamic heat, or the warming up of MOSFETs, during this experiment. Additionally, we completed our simulation experiment and got the results for each simulation. We saw the dynamic heat of MOSFETs in this experiment. Additionally, we cross-validated our simulation and experiment results with the theoretical findings, and for each gate, we obtained results that were near to the theoretical value.