AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH

Faculty of Science and Technology

Lab Report 7

Lab No: 7

Lab title: Implementation of Asynchronous and synchronous counters using flip-flops.

Course Title: DIGITAL LOGIC AND CIRCUITS LAB

Course Code: EEE3102 **Section:** L

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Experiment no: 7

Title: Implementation of Asynchronous and synchronous counters using flip-flops.

Introduction:

The flip-flops make up the majority of the counter. The flip-flop flip order allows for the division of the counter into synchronous and asynchronous. When the count pulse is input, all flip-flops in a synchronous counter flip simultaneously; in an asynchronous counter, not all flip-flops flip simultaneously. An addition counter, a subtraction counter, and a reversible counter (also known as an up/down counter) can all be characterized according to how the number in the counter changes during the counting process. Up and down counters are referred to as reversible counters. The up counter counts up with the continuous input of counting pulses, and the down counter counts down with the continuous input of counting pulses.
Counters are classified into two broad categories according to the way they are clocked: asynchronous and synchronous. In asynchronous counters, commonly called ripple-counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop. In synchronous counters, theclock input is connected to all of the flip-flops so that they are clocked simultaneously.
The objective of this experiment is designing of the following counters using J-K Flip-Flops (IC 74LS76)

(a) n-bit Binary Asynchronous Counter
(b) n-bit Binary Synchronous Counter

Theory and Methodology:

Asynchronous counter:

Asynchronous counters are those whose output is free from the clock signal. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be a delay in producing output. The required number of logic gates to design asynchronous counters is very less.

Timing diagram:

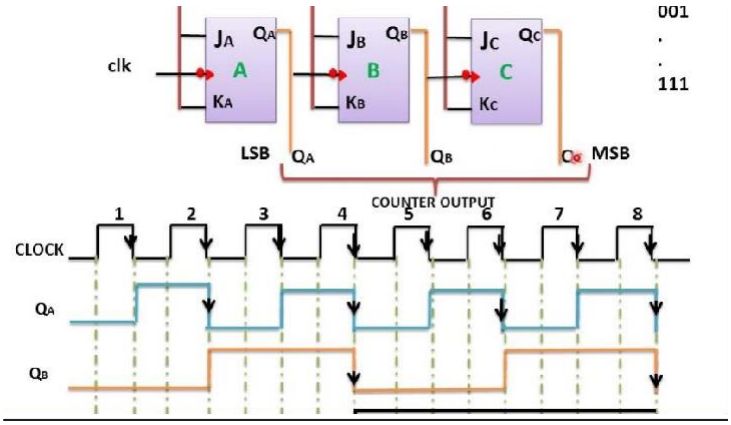


Figure 1: 3-bit Asynchronous counter and its timing diagram

In an asynchronous counter, a clock pulse drives FF0. The output of FF0 drives FF1 which then drives the FF2 flip flop. All J and K inputs are connected to Logic 1. Therefore, each flip-flop will toggle with the negative transition at its clock input. The 3-bit asynchronous counter consists of 3 JK flip-flops. The overall propagation delay time is the sum of individual delays. Initially, all flip-flops are reset to produce 0. The output conditions are Q2Q1Q0 = 000. When the first clock pulse is applied, the FF0 changes state on its negative edge. Therefore, Q2Q1Q0 = 001. On the negative edge of the second clock pulse flip flop FF0 toggles. Its output changes from 1 to 0. This being a negative change, FF1 changes state. Therefore, Q2Q1Q0 = 010. Similarly, the output of flipflop FF2 changes only when there is a negative transition at its input when the fourth clock pulse is applied. The output of the flip-flops is a binary number equivalent to the number of clock pulses received. The output conditions are as shown in the truth table. On the negative edge of the eighth pulse, the counter is reset.

3-bit asynchronous counter truth table:

Counter State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 1

The counter acts as a frequency divider. FF0 divides clock frequency by 2, FF1 divides clock frequency by 4, and FF2 divides clock frequency by 8. If n flip flops are cascaded, we get 2n2n output conditions. The largest binary number counted by n cascaded flip flops has a decimal equivalent of 2n−12n−1. The counter has a count of the largest binary number 111 which has a decimal equivalent of 23−1=7.

Synchronous counter:

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The most important advantage of synchronous counters is that there is no cumulative time delay because all flip-flops are triggered in parallel. Thus, the maximum operating frequency for this counter will be significantly higher than for the corresponding ripple counter.

Table 1 shows the contents of a three-bit up-counter for eight consecutive clock cycles, assuming that the count is initially 0. Observing the pattern of bits in each row of the table, it is apparent that bit Q0 changes on each clock cycle. Bit Q1 changes only when Q0 = 1. Bit Q2 changes only when both Q1 and Q0 are equal to 1. In general, for an n-bit up-counter, a given flip-flop changes its state only when all the preceding flip-flops are in the state Q = 1.

T1 = Q0
T2 = Q0Q1
T3 = Q0Q1Q2
T4= Q0Q1Q2Q3
.
.
.
Tn = Q0Q1 ⋯Qn−1

Clock cycle	Q_2 Q_1 Q_0
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1
8	0 0 0

Q_1 changes
Q_2 changes

The Circuit diagram of a three-bit counter based on these expressions is given in Figure 9.2a. Figure 9.2b gives a timing diagram. It shows that the circuit behaves as a modulo-16 up-counter. Because all changes take place with the same delay after the active edge of the Clock signal, the circuit is called a synchronous counter.

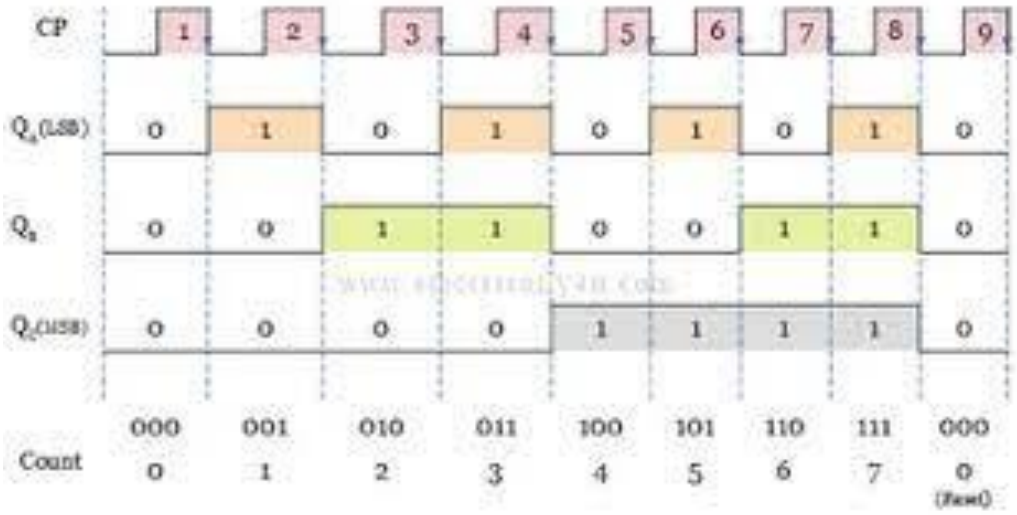


Figure: Three bit Synchronous Up Counter.

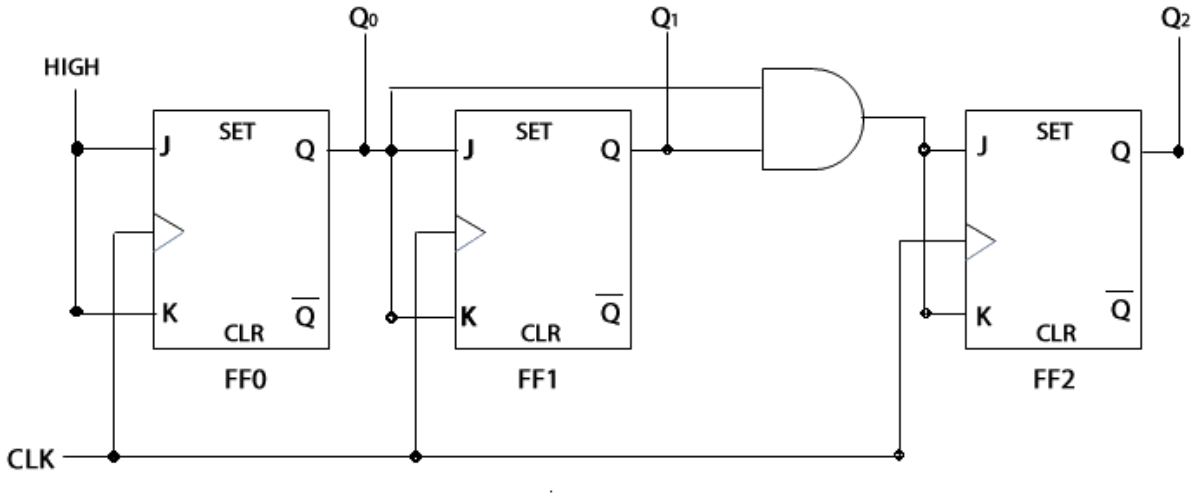


Fig : three bit Synchronous Up Counter.

3-bit synchronous counter truth table:

Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

Pin Configuration of 74LS76 and 7408

There are 2 J-K Flip Flops in one IC. Here is the pin configuration of the IC 74LS76:

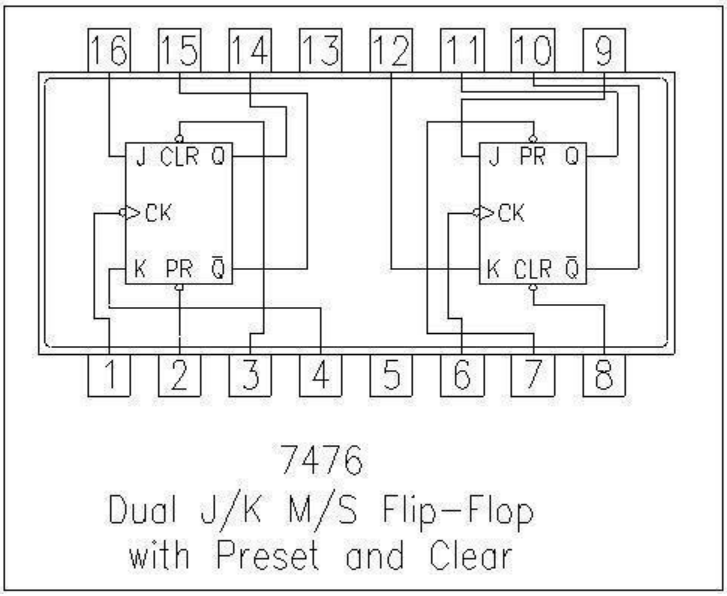


Figure 9.3: IC 74LS76

IC 7408 contains 4 AND gates in it. The pin configuration is shown below:

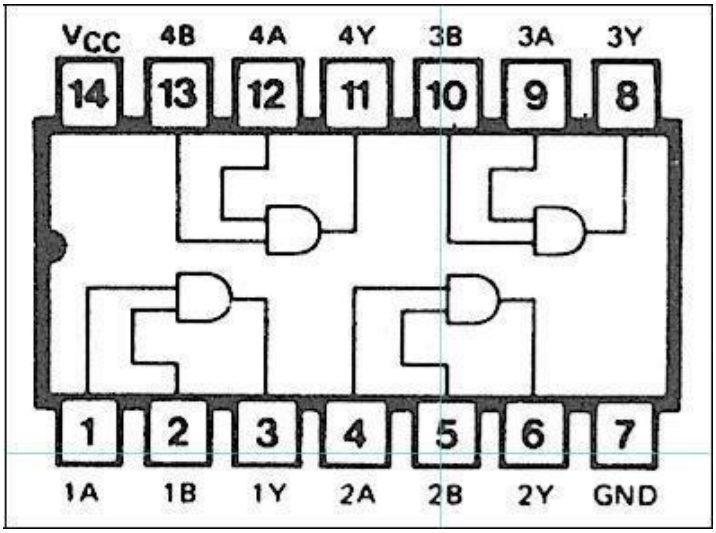
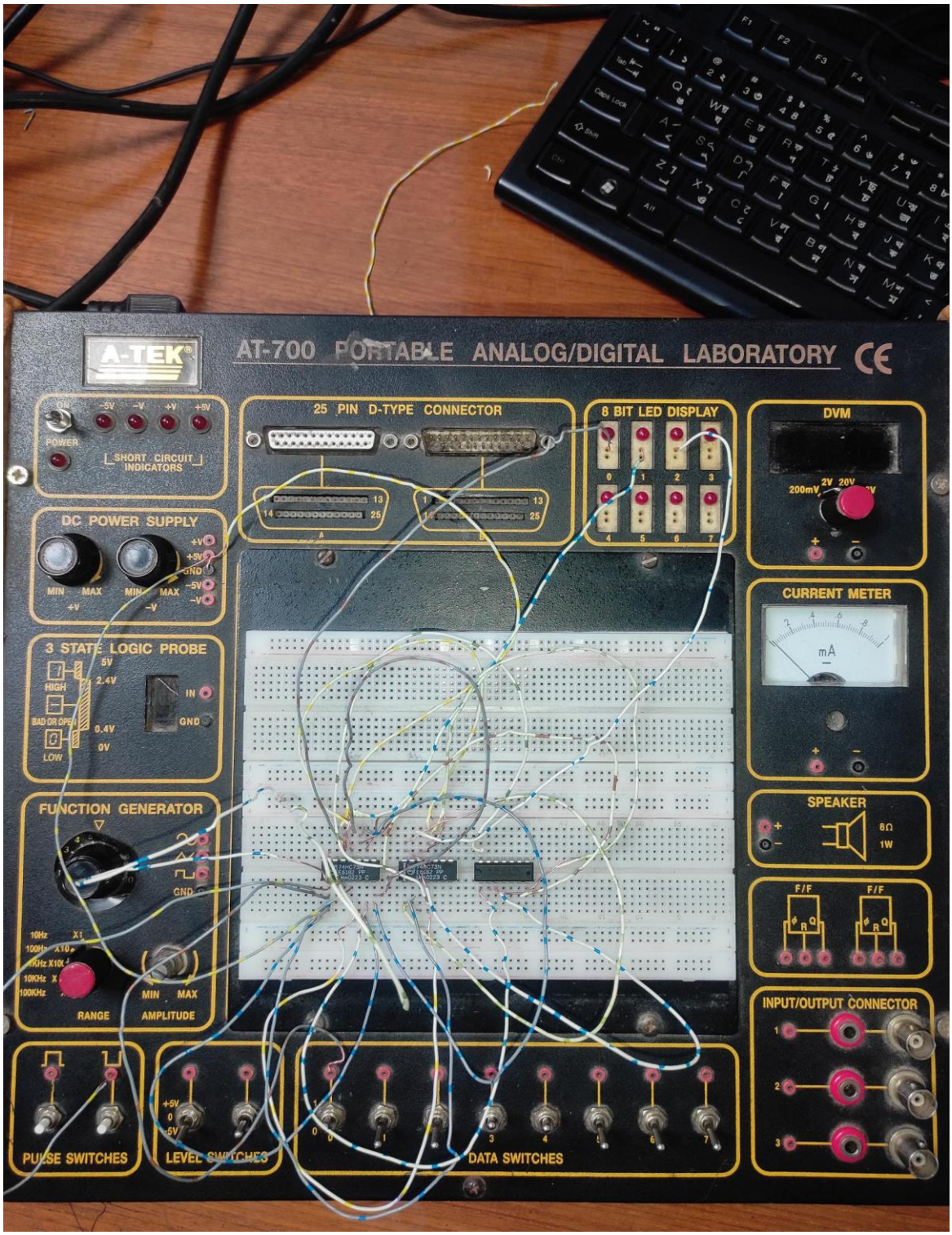


Figure 9.4: IC 7408.

Lab work:
3-Bit Asynchronous

3-bit Synchronous



Results & Simulations:

The resistor is connected with every Q' of J-K flip-flops to view in transient analysis.

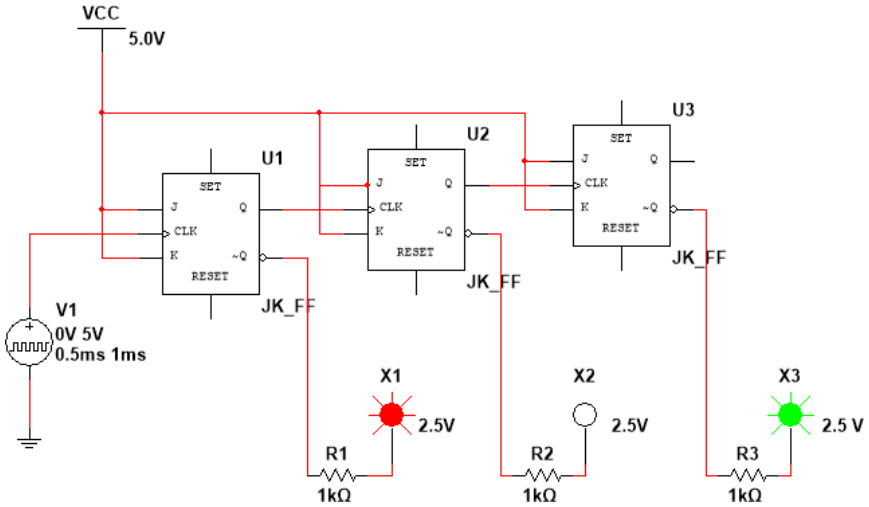


Fig : 3-bit Asynchronous Up-Counter.

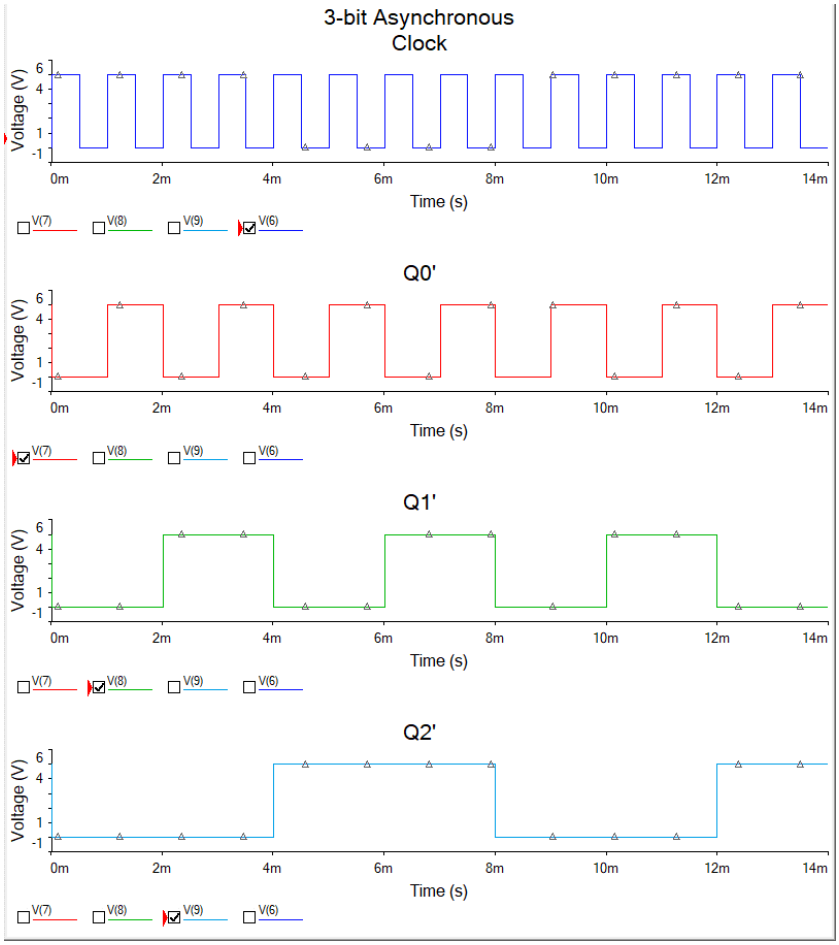


Fig: Transient Analysis of 3-bit Asynchronous Up-Counter.

Questions with answers :

1. Design a 4-bit Asynchronous UpCounter.

Ans :

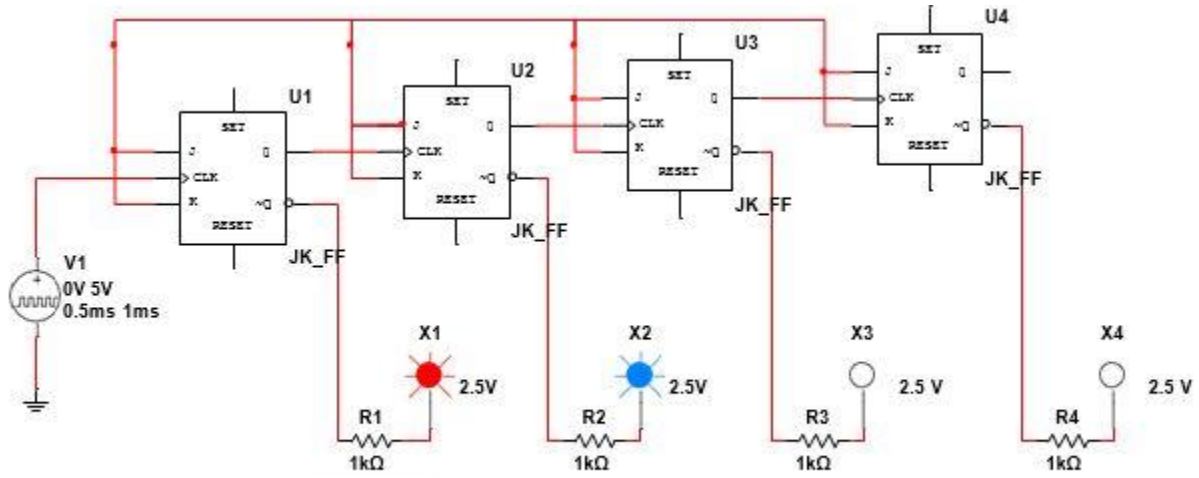


Fig: 4-bit Asynchronous Up-Counter.

2. Design a 4-bit Synchronous Up-Counter.

Ans:

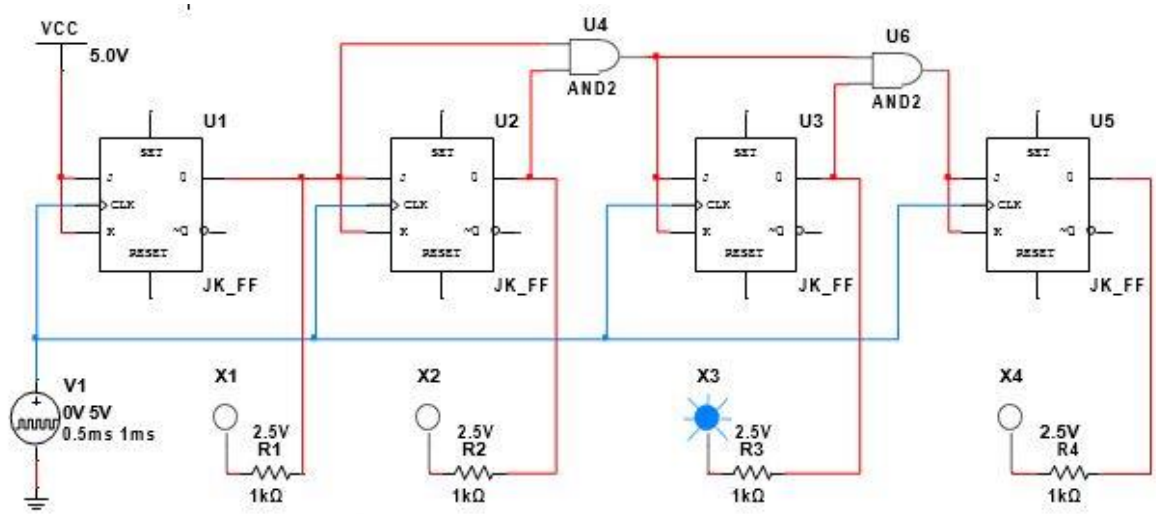


Fig: 4-bit Synchronous Up-Counter.

Discussion & Conclusion:

The main goal of this experiment is to use the J-K Flip-Flop to create synchronous and asynchronous counters. To simulate the diagram, we used the NI Multisim program. We have employed numerous tools. The JK flip-flop, the AND gate, LED lighting or displays, trainer boards, oscilloscopes, and connecting wires are among them. First, using NI Multisim software, we created a circuit diagram and tested it using an asynchronous counter. When the input was 1, the LED flickered and we displayed the number. We created a circuit diagram for a synchronous counter in the NI Multisim software and tested it. The LED switched on and off when the input was 1.