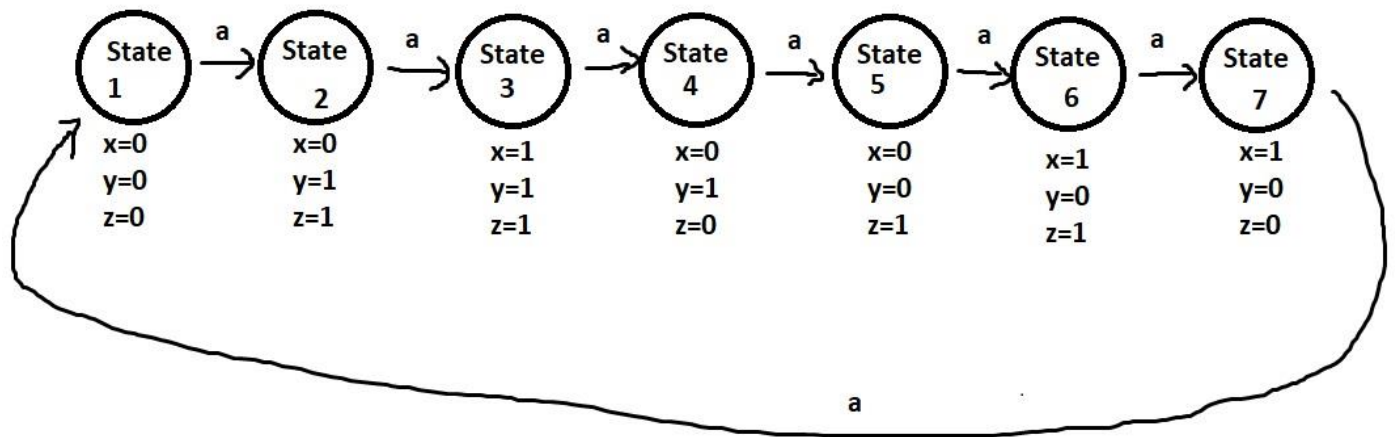


Step 1: Create FSM



Step 2: Obtain architecture:

- 7 States (3 bits register)
- 3 bits for coming states
- xyz is output
- a is input

Step 3: Encode states

	R2	R1	R0
State 1	0	0	0
State 2	0	1	1
State 3	1	1	1
State 4	0	1	0
State 5	0	0	1
State 6	1	0	1
State 7	1	0	0

Step 4: Generate state table:

→ Inputs: R2, R1, R0, a

→ Outputs: N2, N1, N0

→ The output xyz will be equal to R2,R1,R0 so they will not be on the truth table.

→ R2 = x

→ R1 = y

→ R0 = z

	R2	R1	R0	a		N2	N1	N0
State 1	0	0	0	0		0	0	0
	0	0	0	1		0	1	1
State 5	0	0	1	0		0	0	1
	0	0	1	1		1	0	1
State 4	0	1	0	0		0	1	0
	0	1	0	1		0	0	1
State 2	0	1	1	0		0	1	1
	0	1	1	1		1	1	1
State 7	1	0	0	0		1	0	0
	1	0	0	1		0	0	0
State 6	1	0	1	0		1	0	1
	1	0	1	1		1	0	0
Will not happen	1	1	0	0		x	x	X
	1	1	0	1		x	x	X
State 3	1	1	1	0		1	1	1
	1	1	1	1		0	1	0

Step 5: Obtain Boolean expressions and draw controller

Karnaugh Map for N2:

R0.a \ R2.R1	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	x	x	0	1
10	1	0	1	1

$$N2 = R2.a' + R2'.R0.a + R2.R1'.R0$$

Karnaugh Map for N1:

R0.a \ R2.R1	00	01	11	10
00	0	1	0	0
01	1	0	1	1
11	x	x	1	1
10	0	0	0	0

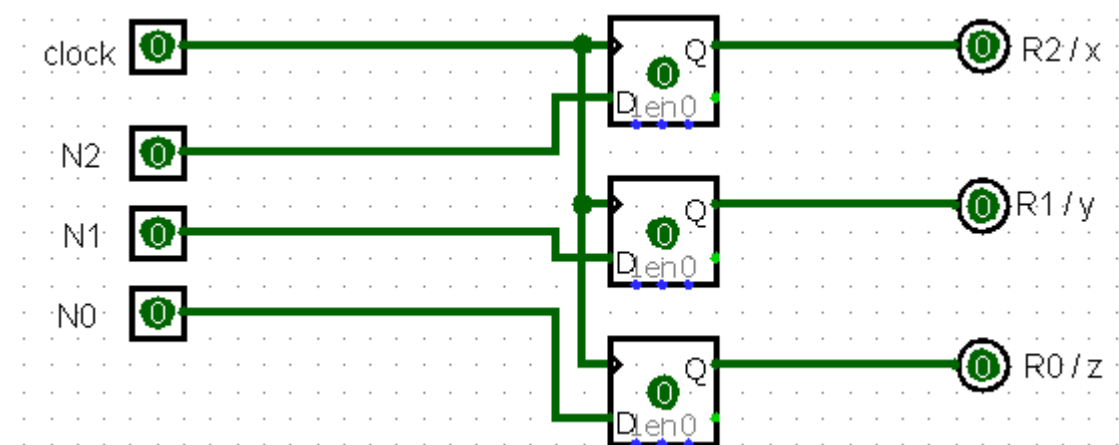
$$N1 = R1.R0 + R1.a' + R2'.R1'.R0'.a$$

Karnaugh Map for N0:

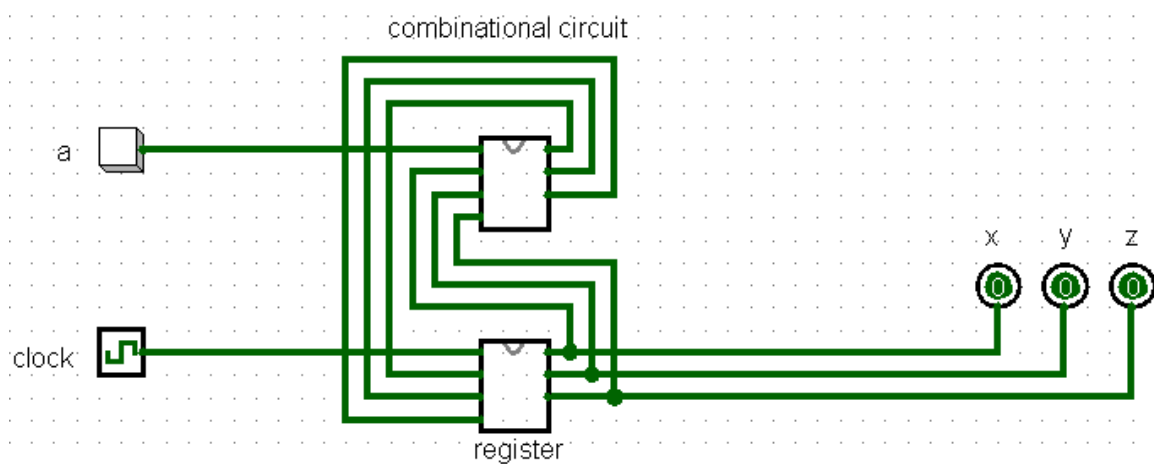
R0.a \ R2.R1	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	x	x	0	1
10	0	0	0	1

$$N0 = R2'.a + R2'.R0 + R0.a'$$

Register Part:



Entire circuit:



Combinational part:

