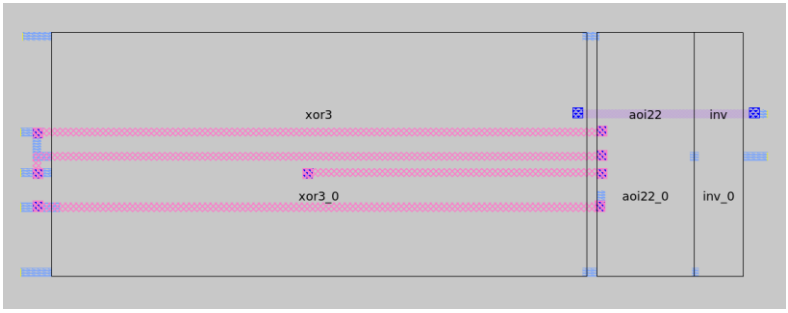
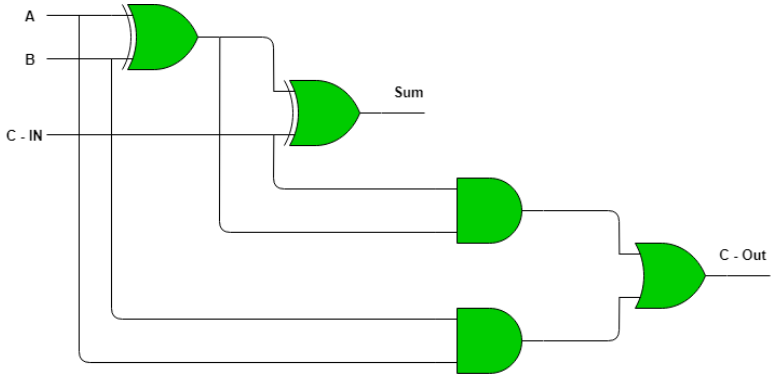
GTU Department of Computer Engineering
CSE 436/536– Fall 2022
Homework #3

Hasan Mutlu
1801042673

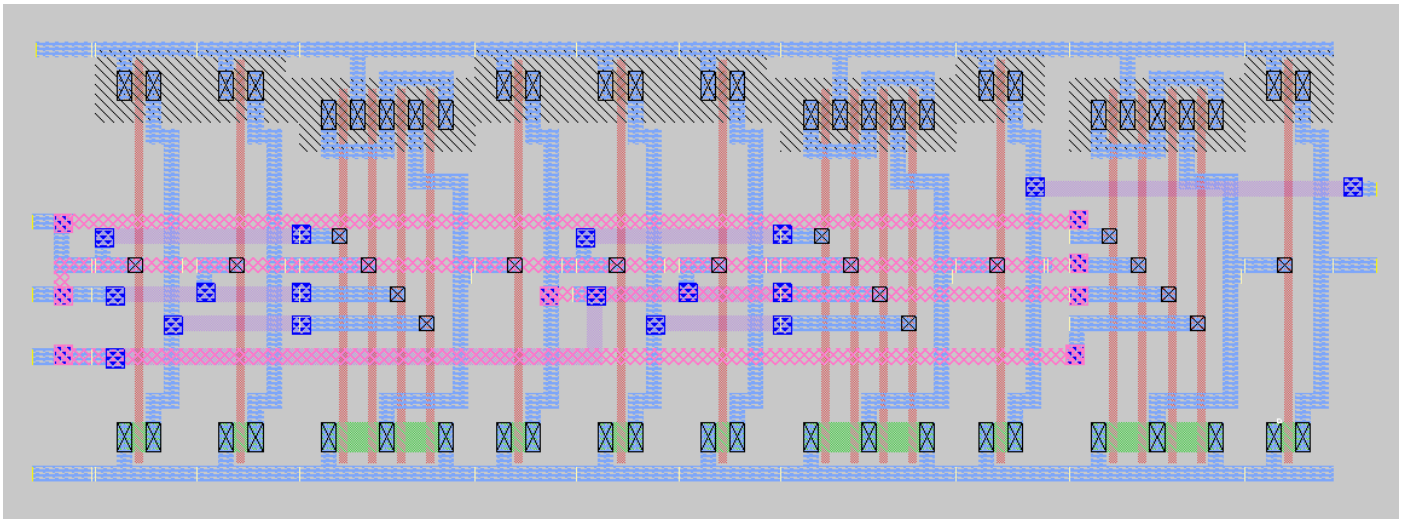
Full Adder Layout





The circuit contains three main standart cell library components. One XOR3 component for sum and one AOI22 and INV for the cout. These SCL components are designed again for this homework. The circuits logic schematic is as above.

The XOR3 is derived by using two XOR2 gates. XOR2 is derived by using two inverters for inputs, one AOI22 and another inverter to give the output.



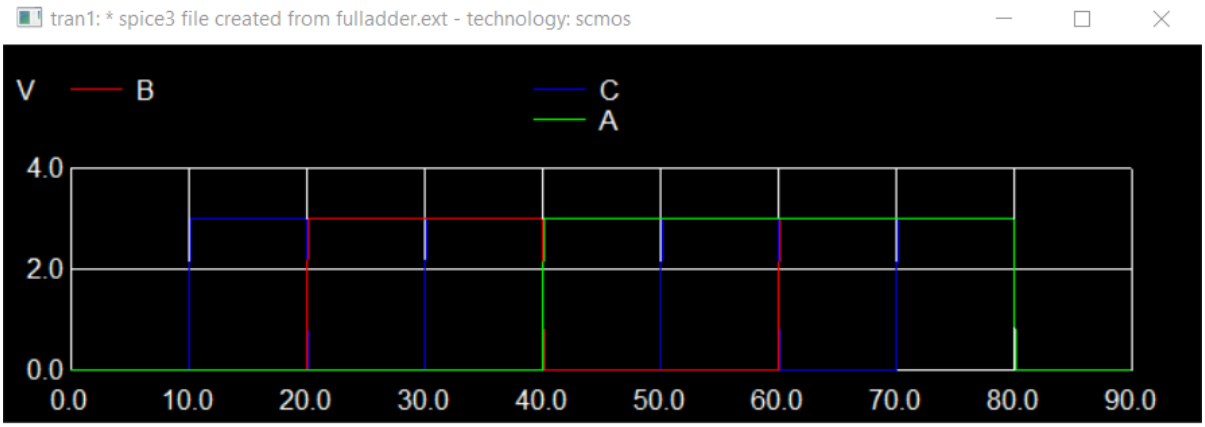
The final representation of the circuit. There are 36 transistors used in the design. 3 layers of metal are used.

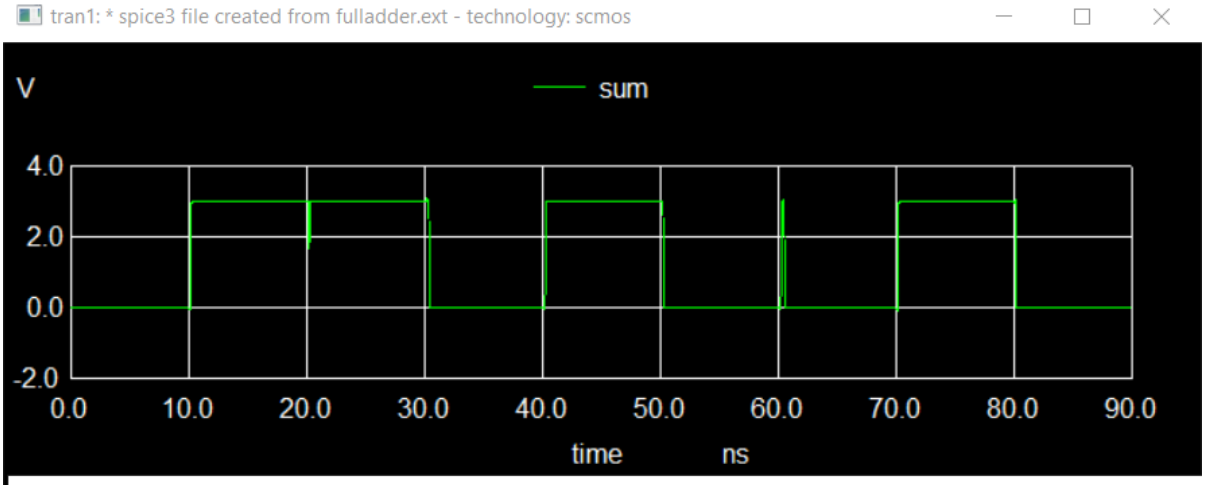
D Flip Flops could not be implemented.

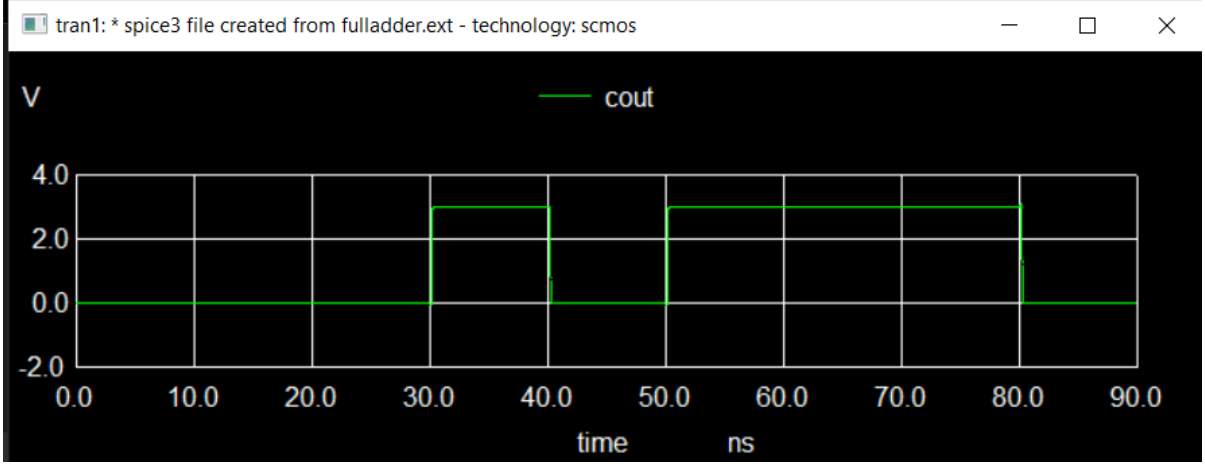
Truth Table of the Circuit

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simulation Results



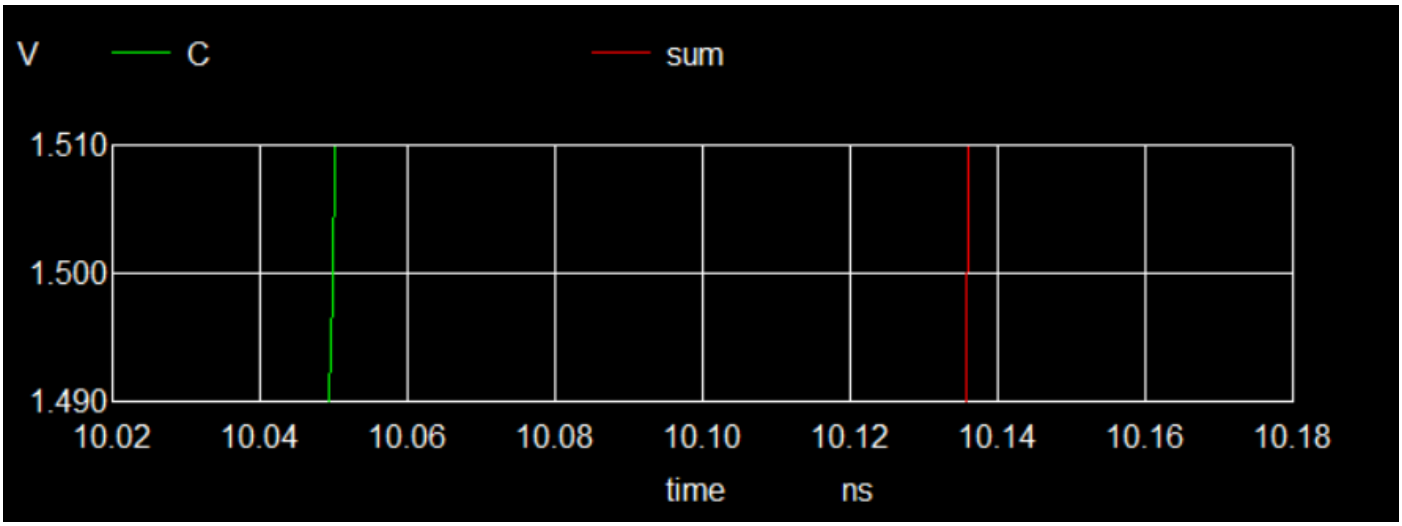




- ➔ VDD is 3 volts.
- ➔ The first graphic is input values. They change in every 10 nanoseconds, going from 000 to 111.
- ➔ Second and third graphics are sum and carry out outputs.

Delay Measurements

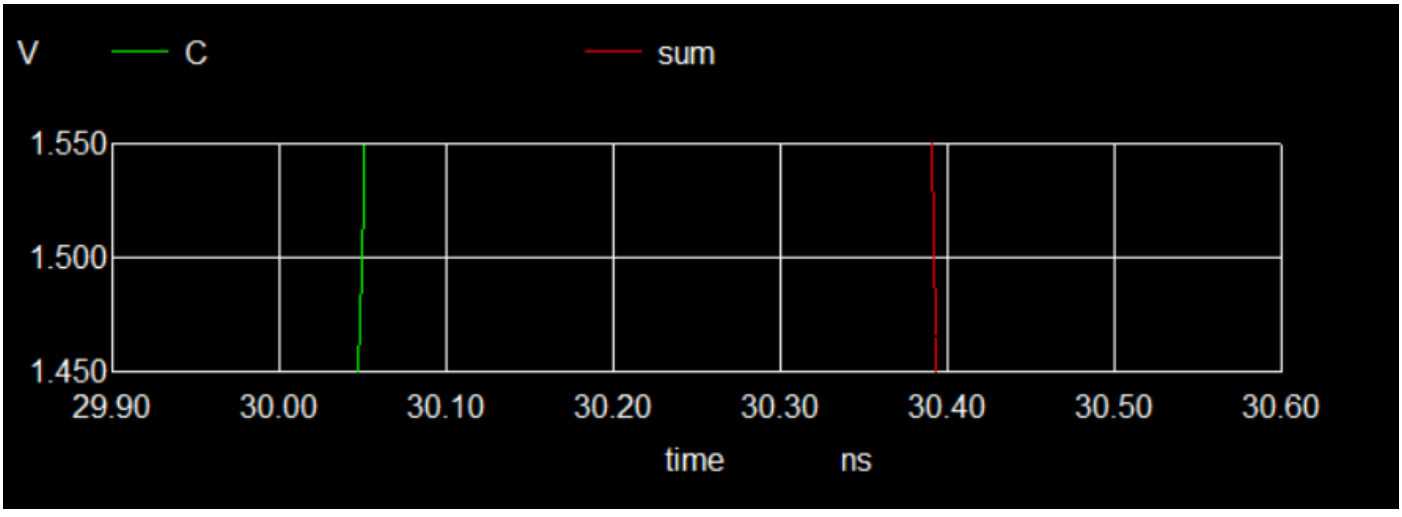
Sum Low to High Delay



x0 = 1.00501e-08, y0 = 1.49995 x1 = 1.01363e-08, y1 = 1.5

1.01363e-08 - 1.00501e-08 = 8.62e-11 = 86.2 picoseconds

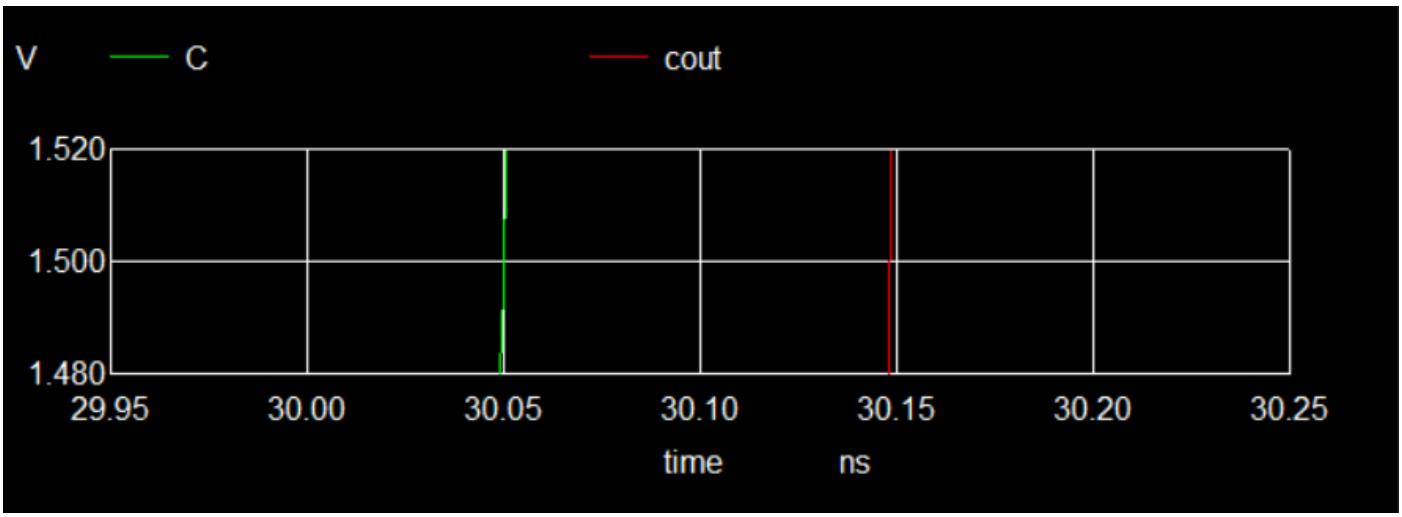
Sum High to Low Delay



x0 = 3.00494e-08, y0 = 1.5 x1 = 3.03918e-08, y1 = 1.5

3.03918e-08 - 3.00494e-08 = 3.424e-10 = 342 picoseconds

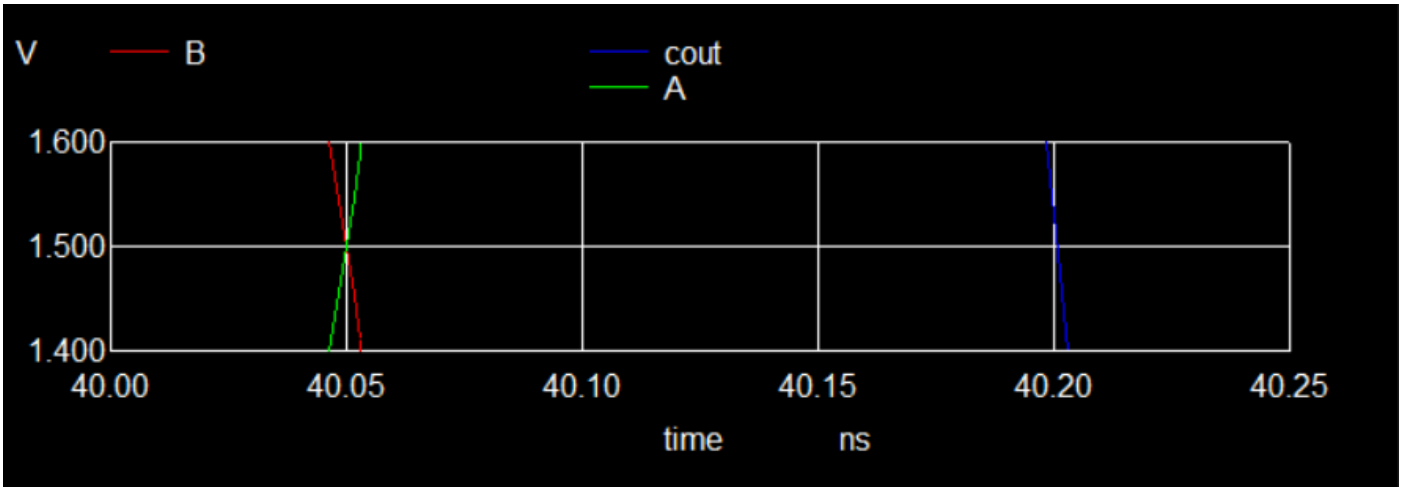
Carry Out Low to High Delay



x0 = 3.00505e-08, y0 = 1.50007 x1 = 3.01485e-08, y1 = 1.5

3.01485e-08 - 3.00505e-08 = 9.8e-11 = 98 picoseconds

Carry Out High to Low Delay



x0 = 4.005e-08, y0 = 1.49623 x1 = 4.02008e-08, y1 = 1.5

4.02008e-08 - 4.005e-08 = 1.508e-10 = 150 picoseconds