**CSE 433 Project 1**

**FSM with Logisim and Quartus**

**Due Date: 25/04/2023 17:00**

In this project, you will design an FSM using the below steps:

1. Design state diagram
2. Fill truth table
3. Construct simplified Boolean expressions from the truth table
4. Design and simulate using both Logisim and Quartus

You will design a seatbelt alert using the following sensors:

W: 1 if the weight on the copilot seat is higher than 20kg.

B: 1 if Belt is buckled up, 0 otherwise.

V: shows the speed as an 8 bit number.

R: 1 if reverse gear is used, 0 otherwise.

It will start sounding after all conditions are true and 1 minute has passed. The conditions are:

1. Speed is higher than 20 km/h
2. The belt is not buckled up.
3. Reverse gear is not used.
4. Copilot is in the car and he/she does not buckle up his/her seatbelt.

If the belt is taken off after being already buckled up while the above conditions are true, the alarm will start sounding without waiting.

The alert will sound with three different frequencies:

Once in each 3 seconds for the first 3 minutes, once in each 2 seconds if not buckled up for the next 2 minutes and once in each 1 second if not buckled up for the next 2 minutes. It will stop for 3 minutes if not buckled up, but will restart that loop after the end of 3 minutes if still not buckled.

Simulate the alarm with buzzer and LED.

Consider the best situation for starting the alarm and stopping it.

You will design your circuit both in Logisim and Quartus in Verilog. Do not use behavioral Verilog. Use the Boolean expressions you found from the truth table. Make simulation using Verilog testbench. Any design that does not base on sequential design will NOT BE ACCEPTED.