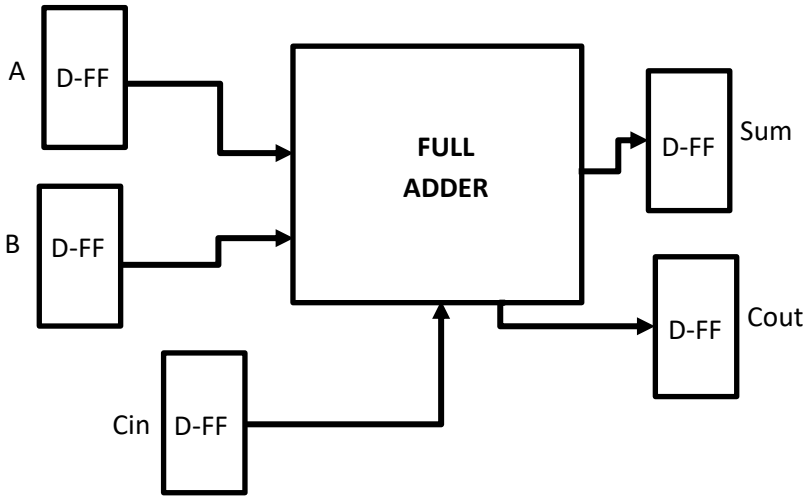
CSE 436/536

Digital Integrated Circuits

Assignment 3

Demo Date 16/12/2022 17:00

In this assignment, using Magic Layout Tool you will design a 0.25um TSMC process full adder cell using your standard cell libraries in the previous assignment.



- ✓ Use minimum area.
- ✓ Design in Magic using SCN5M_DEEP012 technology
- ✓ Convert to Spice.
- ✓ Simulate in Spice to verify the functionality. Test all possible inputs.
- ✓ Compute worst case circuit delay using Spice. use two vector tests for measuring delay.
- ✓ Put all results in a report as a zip file. Name your zip file as:

  StudentName_StudentSurname_StudentId_Assignment3.zip

Be careful in naming conventions.