Date: 01- 11-‘22

Experiment No. : 01

Experiment name: Display 0-9 by Using 8086 Microprocessor and 8255 Programmable Peripheral Interface.

Introduction :

The main objective of this experiment is to display 0-9 in a 7-segment display with the interfacing of 8086 microprocessor and 8255 programmable peripheral interfaces in the Proteus simulation platform.

8086 microprocessor :

8086 microprocessor communicates with 8255 programmable peripheral interfaces via 74HC373 latch to show output in 7 segment display. They are connected via the same data and address bus. The circuit will look like :

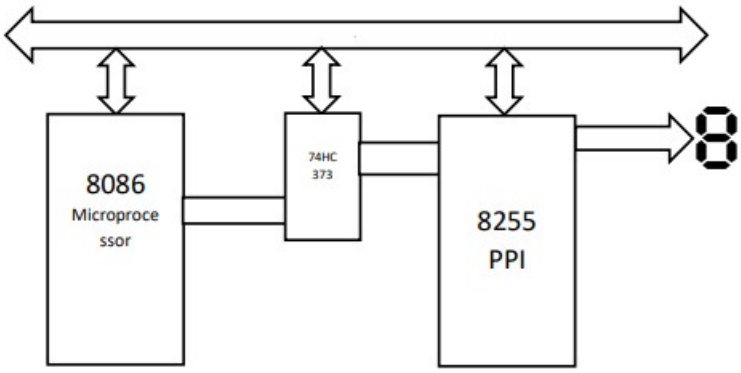


Figure 1: Block diagram of interfacing 7 segment display with 8086 microprocessors

he Intel 8086 is a 16-bit microprocessor that is intended to be used as the central processing unit (CPU) in a microcomputer. The term 16 bit implies that its internal registers, Arithmetic, and Logic Unit (ALU), and many of its instructions are designed to function with 16-bit binary data termed as a word. In the 8086 microprocessors mainly consists of a CPU, memory, and ports. These parts are connected by three buses namely the data bus, the address bus, and the control bus. The 8086 microprocessor possesses a 16-bit data bus, so it can read data from or write data to memory or ports that are either 16 bits or 8 bits at a time. It has a 20-bit address bus, so it can address any one of the 220 or 1048576 memory locations.

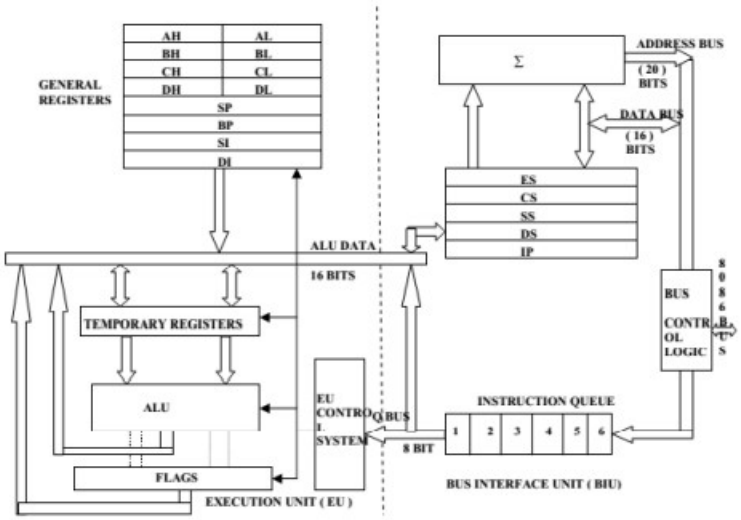


Figure 2: Block diagram of Intel 8086 microprocessor

The basic control bus consists of the signals labeled M/IO, RD, and WR. If the 8086 is doing a read from the memory or port, the RD will be asserted. If the 8086 is doing a write to memory or a port, the WR signal will be asserted. During a memory read or memory writes, the M/IO signal will be high and during port operations, the M/IO signal will be low. The salient feature of the 8086 CPU is that it is divided into two independent functional parts namely the Bus interface unit (BIU) and the Execution Unit (EU).

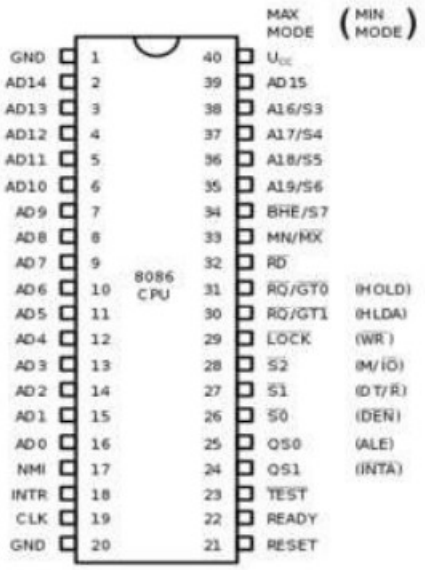


Figure 3 : Pin Diagram of 8086 micro processor.

Pins Descritiption :

1. **AD0-AD15 (Address Data Bus):** Bidirectional address/data lines. These are low order address bus. They are multiplexed with data. When these lines are used to transmit memory address, the symbol A is used instead of AD, for example, A0- A15.

2. **A16 - A19 (Output):** High order address lines. These are multiplexed with status signals.

3. **A16/S3, A17/S4:** A16 and A17 are multiplexed with segment identifier signals S3 and S4.

4. **A18/S5:** A18 is multiplexed with interrupt status S5.

5**. A19/S6:** A19 is multiplexed with status signal S6.

6. **BHE/S7 (Output):** Bus High Enable/Status. During T1, it is low. It enables the data onto the most significant half of data bus, D8-D15. 8-bit device connected to upper half of the data bus use BHE signal. It is multiplexed with status signal S7. S7 signal is available during T3 and T4.

7. **RD (Read):** For read operation. It is an output signal. It is active when low.

8. **Ready (Input):** The addressed memory or I/O sends acknowledgment through this pin. When HIGH, it denotes that the peripheral is ready to transfer data.

9. **RESET (Input):** System reset. The signal is active HIGH.

10. **CLK (input):** Clock 5, 8 or 10 MHz.

11. **INTR:** Interrupt Request.

12. **NMI (Input):** Non-maskable interrupt request.

13. **TEST (Input):** Wait for test control. When LOW the microprocessor continues execution otherwise waits.

14. **VCC:** Power supply +5V dc.

15. **GND:** Ground [1].

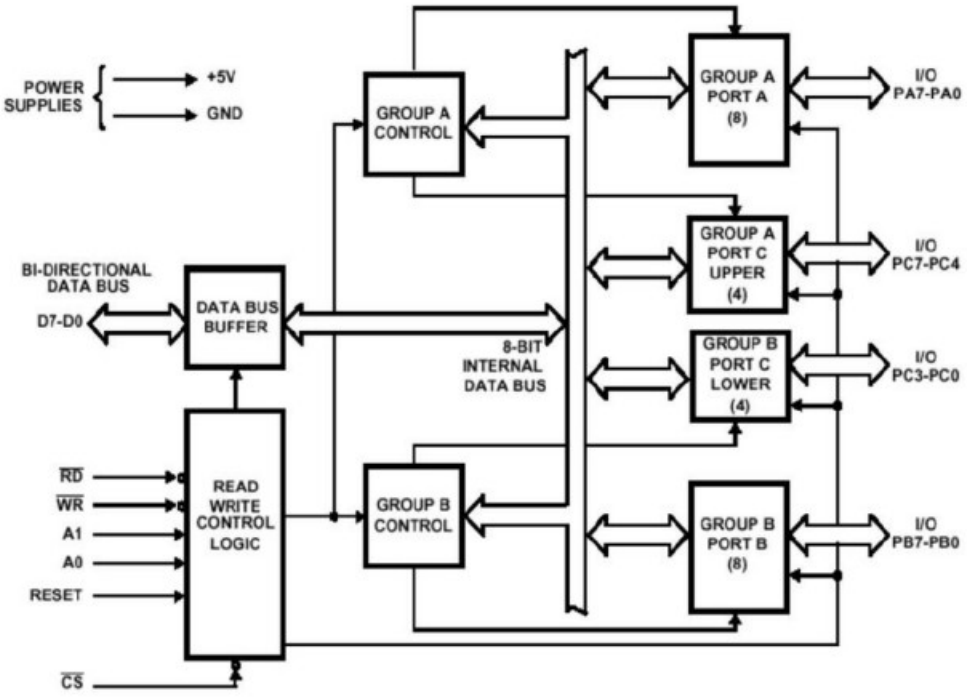


Figure 4: Basic Block diagram of 8255 peripheral device

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues command to both of the Control Groups.

(CS): - Chip Select. A “low" on this input pin enables the communication between the 8255 and the CPU.

(RD): - Read. A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

(**WR):** - Write. A "low" on this input pin enables the CPU to write data or control words into the 8255. (A0 and A1): -Port Select 0 and Port Select 1. These input

signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

(RESET): -Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. There are three basic modes of operation than can be selected by the system software:

- **Mode 0** - Basic Input/Output
- **Mode 1** - Strobed Input/Output
- **Mode 2** - Bi-directional Bus

For this experiment, 8255 will work on mode 0 which means basic input-output mode. It has two control groups; control group A and control group B. Control group A consists of port A and port C upper.

Control group B consists of port C lower and port B. Depending upon the value of CS', A1, and A0 it can be select different ports in different modes as an input-output function or BSR. This is done by writing a suitable word in the control register (control word D0-D7).

Depending upon the value of CS', A1, and A0 it can be select different ports in different modes as an input-output function or BSR. This is done by writing a suitable word in the control register (control word D0-D7). Port A, B, and C both can be used as either input or as output. It can be configured as that which port to use as input and output.

CS'	A1	A0	Port
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	Control Register
1	x	x	No Selection

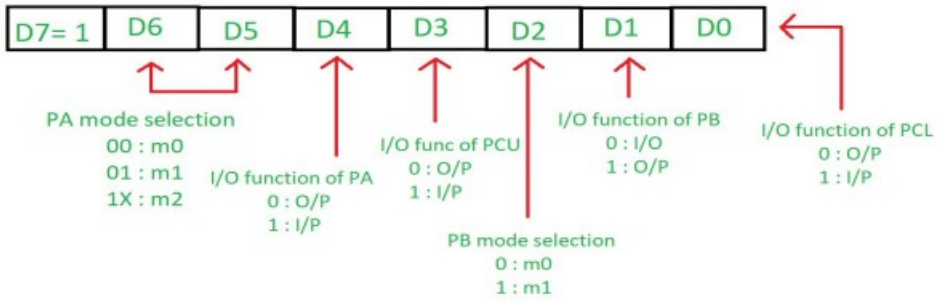


Figure 5 : Control register input-output mode

From figure the D7 value is 1 for use 8255 in I/O mode. D4 is the I/O function selection for port A. When D4 is 0 port A will work in output mode and when 1 port A will work in input mode. Similarly, if D1 is 0, port B will work in output mode, and if 1, port B will work in input mode. Port C is divided into two parts. The lower part of port C is controlled by D0 and the upper part of port C is controlled by D3. As 8255 is programmable, the values are set during programming.

Apparatus:

I. 8086up

II. 8255A PPI

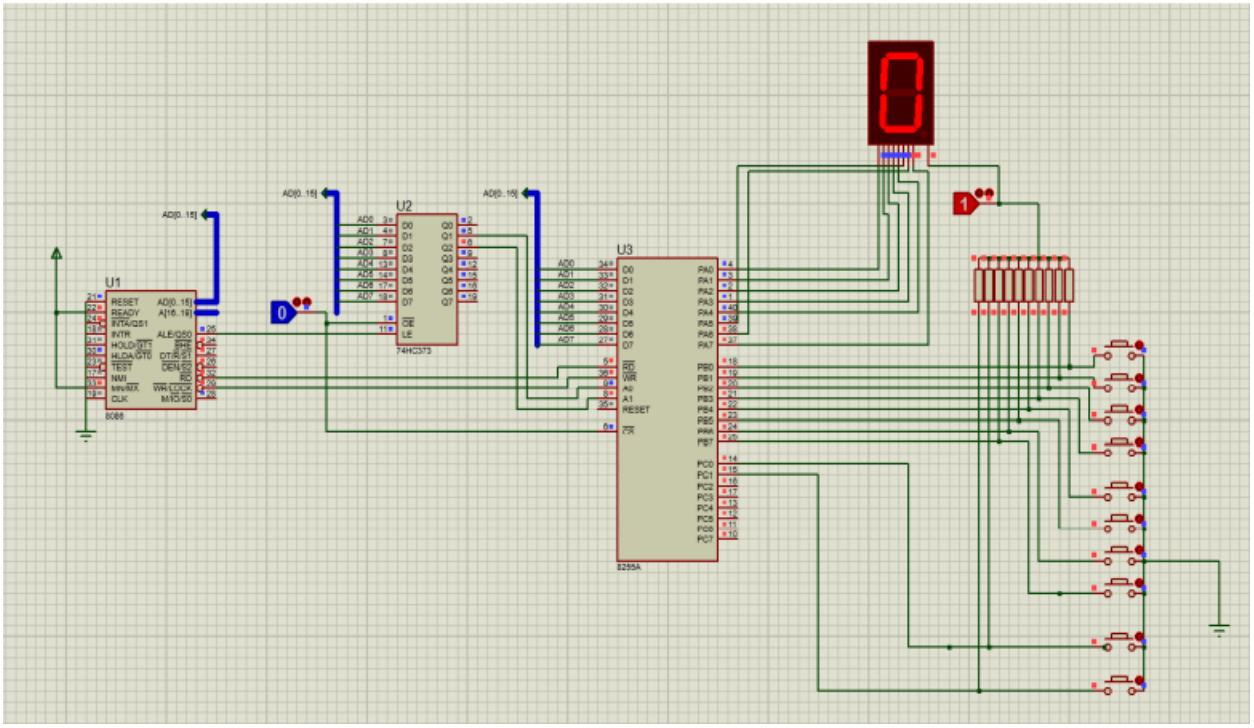
III. 74HC373

IV. Button

V. Logic gate

VI. Resistor

Module:



Code:

```
DATA SEGMENT
 PORTA EQU 00H
 PORTB EQU 02H
 PORTC EQU 04H
PORT_CON EQU 06H

CODE SEGMENT
 ORG 100H
 MOV DX, PORT_CON
MOV AL, 10001011B
 OUT DX, AL

MOV AL, 11000000B
MOV DX, PORTA
 OUT DX,AL

START:
MOV DX, PORTB
 IN AL, DX ;

MOV DX, PORTA
CMP AL, 11111110B

JZ S0
 CMP AL, 11111101B
 JZ S1
 CMP AL, 11111011B
 JZ S2
 CMP AL, 11110111B
 JZ S3
 CMP AL, 11101111B
 JZ S4
 CMP AL, 11011111B
 JZ S5
CMP AL, 10111111B
JZ S6
CMP AL, 01111111B
 JZ S7

MOV DX, PORTC
IN AL, DX

MOV DX, PORTA

CMP AL, 11111110B
 JZ S8
```

```
 CMP AL, 11111101B

Z S9
JMP START
 DISPLAY:
OUT DX,AL
 JMP START

S0:
MOV AL, 11000000B
JMP DISPLAY
 S1:

MOV AL, 11111001B
JMP DISPLAY
 S2:
MOV AL, 10100100B
 JMP DISPLAY
S3: MOV AL, 10110000B
 JMP DISPLAY
S4: MOV AL, 10011001B
JMP DISPLAY
 S5: MOV AL, 10010010B
 JMP DISPLAY
S6:

MOV AL, 10000010B
 JMP DISPLAY
 S7:
 MOV AL, 11111000B
JMP DISPLAY
 S8:
 MOV AL, 10000000B
 JMP DISPLAY
 S9:
 MOV AL, 10010000B
 JMP DISPLAY
 CODE
 ENDS END
```

Discussion :

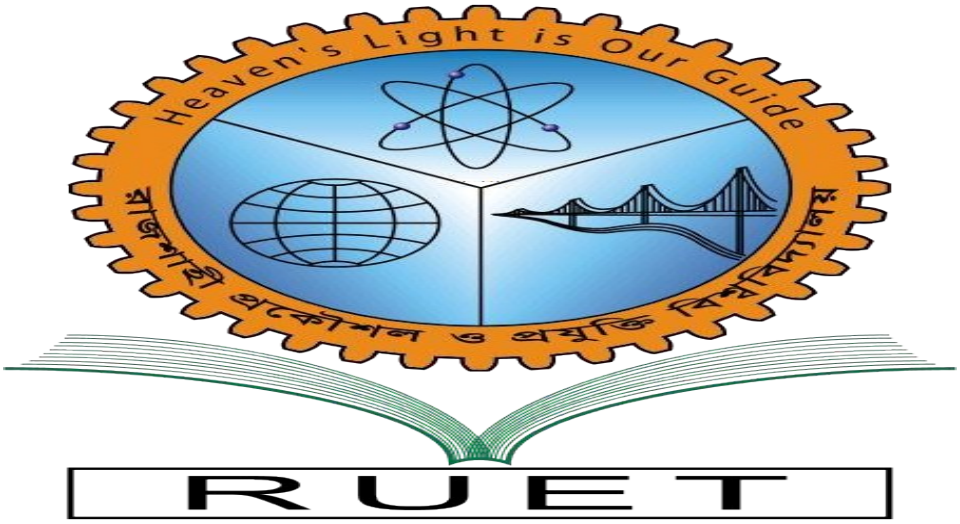
From the experiment we learnt the use of 8086 microprocessor. And we learnt the uses of pin of 8255. We learnt the working of the pins of the 8255 peripheral device. We successfully printed from 0 to 9 in 7 segment display. There was no error in the the code.

Referrence :

[1]2022.[Online].Available:http://eazynotes.com/notes/microprocessor/note s/block-diagram-of-intel-8086.pdf. [Accessed: 31- October- 2022].

[2] ULN2003;Wikipedia.2022.En.wikipedia.org.https://en.wikipedia.org/wi ki/ULN2003A [Accessed: 31-october-2022].

3] Interfacing Stepper Motor to 8086 using 8255. 2022. Jntuimplab.blogspot.com.http://jntuimplab.blogspot.com/2008/01/interfa cing-stepper-motor-to-8086-using.html [Acessed: 31 - October -2022.



Department of Electrical & Computer Engineering

Course No: ECE 3212

Course Title: Peripheral and Interfacing Sessional

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