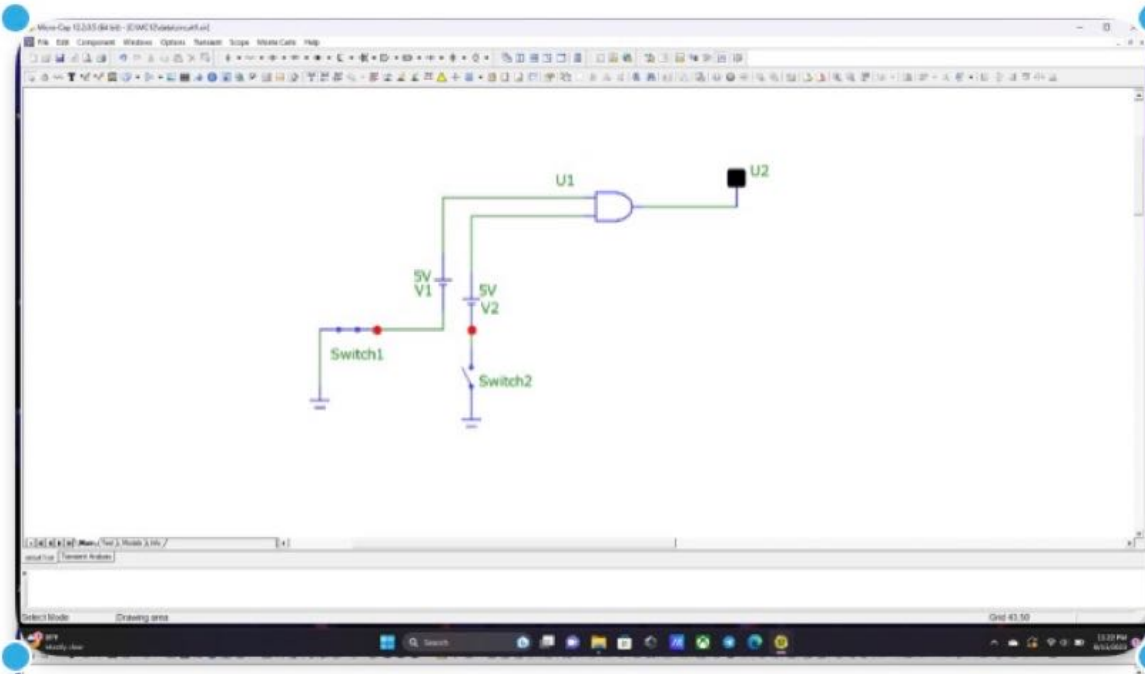
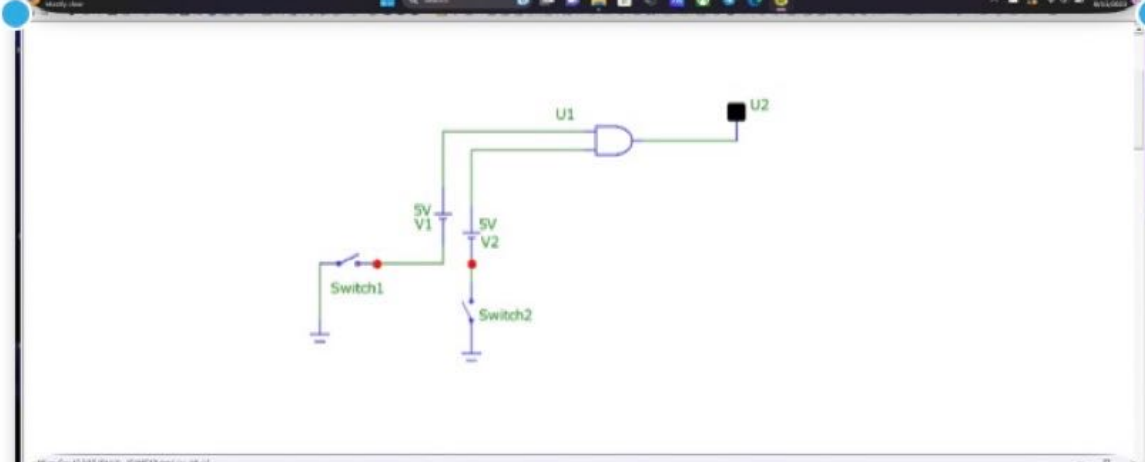
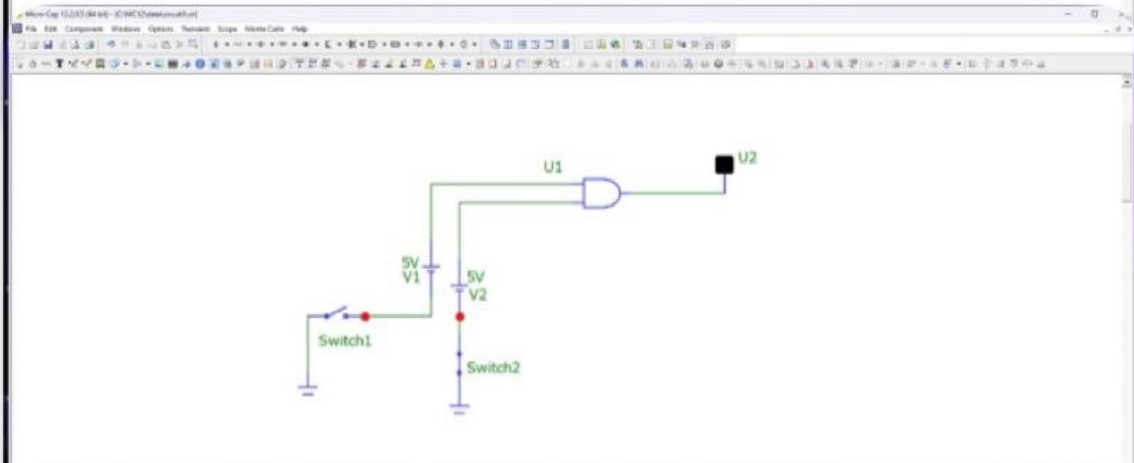
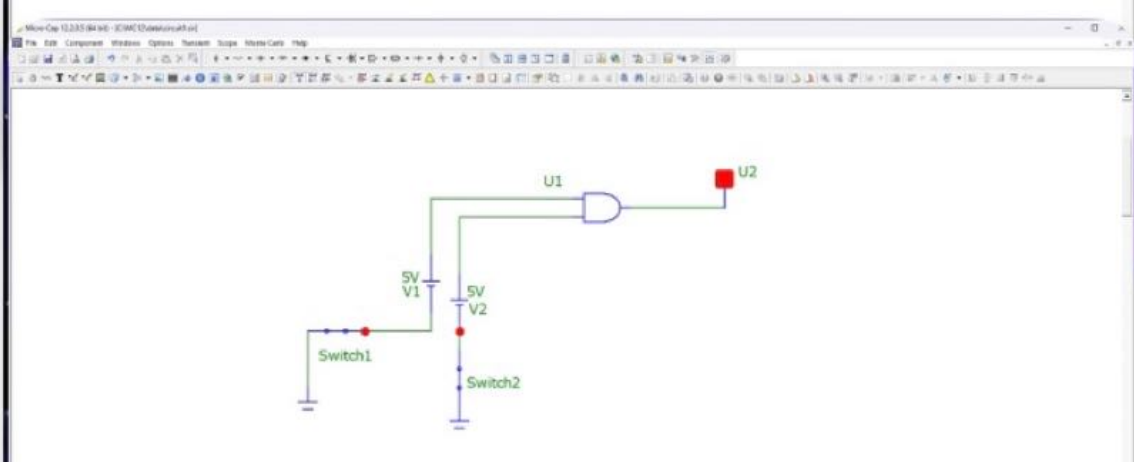
AND gate

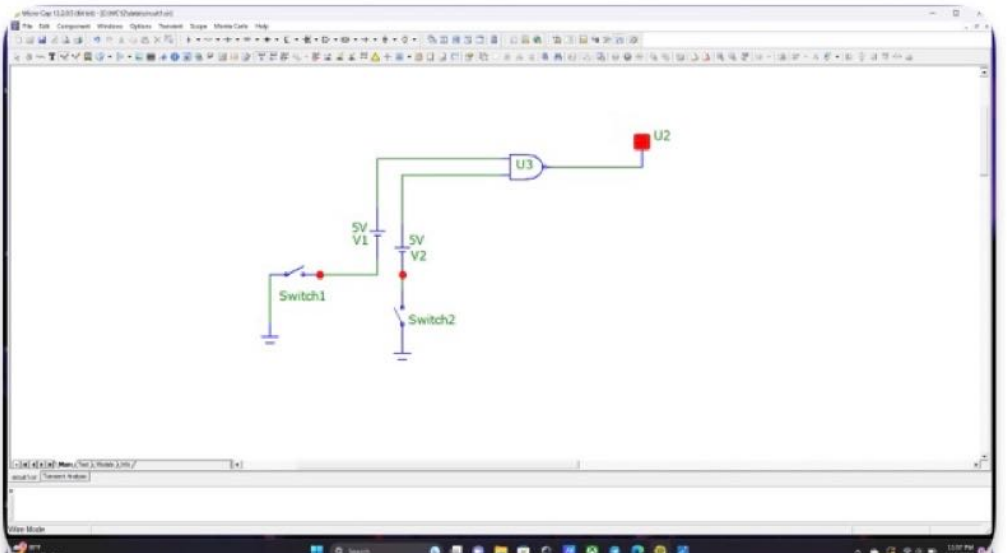

U1
U2
5V
V1
5V
V2
Switch1
Switch2

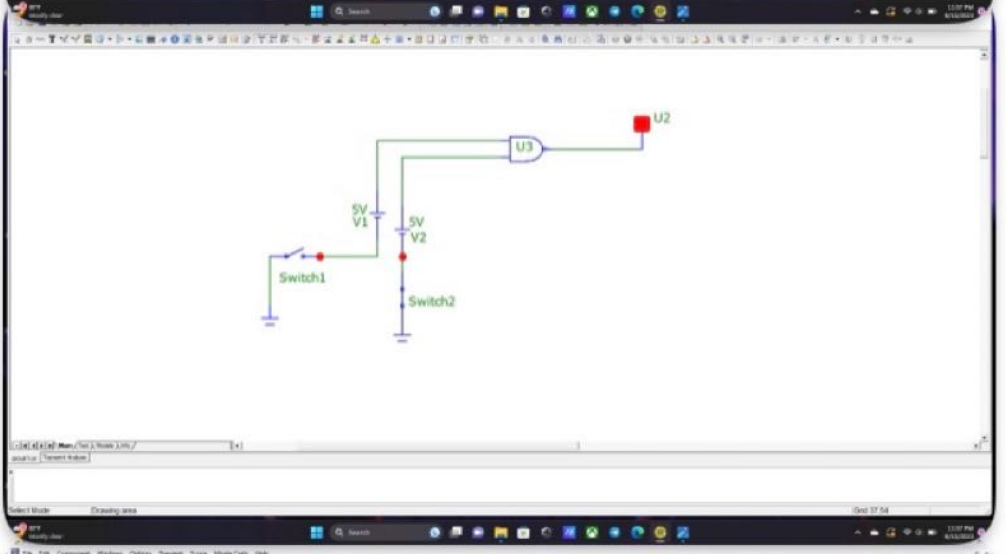

U1
U2
5V
V1
5V
V2
Switch1
Switch2

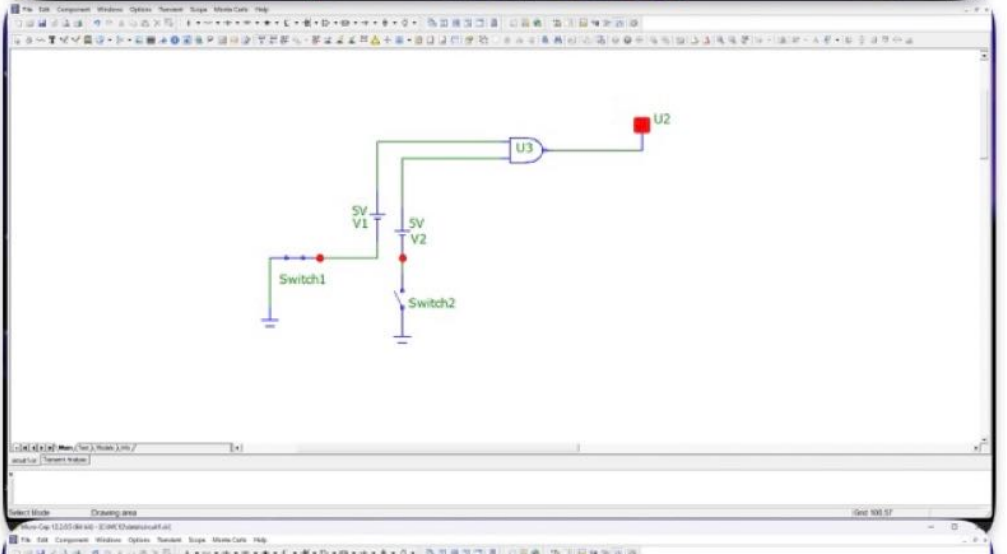

U1
U2
5V
V1
5V
V2
Switch1
Switch2

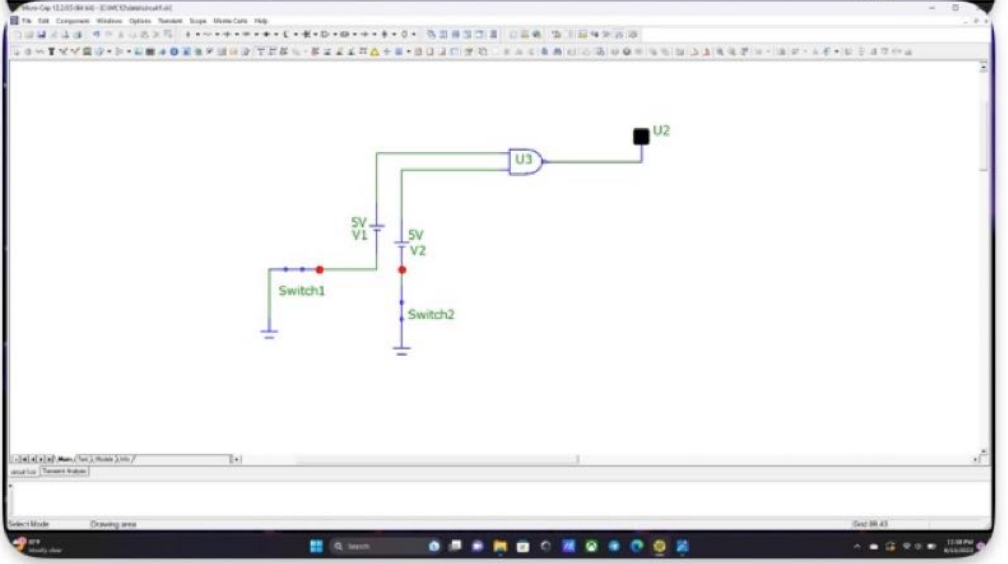

U1
U2
5V
V1
5V
V2
Switch1
Switch2

NAND

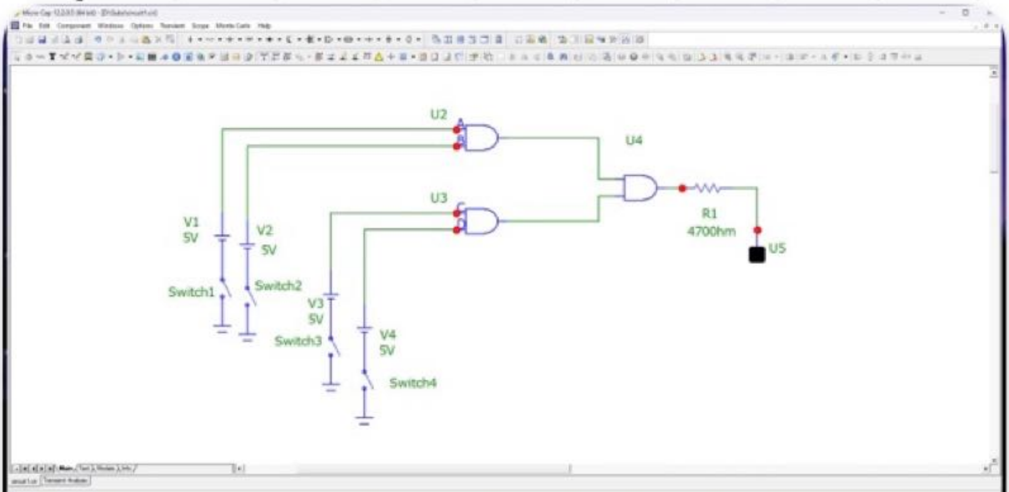

U2
U3
5V
V1
5V
V2
Switch1
Switch2

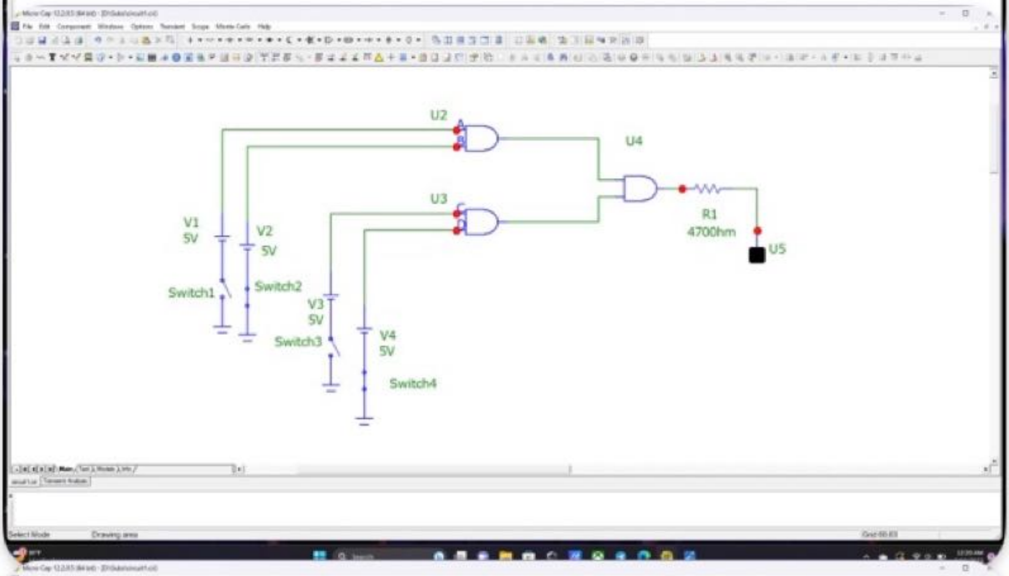

U2
U3
5V
V1
5V
V2
Switch1
Switch2

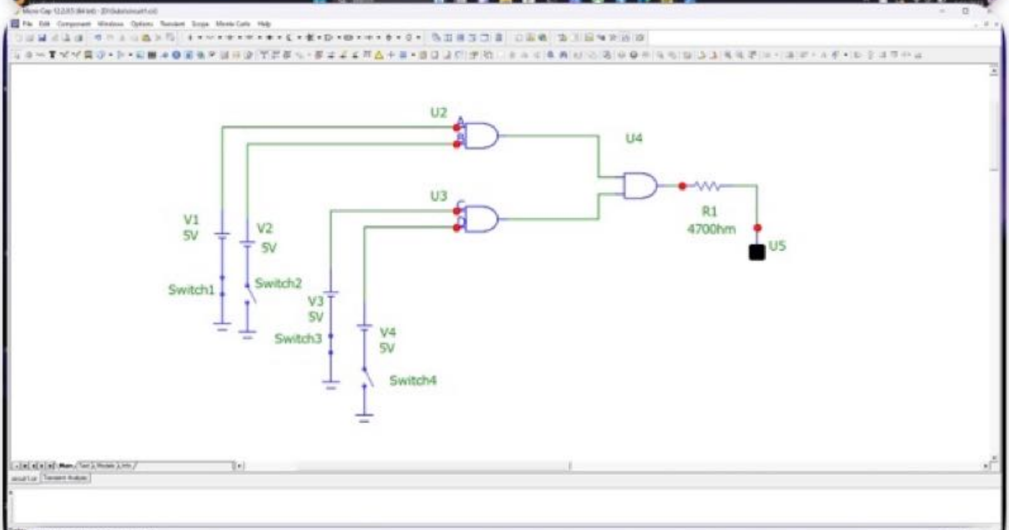

U2
U3
5V
V1
5V
V2
Switch1
Switch2

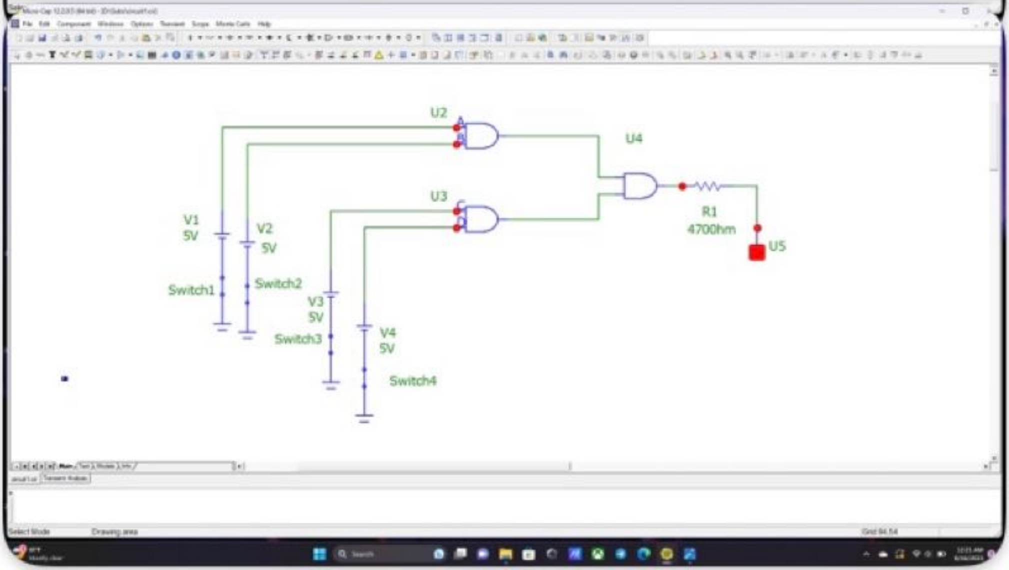

U2
U3
5V
V1
5V
V2
Switch1
Switch2

A part


U2
U3
U4
V1
5V
V2
5V
V3
5V
V4
5V
Switch1
Switch2
Switch3
Switch4
R1
4700hm
U5


U2
U3
U4
V1
5V
V2
5V
V3
5V
V4
5V
Switch1
Switch2
Switch3
Switch4
R1
4700hm
U5


U2
U3
U4
V1
5V
V2
5V
V3
5V
V4
5V
Switch1
Switch2
Switch3
Switch4
R1
4700hm
U5


U2
U3
U4
V1
5V
V2
5V
V3
5V
V4
5V
Switch1
Switch2
Switch3
Switch4
R1
4700hm
U5

Experiment 1

Part (A)

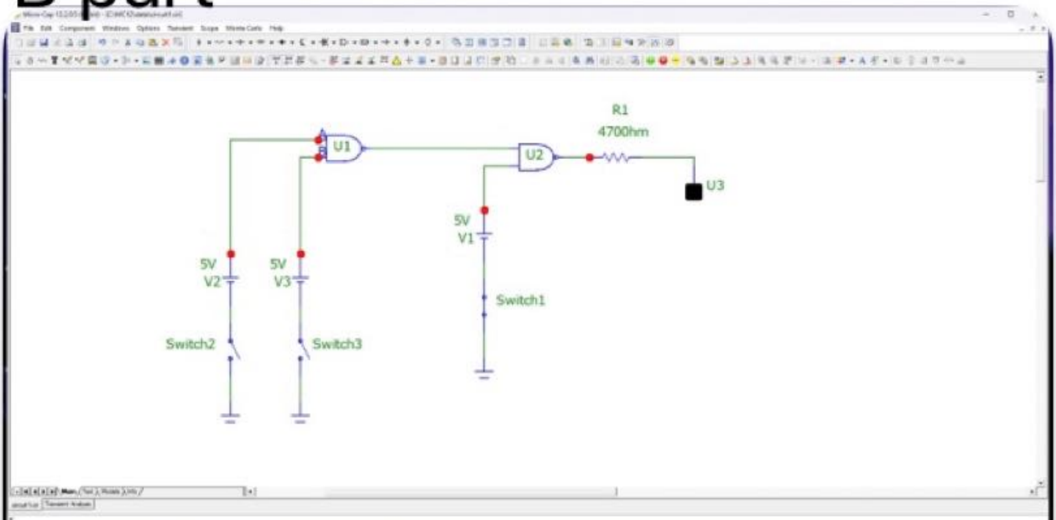
A	B	C	D	Q_1
0	0	0	0	0
0	1	0	1	0
1	0	1	0	0
1	1	1	1	1

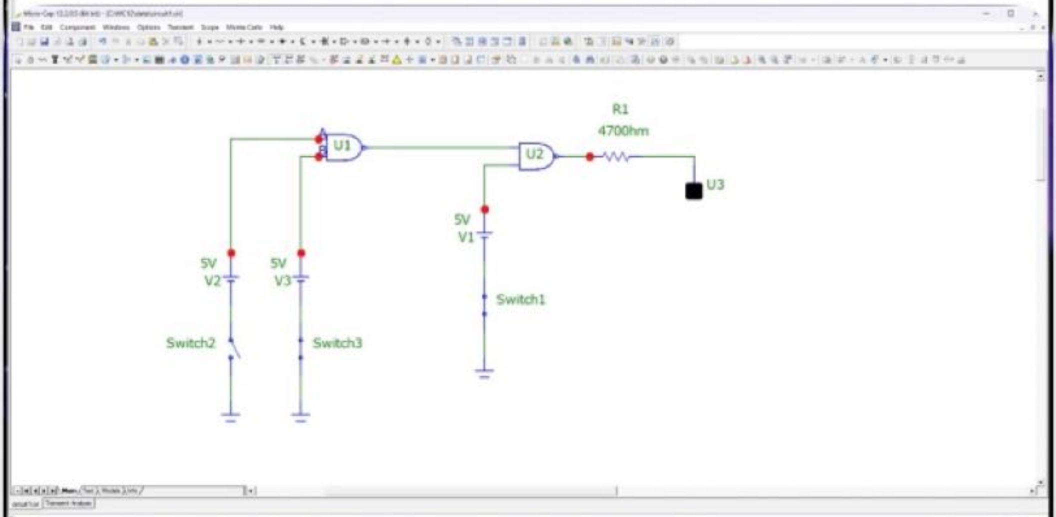
① $Q_1 = (A \cdot B) \cdot (C \cdot D)$

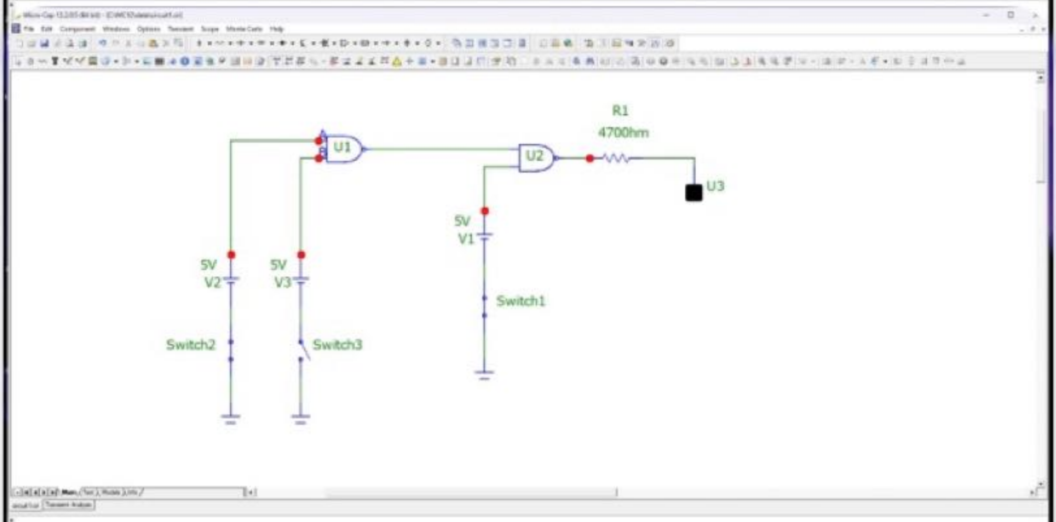
② q_1 is 1, only when
inputs are 1
q_1 is not 1, If one of
the inputs is 0

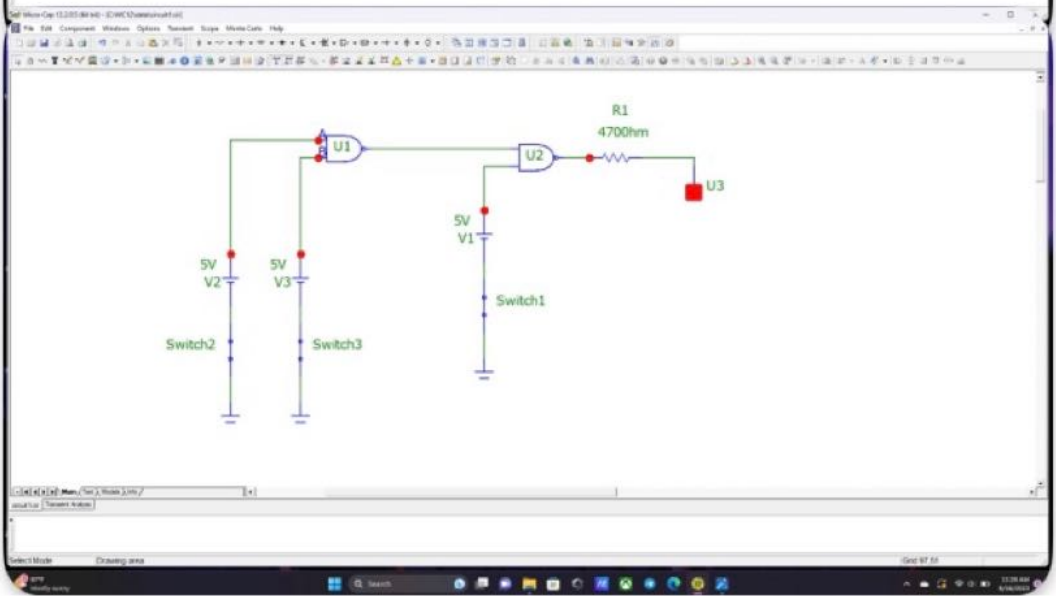
③ 16 combinations

B part


R1
4700hm
U1
U2
U3
5V
V1
5V
V2
5V
V3
Switch1
Switch2
Switch3


R1
4700hm
U1
U2
U3
5V
V1
5V
V2
5V
V3
Switch1
Switch2
Switch3


R1
4700hm
U1
U2
U3
5V
V1
5V
V2
5V
V3
Switch1
Switch2
Switch3


R1
4700hm
U1
U2
U3
5V
V1
5V
V2
5V
V3
Switch1
Switch2
Switch3

Part (B)

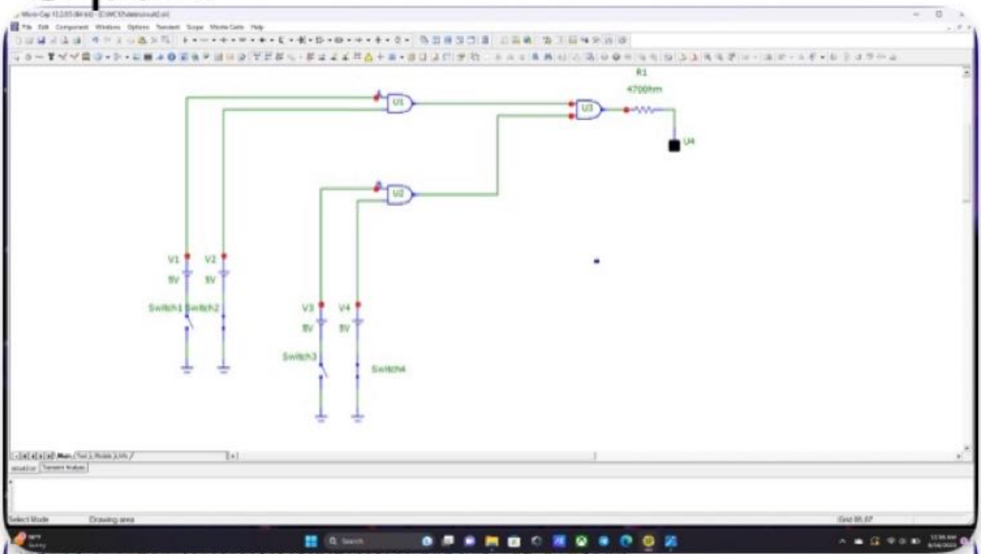
Q1

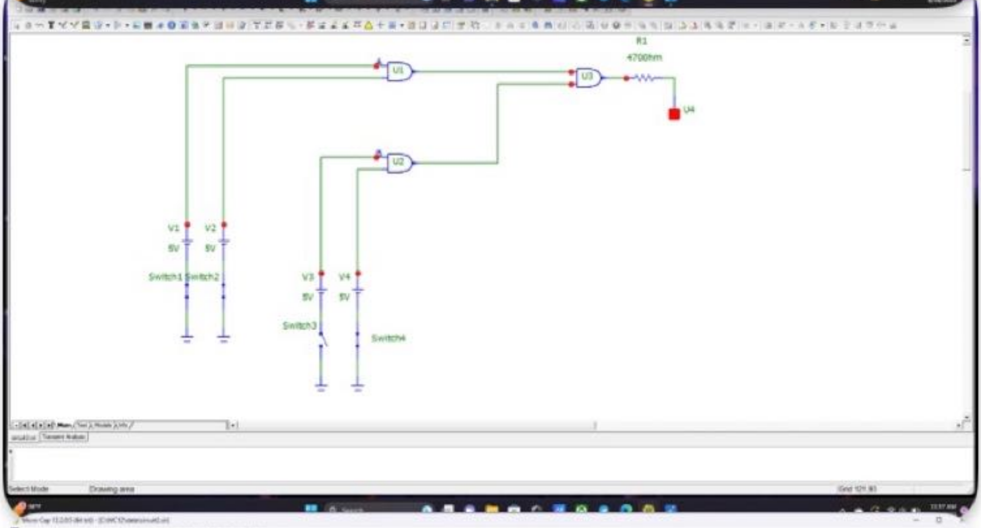
A	B	Q_1
0	0	0
0	1	0
1	0	0
1	1	1

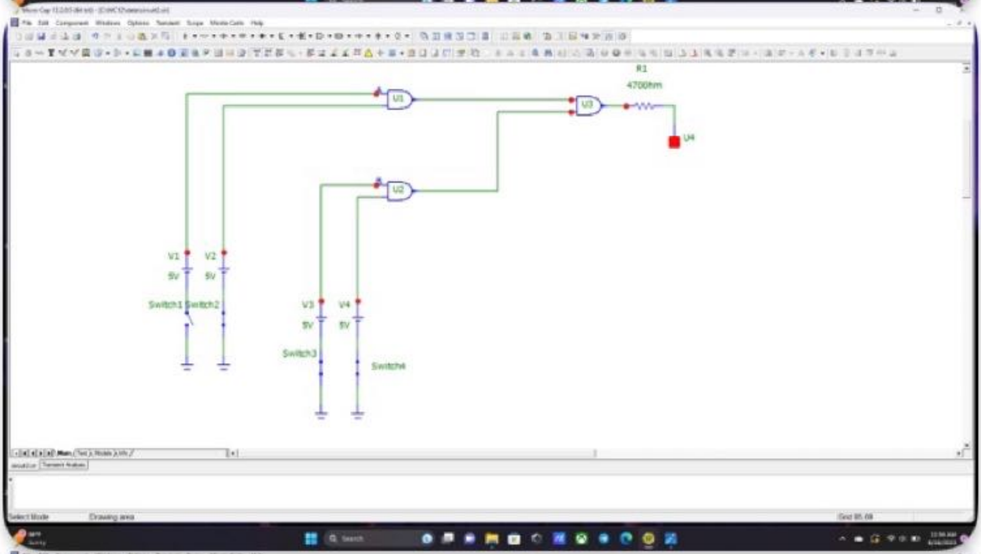
(a) $Q_1 = A \cdot B$

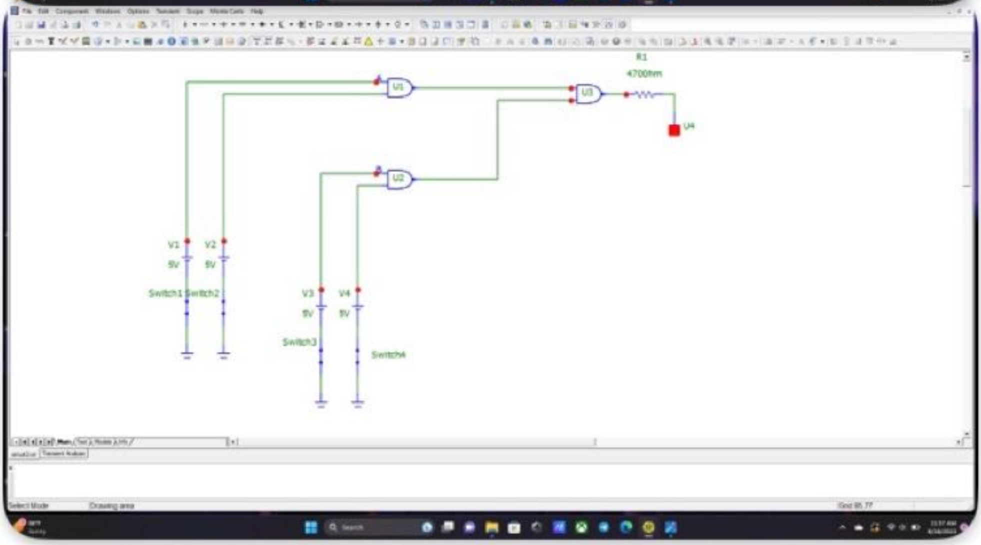
(b) A Logical And operation

C part


U1
U2
U3
R1
470Ohm
U4
V1
V2
5V
5V
Switch1
Switch2
V3
V4
5V
5V
Switch3
Switch4


U1
U2
U3
R1
470Ohm
U4
V1
V2
5V
5V
Switch1
Switch2
V3
V4
5V
5V
Switch3
Switch4


U1
U2
U3
R1
470Ohm
U4
V1
V2
5V
5V
Switch1
Switch2
V3
V4
5V
5V
Switch3
Switch4


U1
U2
U3
R1
470Ohm
U4
V1
V2
5V
5V
Switch1
Switch2
V3
V4
5V
5V
Switch3
Switch4

Part (c)

(a)

A	B	Q_1
0	0	0
0	1	1
1	0	1
1	1	1

a) $Q_1 = A + B$

b) A logical or operation