CS-223
Digital Design
Section: 3
PROJECT REPORT
Programmable Processor

Mehmet Hasat Serinkan
21901649
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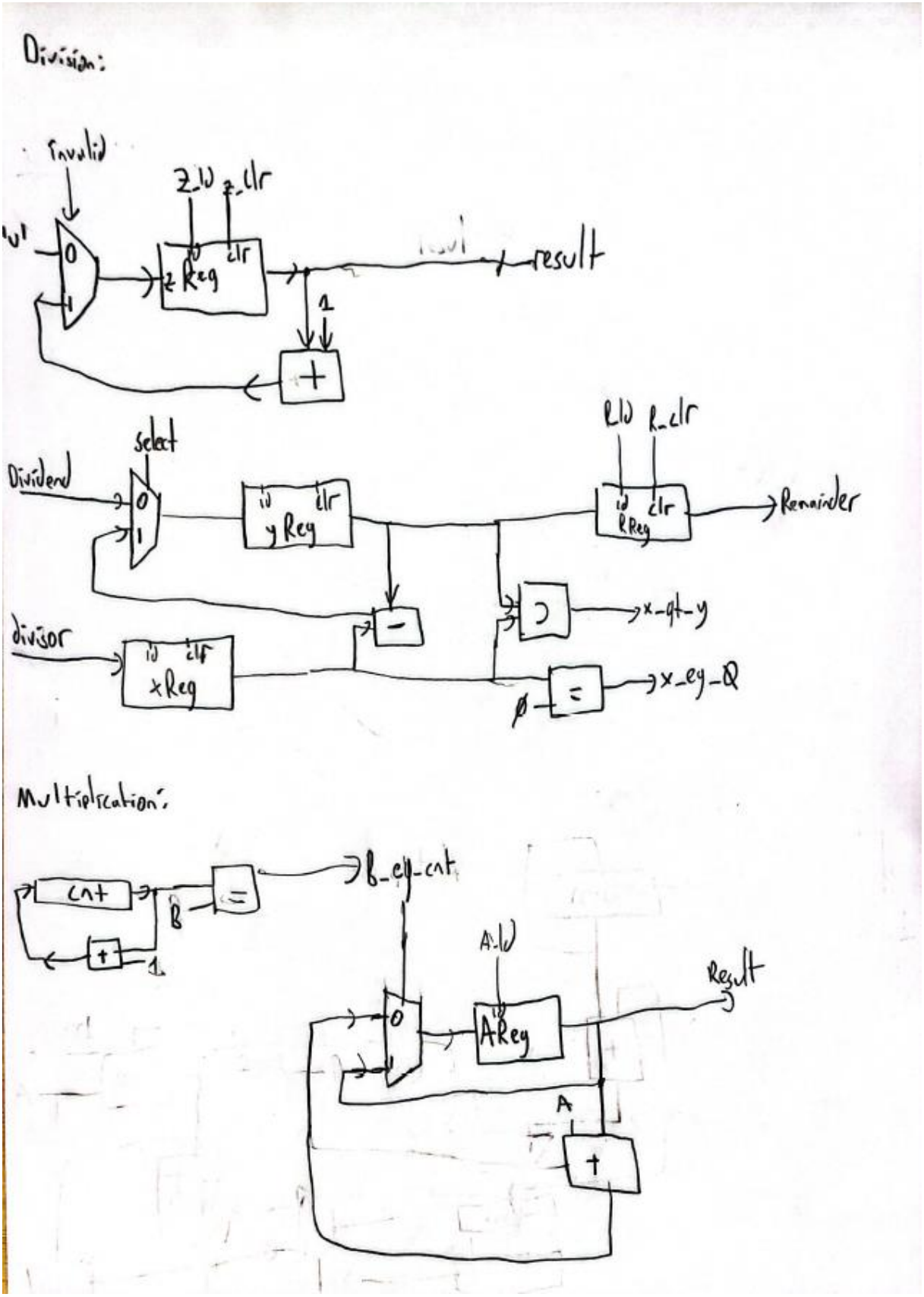
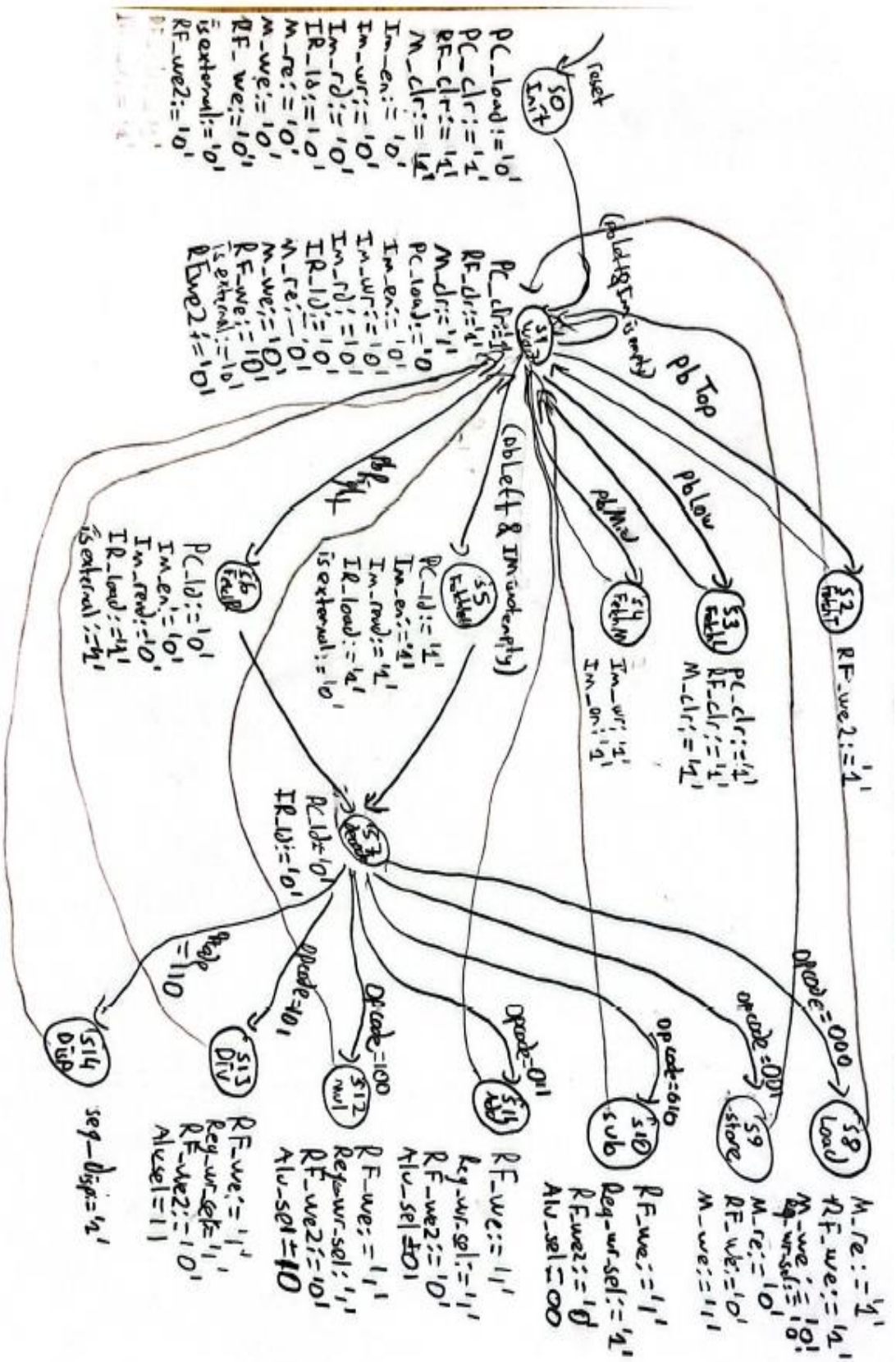
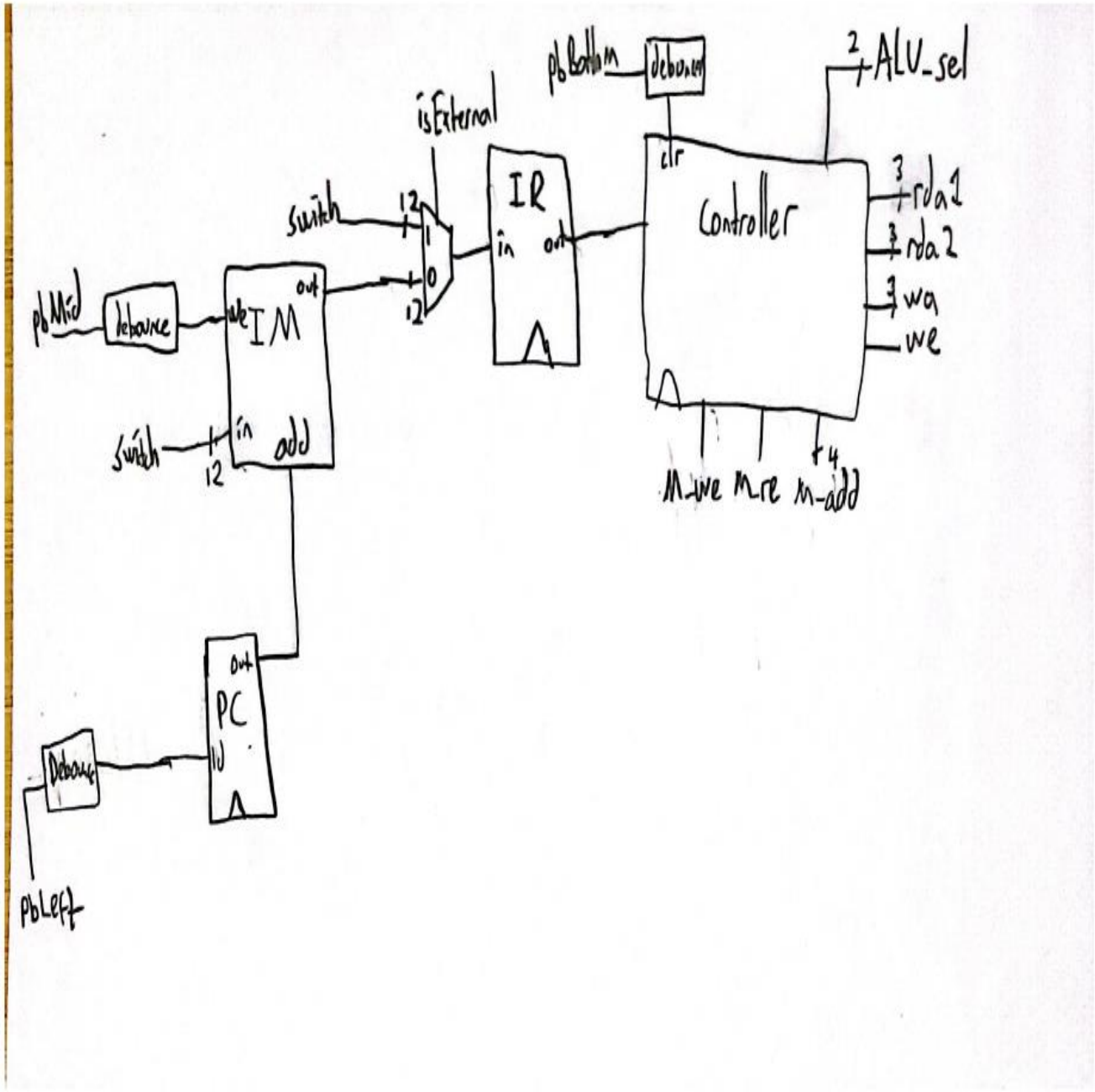
B) RTL schematics for Multiplication and Division operations



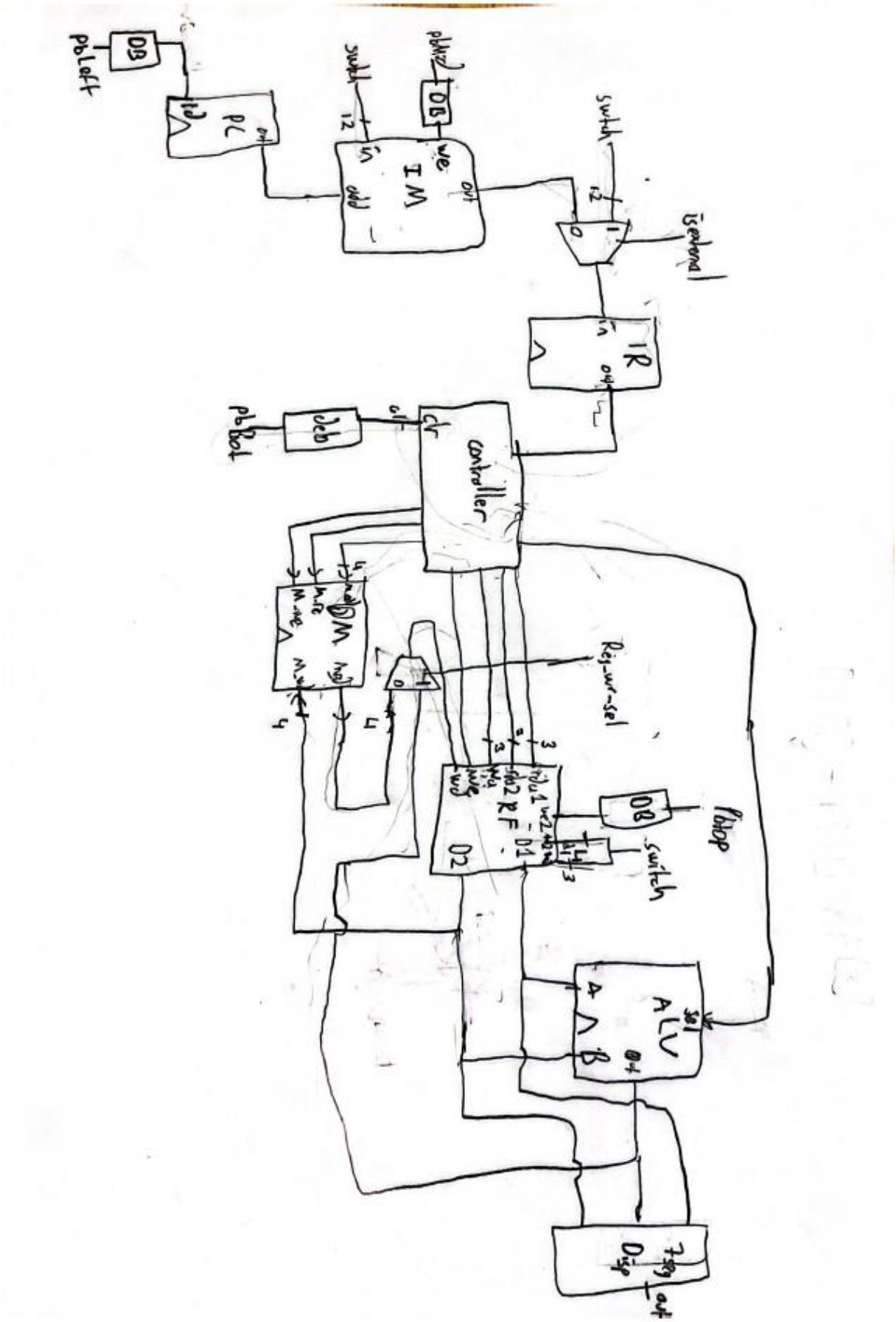
C) Controller High-Level State Machine Diagram



D) Controller Block Diagram



E) Controller/Datapath Top Module Block Diagram



F) Testbenches

```
`timescale 1ns / 1ps
module testbench2();
logic clk, load ;
logic [11:0] in, out;

instructionRegister dut(clk, load, in, out);

always
    begin
        clk <= 1; # 5; clk <= 0; # 5;
    end

initial begin

        load = 0;
        in = 12'b101010000001; # 10;
        in = 12'b110010000001; # 10;

        load = 1;
        in = 12'b100100100000; # 10;
        in = 12'b010010101001; # 10;
        in = 12'b000000010010; # 10;
        in = 12'b000110010010; # 10;
        in = 12'b001000010100; # 10;
        in = 12'b101010000001; # 10;
        in = 12'b110010000001; # 10;
        in = 12'b010000000000; # 10;
        in = 12'b011000000000; # 10;
        in = 12'b100000000000; # 10;
        in = 12'b100000000011; # 10;
        in = 12'b010010101000; # 10;
        in = 12'b010110100000; # 10;
        in = 12'b000000011000; # 10;
    end
endmodule
```

```
`timescale 1ns / 1ps
module testbench1();
logic clk, write, read,clr;
logic [3:0] address;
logic [3:0] data;
logic [3:0] out;
dataMemory dut (clk, clr, read, write, address, data, out );
always
    begin
        clk <= 1; # 5; clk <= 0; # 5;
    end

initial begin
 write = 1; read = 0; clr = 1;
 data = 4'b0000; address = 4'b0000;
 #10;
 clr = 0;
 data = 4'b0010; address = 4'b0001;
 #10;
 data = 4'b0100; address = 4'b0010;
 #10;
 data = 4'b0110; address = 4'b0011;
 #10;
 data = 4'b1000; address = 4'b0100;
 #10;
 data = 4'b1010; address = 4'b0101;
 #10;
 data = 4'b1100; address = 4'b0110;
 #10;
 data = 4'b1110; address = 4'b0111;
 #10;
 data = 0; read = 1; write = 0;
 data = 4'b0000; address = 4'b0000;
 #10;
 data = 4'b0010; address = 4'b0001;
 #10;
 data = 4'b0100; address = 4'b0010;
 #10;
 data = 4'b0110; address = 4'b0011;
 #10;
 data = 4'b1000; address = 4'b0100;
 #10;
 data = 4'b1010; address = 4'b0101;
 #10;
 data = 4'b1100; address = 4'b0110;
 #10;
 data = 4'b1110; address = 4'b0111;
 #10;
 end

endmodule
```