CS-223

Digital Design

Section: 3

LAB 4

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A) State Transition Diagram

Reset

State Encoding

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S3 S2 S1 S0 | | | | States |
| 0 | 0 | 0 | 0 | S0 |
| 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 1 | 0 | S2 |
| 0 | 0 | 1 | 1 | S3 |
| 0 | 1 | 0 | 0 | S4 |
| 0 | 1 | 0 | 1 | S5 |
| 0 | 1 | 1 | 0 | S6 |
| 0 | 1 | 1 | 1 | S7 |
| 1 | 0 | 0 | 0 | S8 |
| 1 | 0 | 0 | 1 | S9 |

Output Encoding

|  |  |  |
| --- | --- | --- |
| Y1 Y0 | | Output |
| 0 | 0 | Green |
| 0 | 1 | Yellow |
| 1 | 0 | Red |

State Transition Table

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Current State** | | | | **Inputs** | | **Next State** | | | |
| S3 | S2 | S1 | S0 | SA | SB | S3’ | S2’ | S1’ | S0’ |
| 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | X | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | X | X | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | X | X | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | X | X | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | X | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | X | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | X | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | X | X | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | X | X | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | X | X | 0 | 0 | 0 | 0 |

Output Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Current State** | | | | **Outputs** | | | |
| S3 | S2 | S1 | S0 | LA1 | LA0 | LB1 | LB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

Next States Equations

S3’ = (S3! S2 S1 S0) + (S3 S2! S1! S0!)

S2’ = (S3! S2 S1!) + (S3! S2 S0!) + (S3! S2! S1 S0)

S1’= (S3! S1 S0!) + (S3! S2! S1! SA! SB) + (S3! S2! S1! S0 SB) + (S3! S2 S1! S0 SA)

S0’= (S3 S2! S1! S0!) + (S3! S0! SA SB) + (S3! S2 S0! SA) + (S3! S1! S0 SB!) + (S3! S2! S1 S0!) + (S3! S2 S1! SA!)

Output Equations

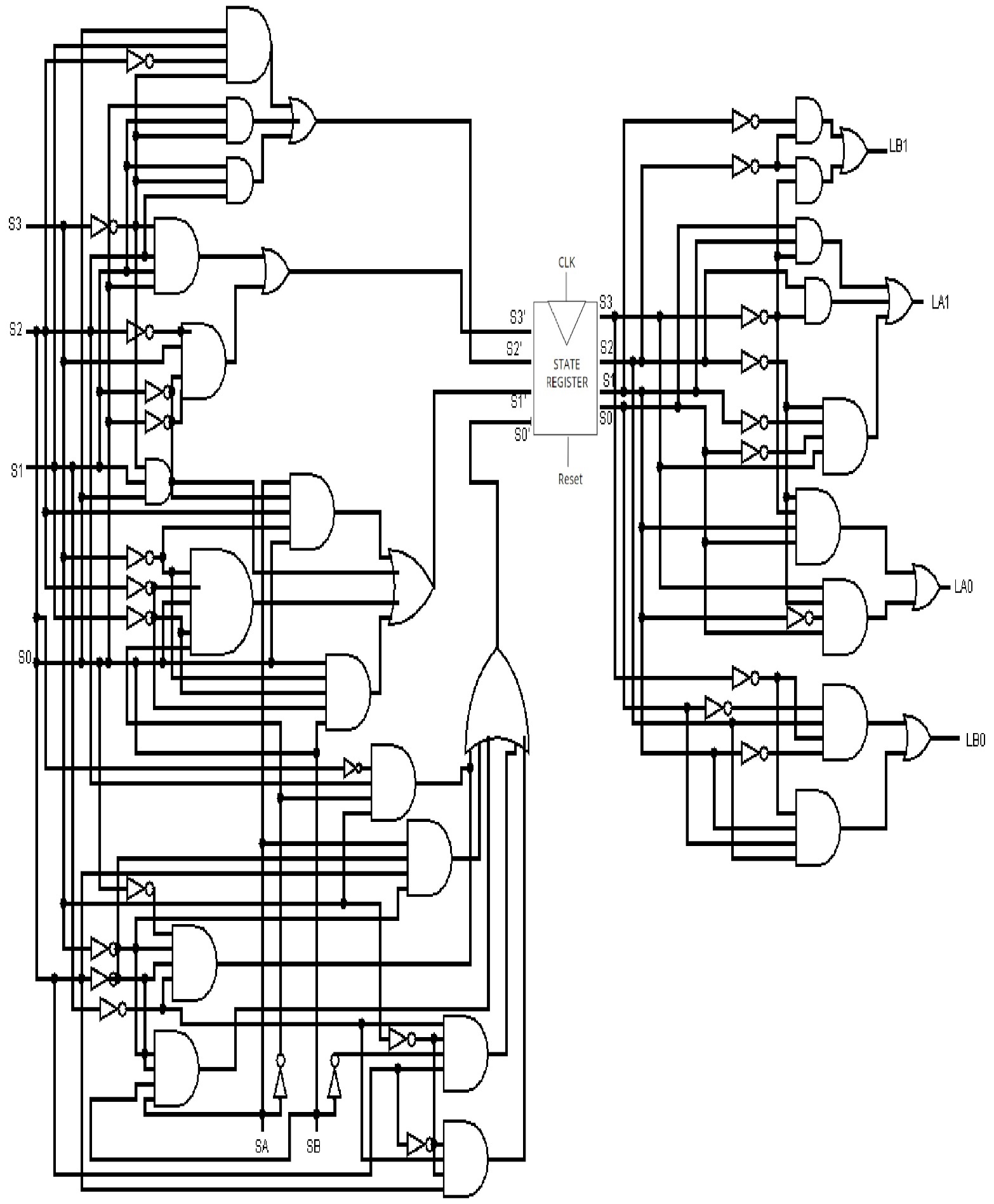
LA1 = (S3! S2) + (S3! S1 S0) + (S3 S2! S1! S0!)

LA0 = (S3! S2! S1 S0!) + (S3 S2! S1! S0)

LB1= (S3! S2!) + (S2! S1!)

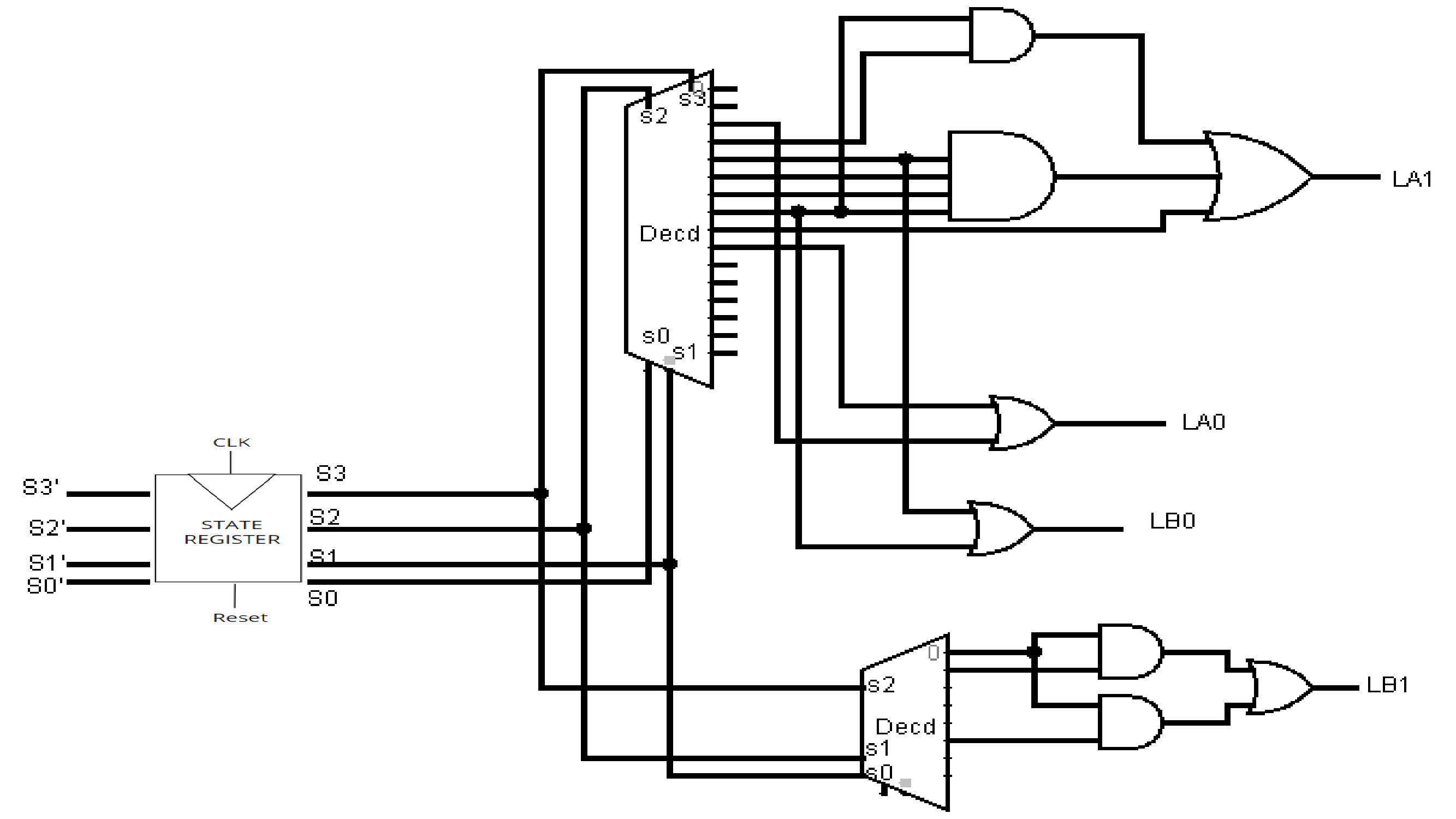
LB0 = (S3! S2 S1! S0!) + (S3! S2 S1 S0)

B) Finite State Machine schematic

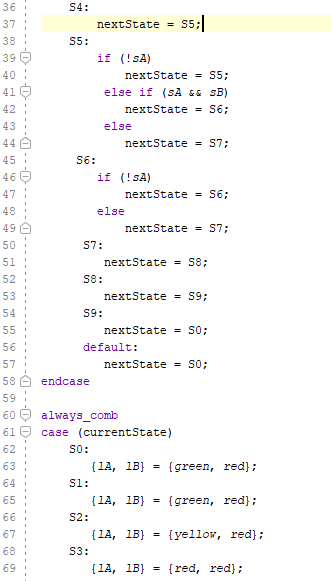
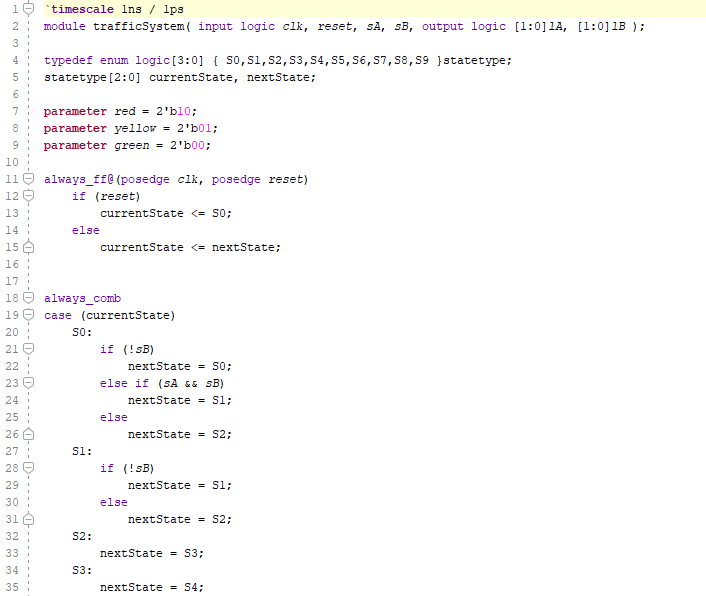


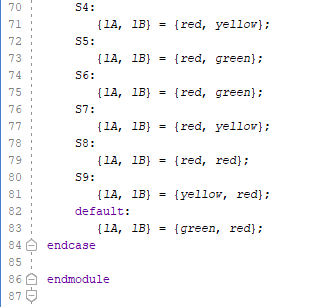
C) Since there are 10 states, 4 flip flops will be required.

D) The next state logic will be same. Output logic will look something like this:



E) Codes





Testbench:

