THE UNIVERSITY OF AZAD JAMMU & KASHMIR, MUZAFFARABAD

COURSE TITLE	**CALD**
COURSE CODE	**CS-1205**
LAB TITLE	**ADDER-SUBTRACTOR**
STUDENT NAME	**HASEEB SHEIKH**
STUDENT ROLL NUMBER	**2024-SE-31**
INSTRUCTOR NAME	**ENGR. SIDRA RAFIQUE**
SUBMISSION DATE	**AUG 09, 2025**

DEPARTMENT OF SOFTWARE ENGINEERING

CALD

Lab 6

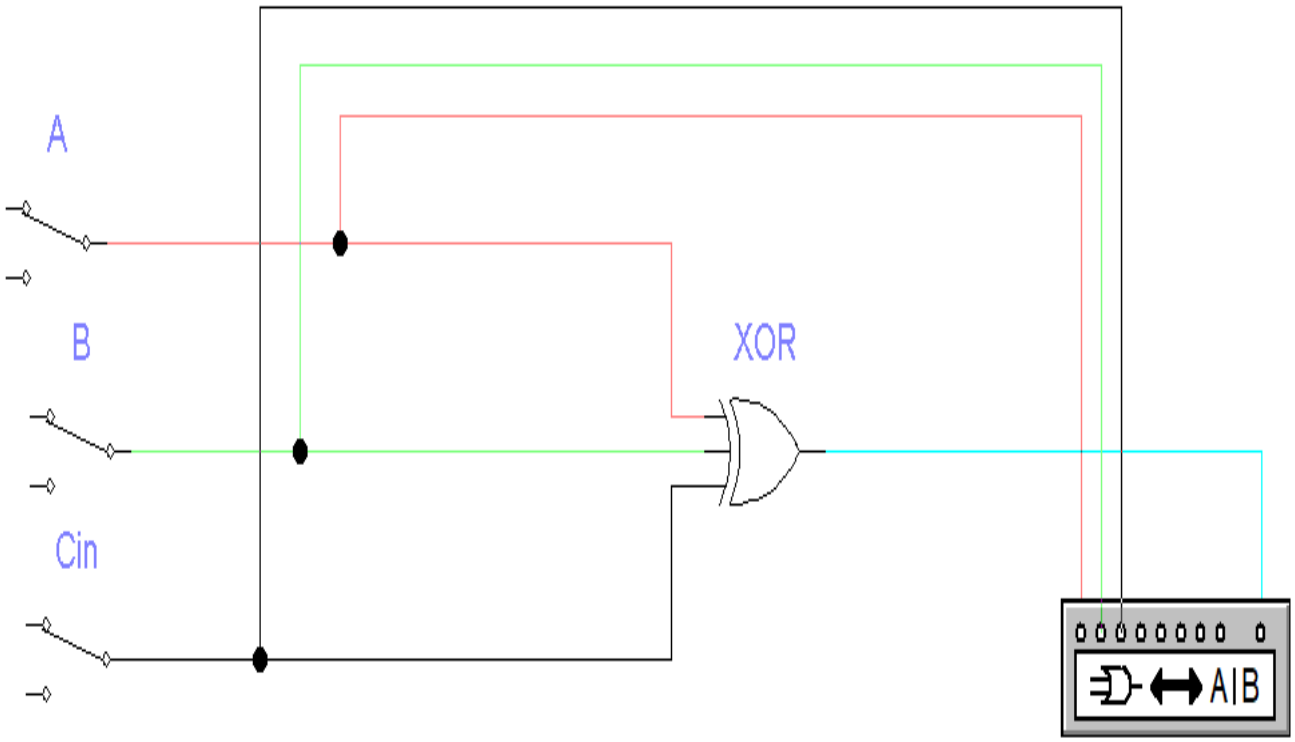
Objective:

This experiment aims to demonstrate the working of the full adder as well as the working of half subtractor.

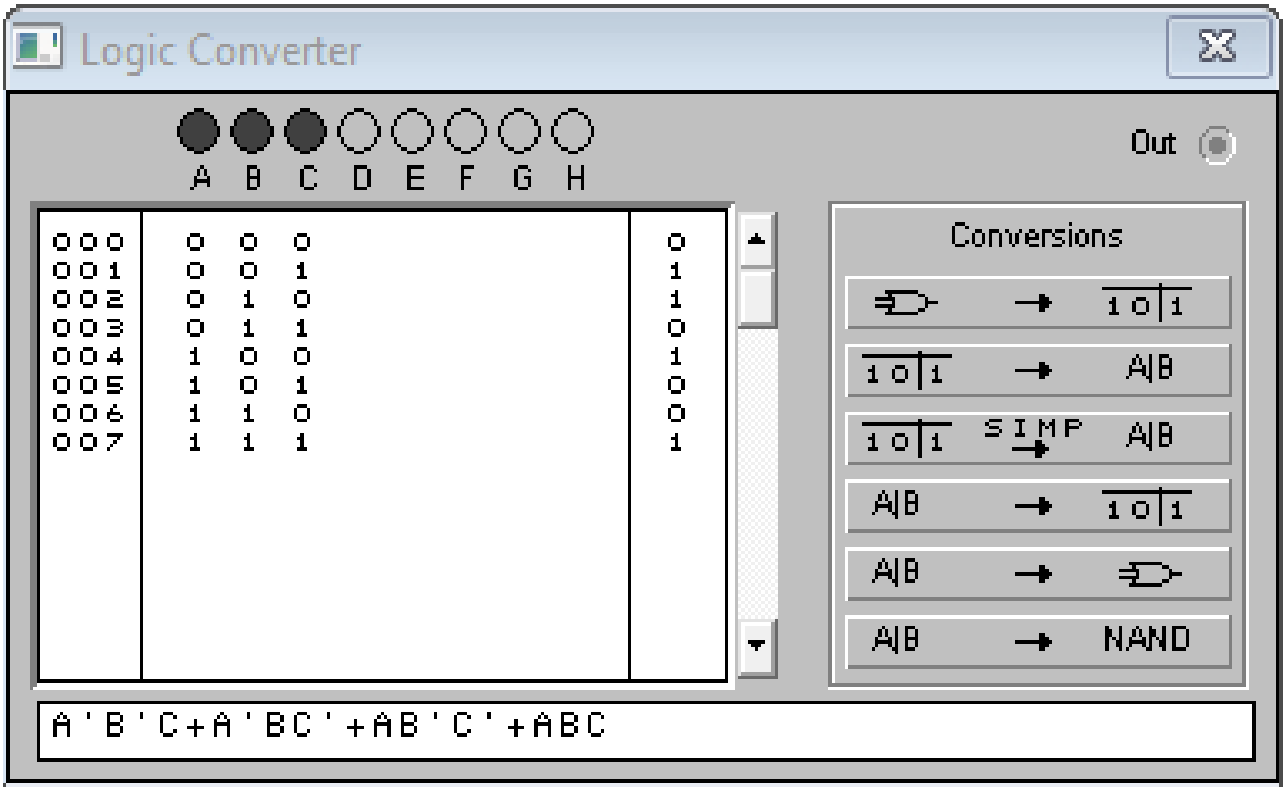
Experiment on EWB

Full Adder Using Logic Gates

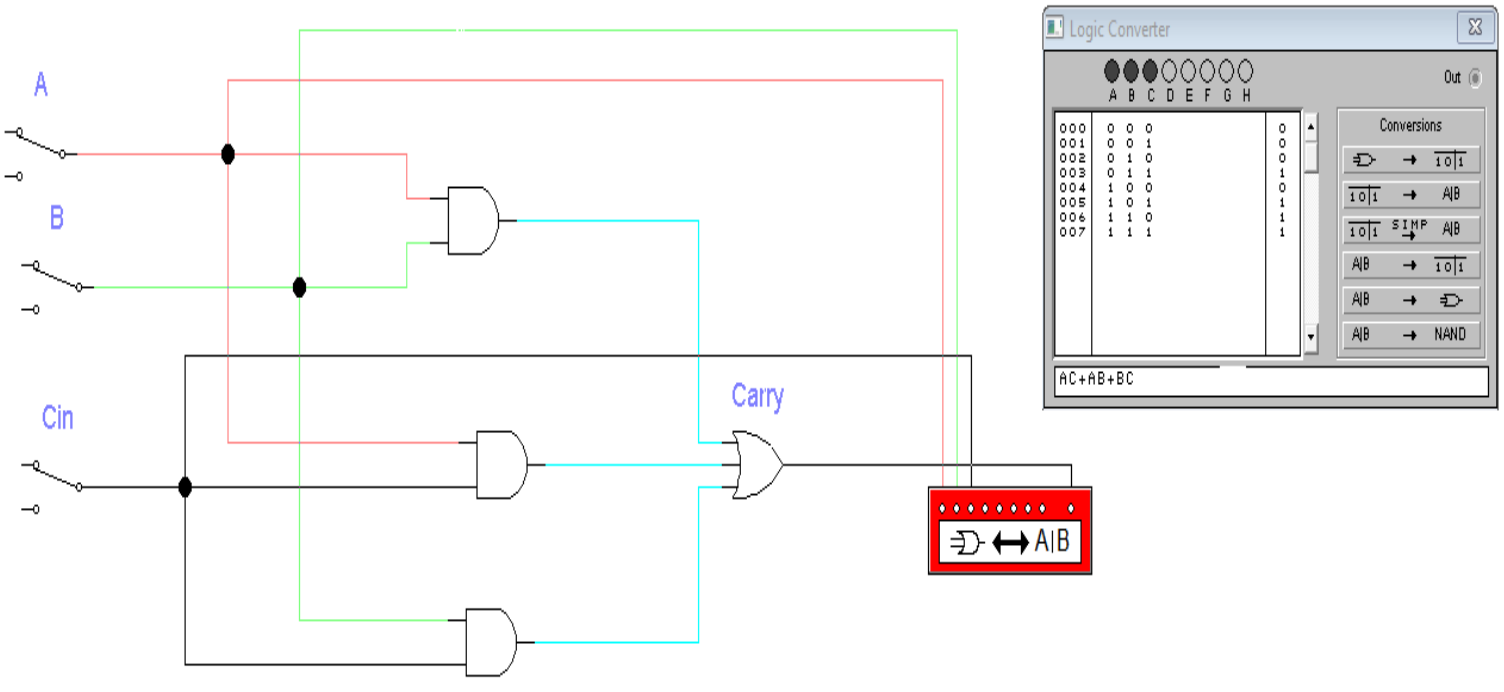
Sum Output



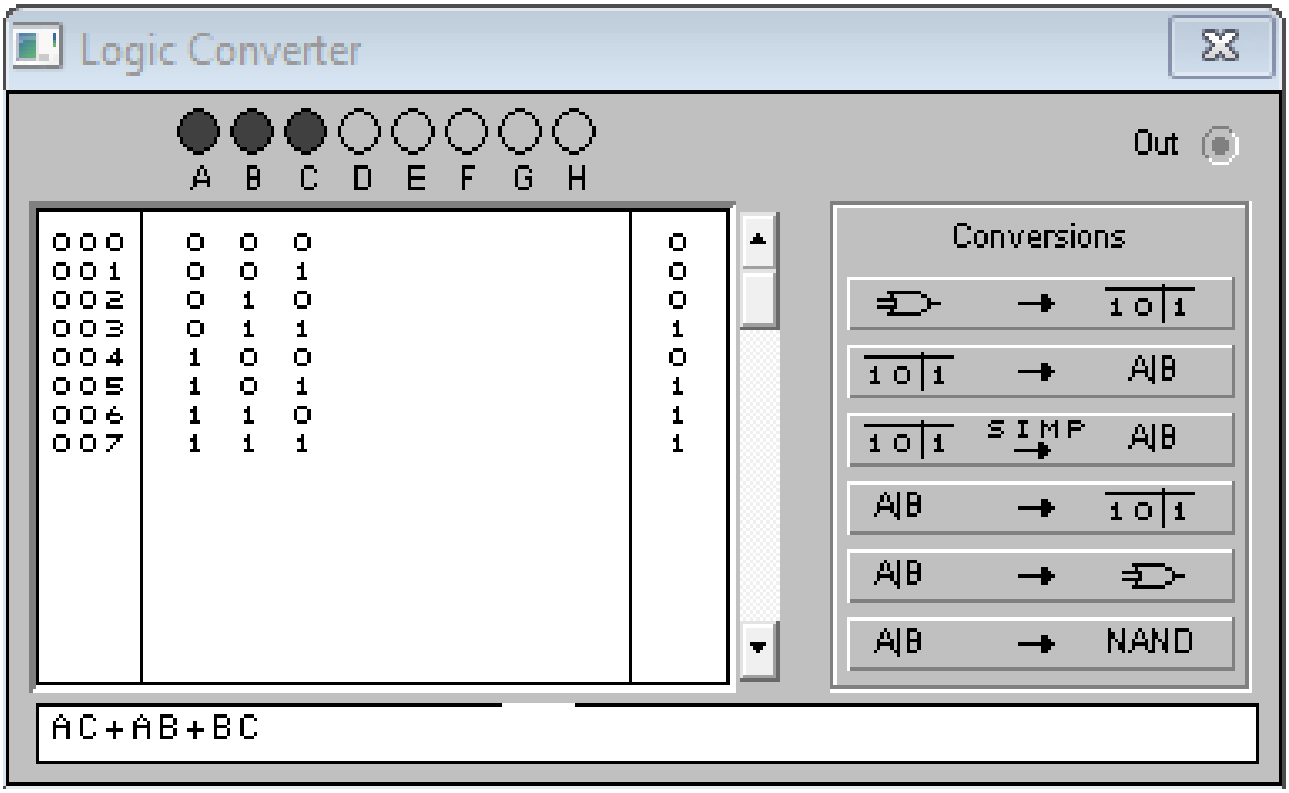
Truth Table



Carry Output

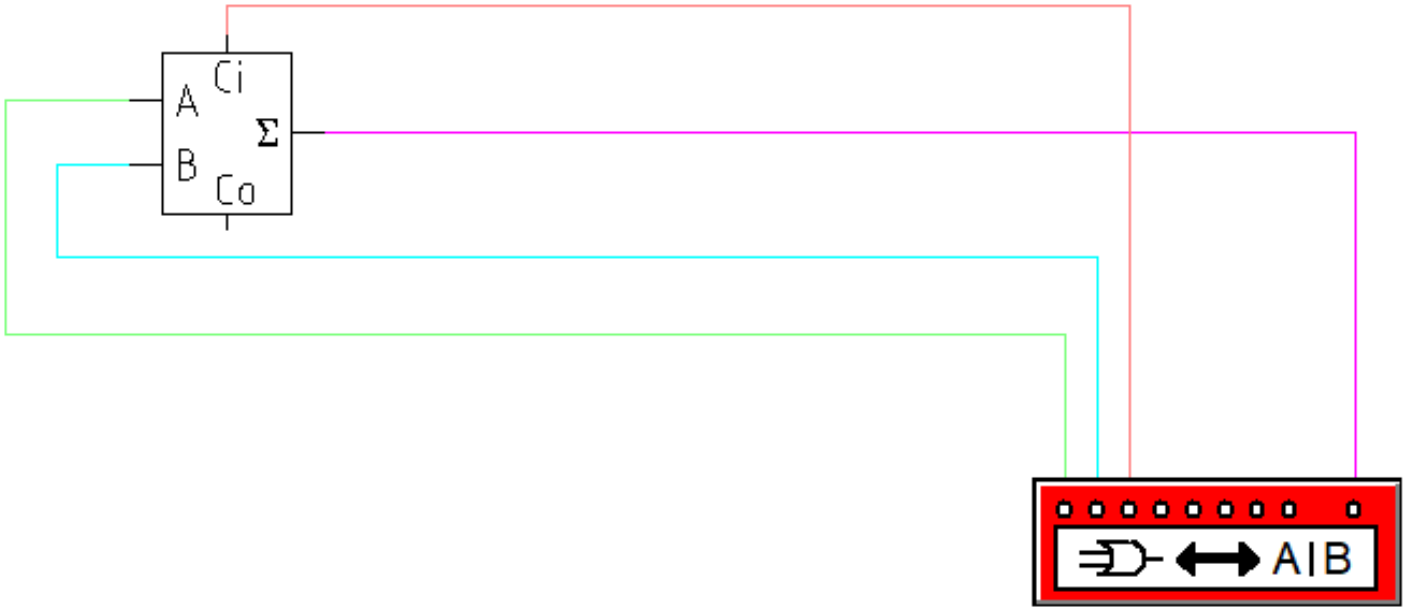


Truth Table

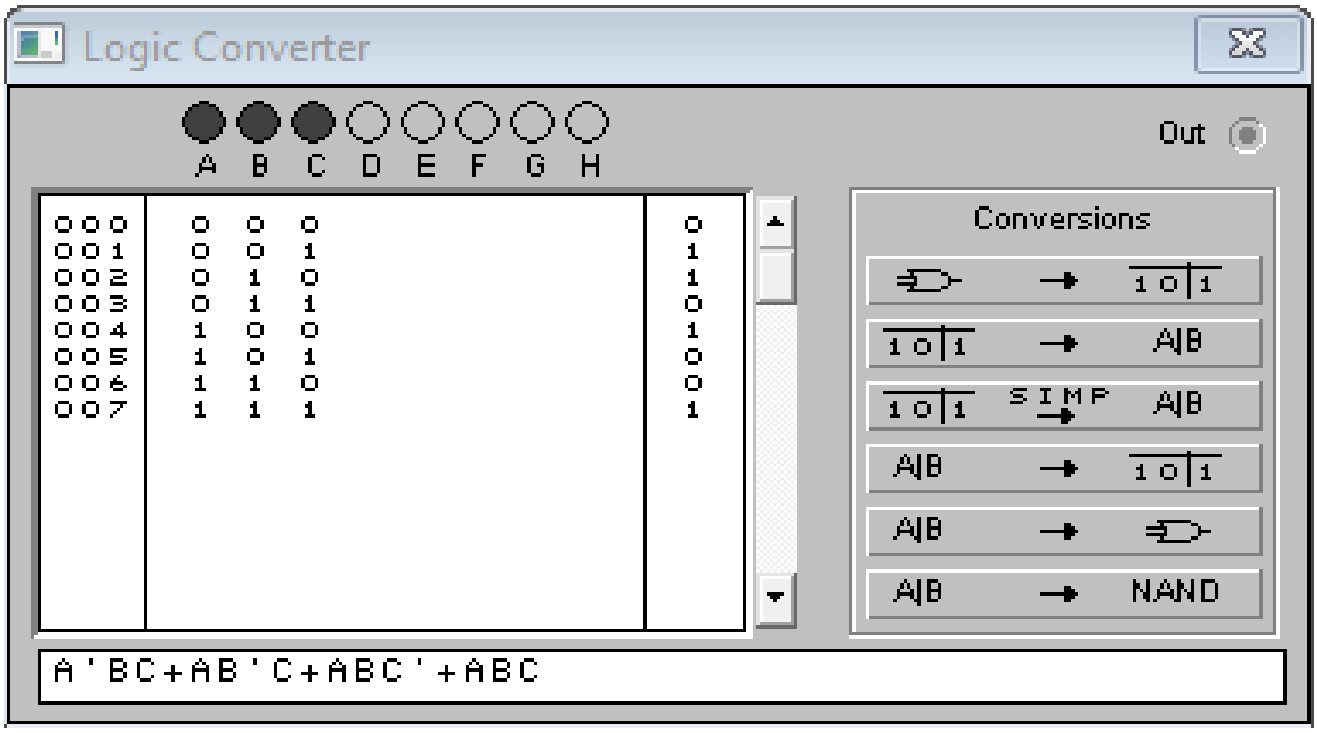

Logic Converter
A B C D E F G H
Out
000 0 0 0 0
001 0 0 1 0
002 0 1 0 0
003 0 1 1 1
004 1 0 0 0
005 1 0 1 1
006 1 1 0 1
007 1 1 1 1
Conversions
1 0 1
A|B
SIMP
NAND
A'C+AB+BC

Using Built-In Full Adder

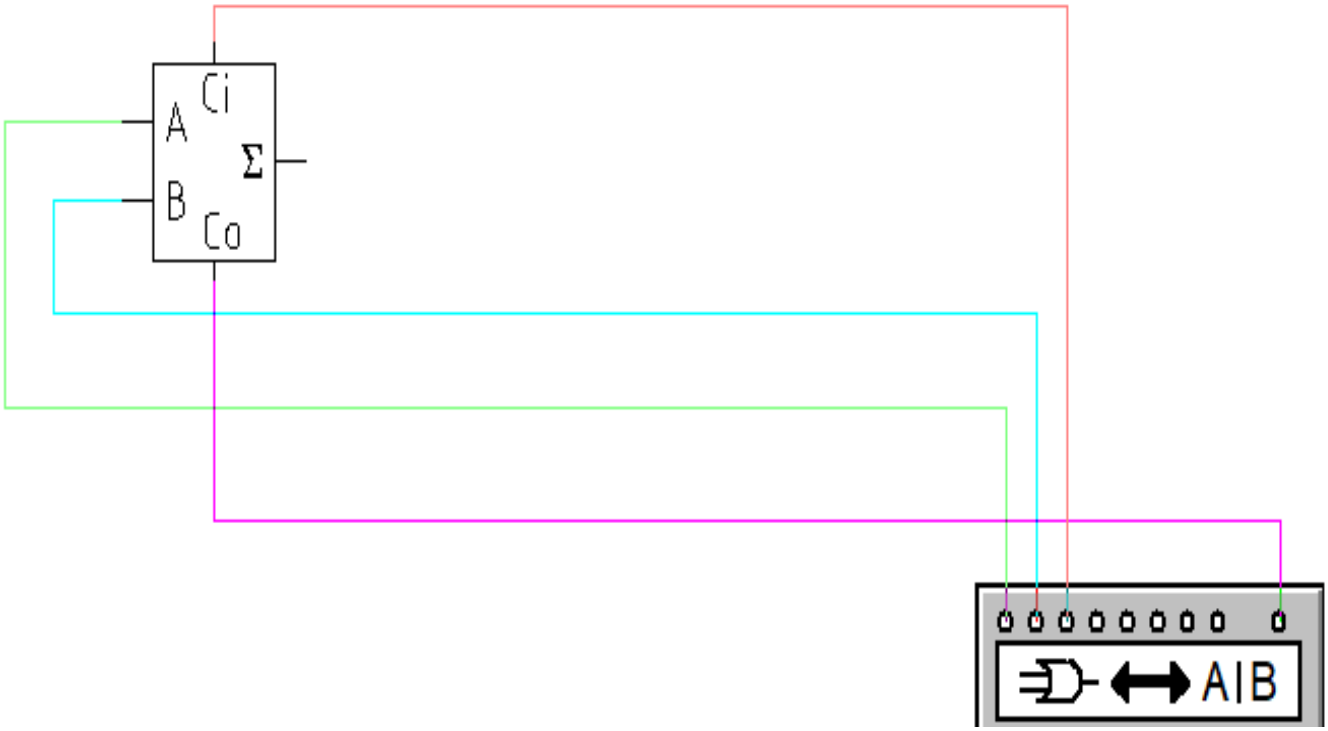
Sum Output



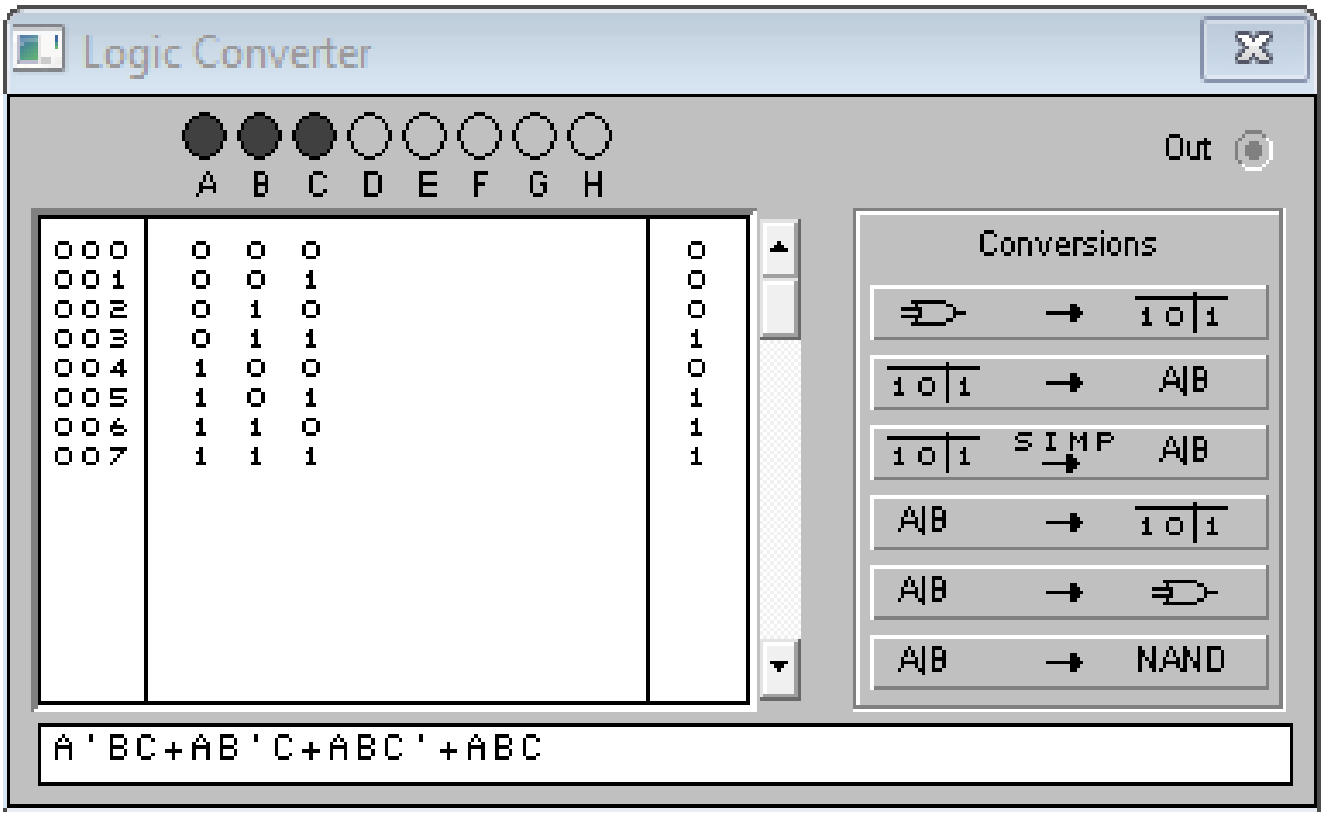
Truth Table



Carry Output

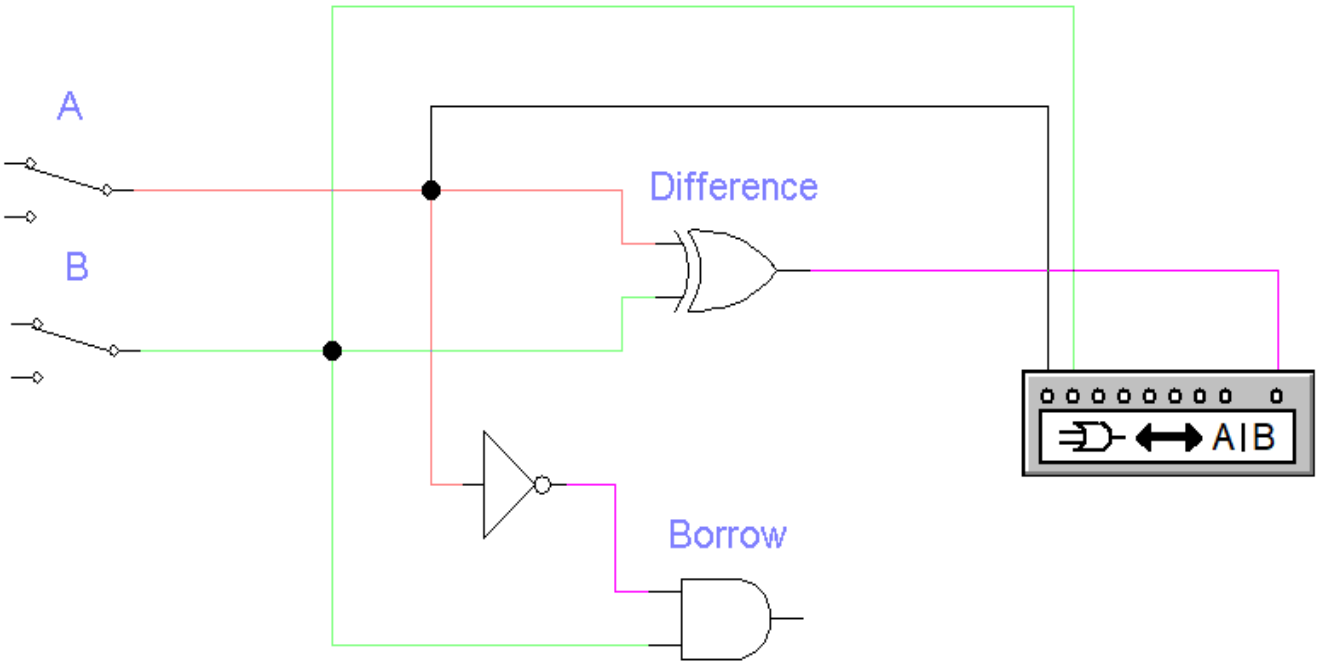


Truth Table

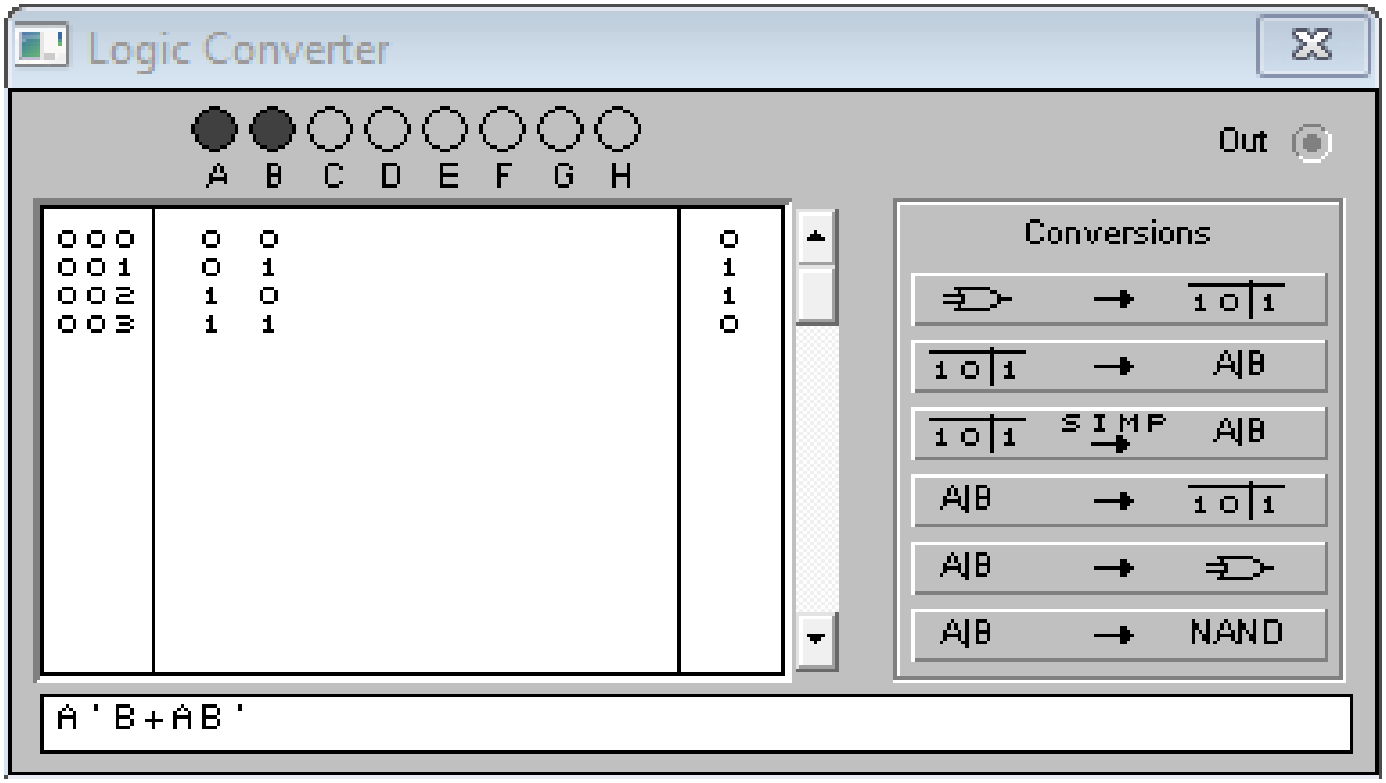


Half Subtractor

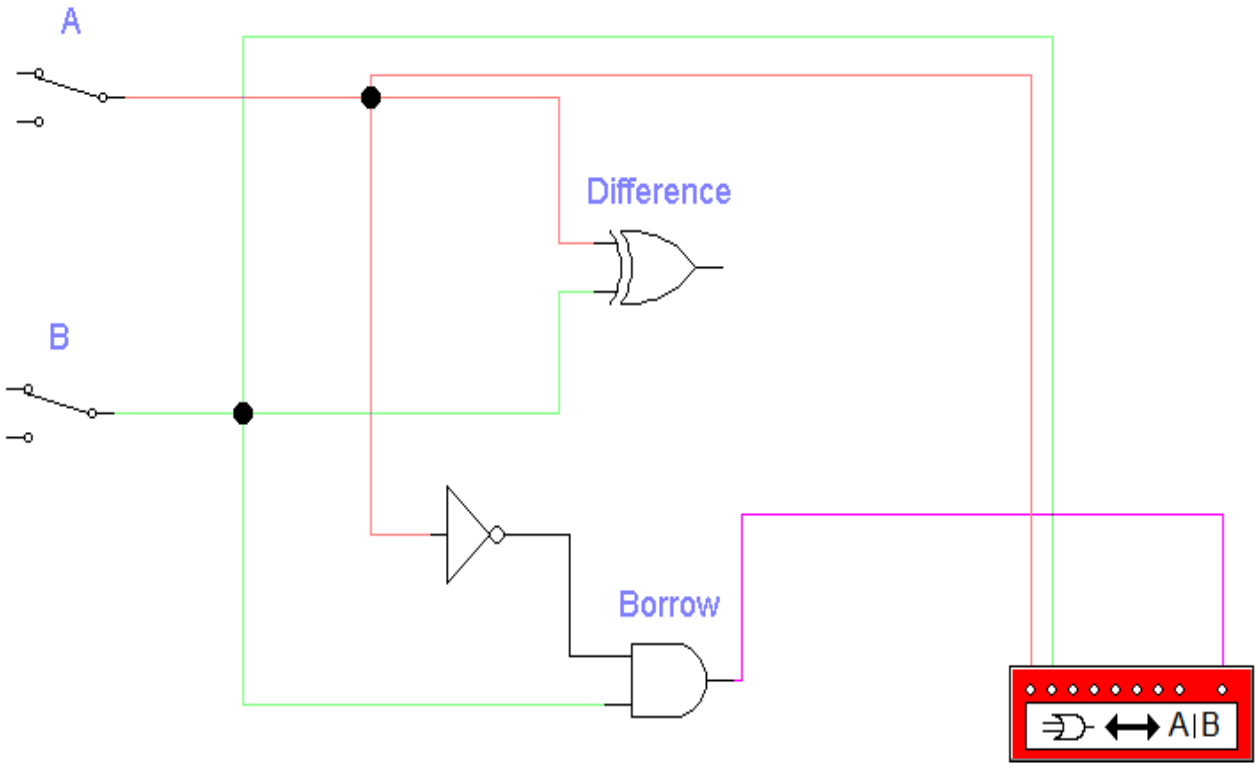
Difference Output



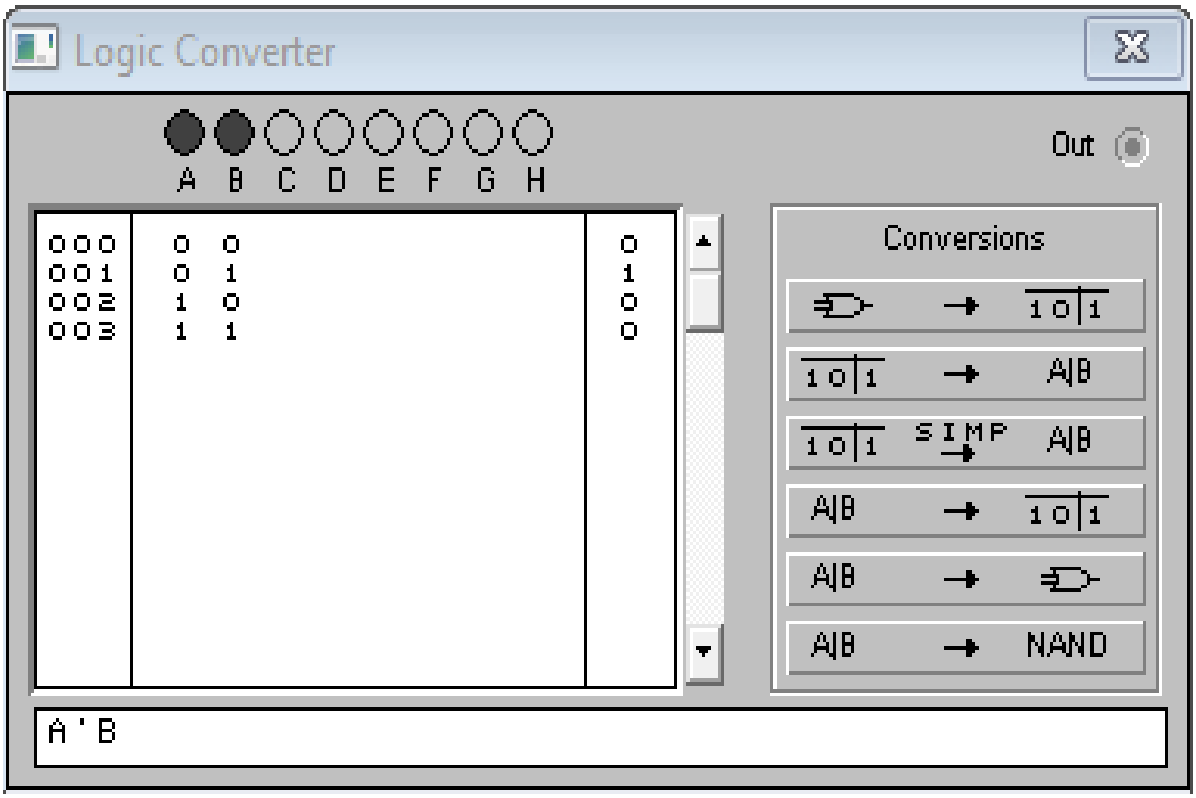
Truth Table



Borrow Output

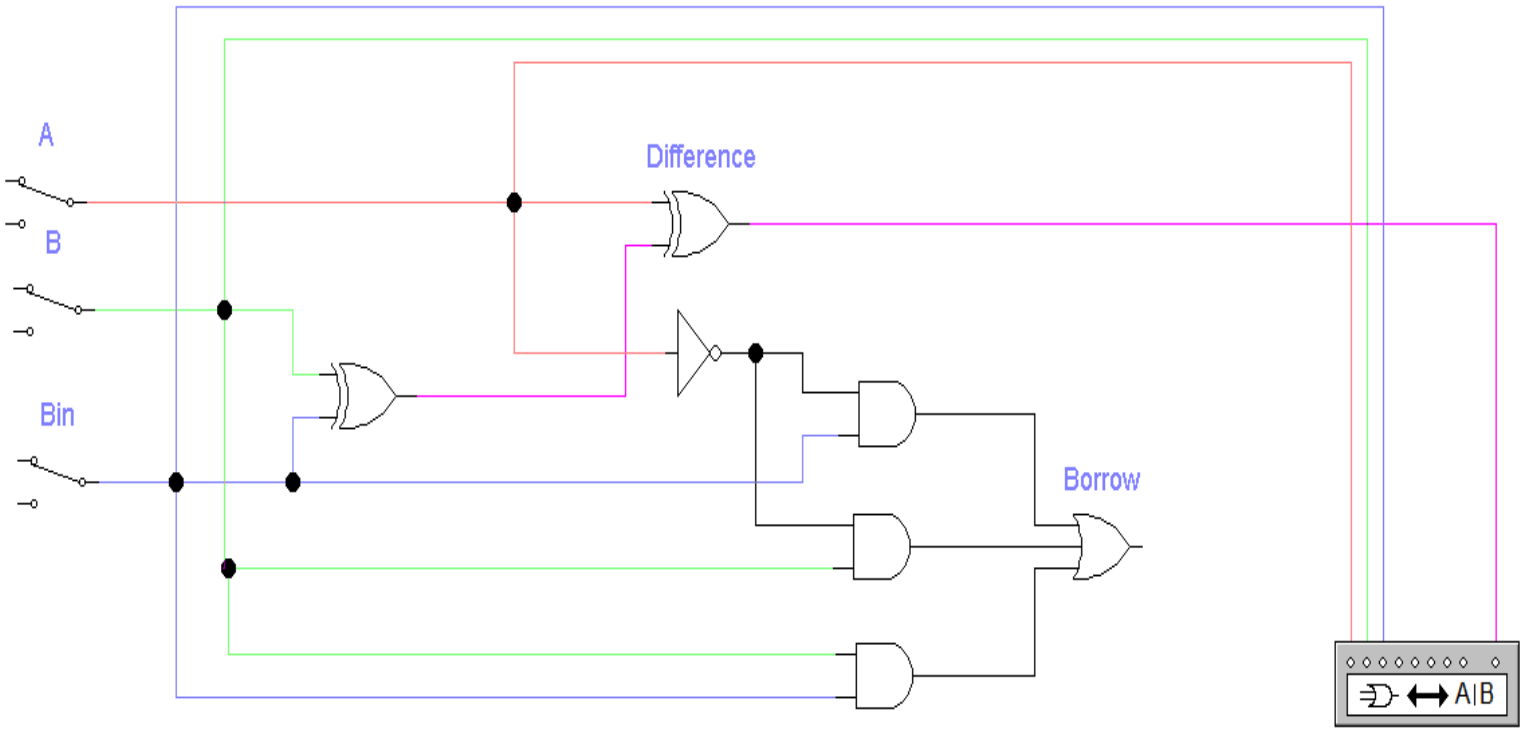


Truth Table

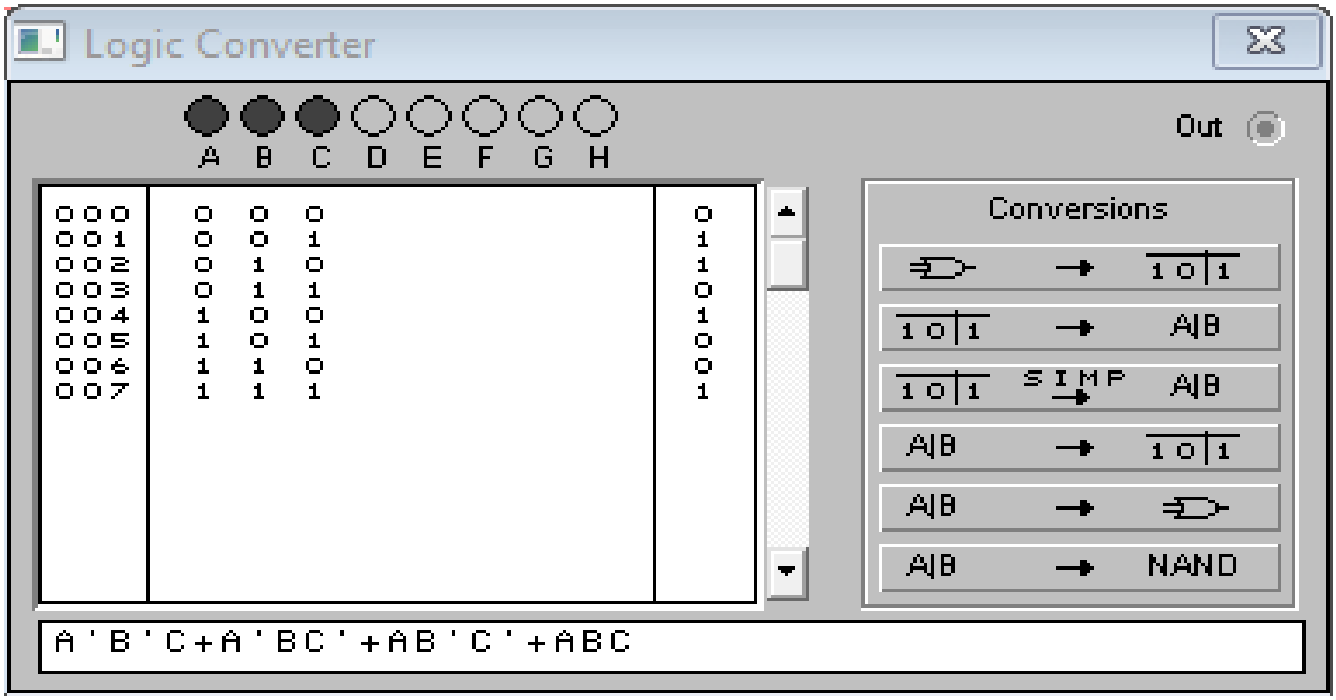


Full Subtractor

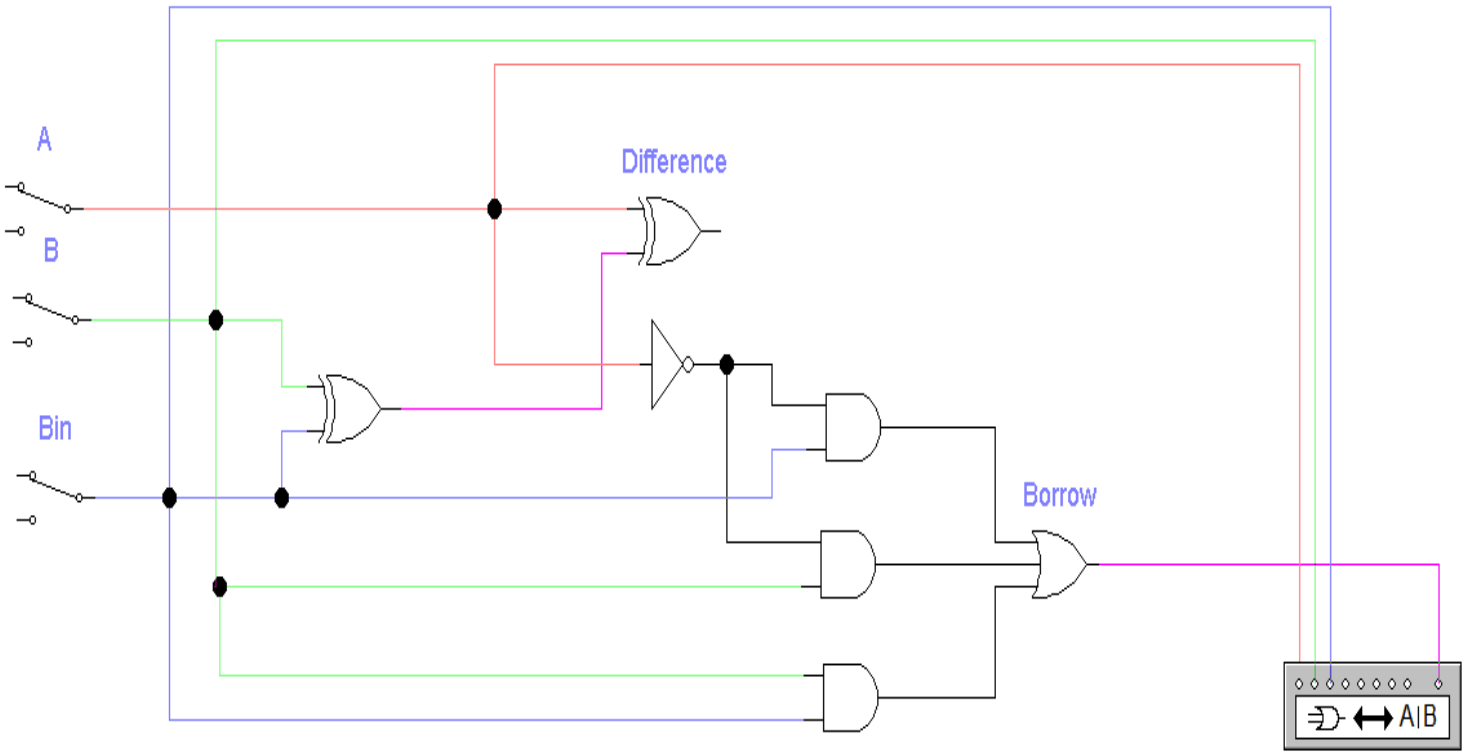
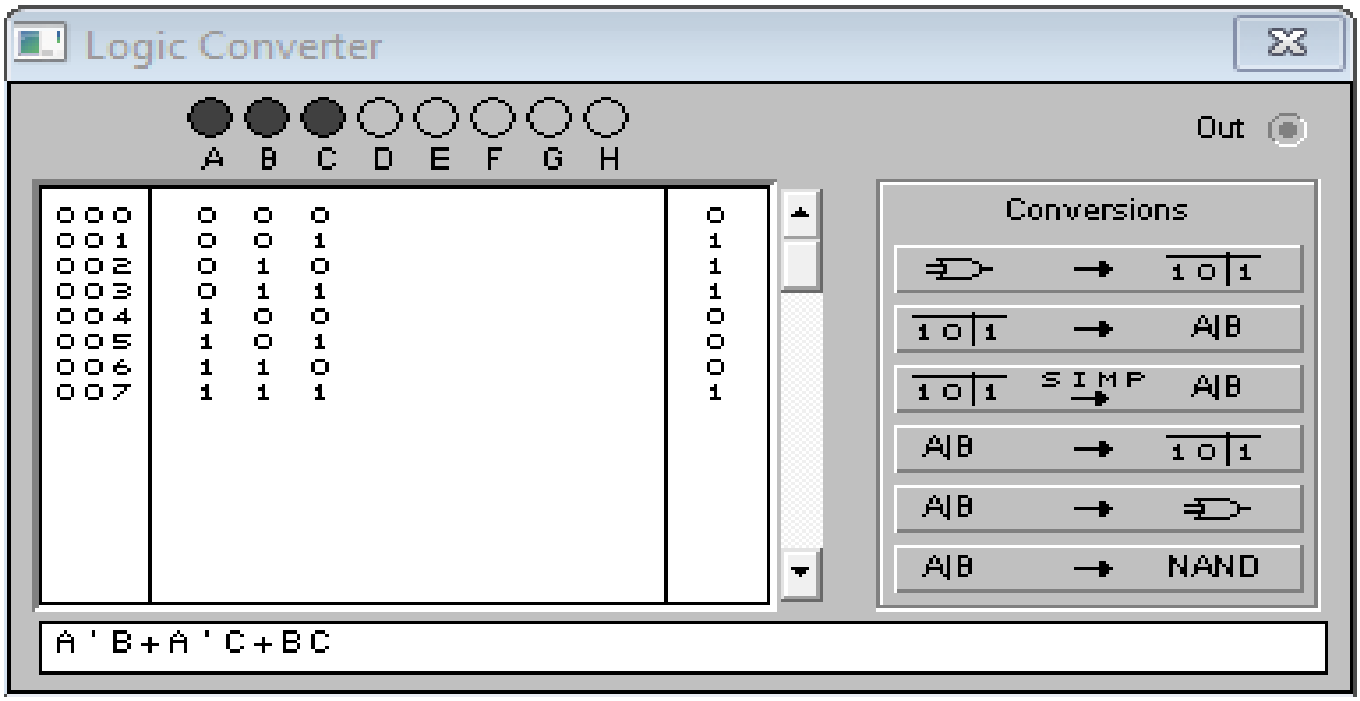
Difference Output



Truth Table



Borrow Output



Truth Table