THE UNIVERSITY OF AZAD JAMMU & KASHMIR, MUZAFFARABAD

COURSE TITLE	**CALD**
COURSE CODE	**CS-1205**
LAB TITLE	**BASIC LOGIC GATES**
STUDENT NAME	**HASEEB SHEIKH**
STUDENT ROLL NUMBER	**2024-SE-31**
INSTRUCTOR NAME	**ENGR. SIDRA RAFIQUE**
SUBMISSION DATE	**JUNE 04, 2025**

DEPARTMENT OF SOFTWARE ENGINEERING

Contents

CALD

Lab 3

Objective:

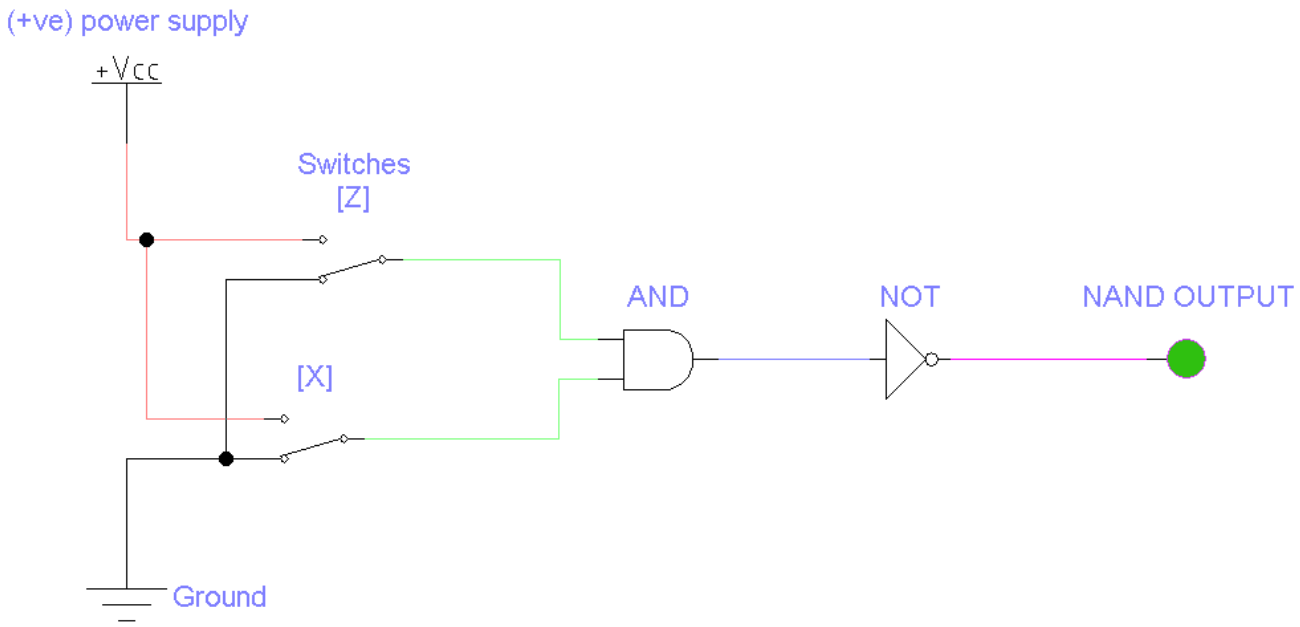
This experiment aims to demonstrate how a combination of **AND**, **OR** and **NOT** gates can be utilized to replicate the behavior of a **NAND** and **NOR** gates, thereby reinforcing the foundational concepts of digital logic design.

Experiment on EWB(NAND)

1: Verification using a probe

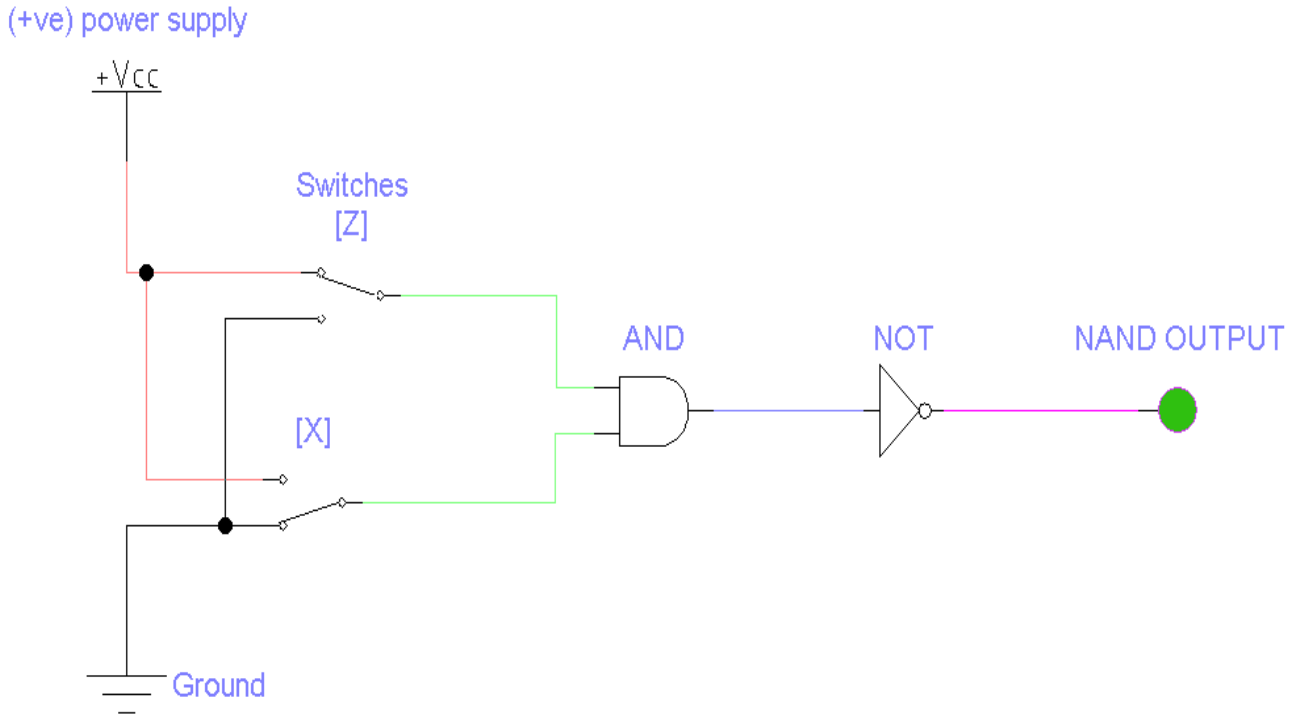
First Combination:

- Switch Z: 0
- Switch X: 0



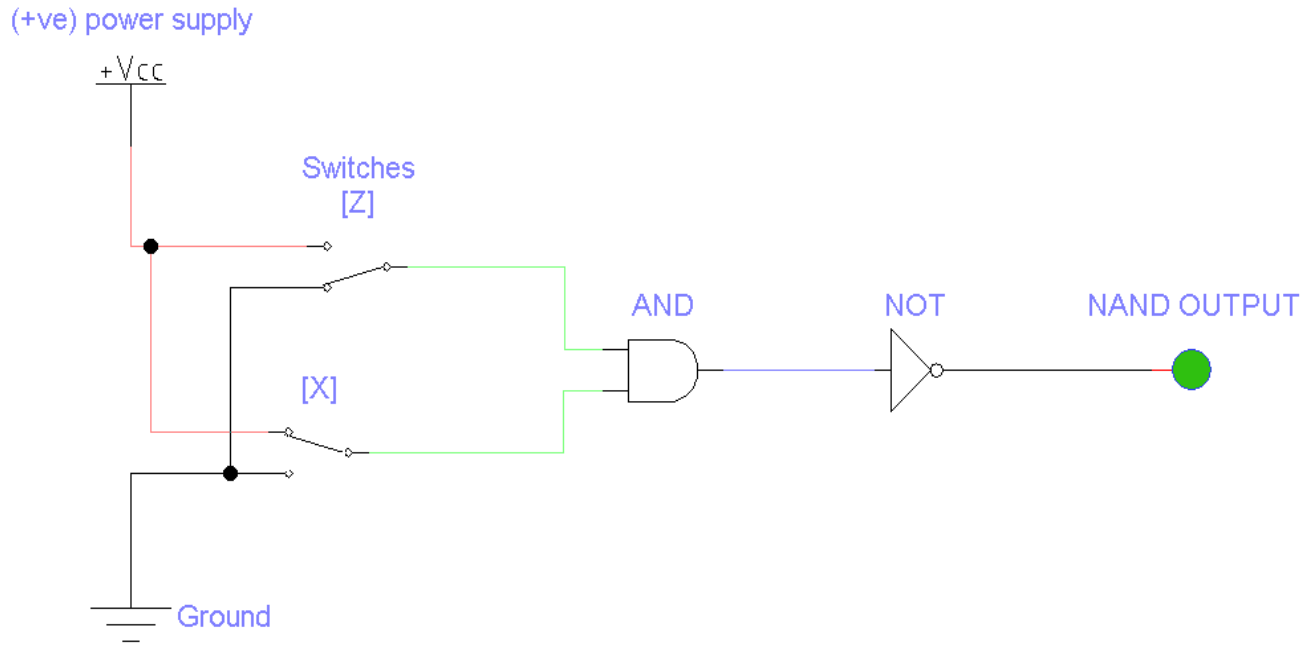
Second Combination:

- Switch Z: 1
- Switch X: 0



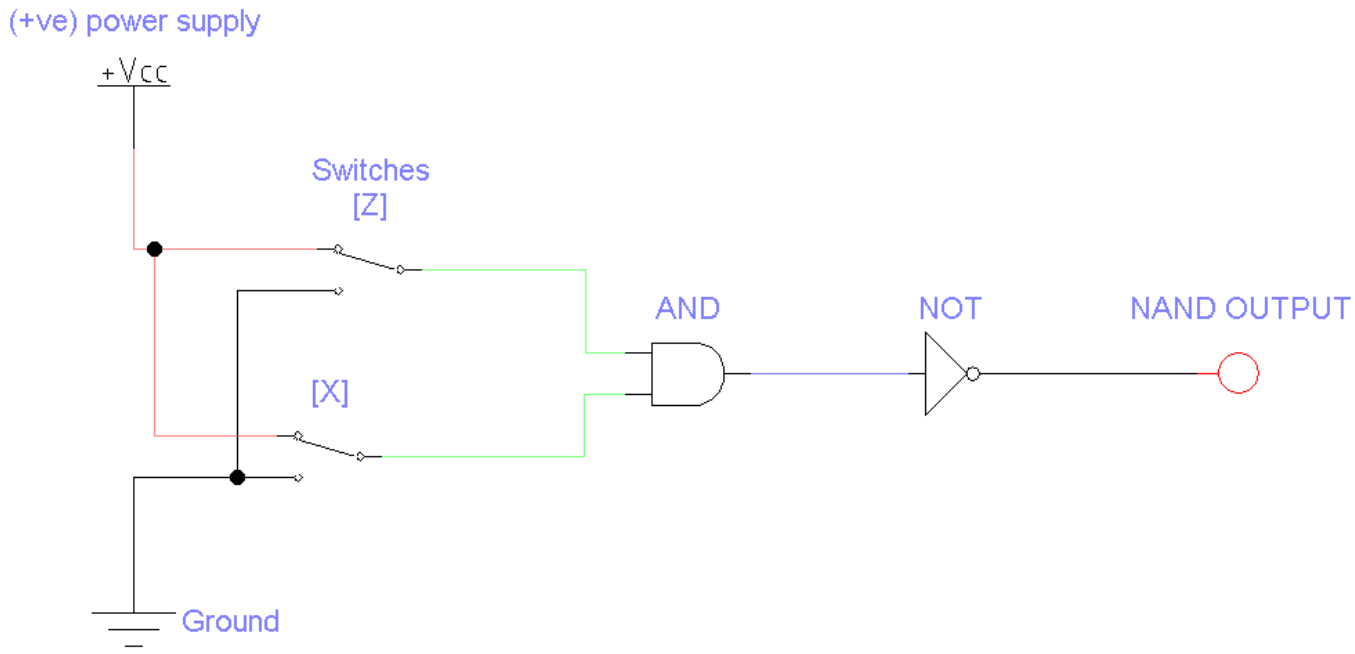
Third Combination:

- Switch Z: 0
- Switch X: 1

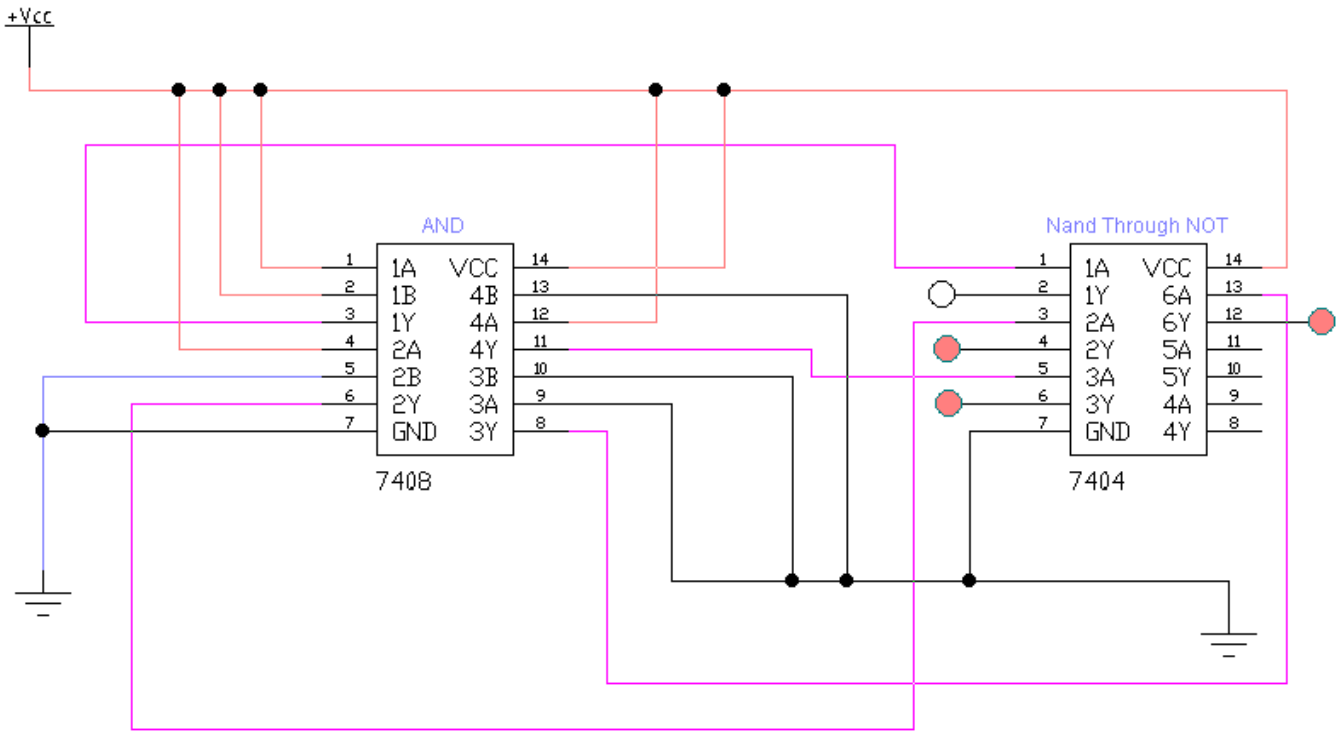


Fourth Combination:

- Switch Z: 1
- Switch X: 1

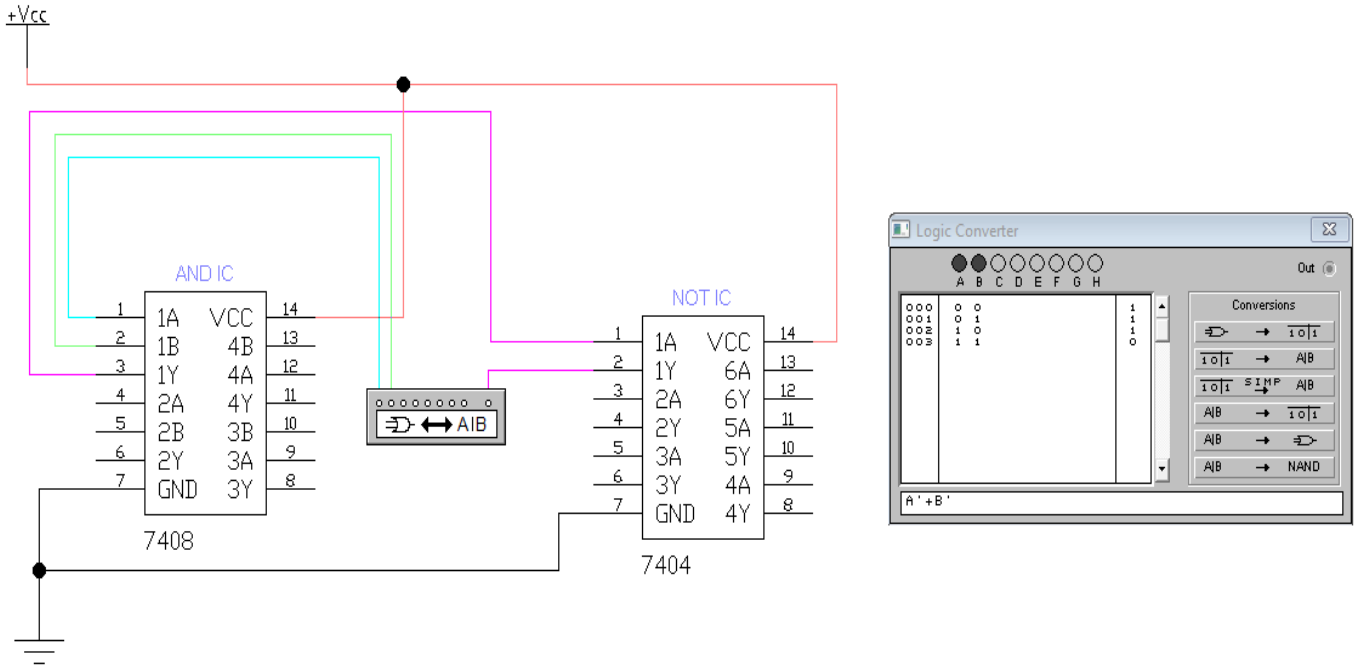


2: Verification using ICs

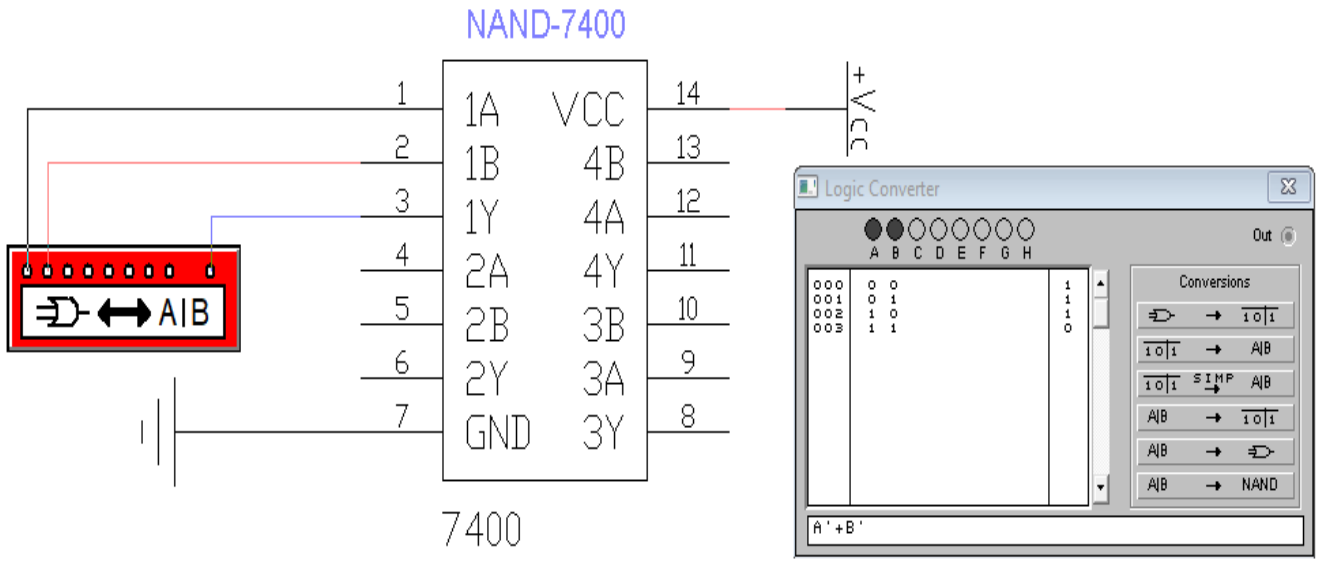


3: Verification by truth table

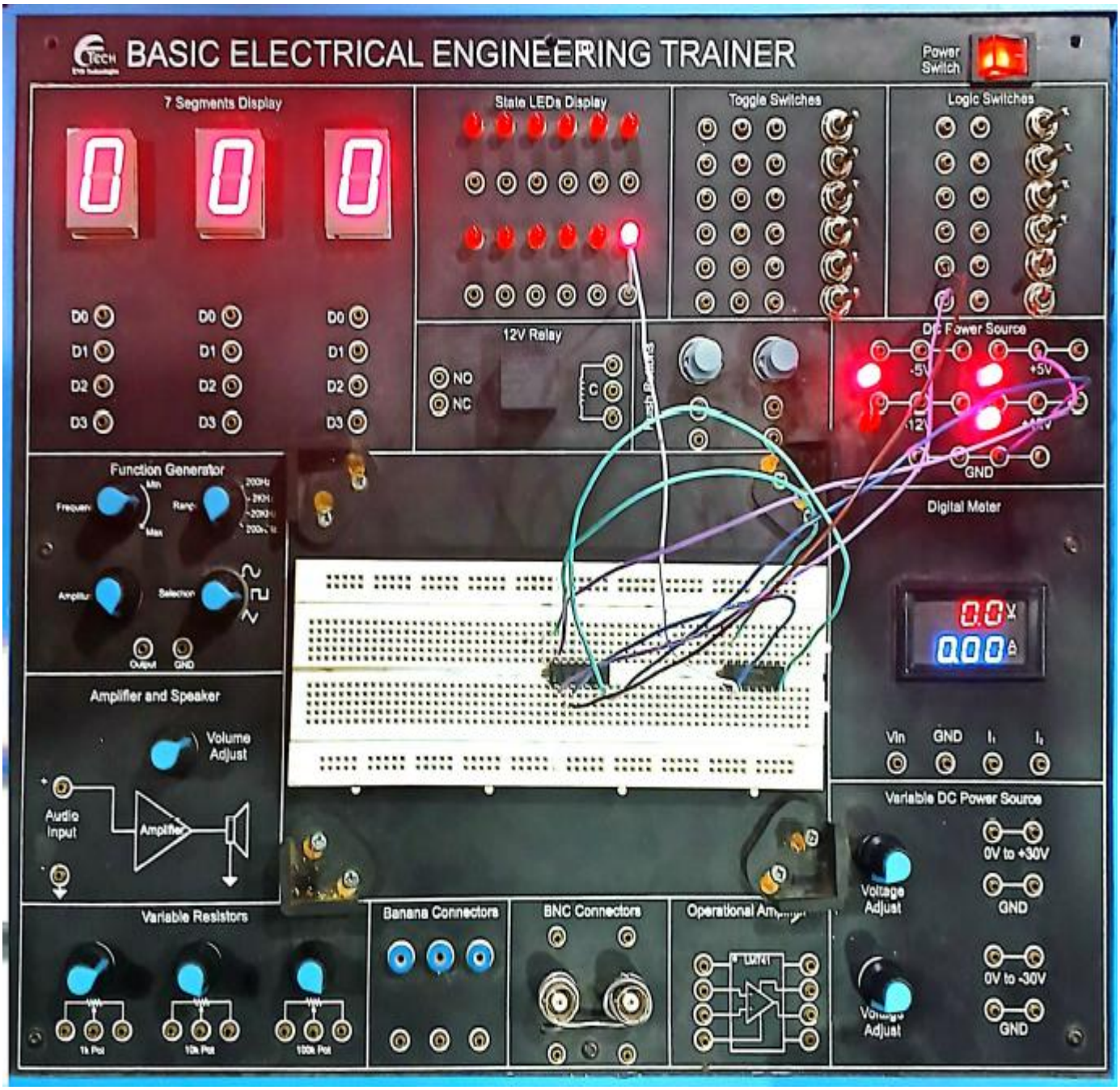
Truth table of the combination:



Truth table of NAND:



Experiment on Hardware



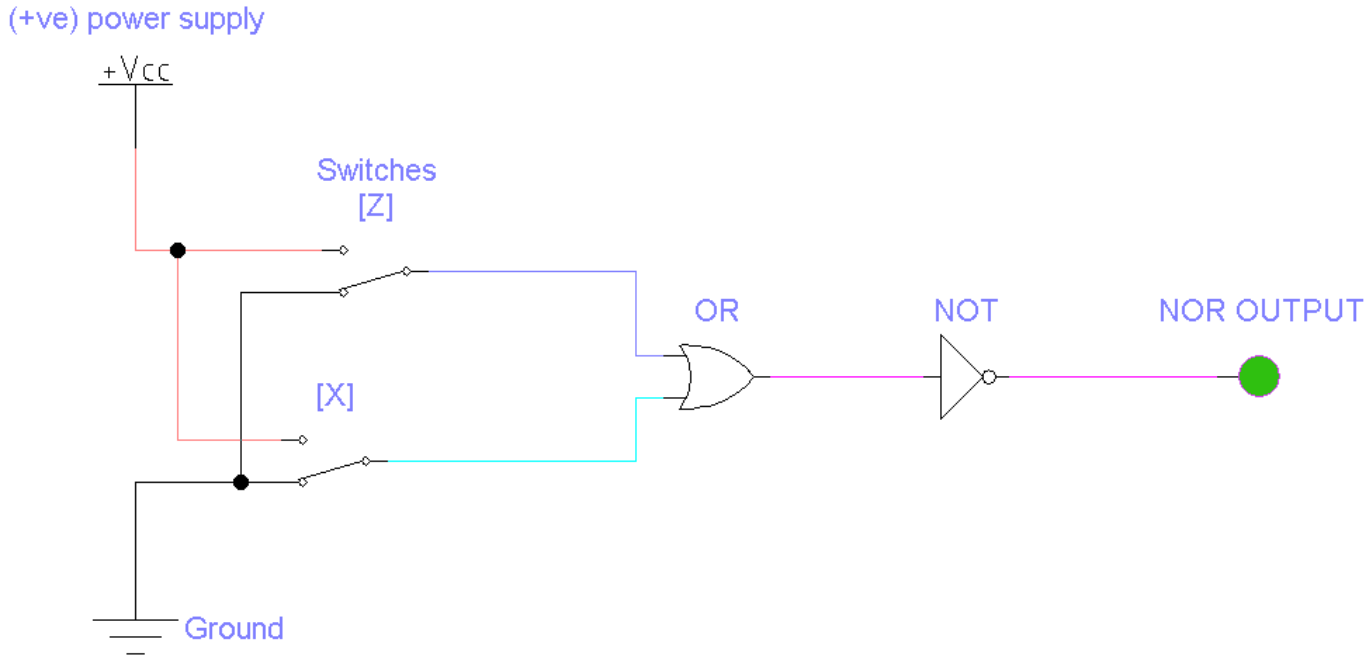
- The output of the combination shows that the probe glows when both the inputs A and B are 0.

Experiment on EWB (NOR)

1: Verification using a probe

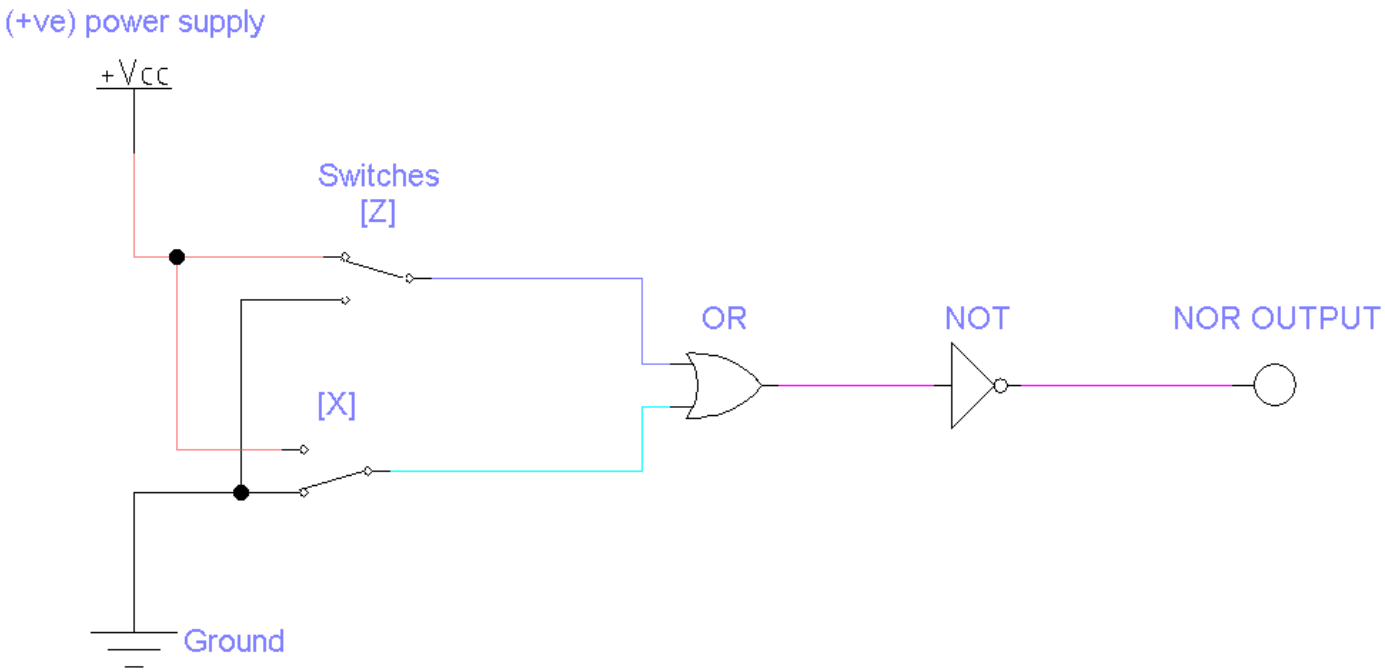
First Combination:

- Switch Z: 0
- Switch X: 0



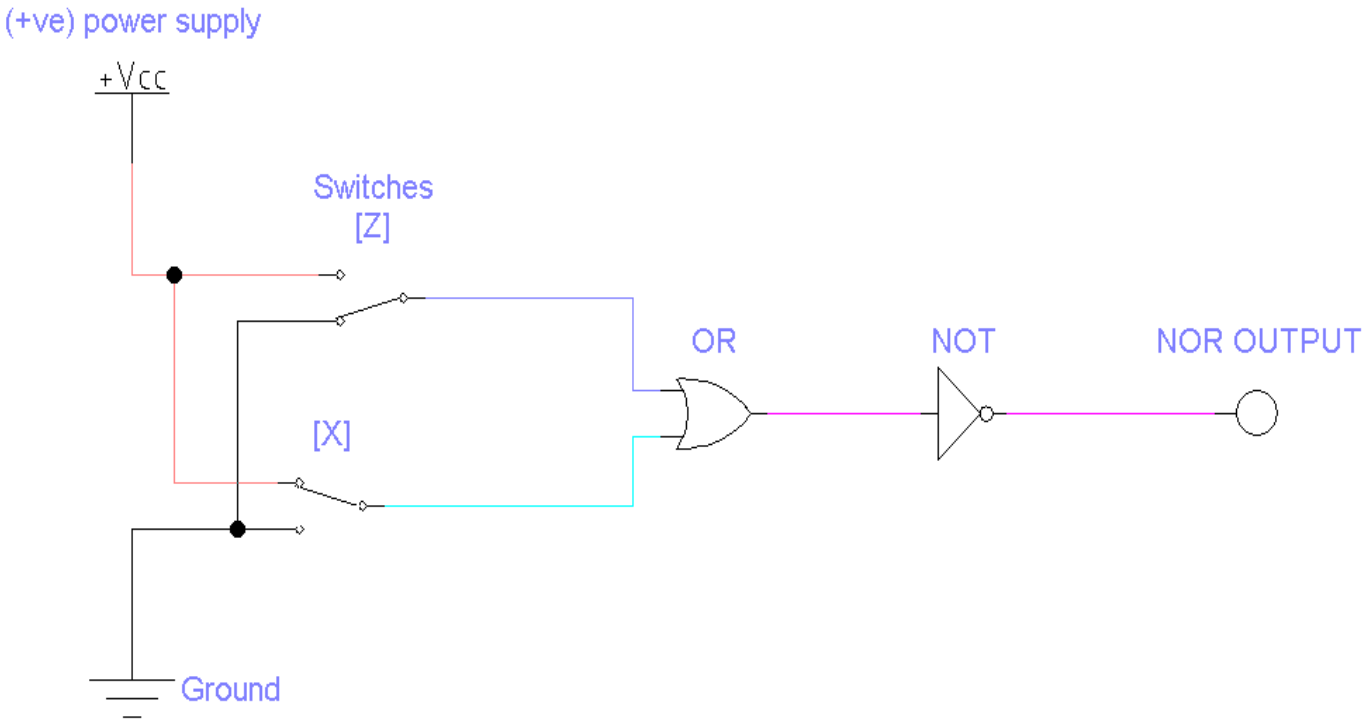
Second Combination:

- Switch Z: 1
- Switch X: 0



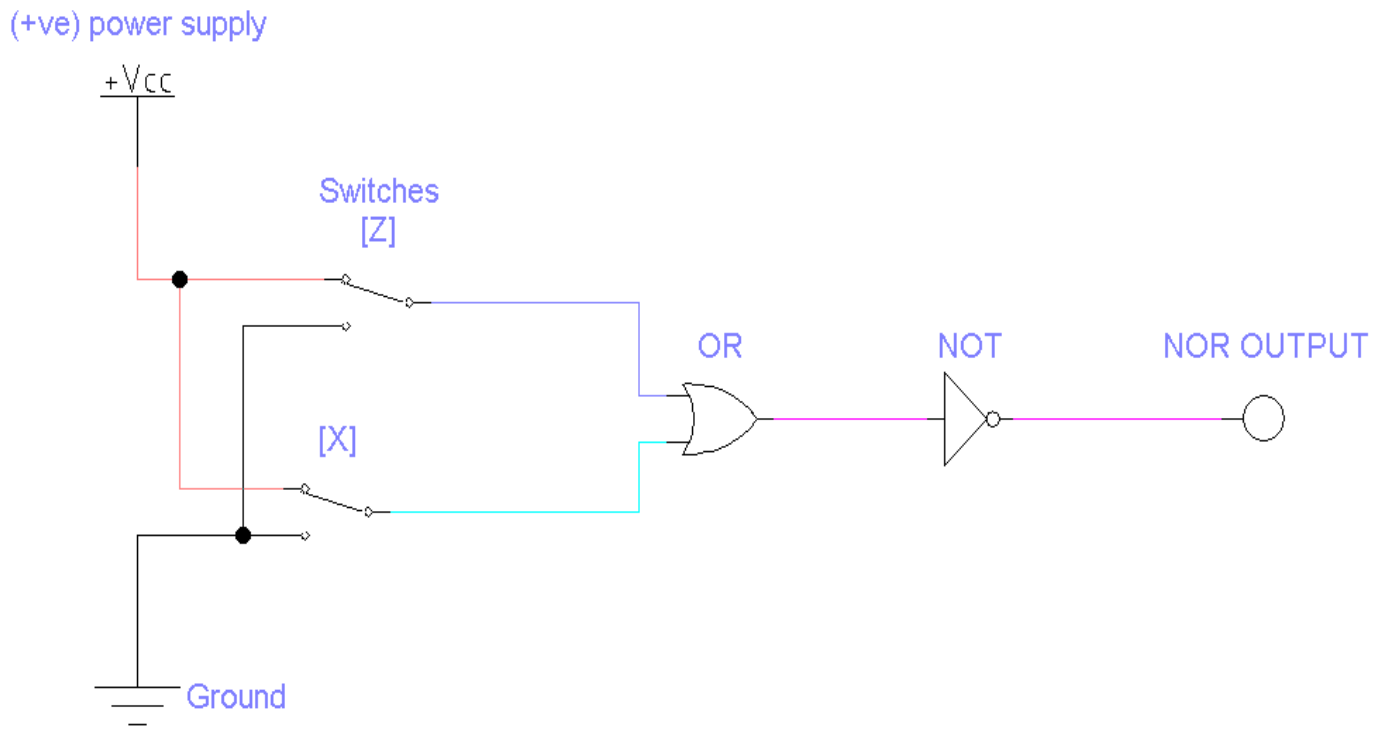
Third Combination:

- Switch Z: 0
- Switch X: 1

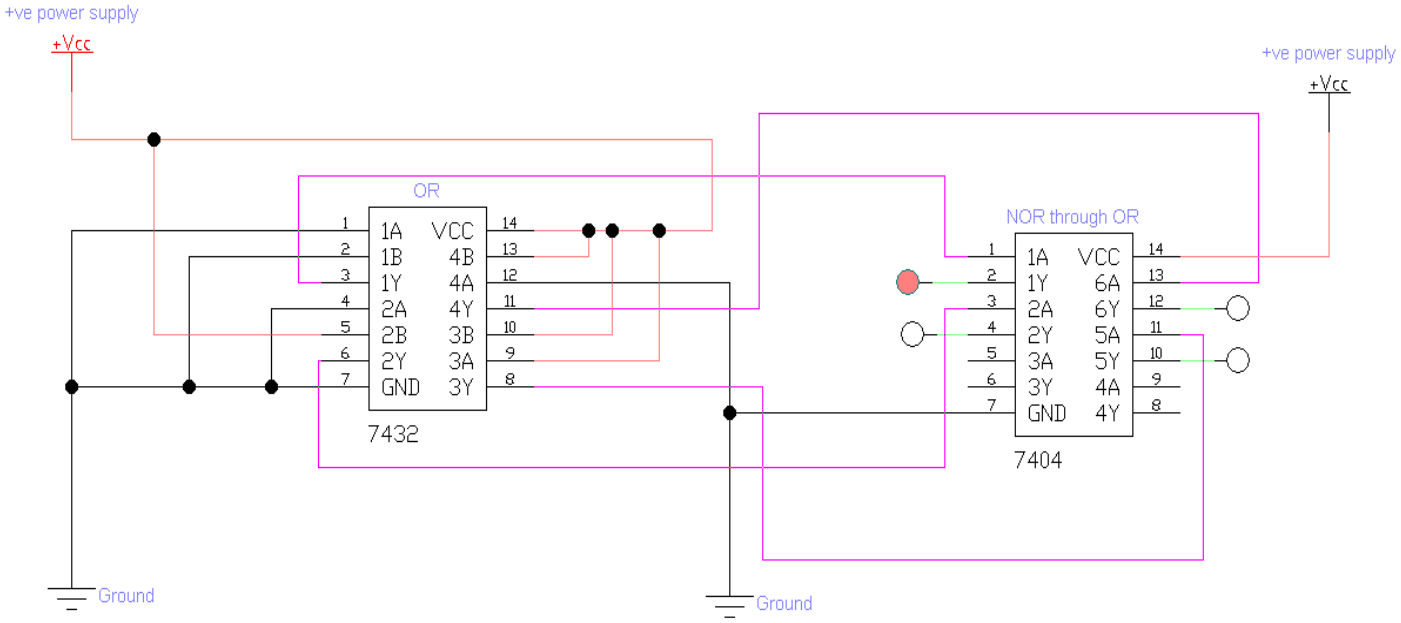


Fourth Combination:

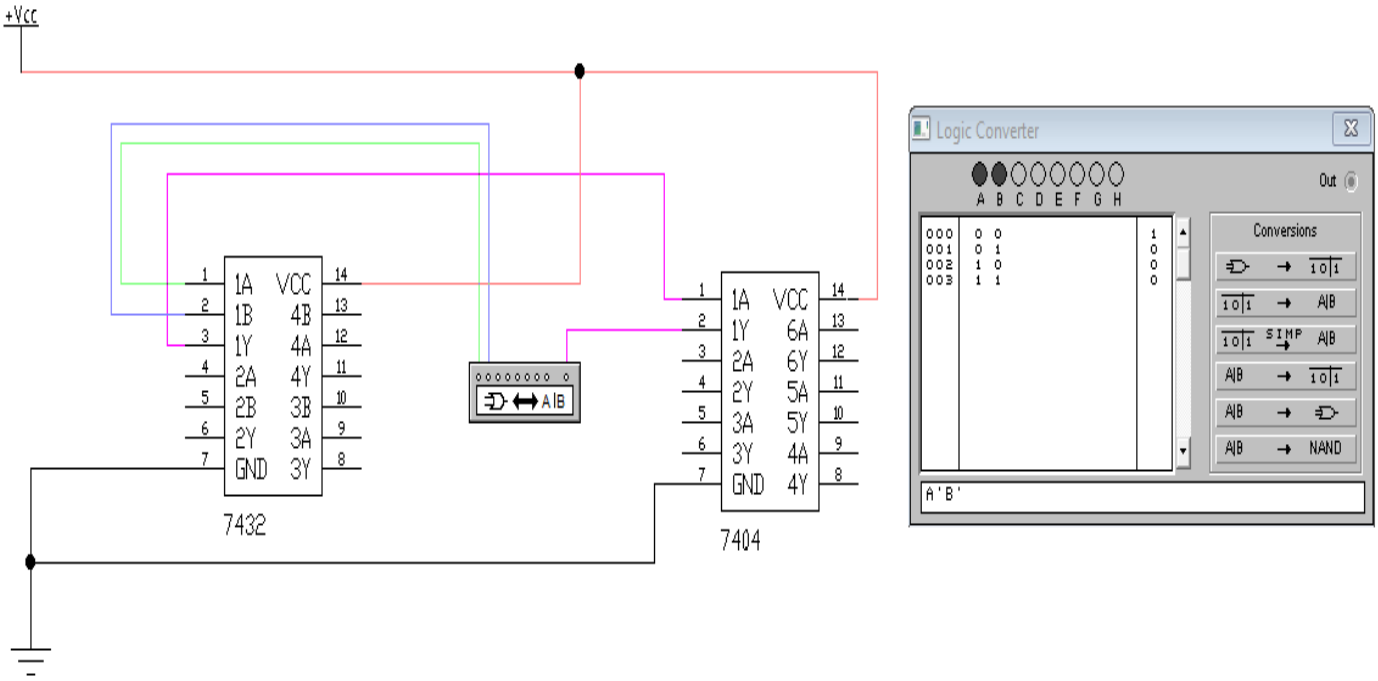
- Switch Z: 1
- Switch X: 1



2: Verification using ICs



3: Verification by truth table



Experiment on Hardware