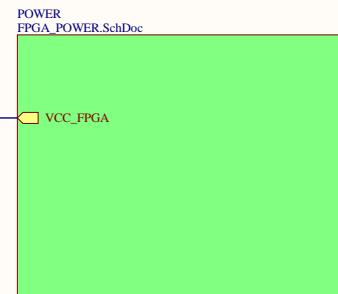
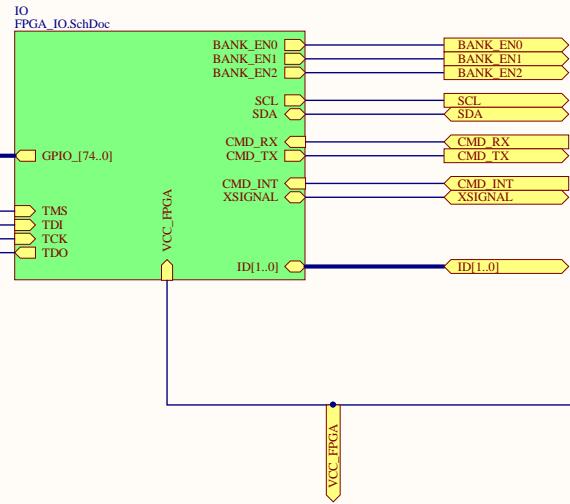
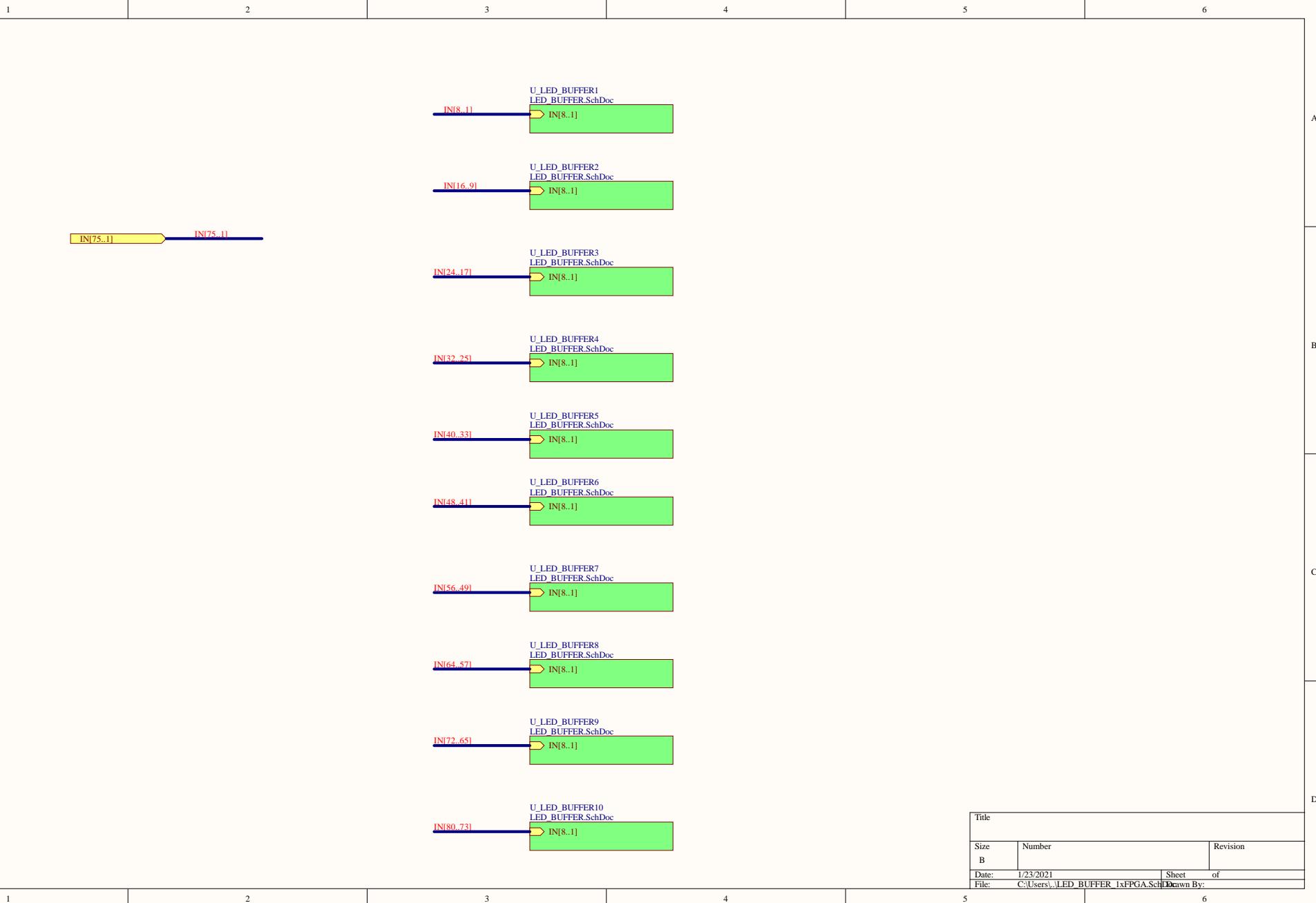


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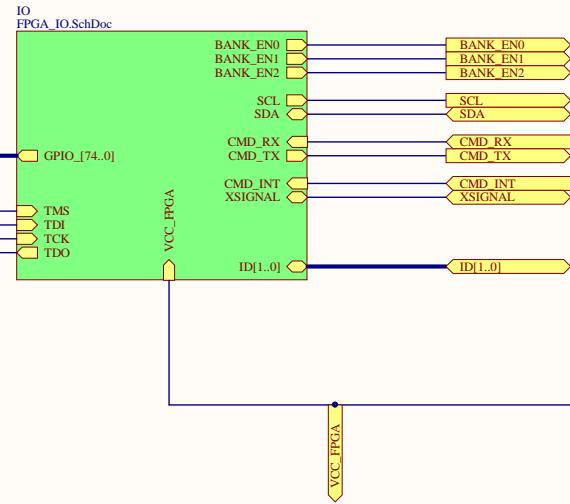
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1 2 3 4 5 6

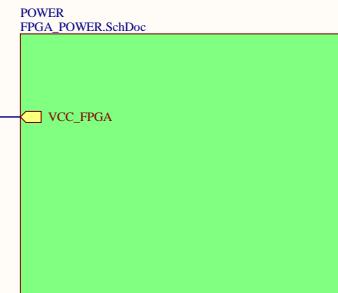
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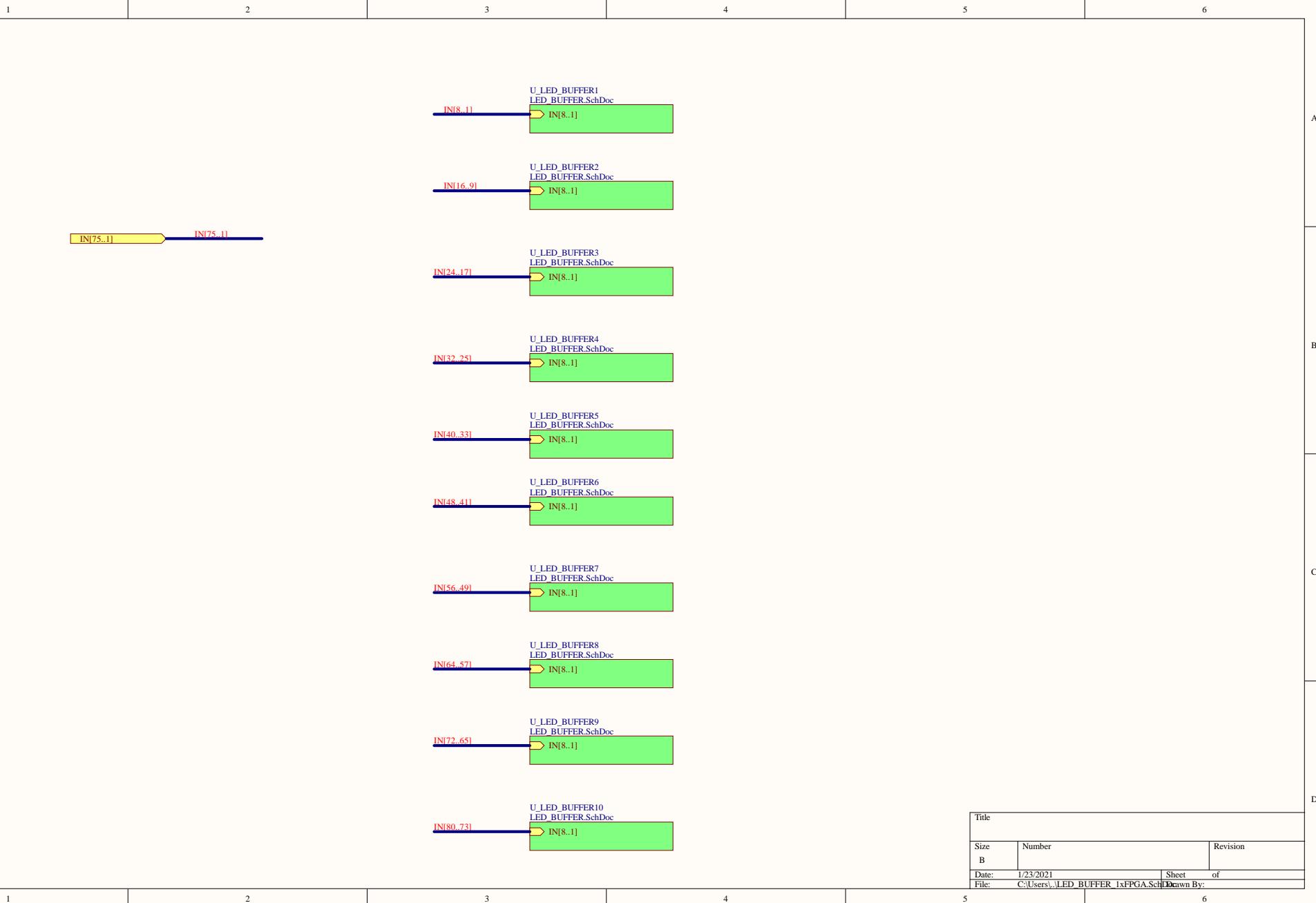


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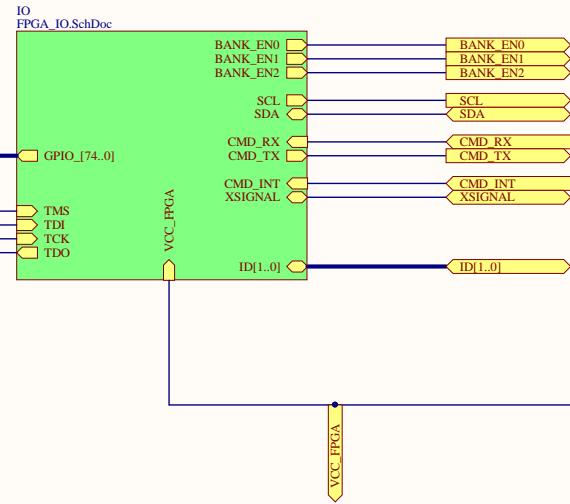
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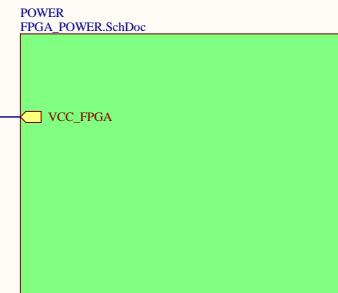
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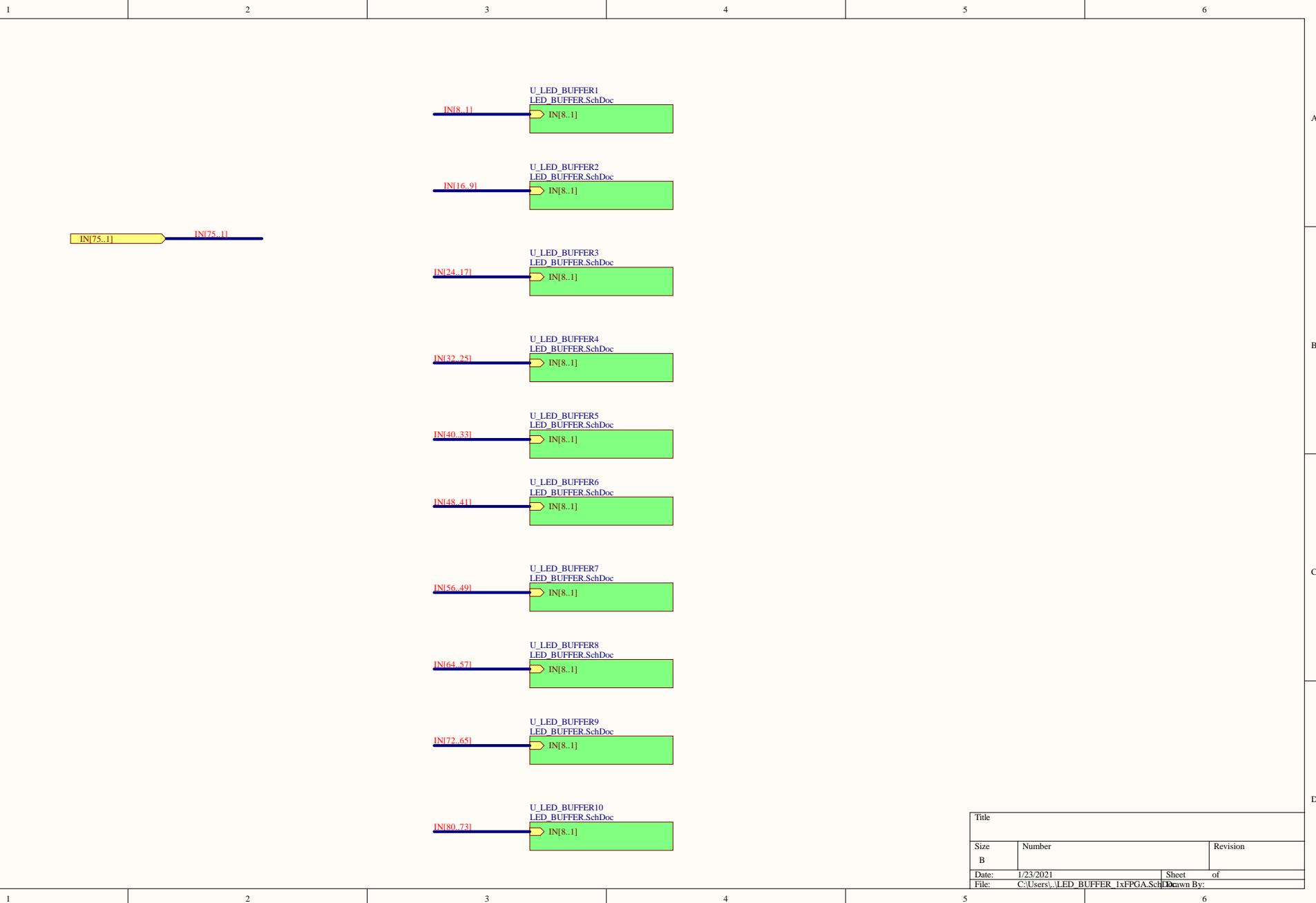


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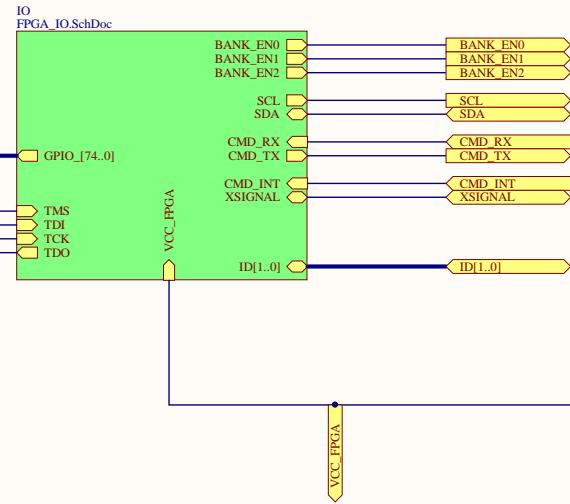
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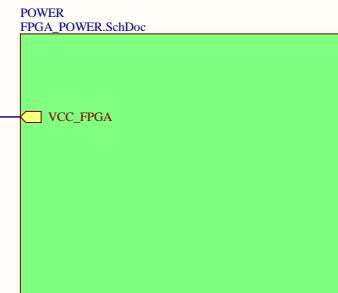
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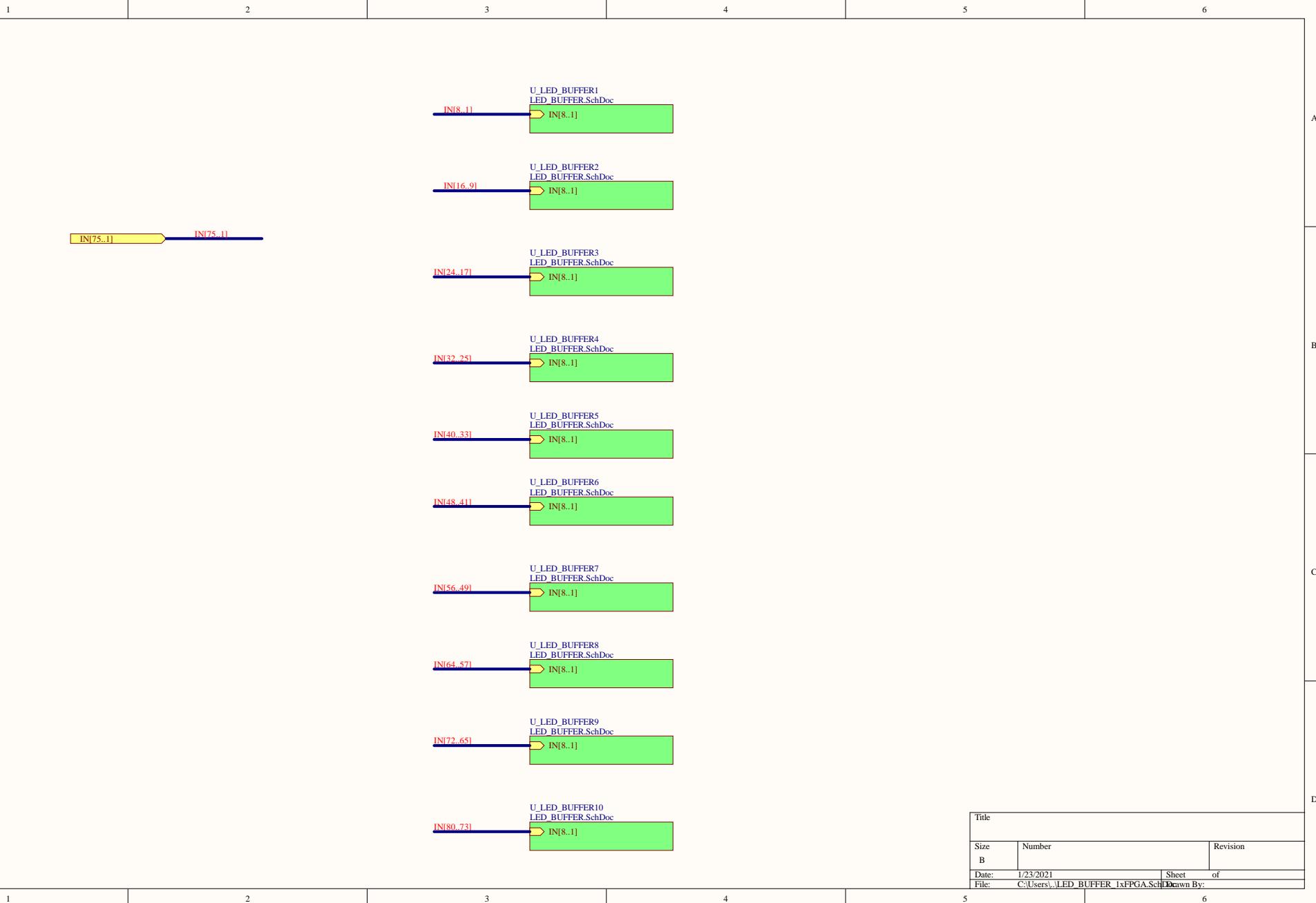


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C

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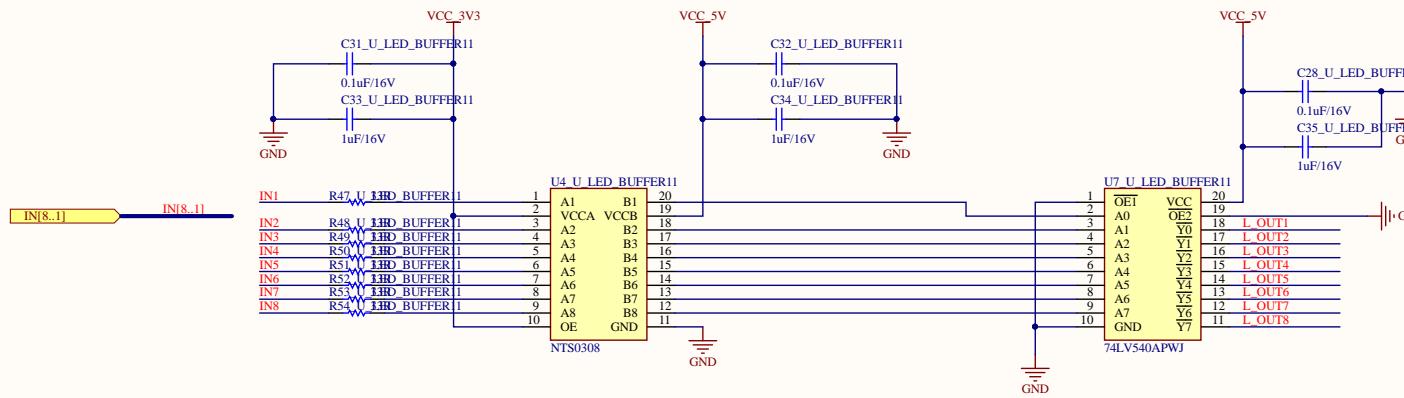
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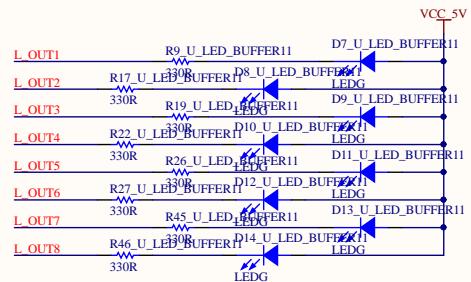
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INx are outputs of FPGA switching at 1Mhz.
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Logic Low = 0V

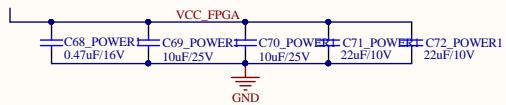
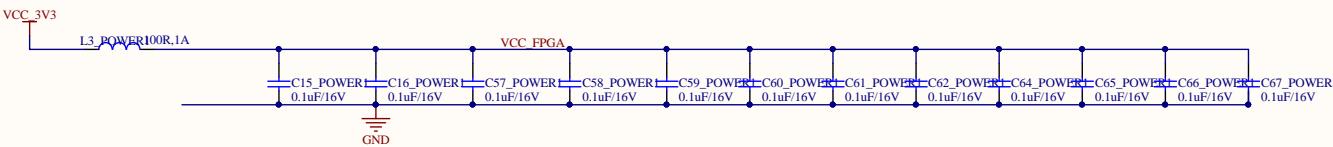
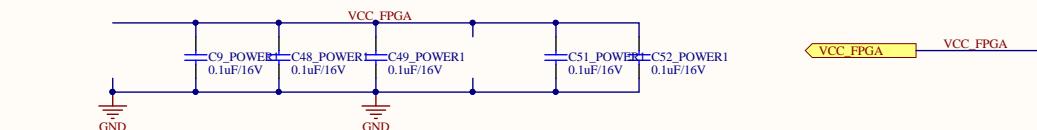
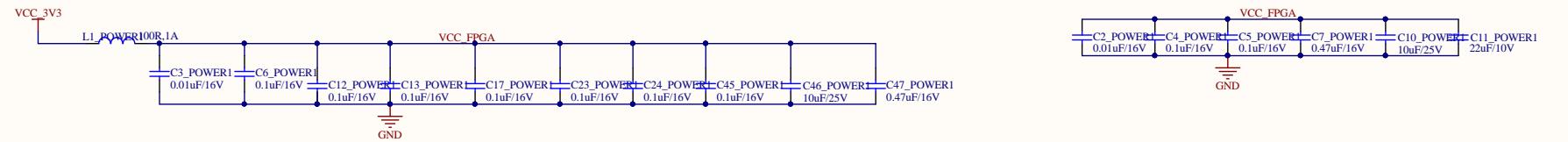
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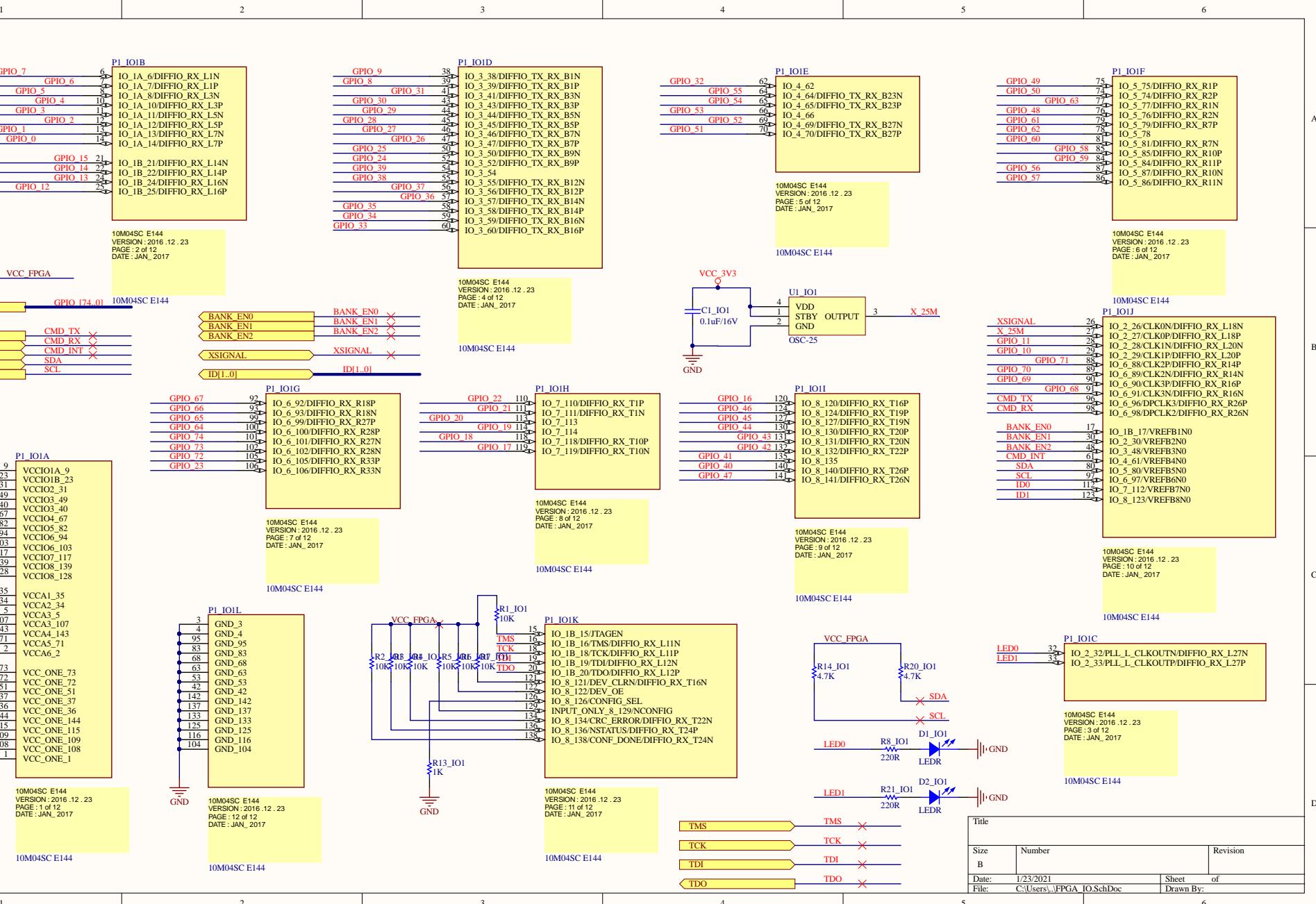
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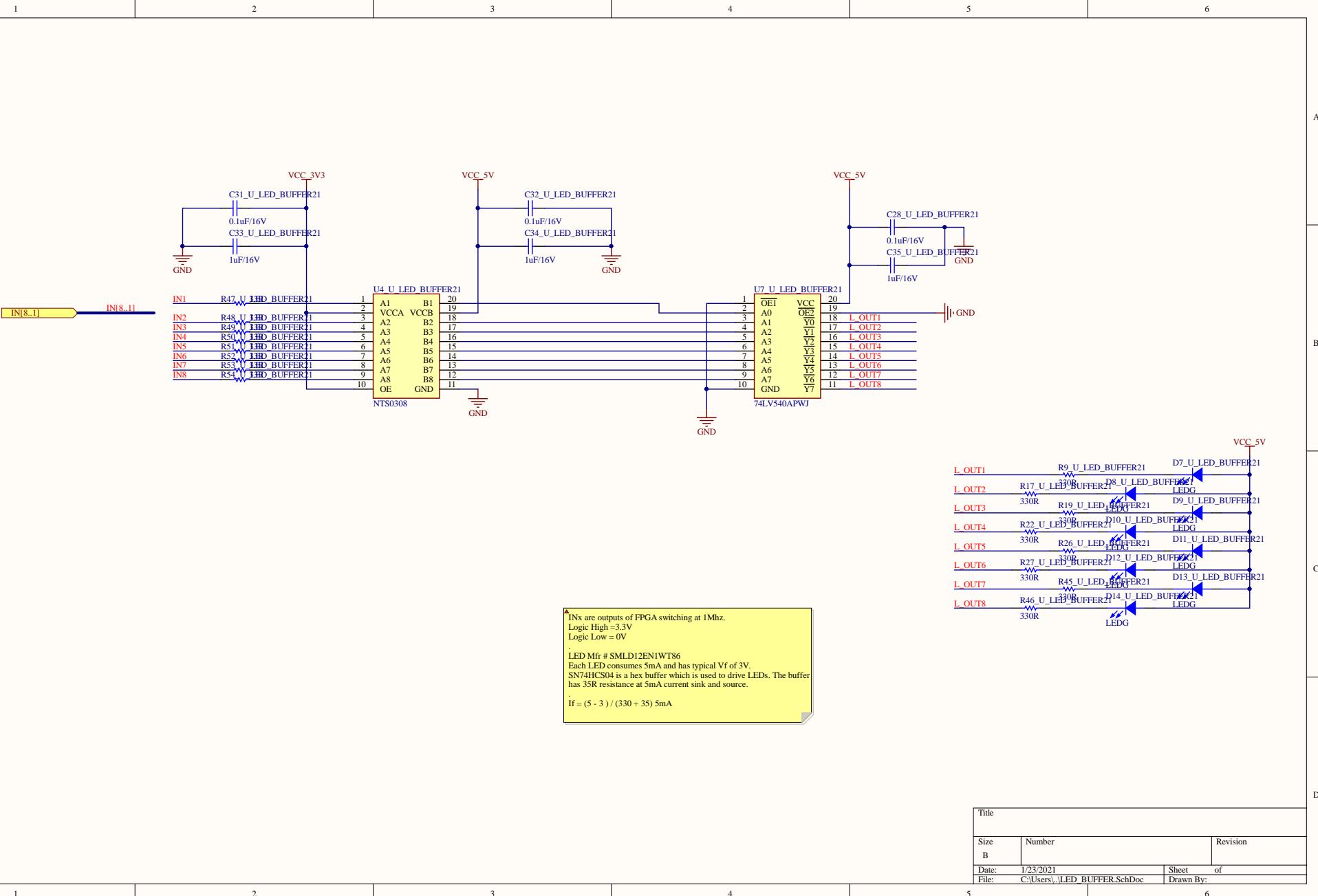
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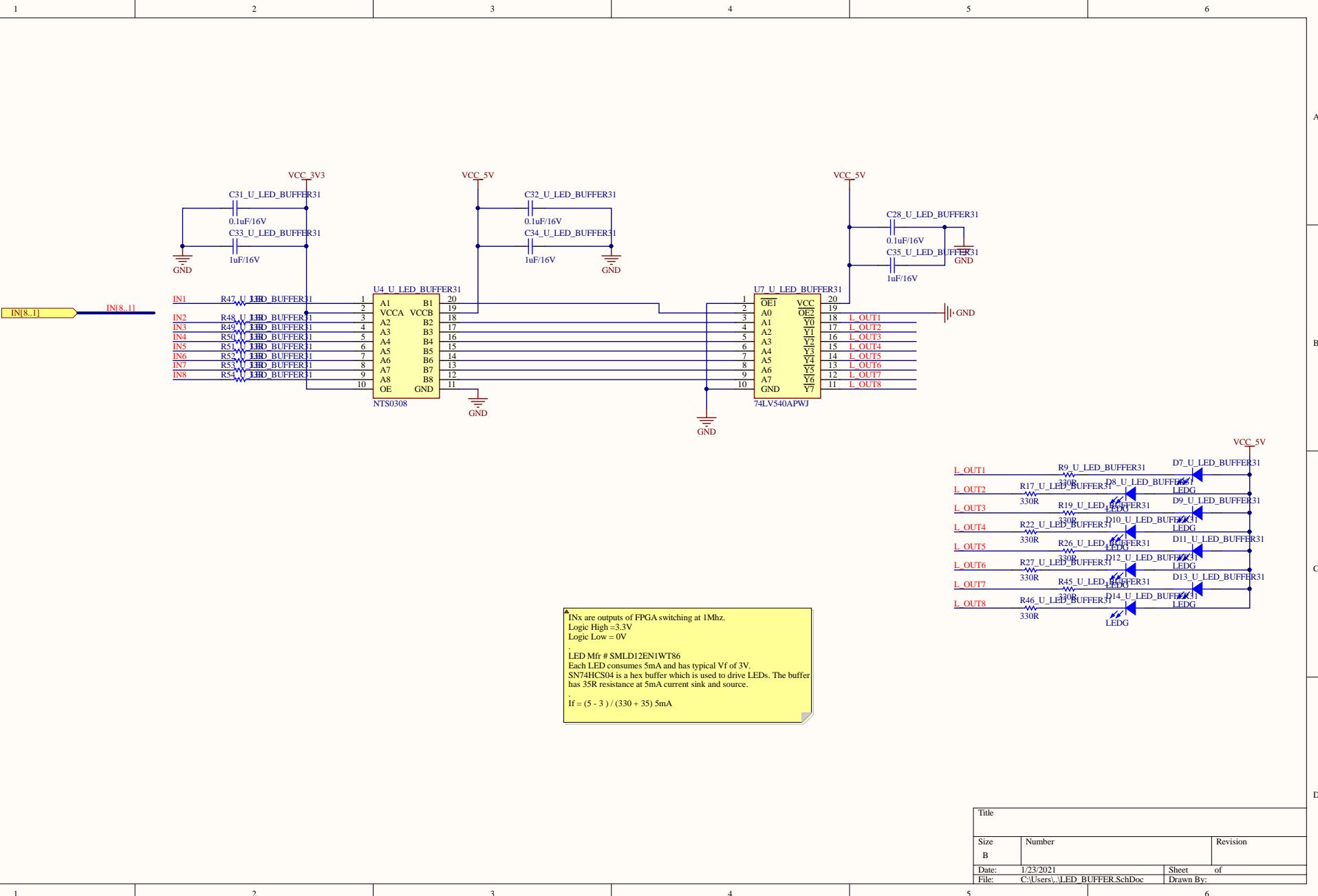


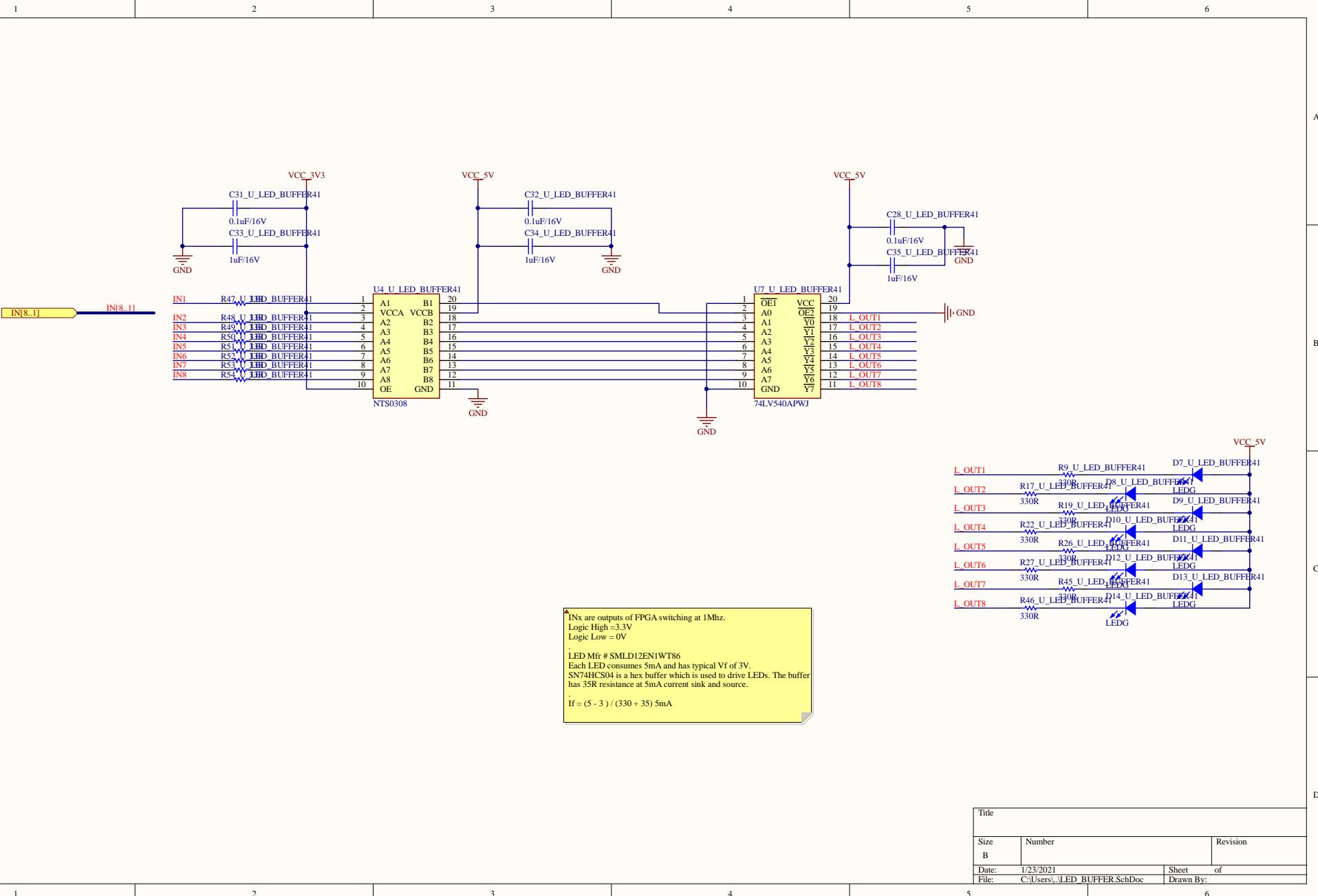
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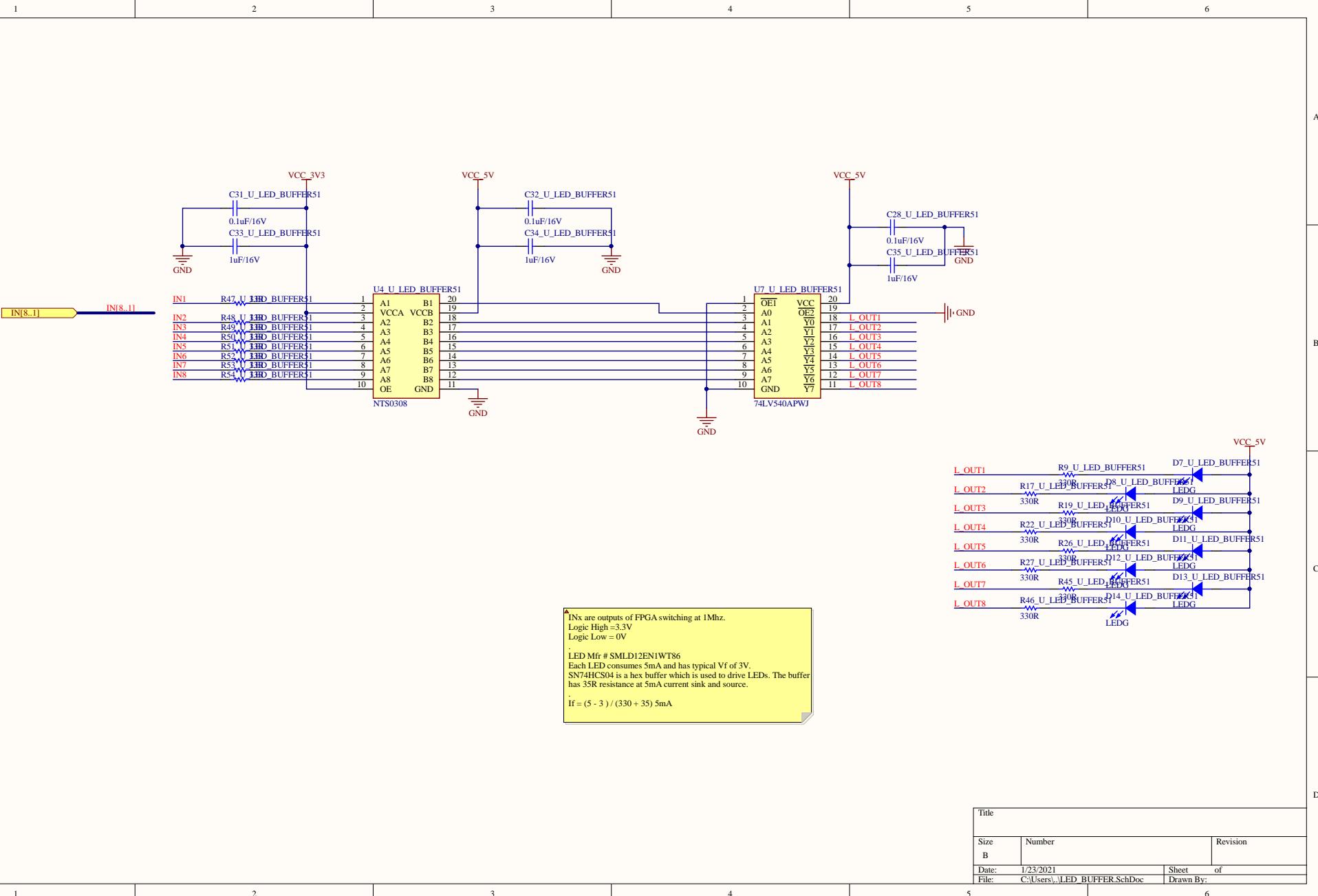
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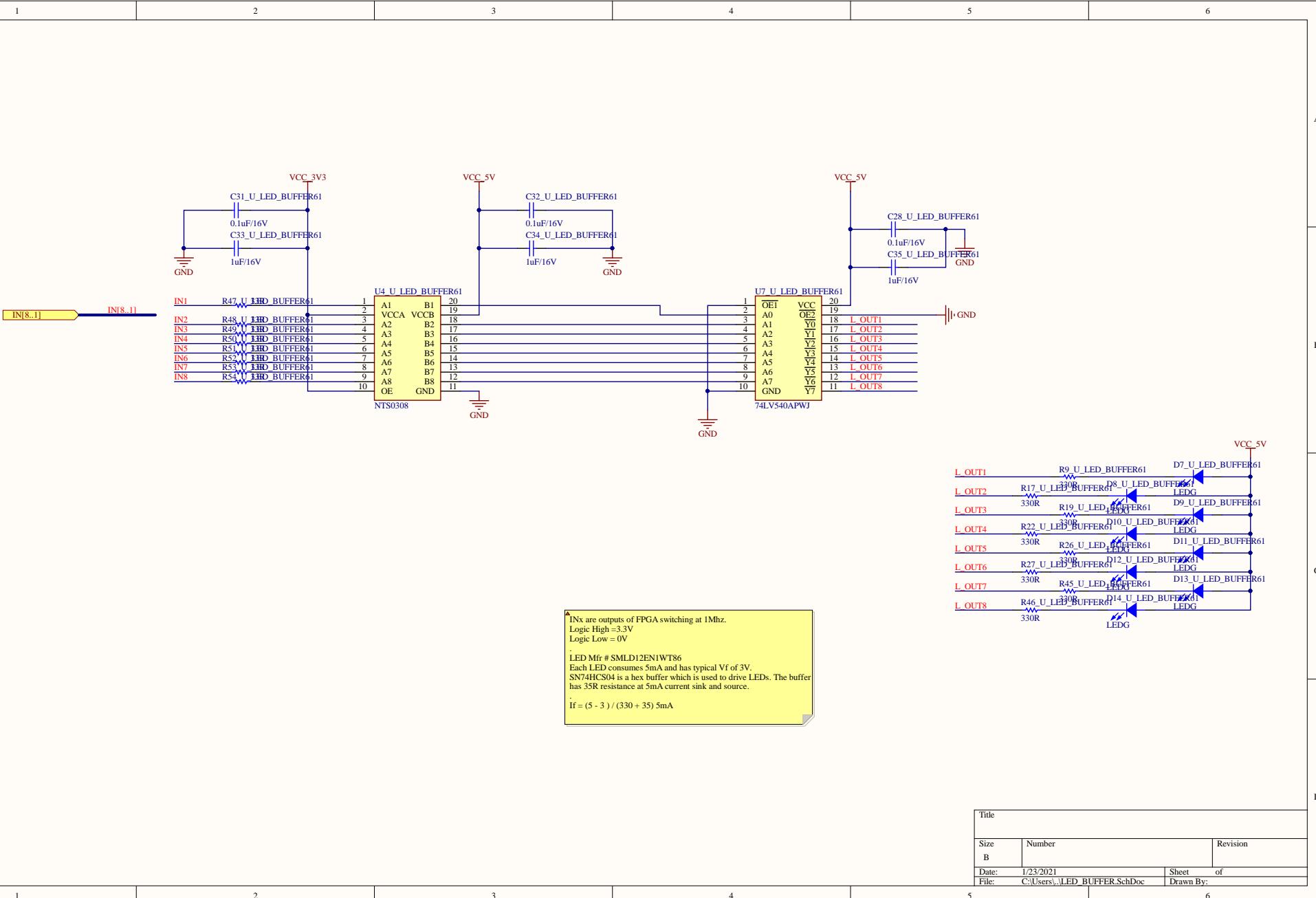


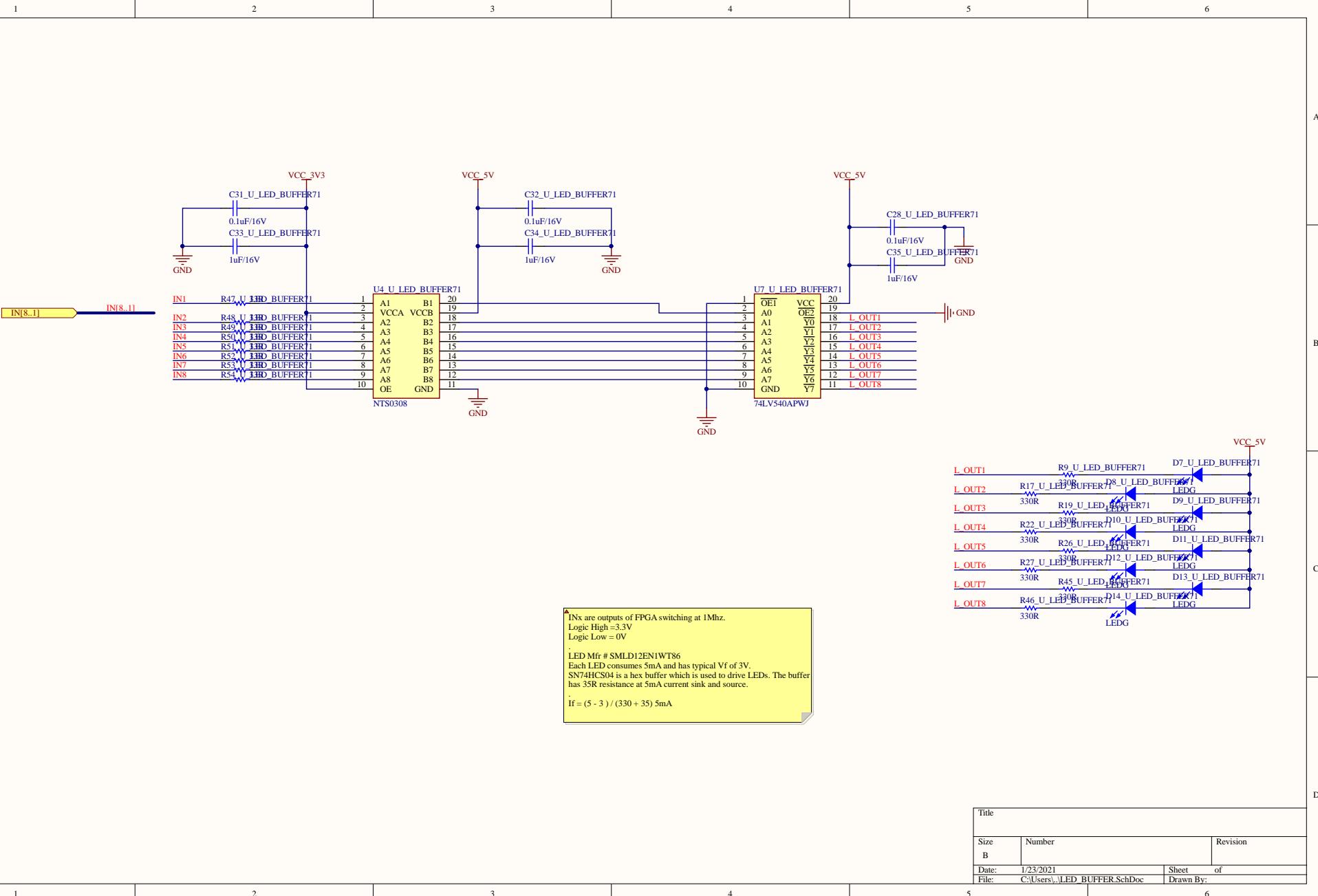


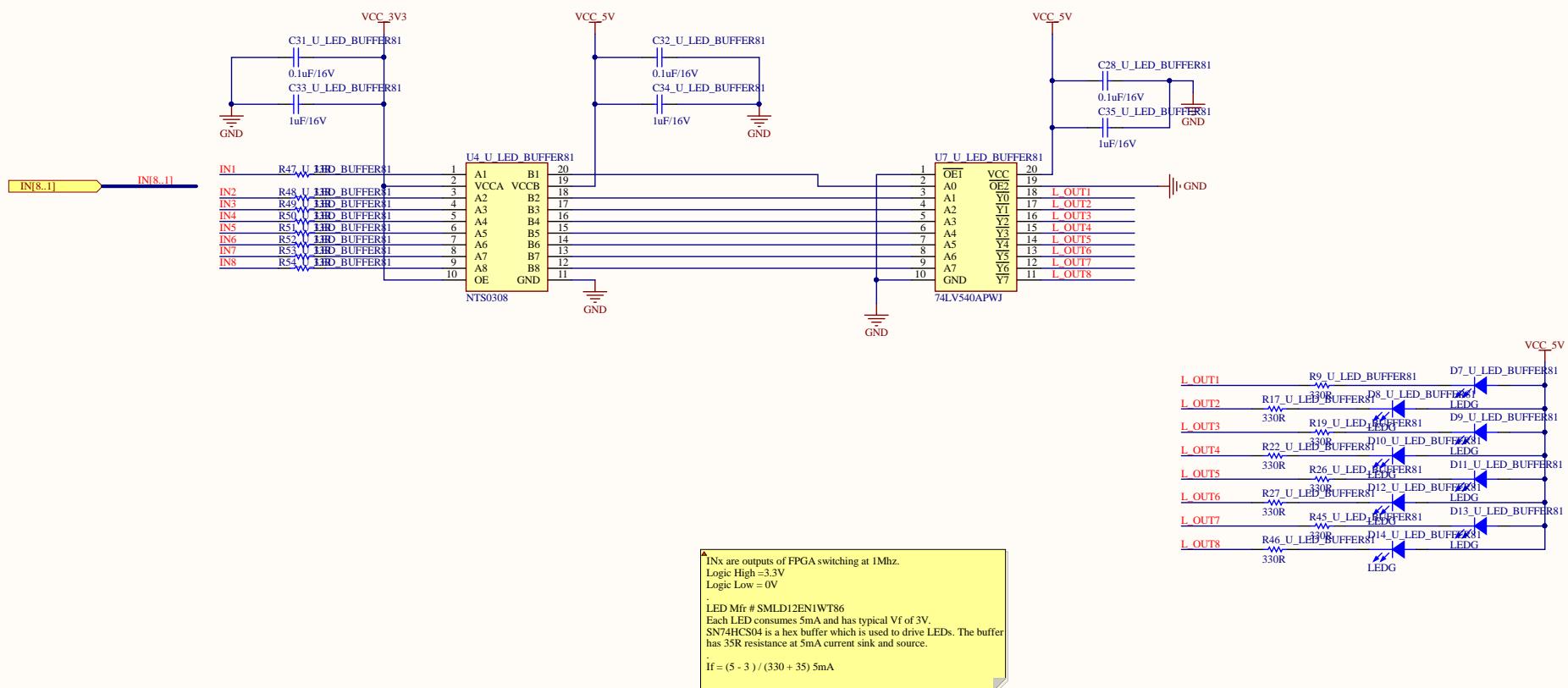




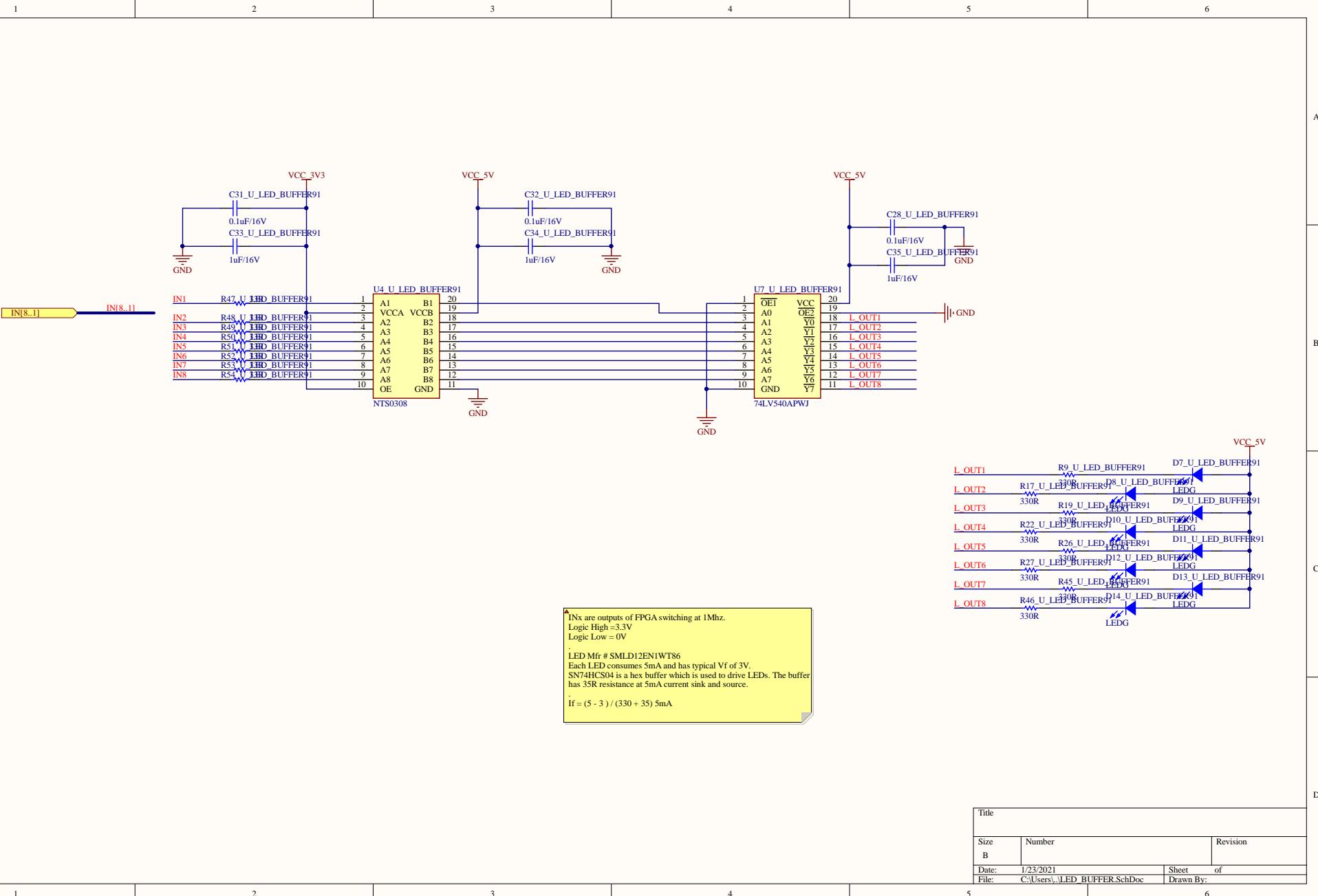








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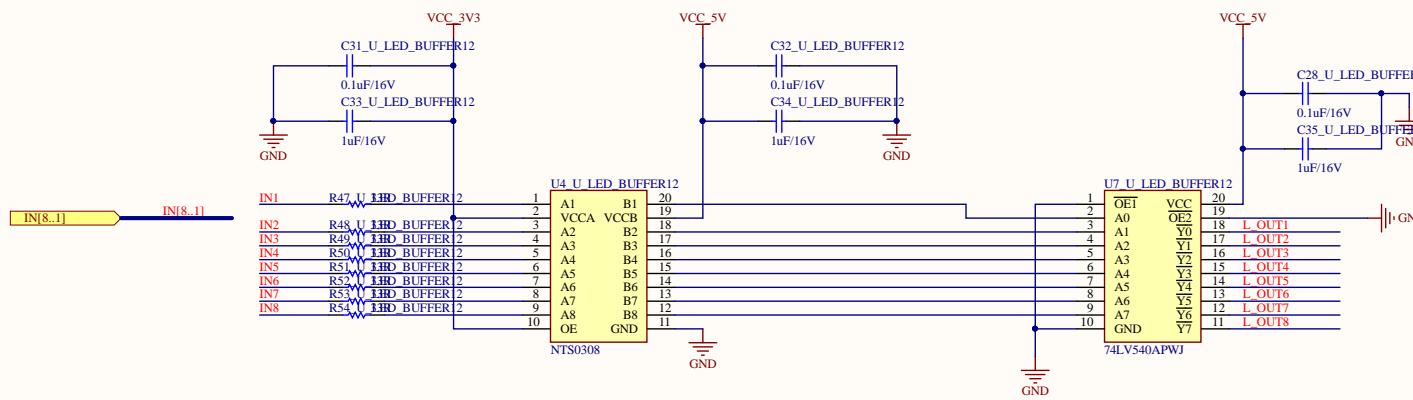
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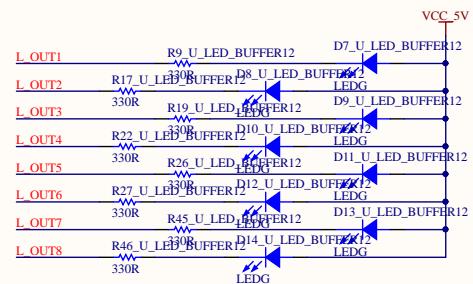
D



INx are outputs of FPGA switching at 1Mhz.
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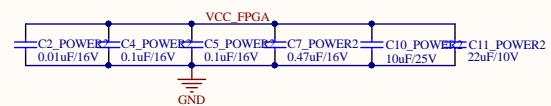
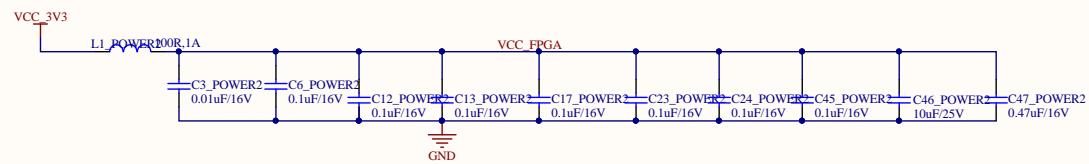
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Title		
Size	Number	Revision
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File: C:\Users\LED BUFFER.SchDoc	Drawn By:	

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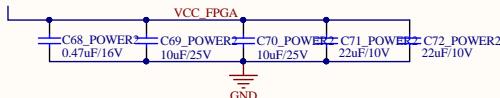
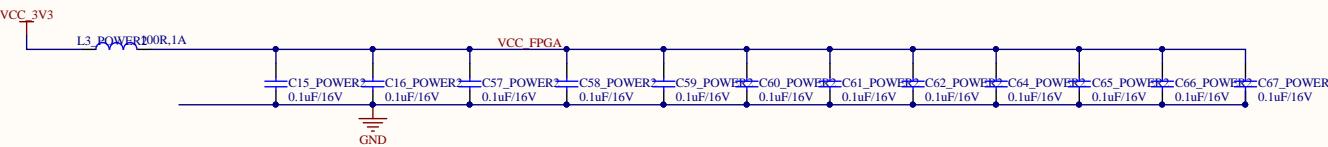
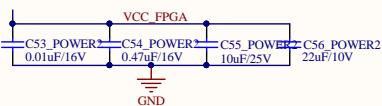
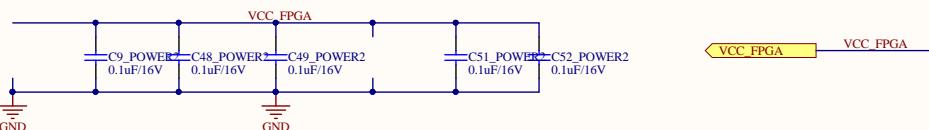
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C

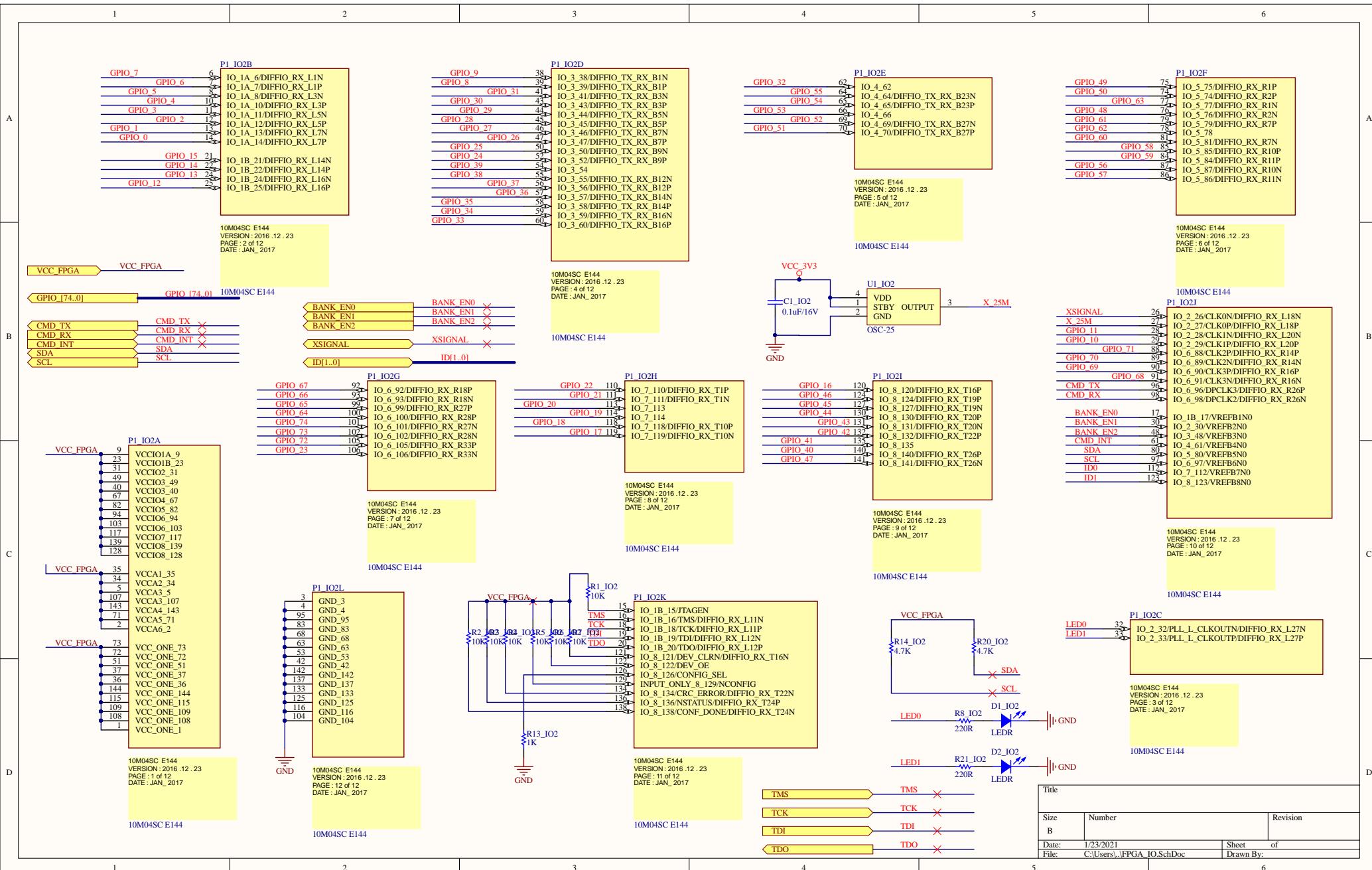
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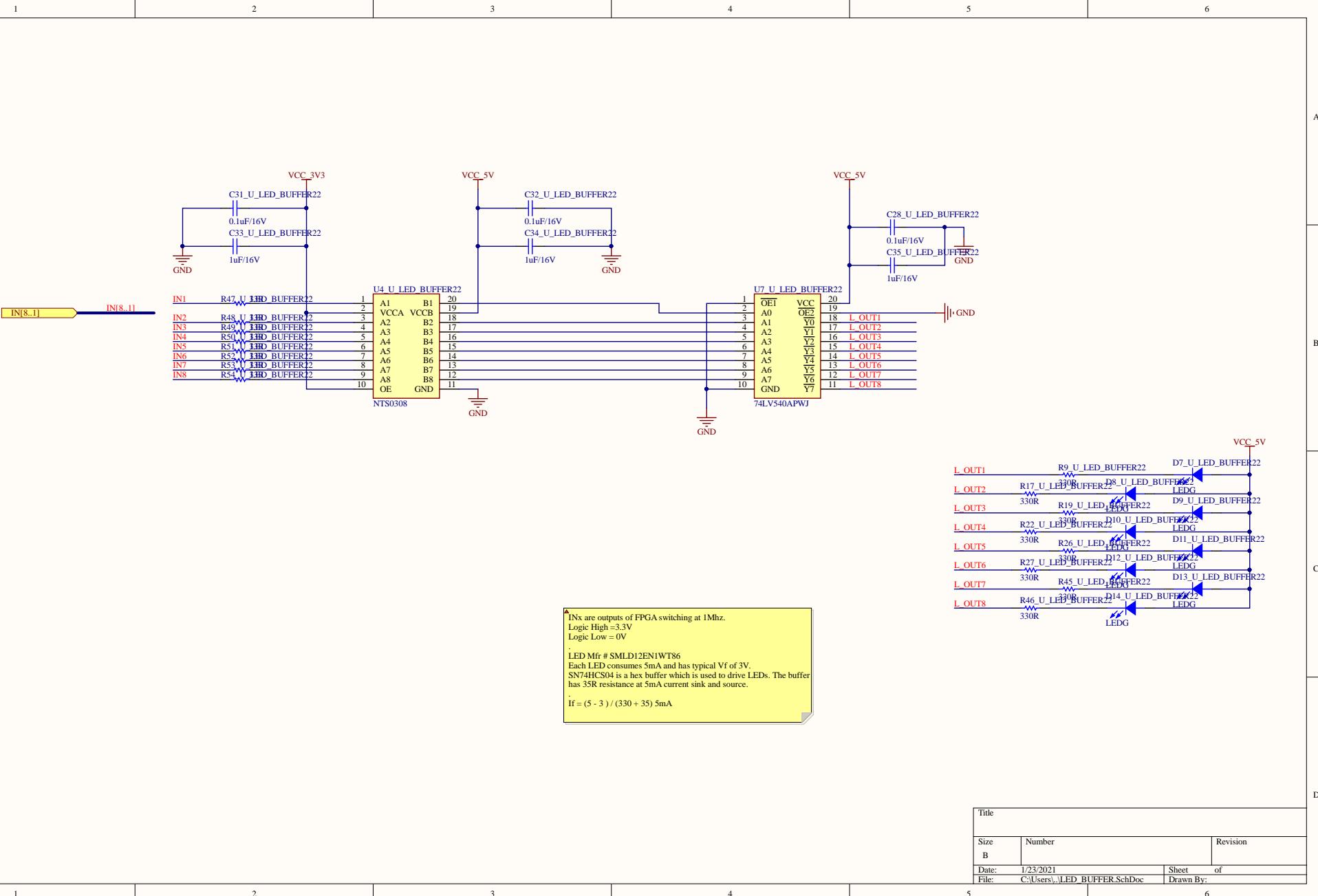
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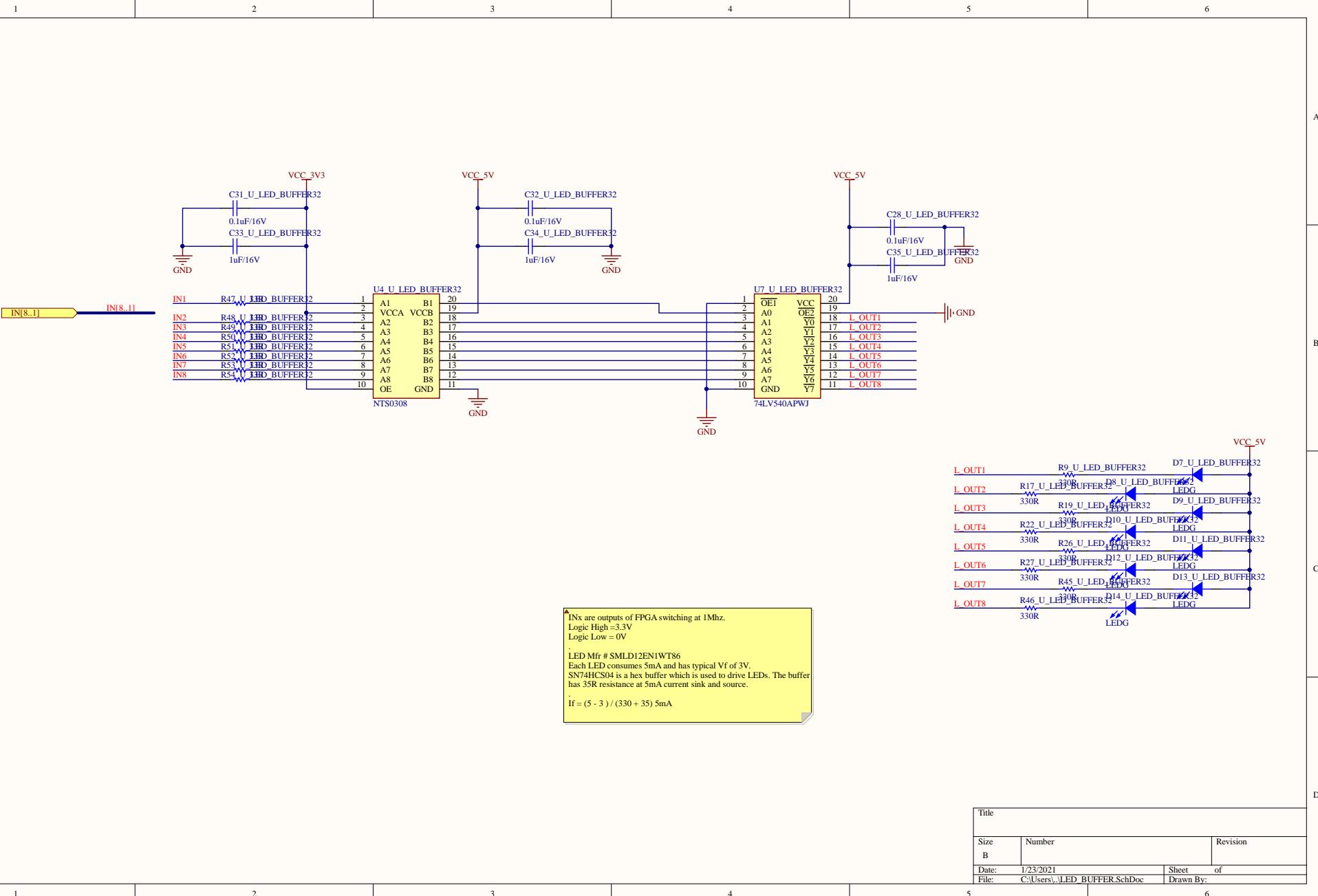


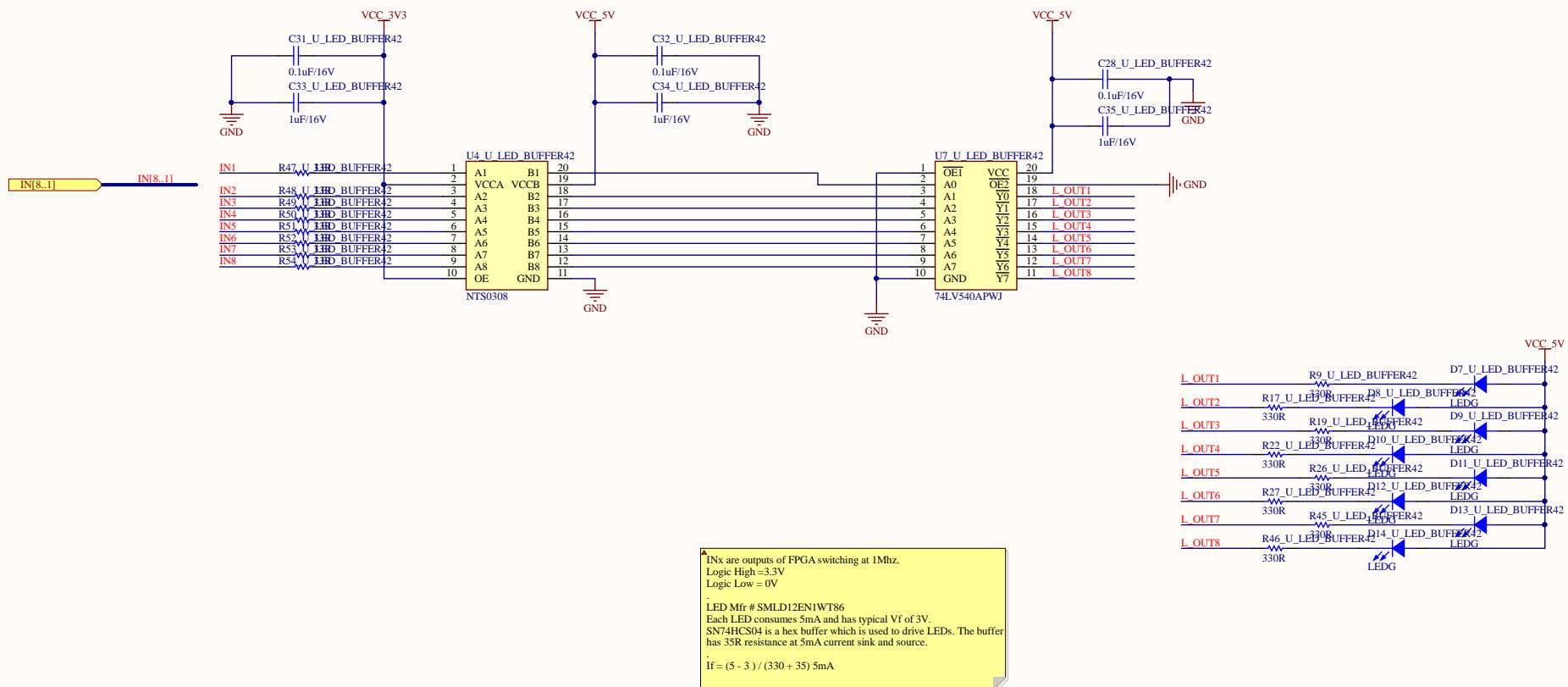
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1 2 3 4 5 6









Title		
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File: C:\Users\LED BUFFER.SchDoc		Drawn By:

1 2 3 4 5 6

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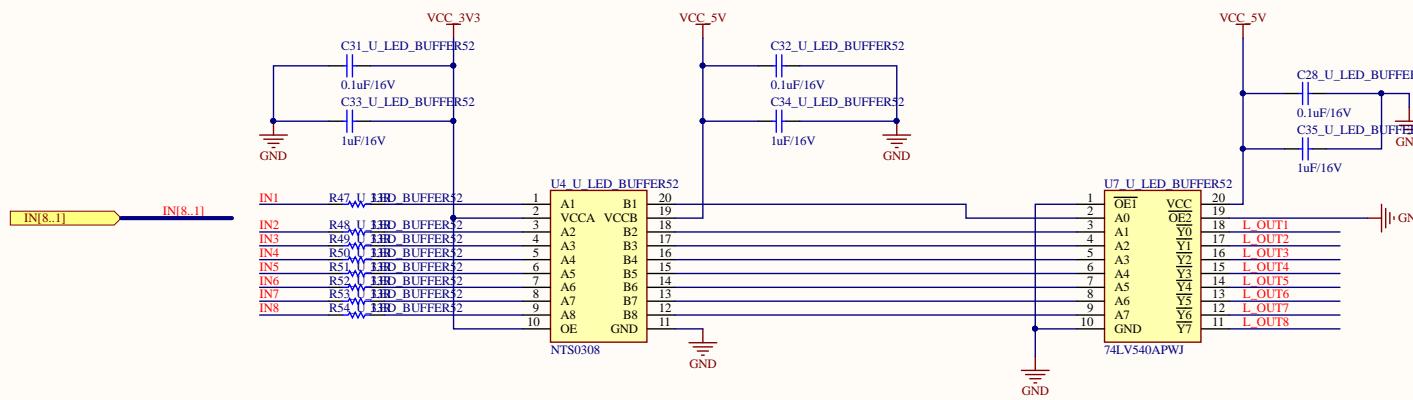
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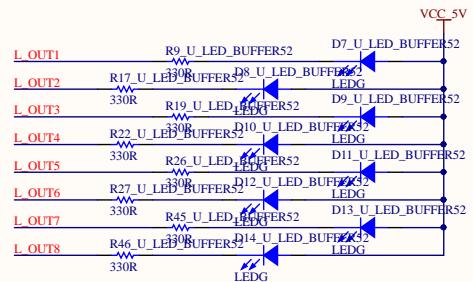
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1 2 3 4 5 6

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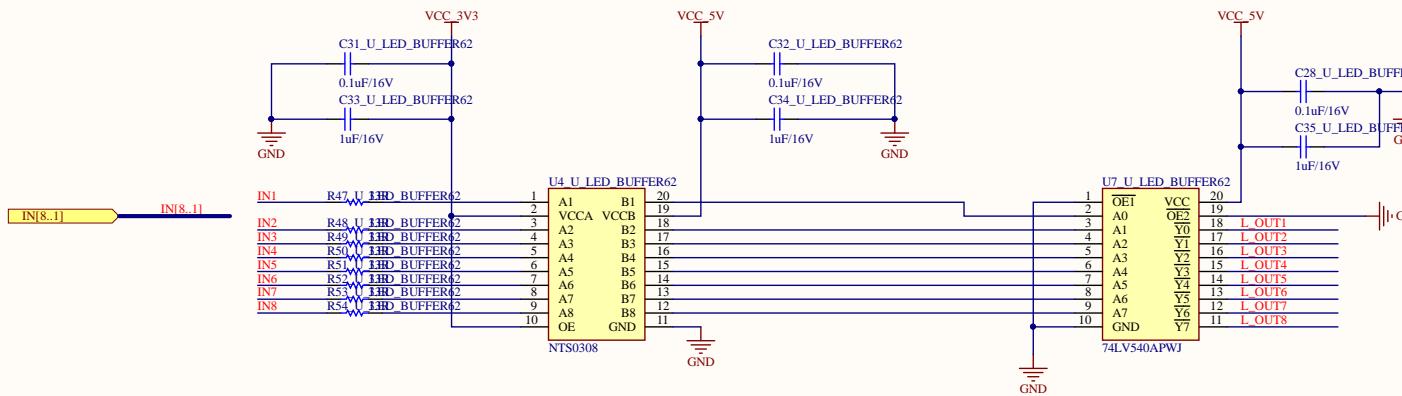
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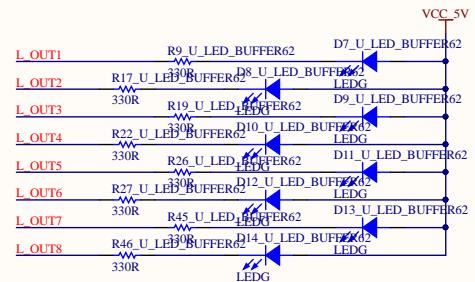
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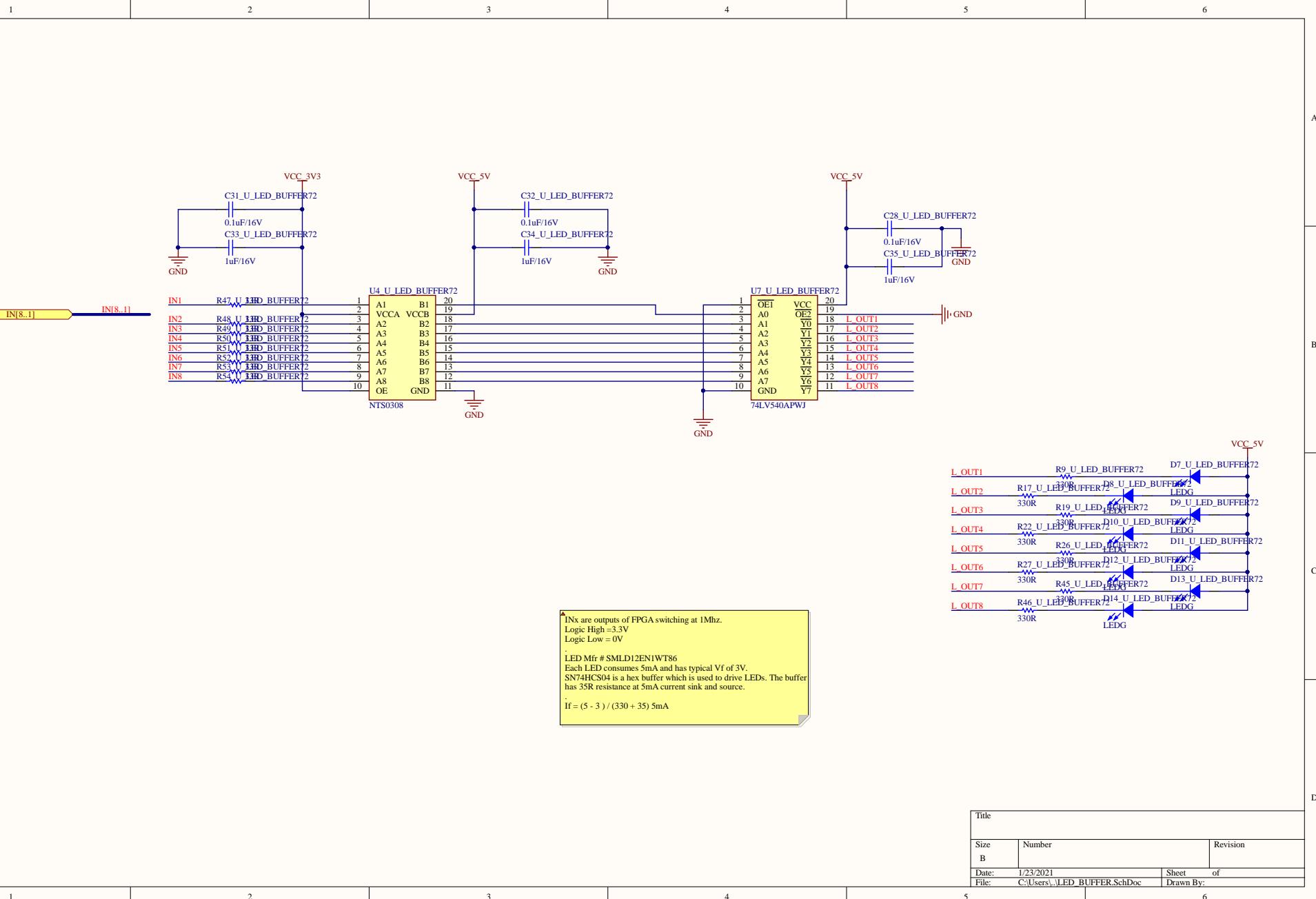
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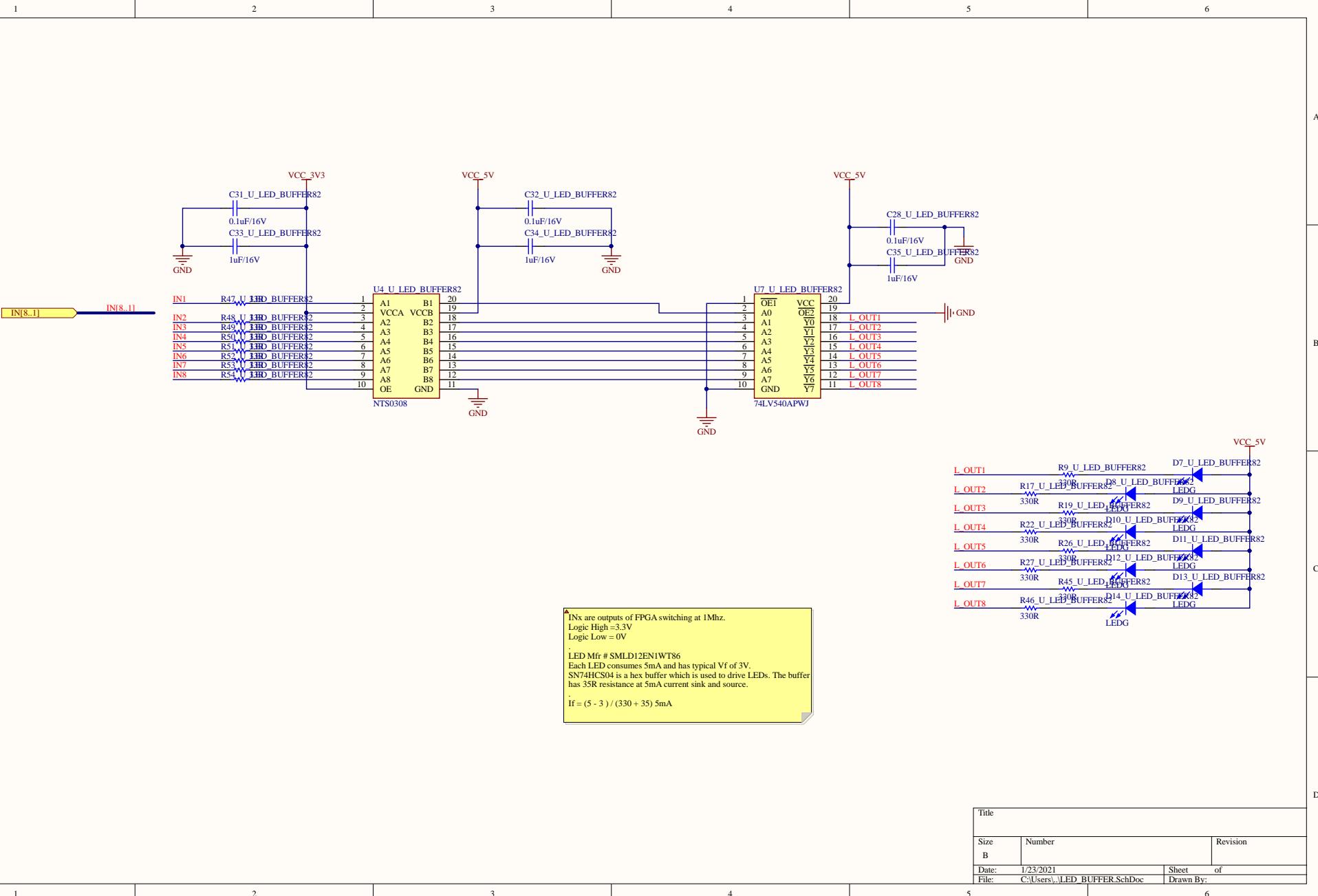
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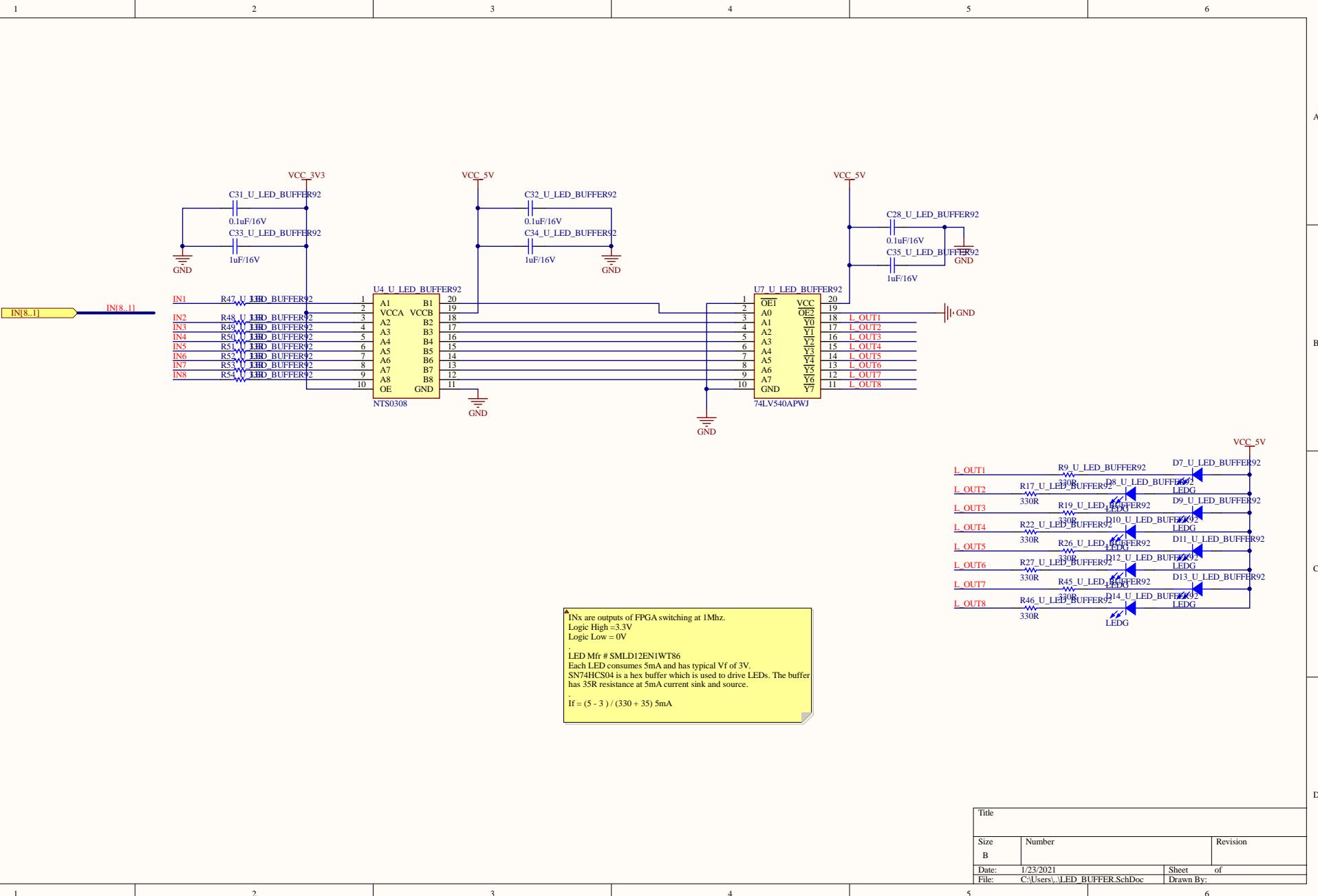


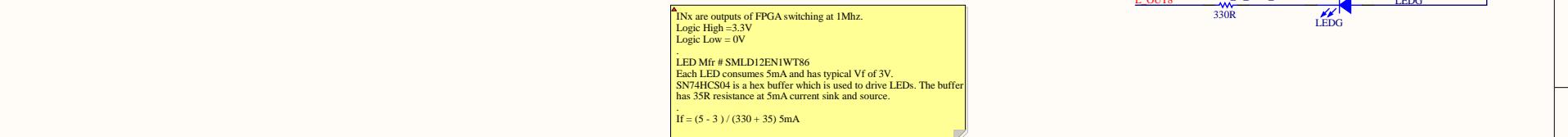
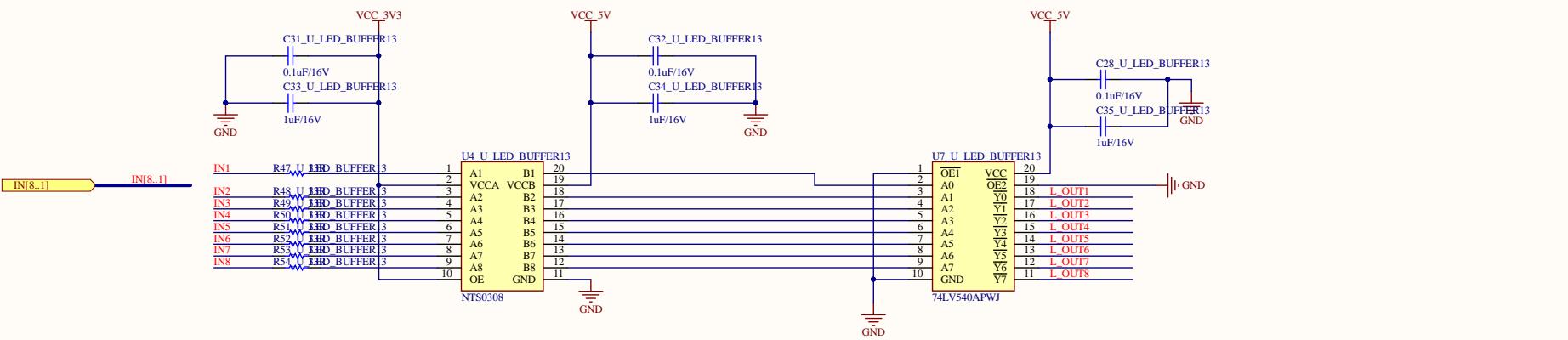
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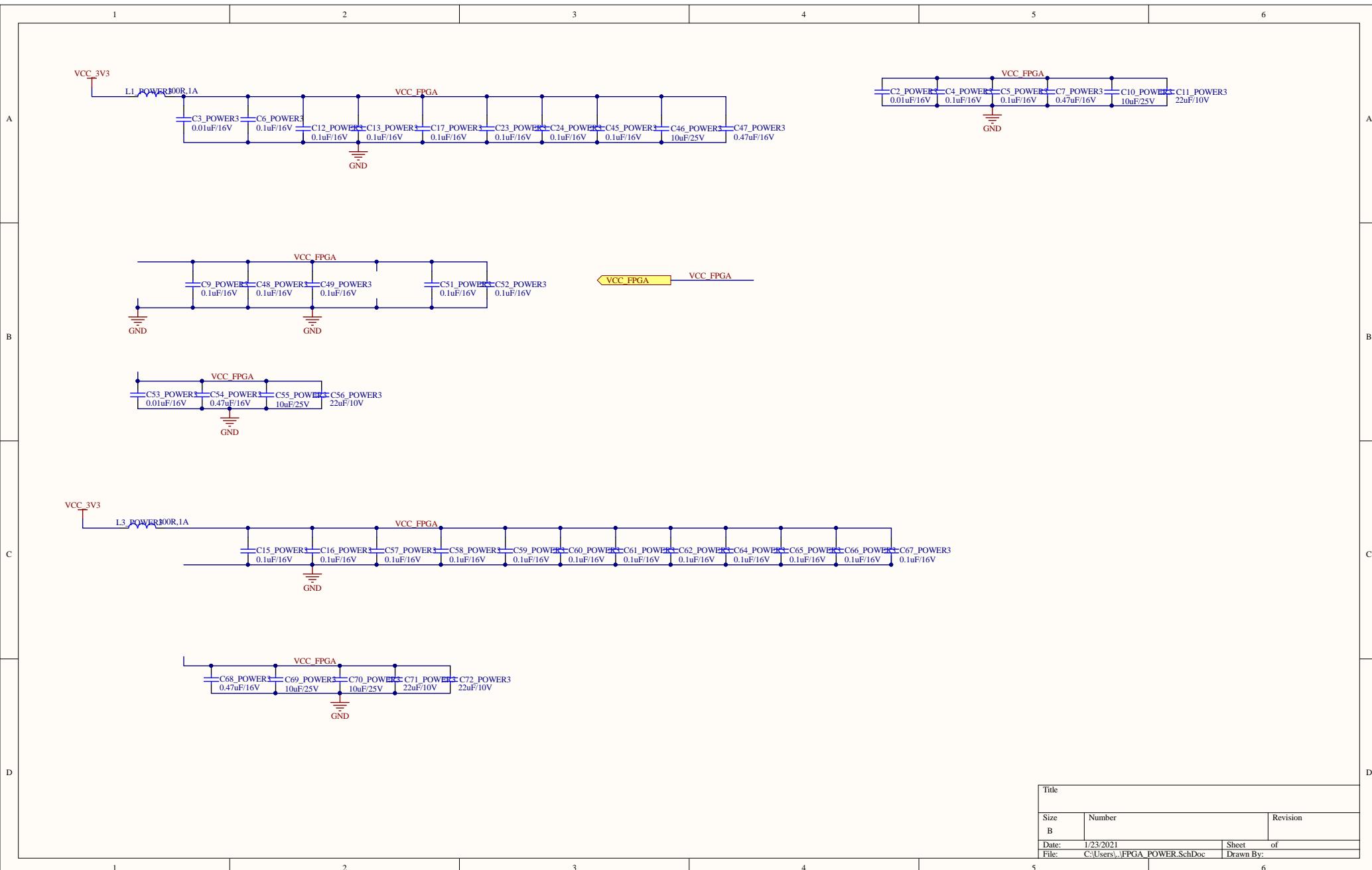


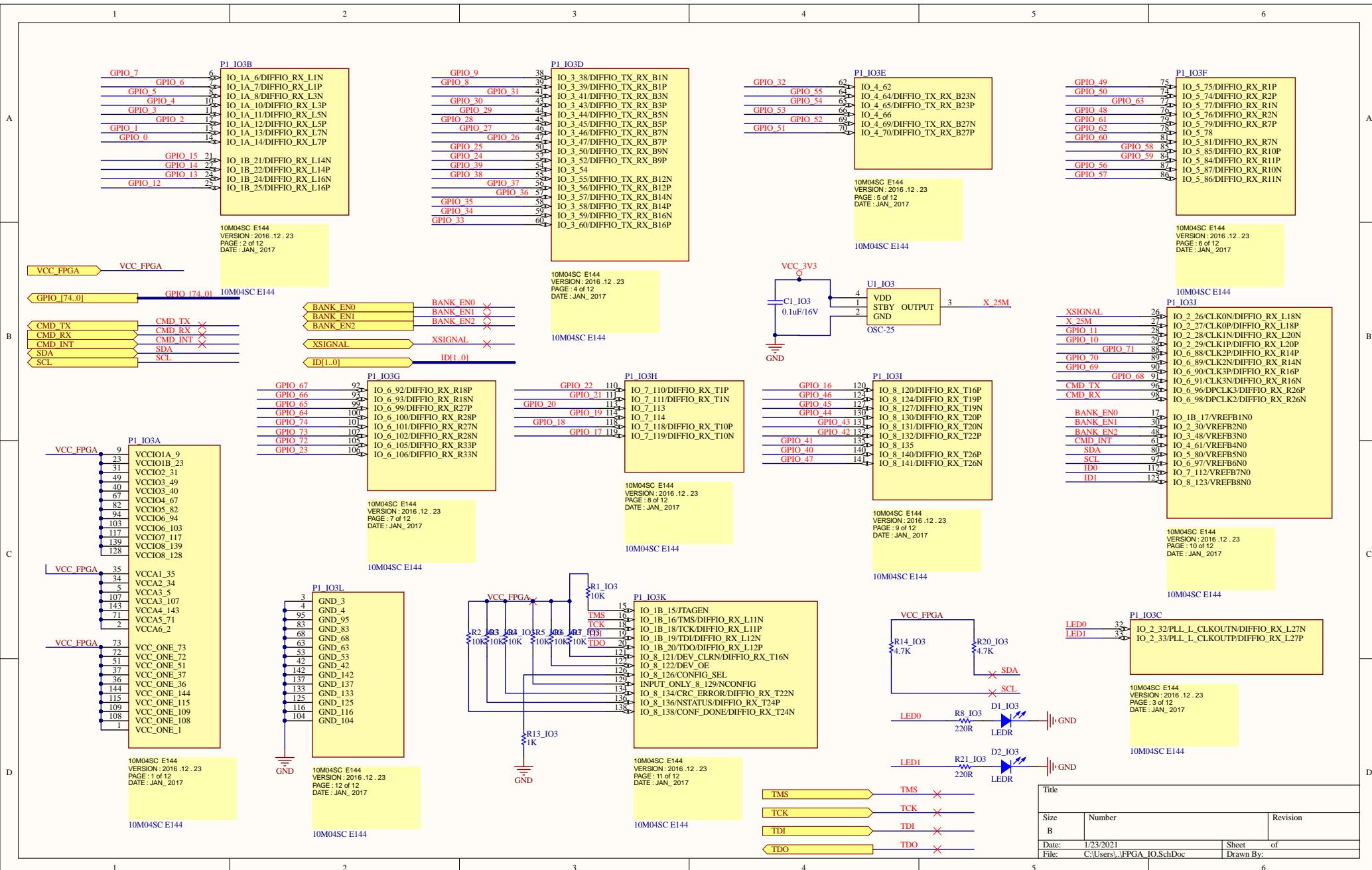
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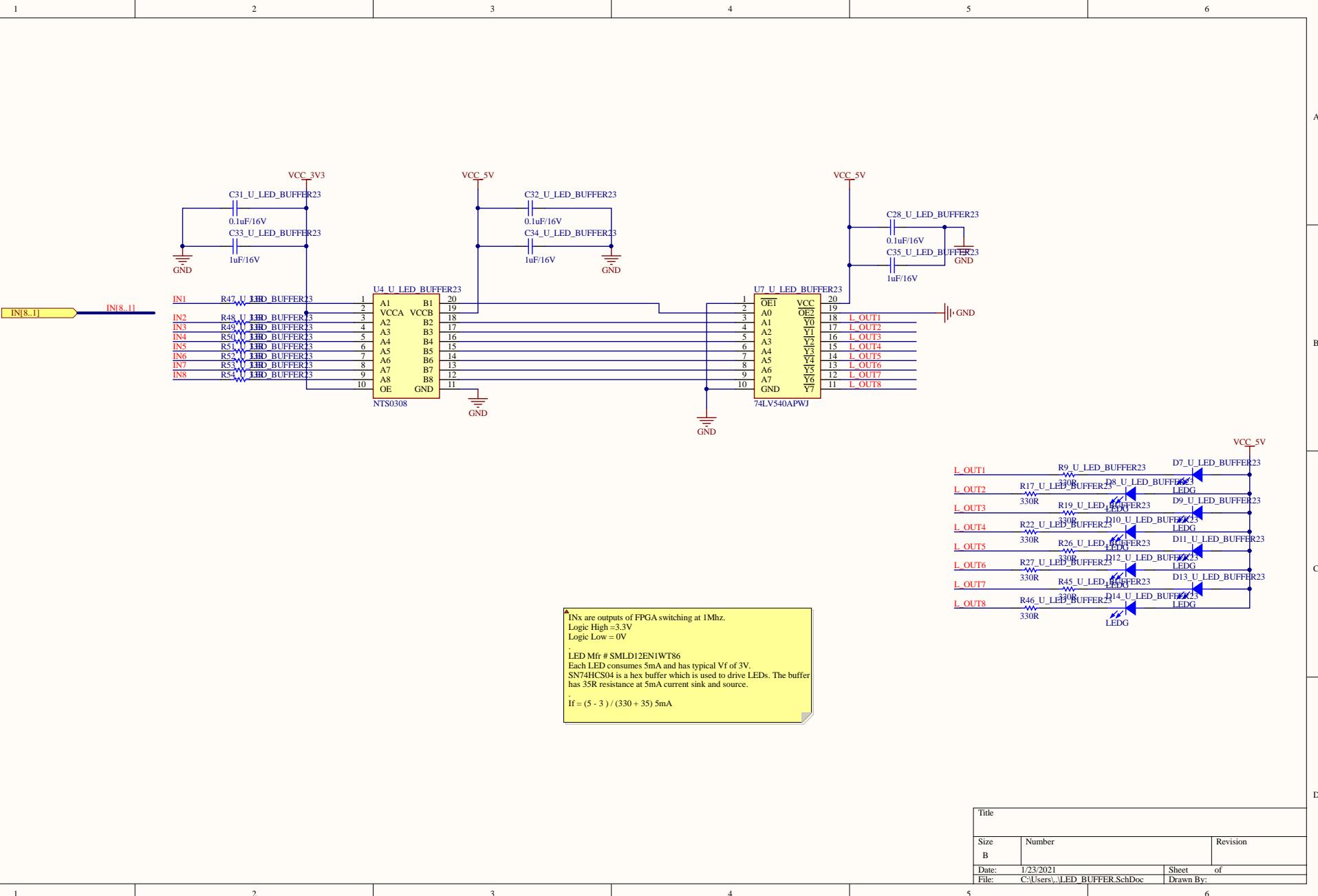
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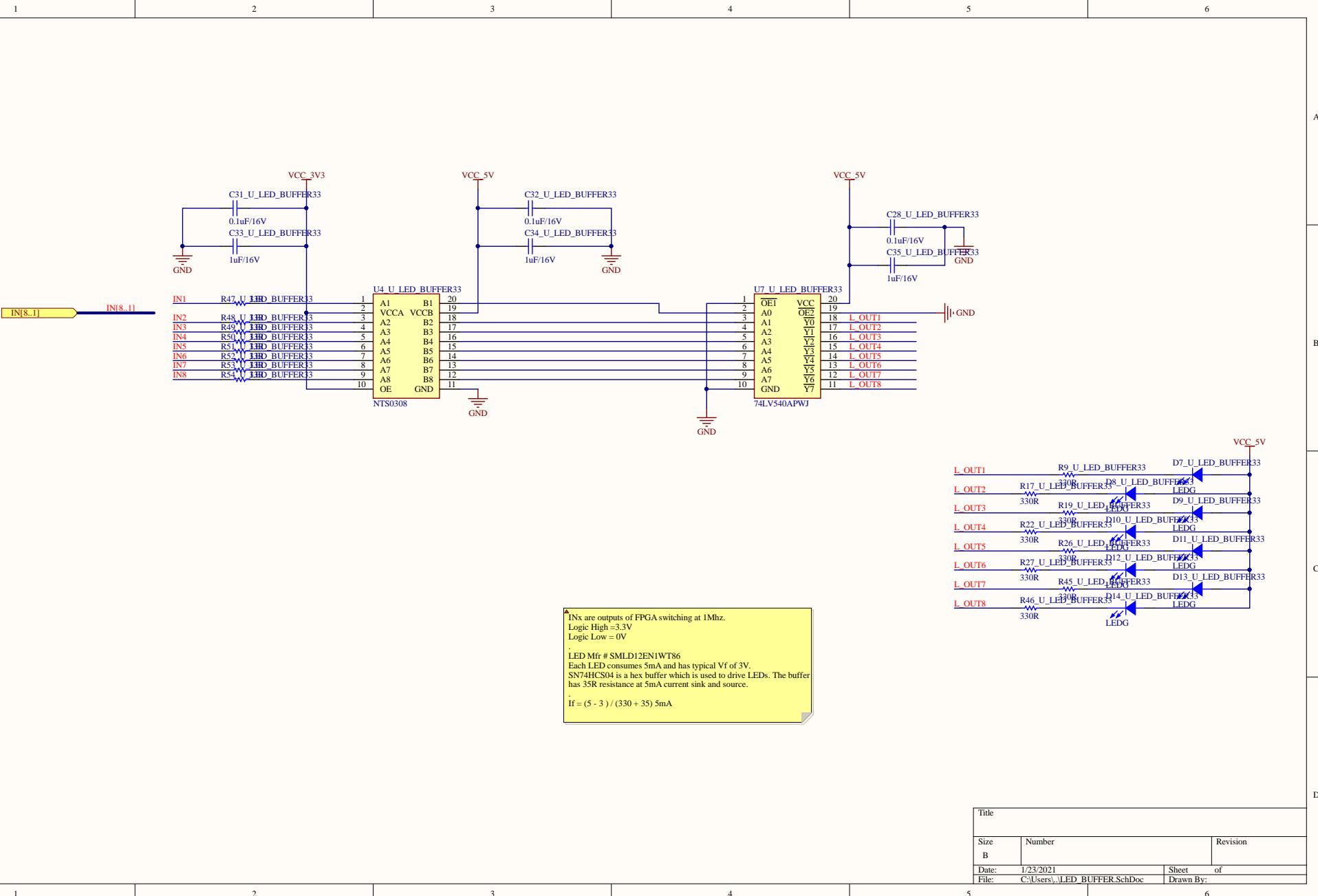
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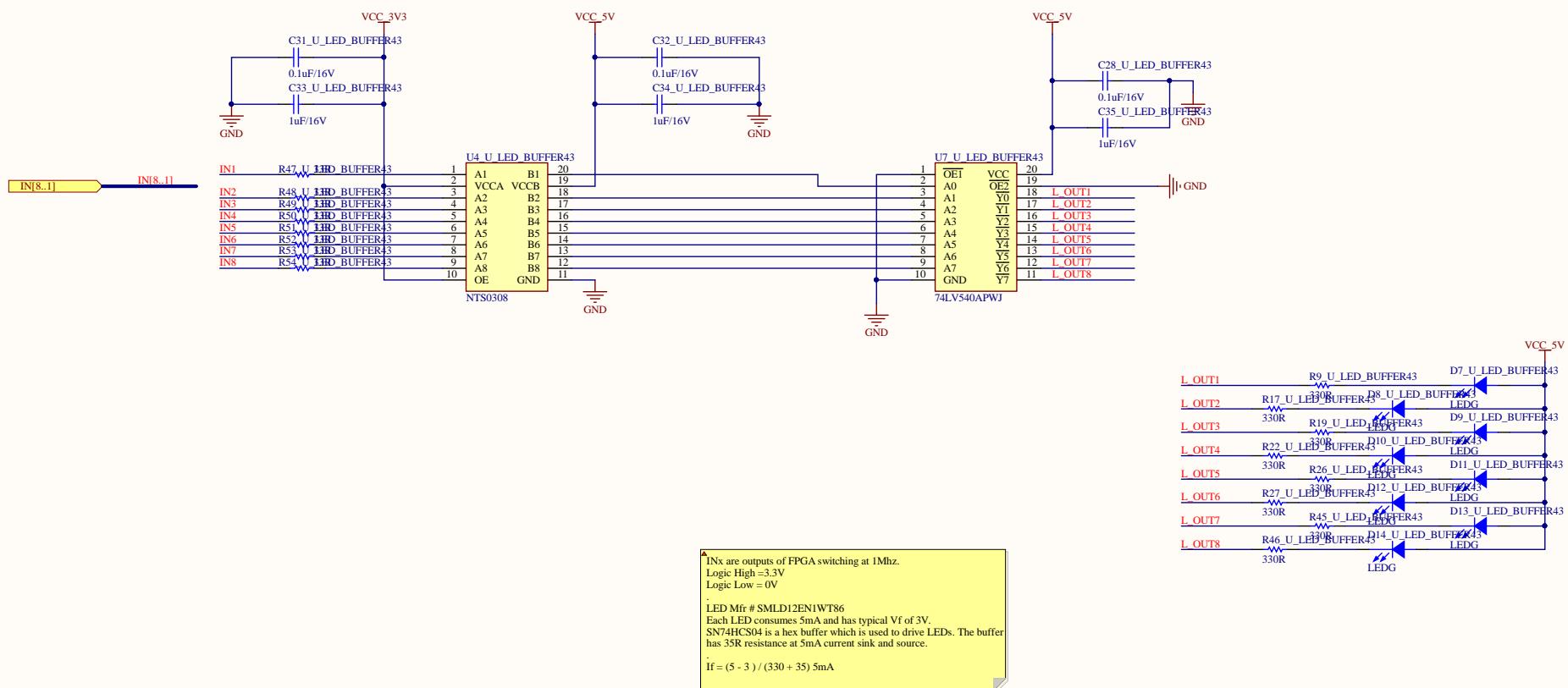
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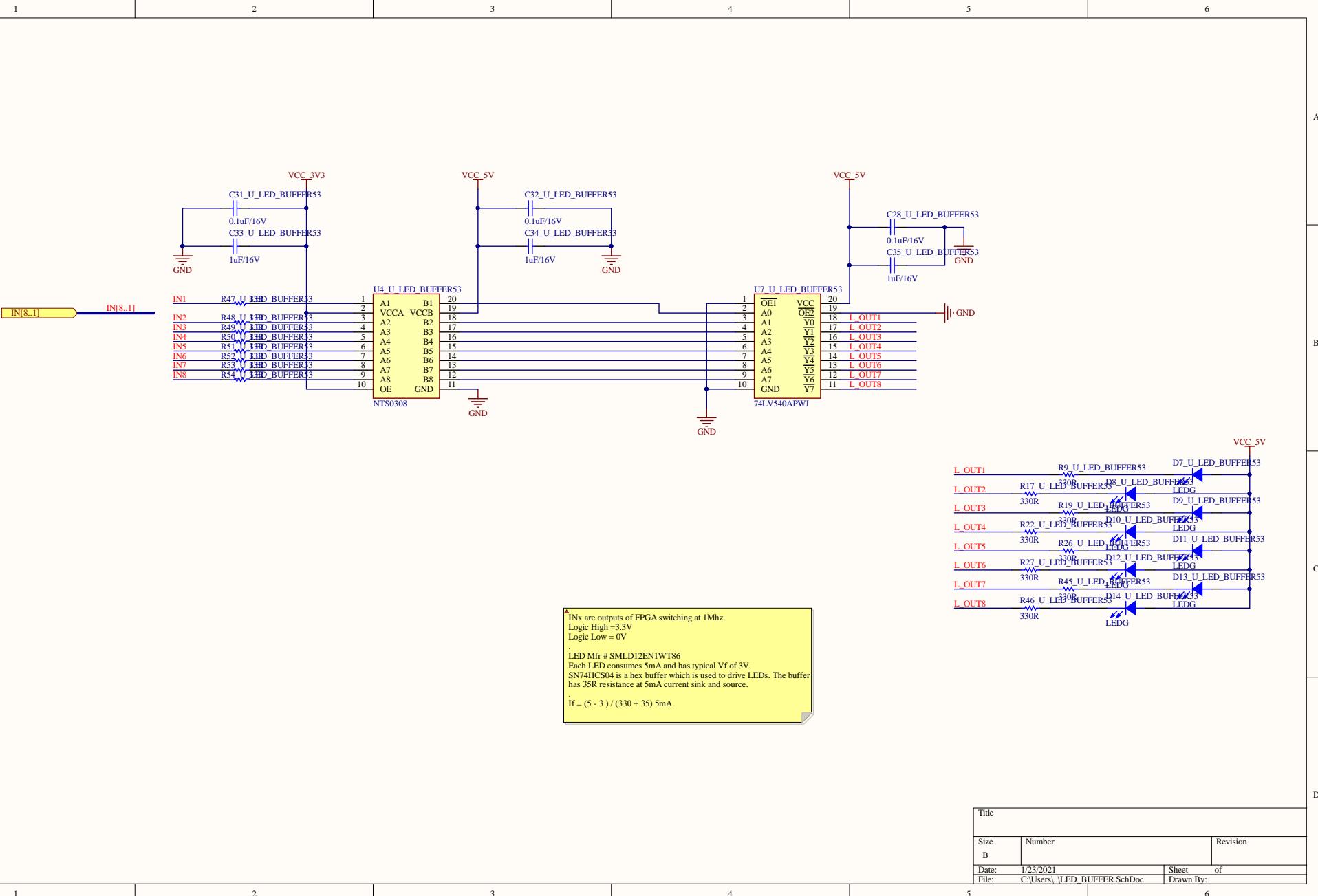








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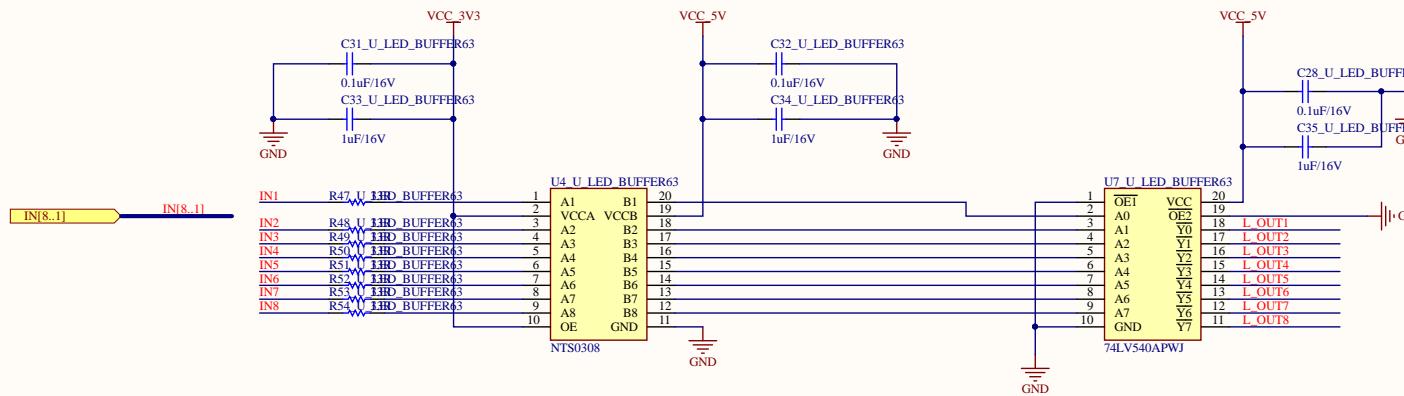
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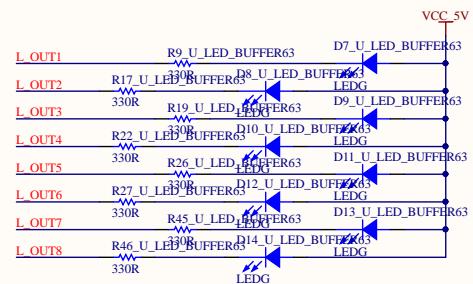
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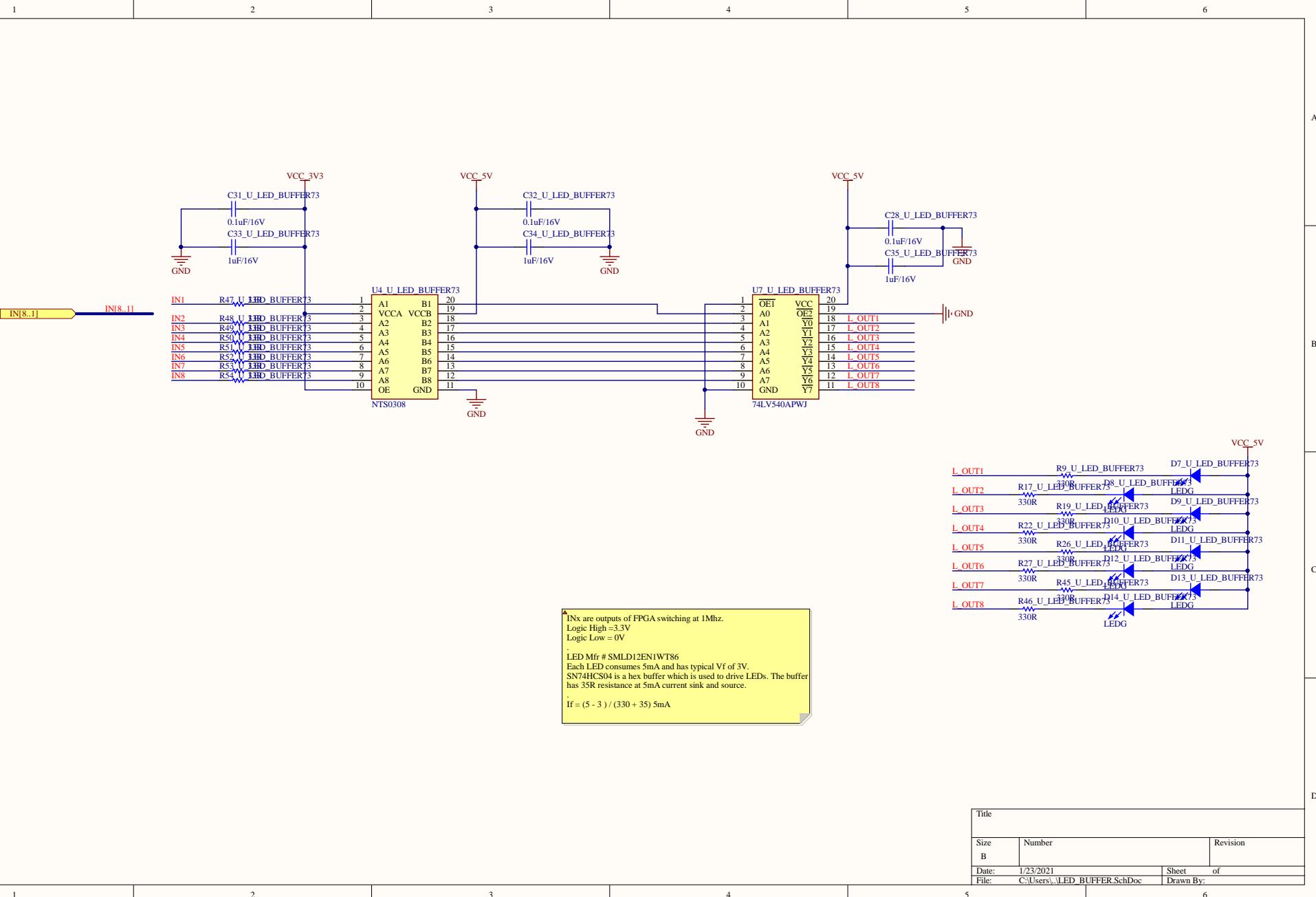
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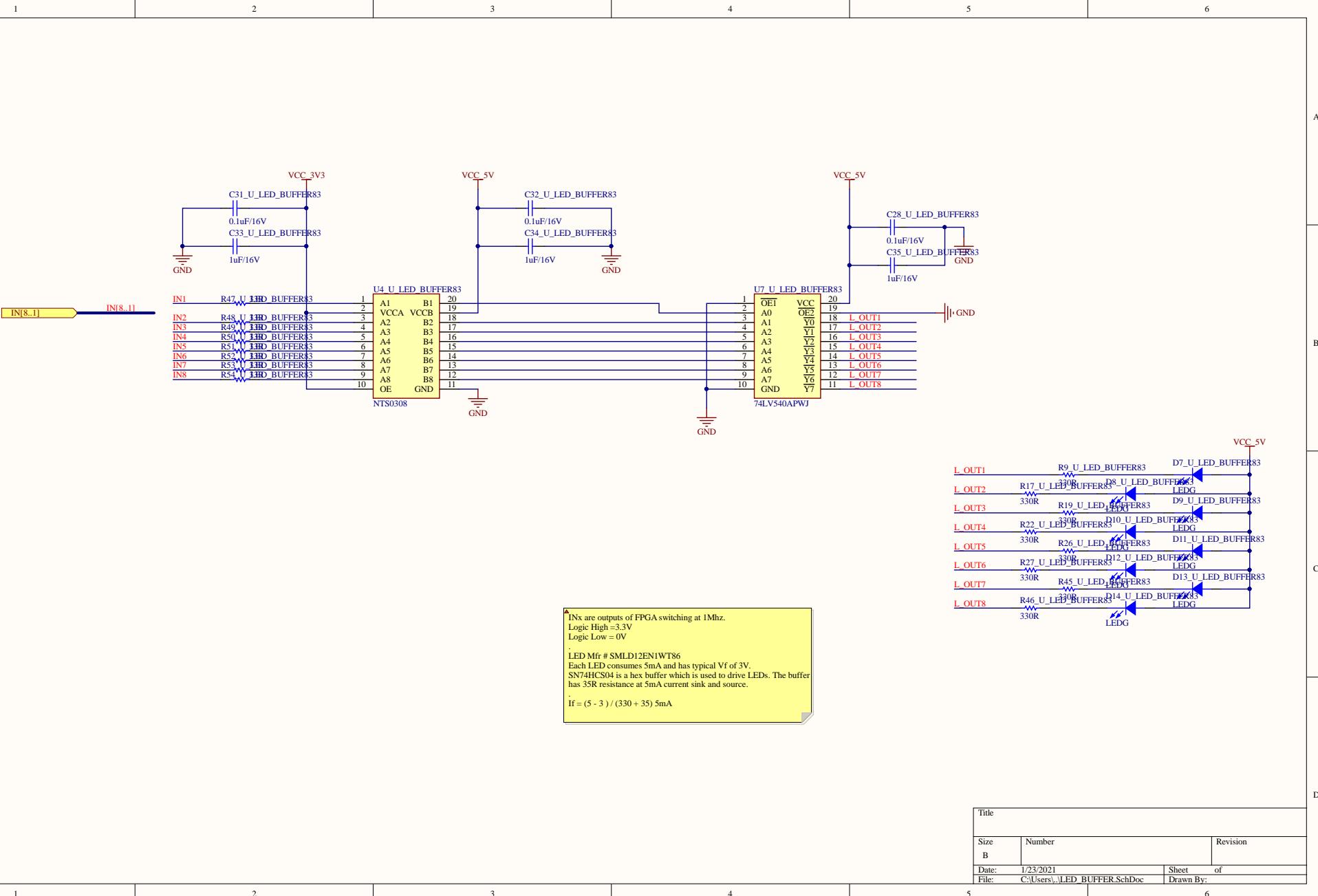
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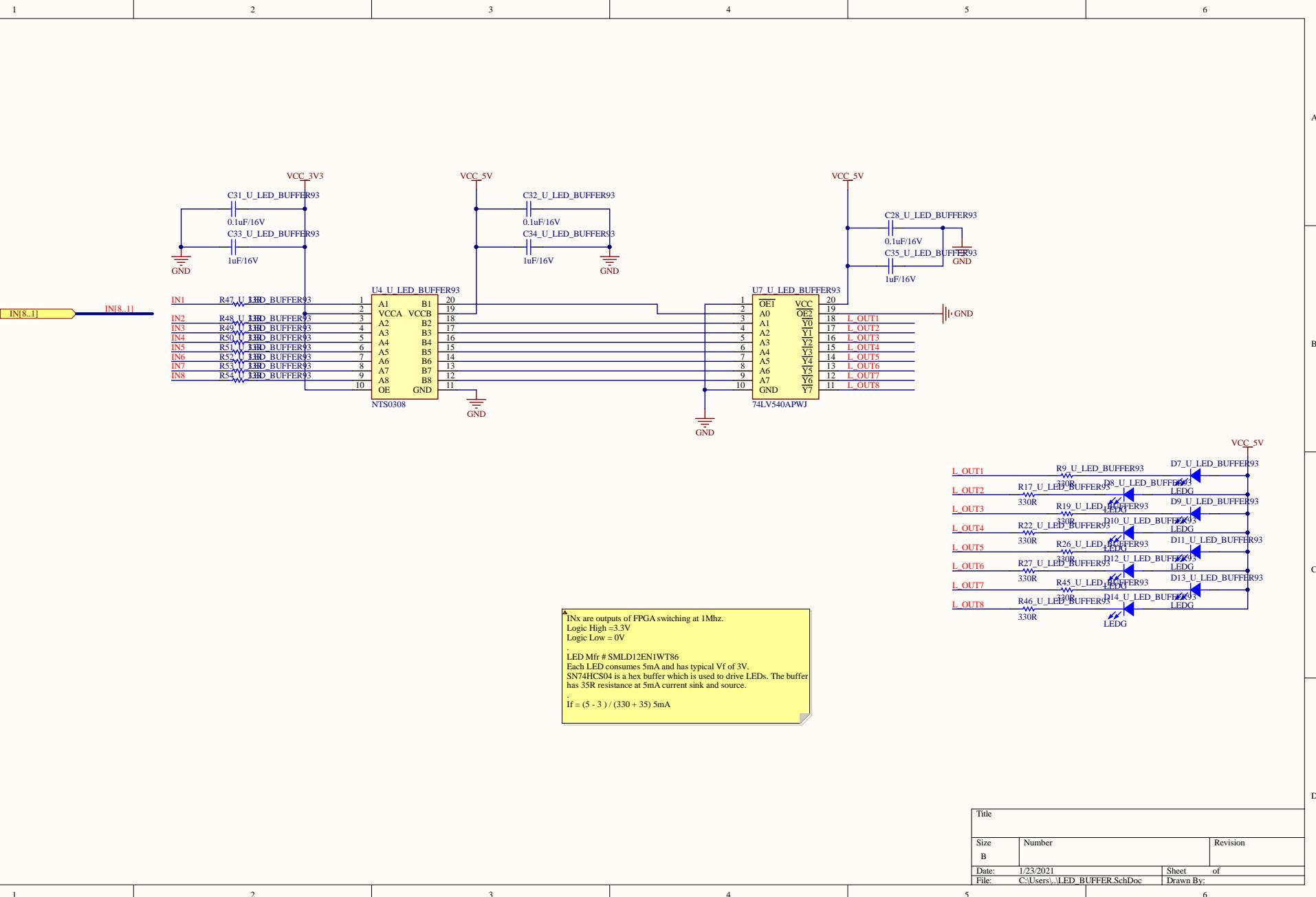
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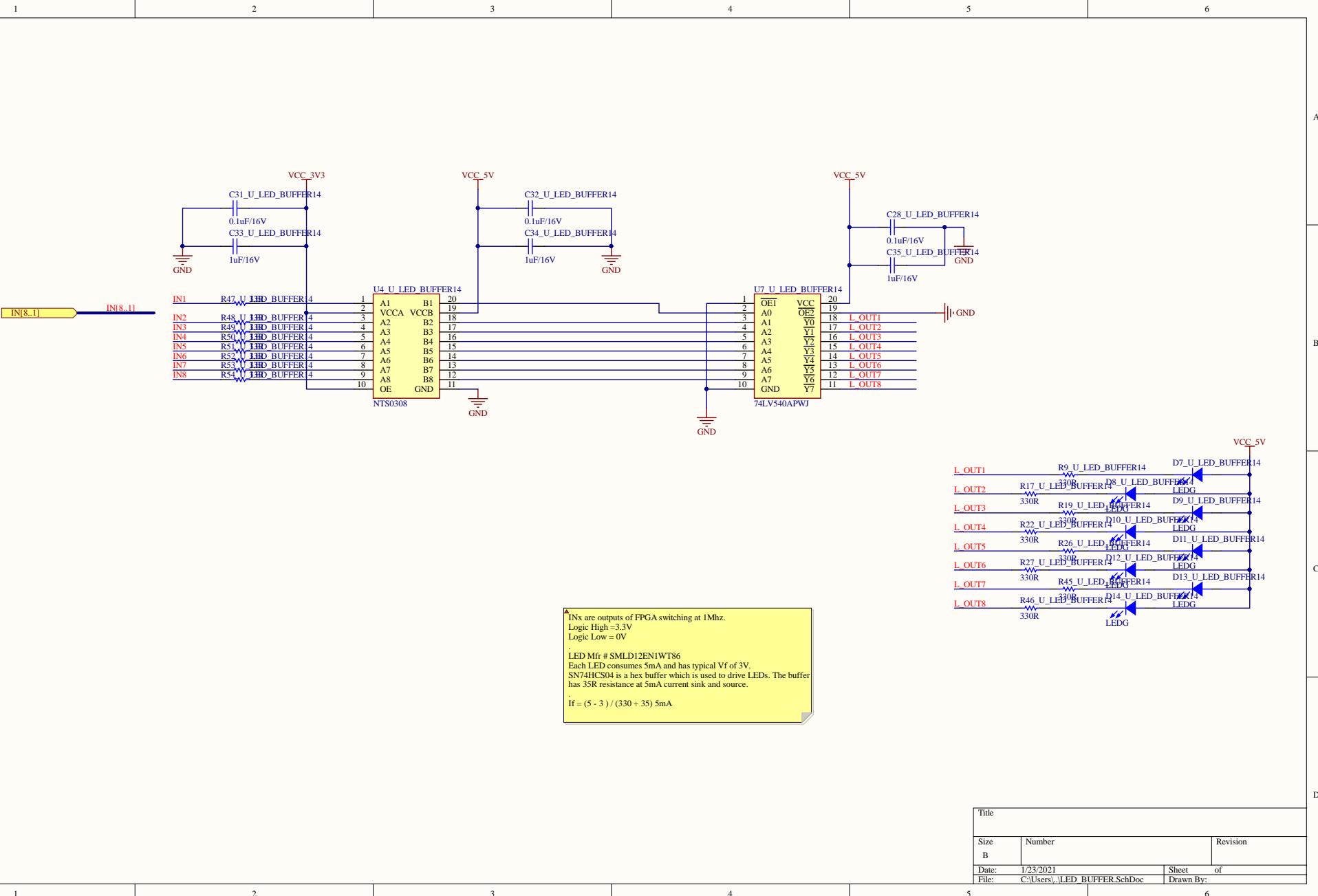


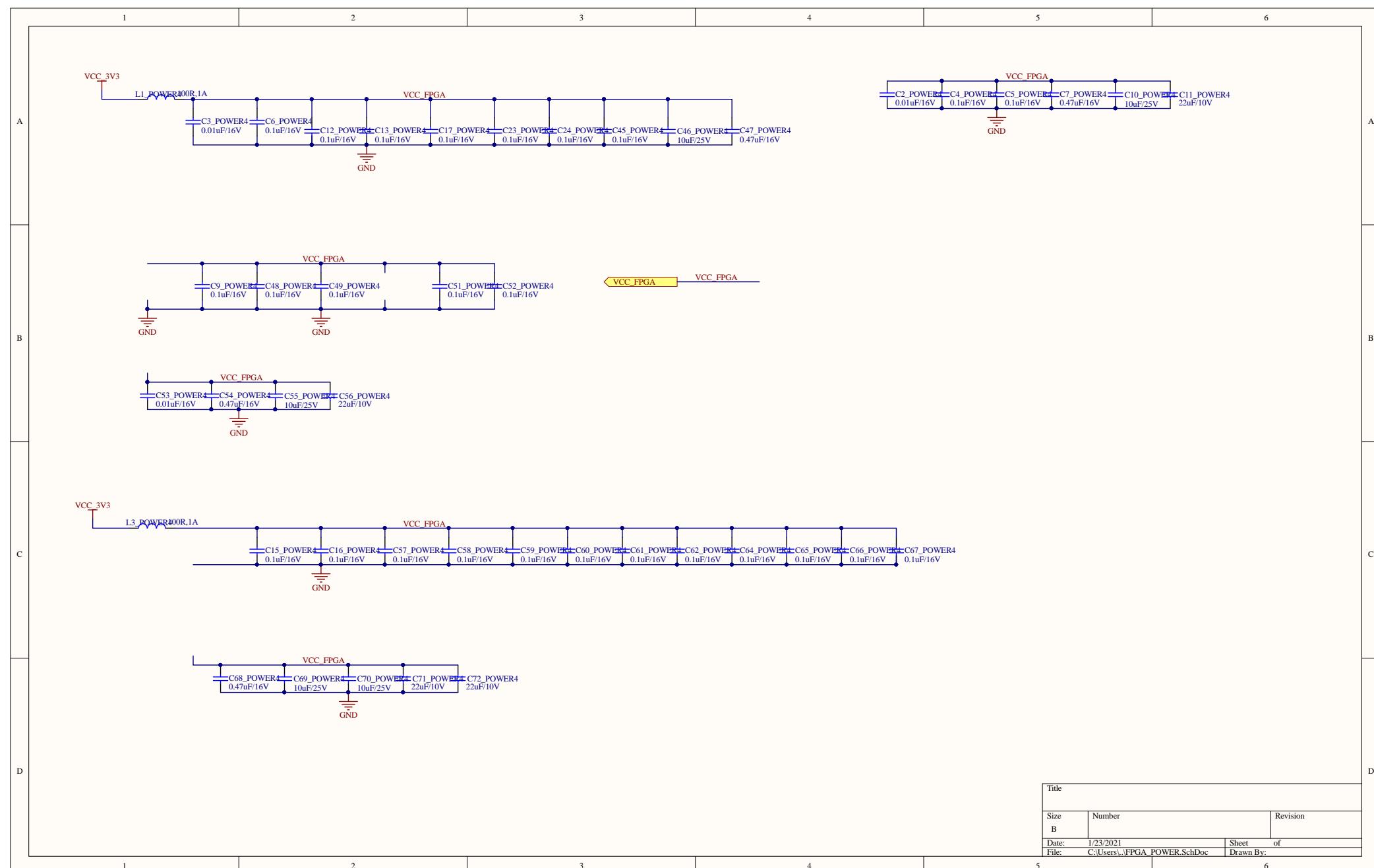
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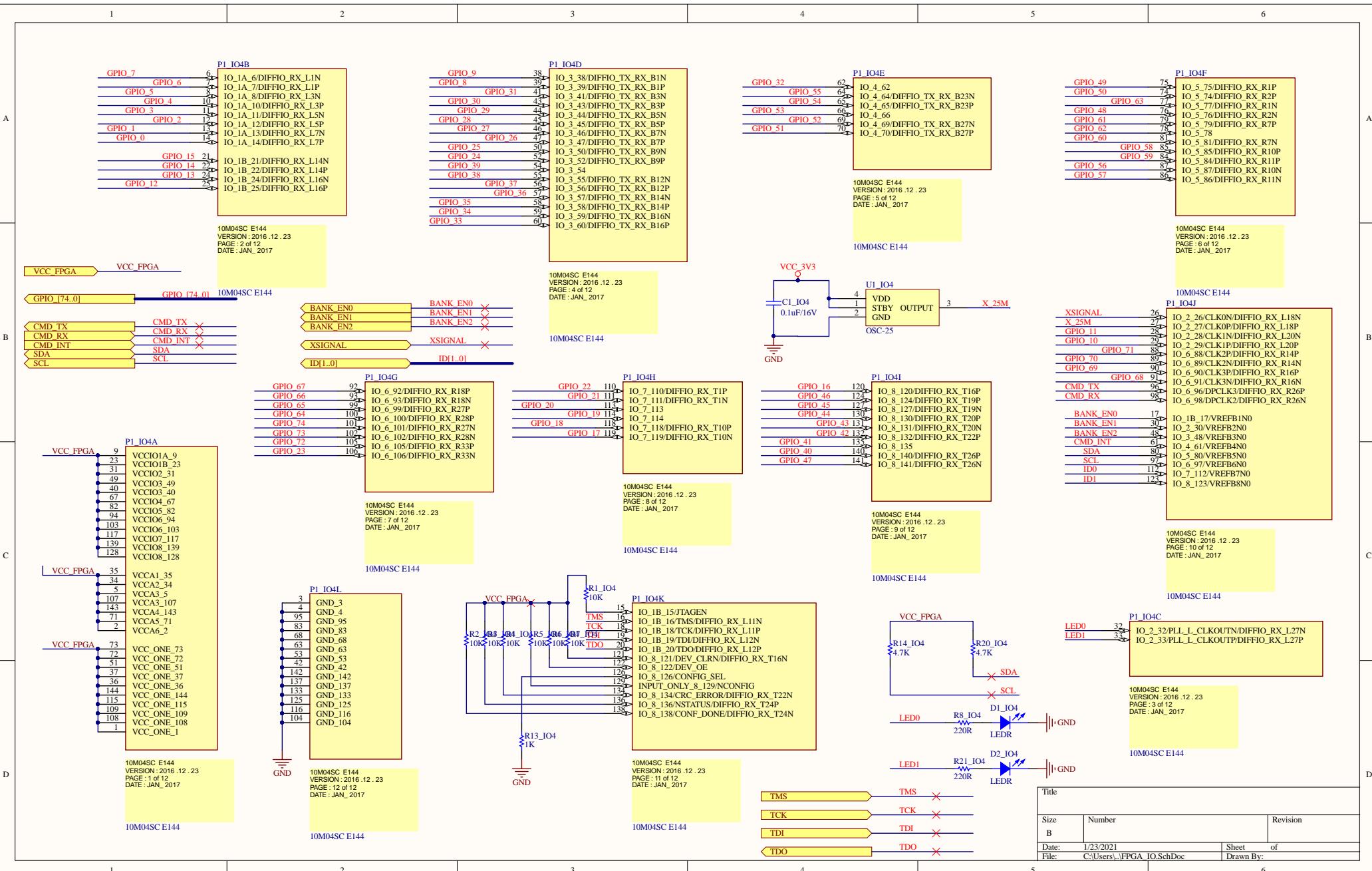


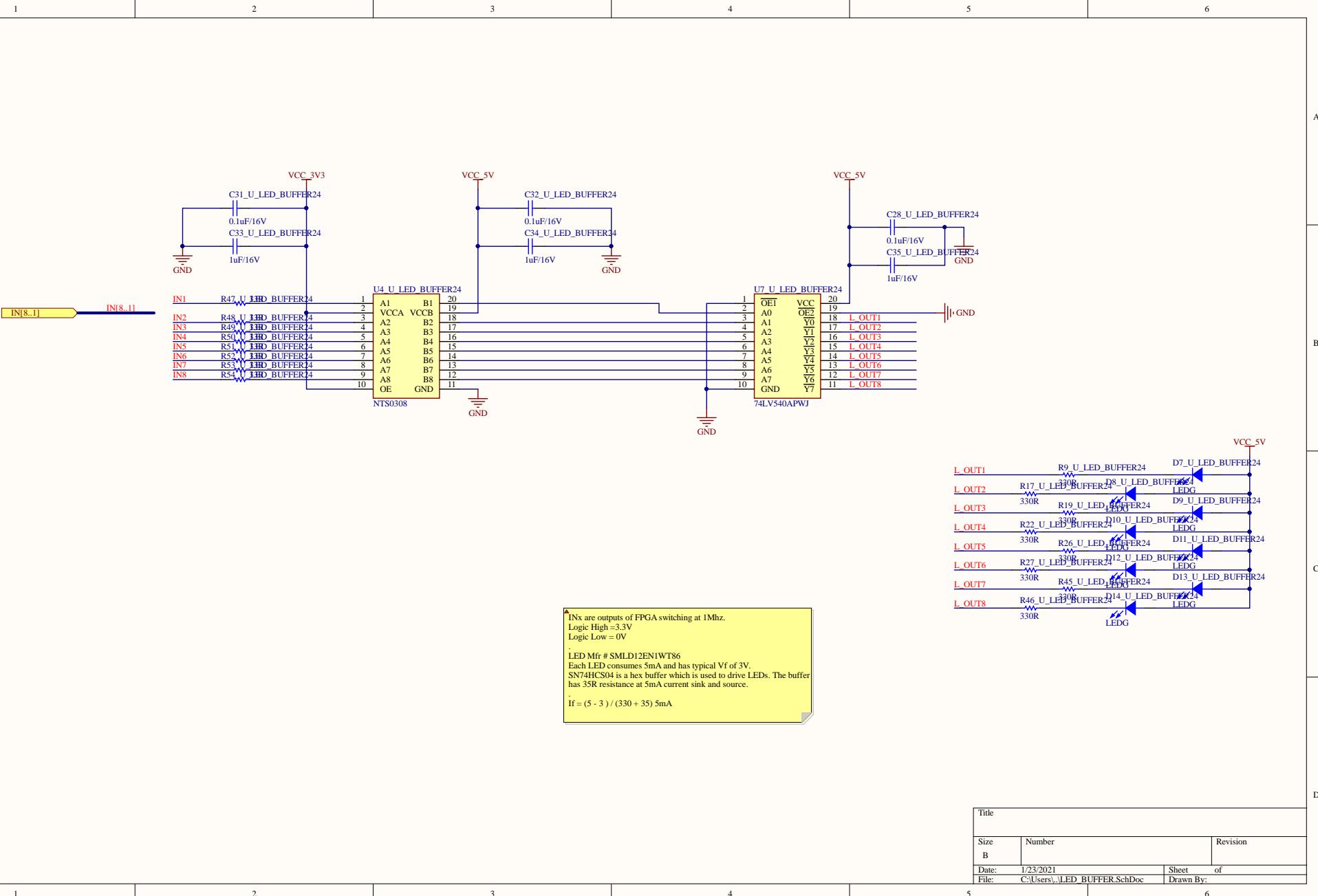


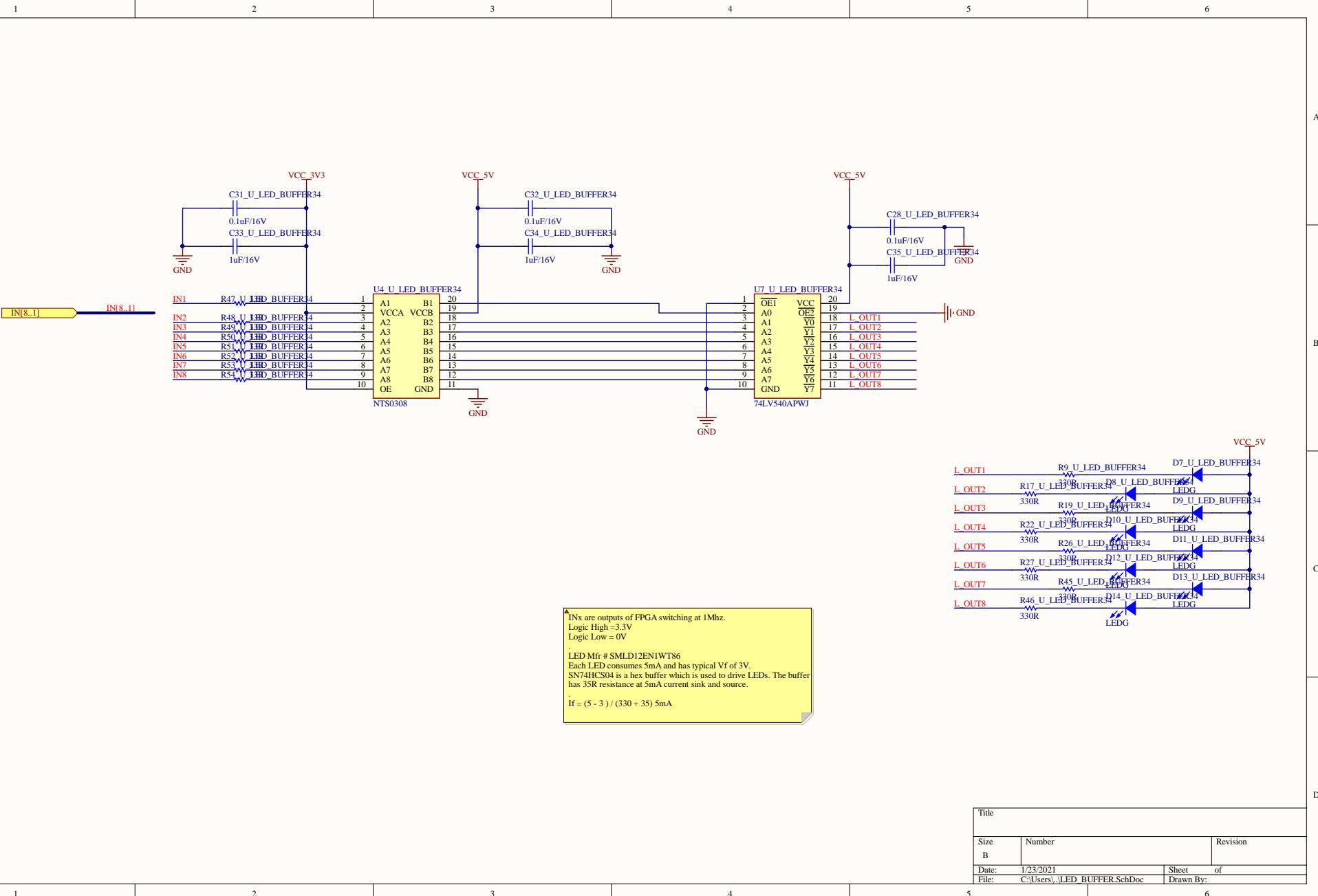


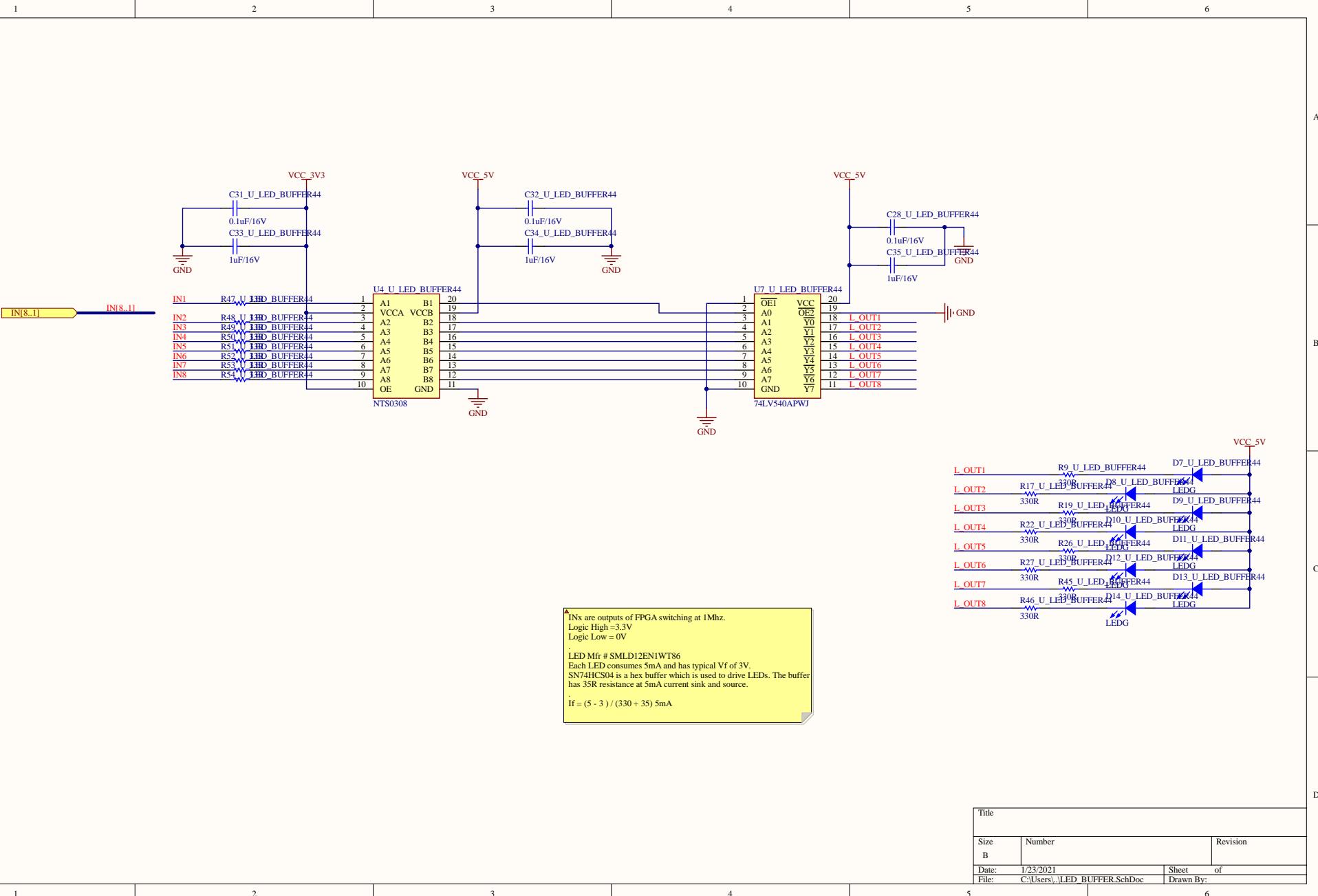


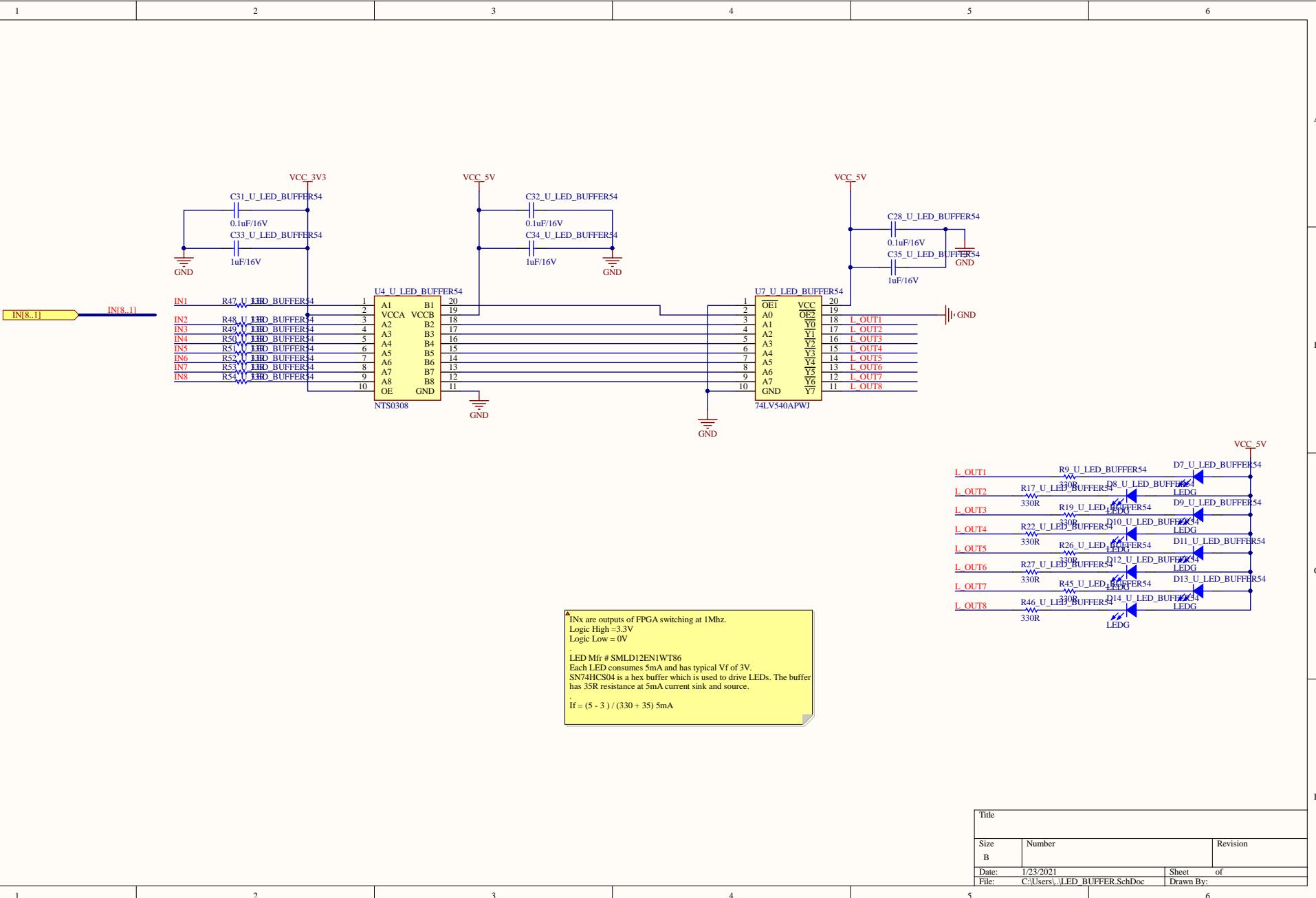


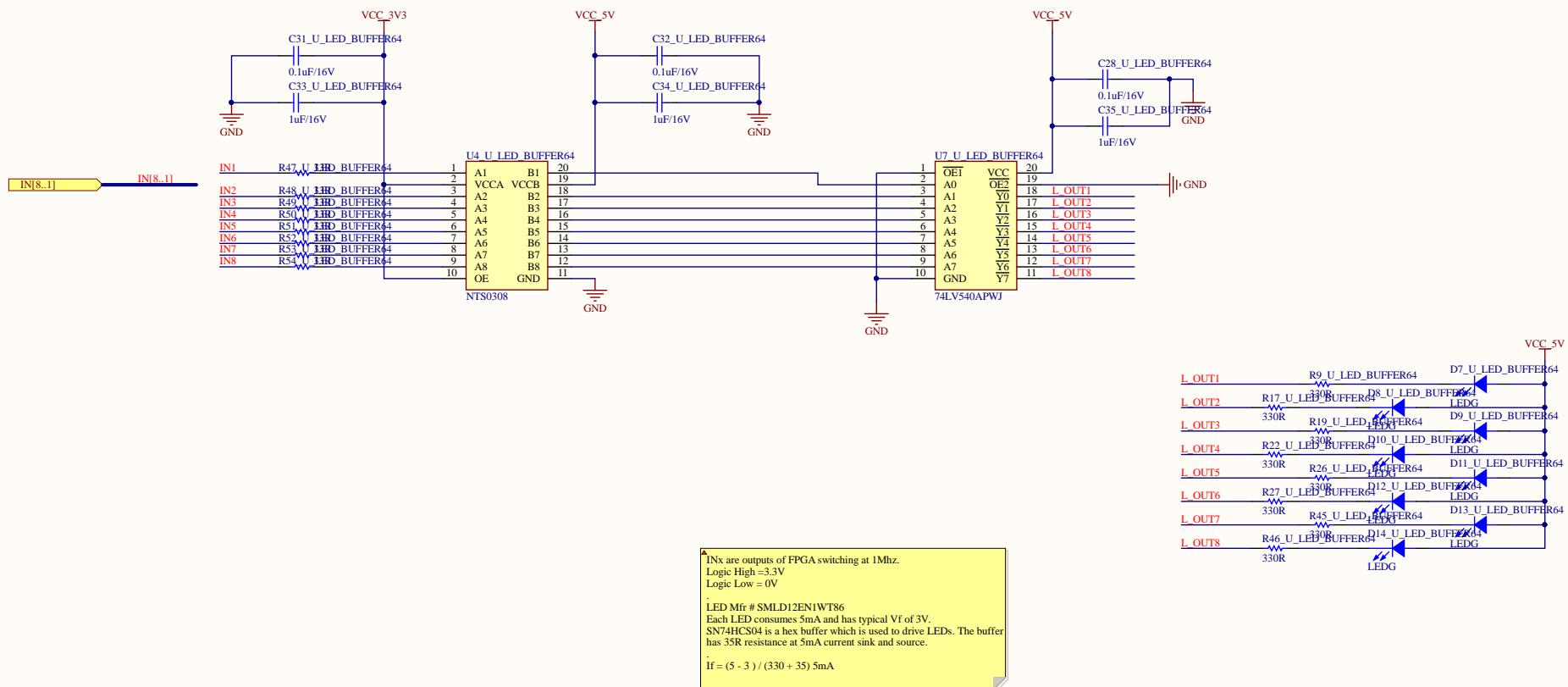




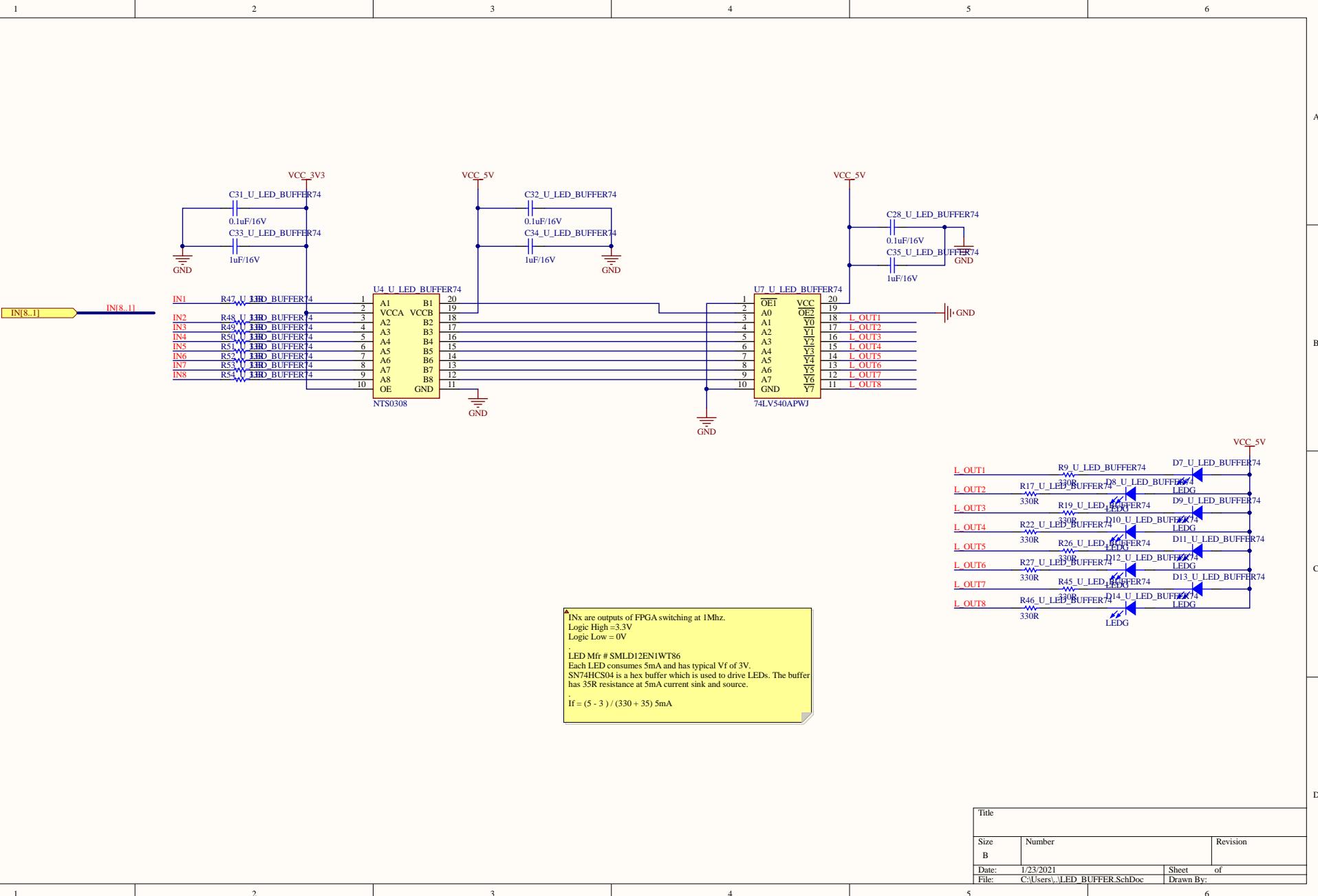


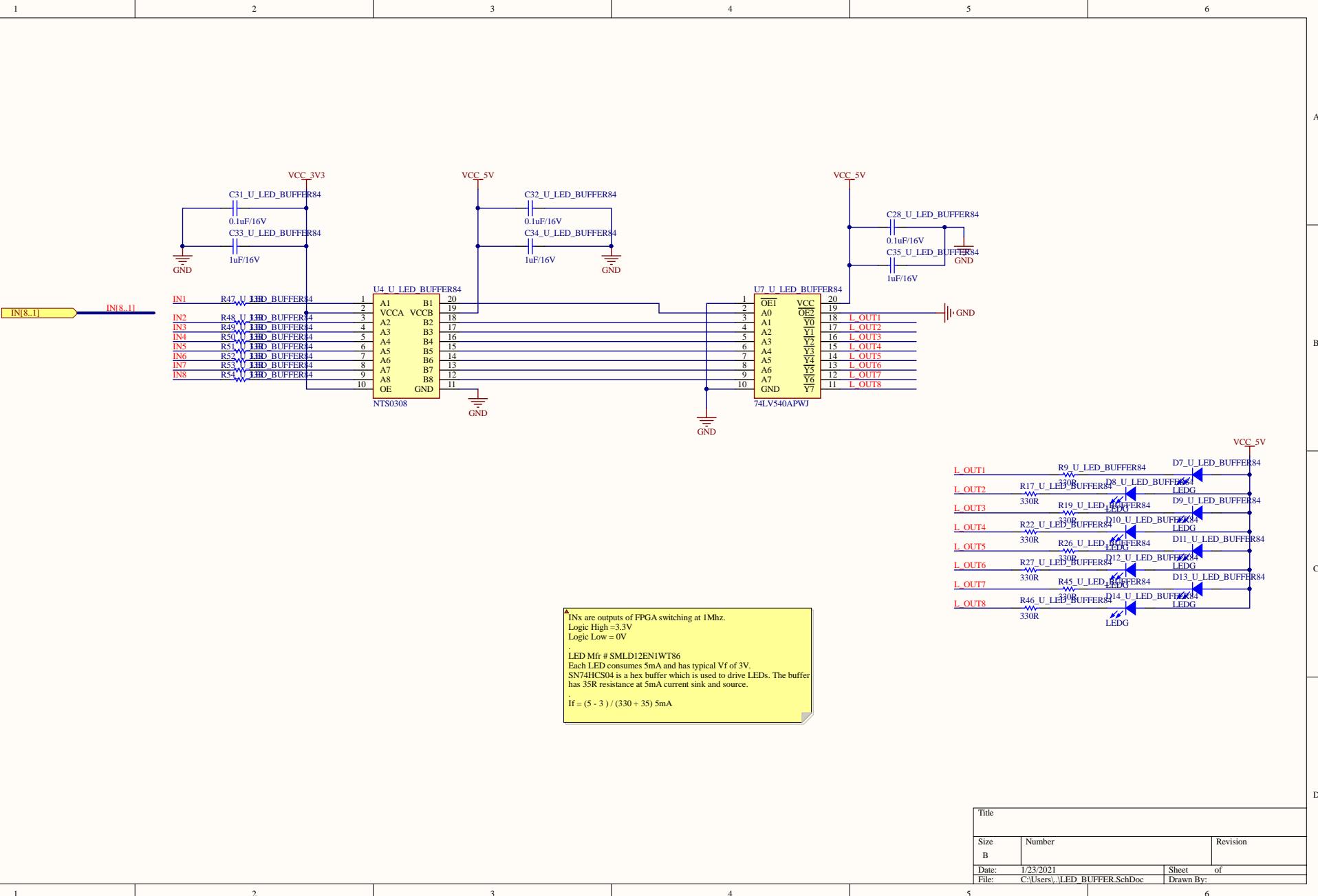


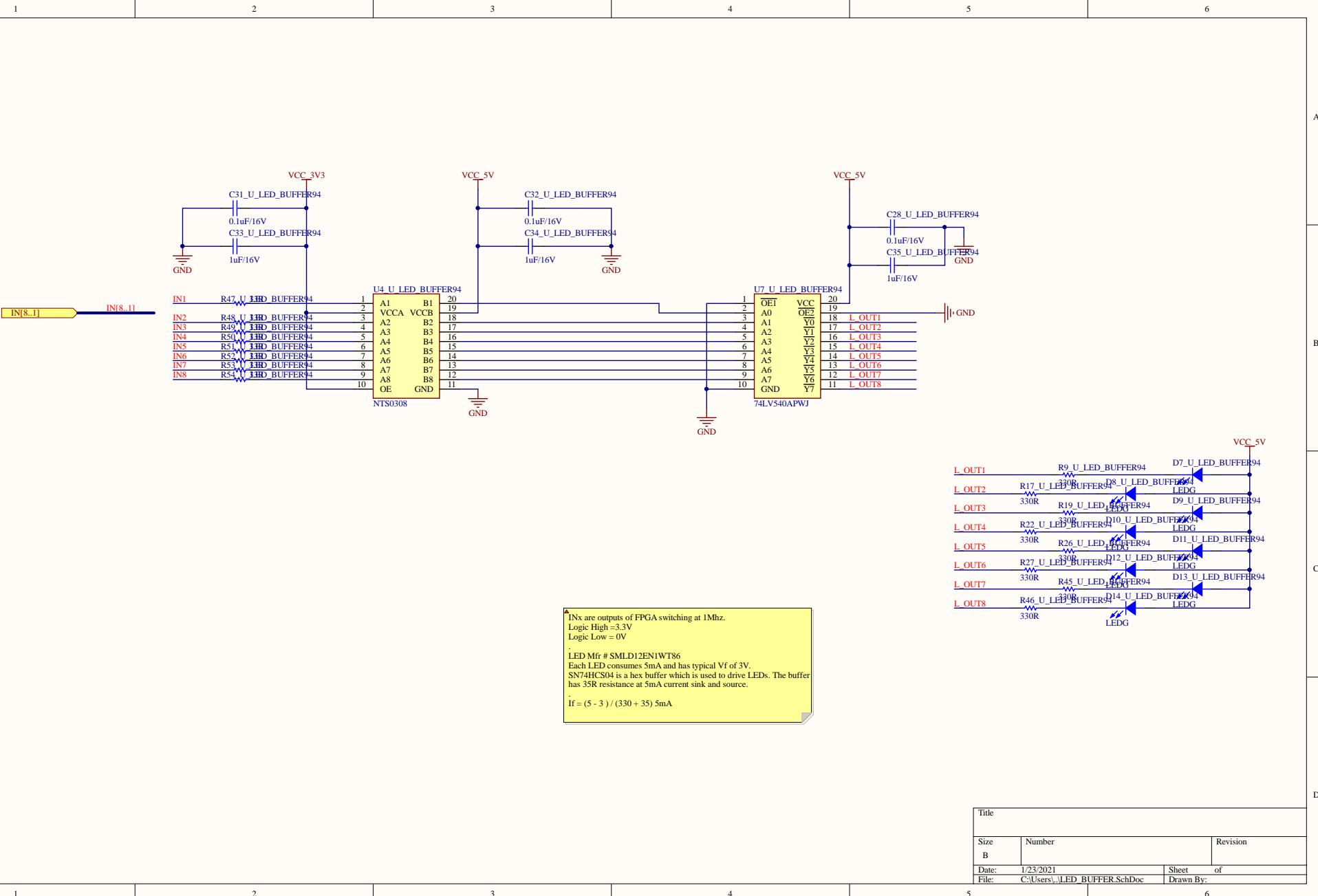


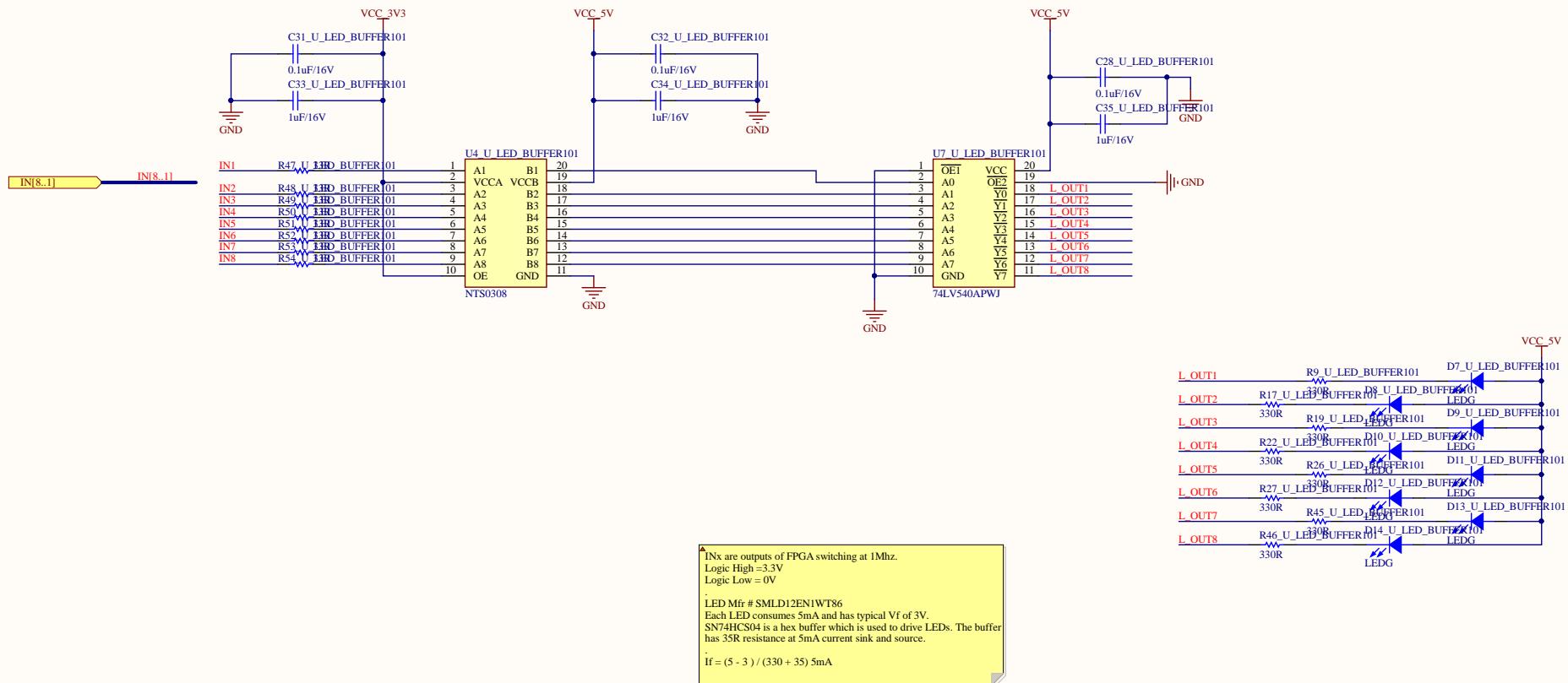


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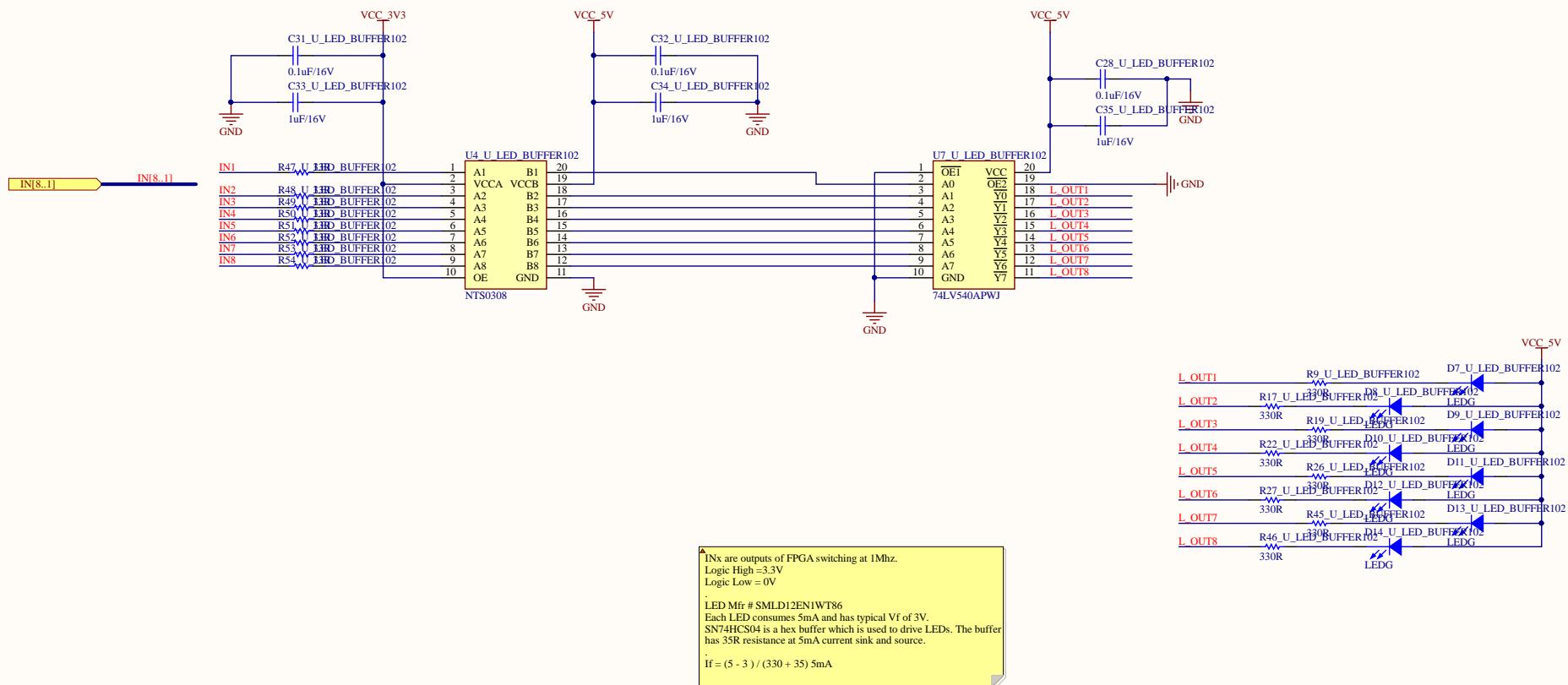




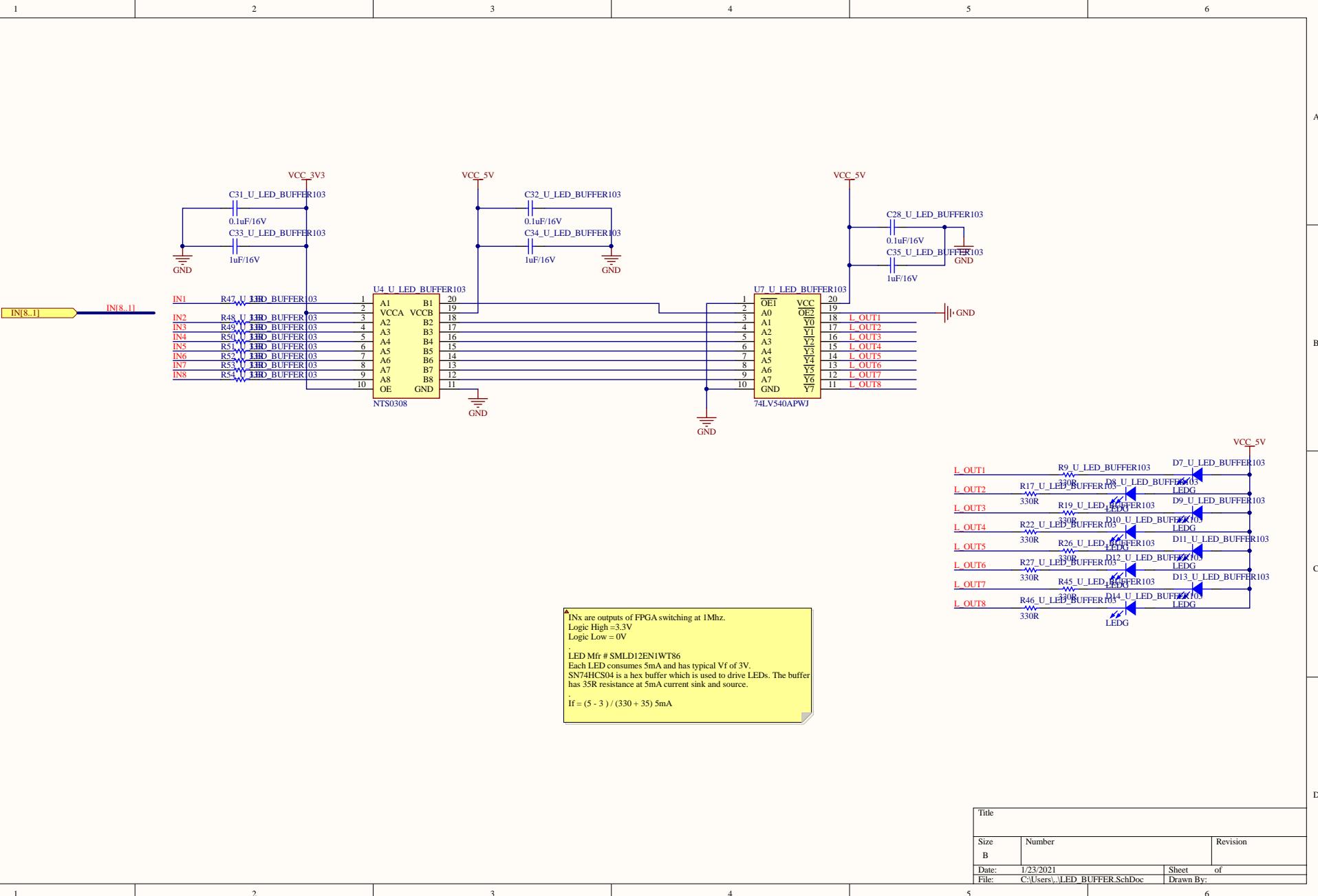


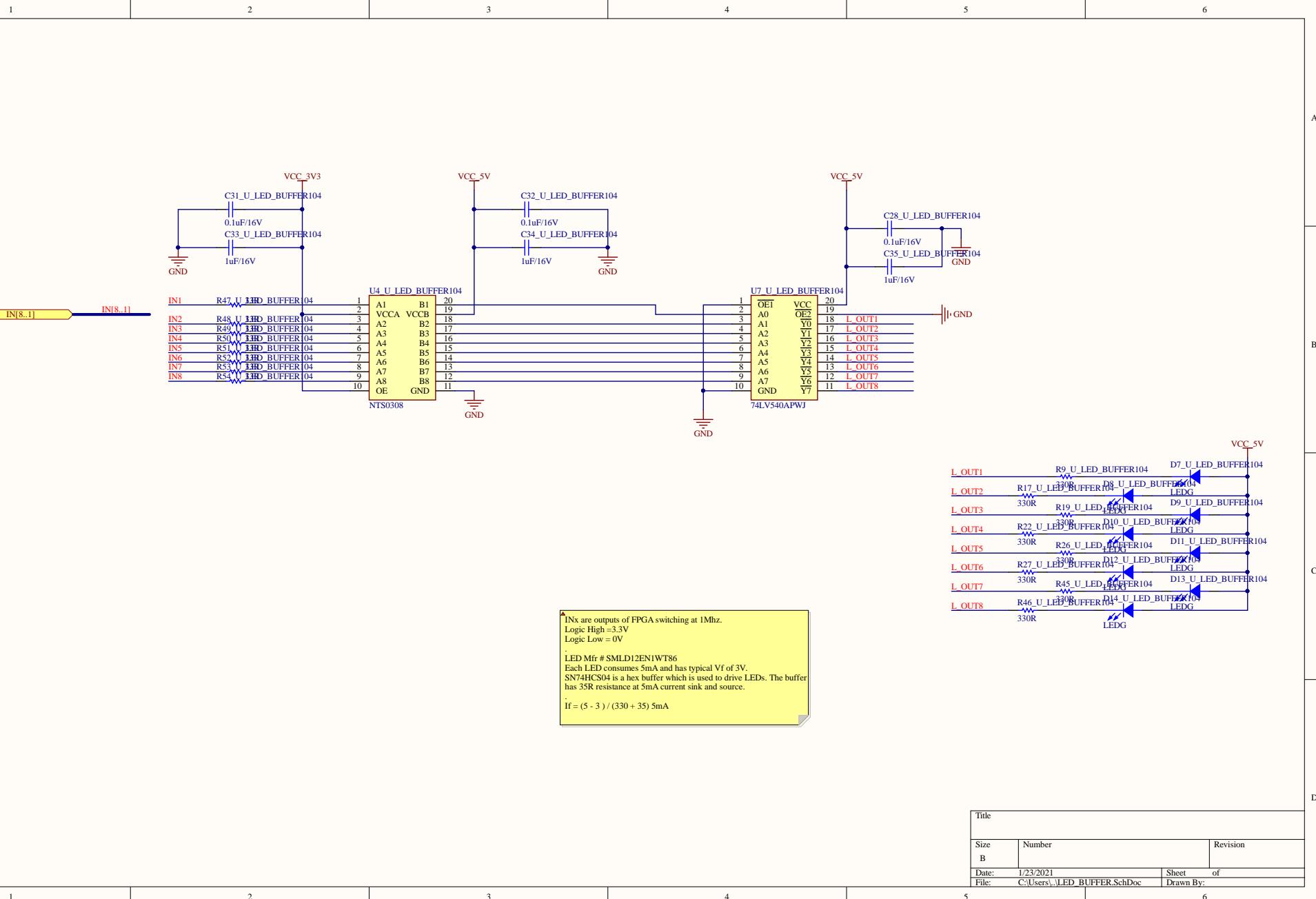


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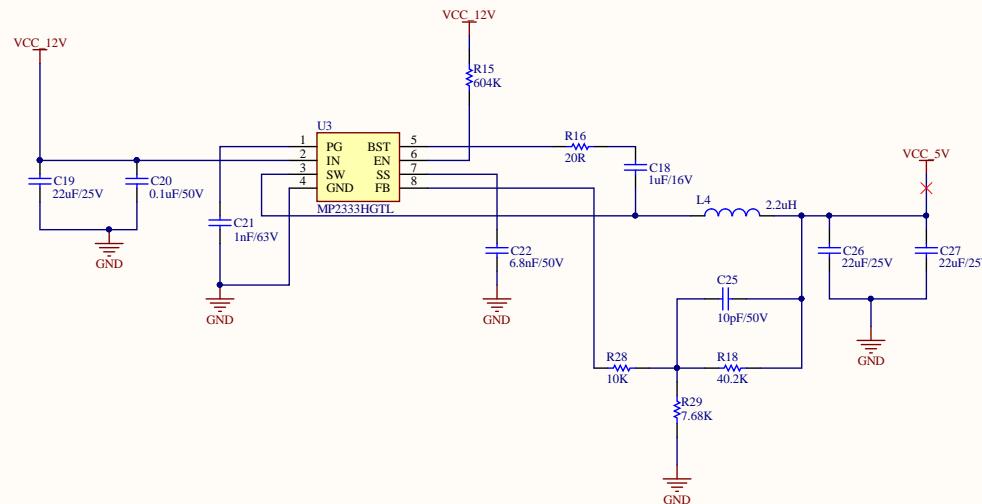
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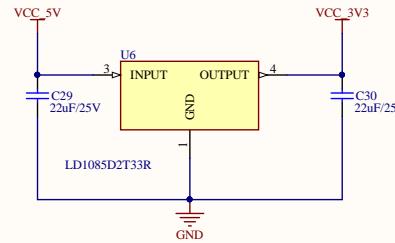


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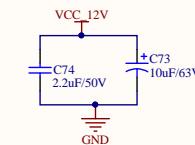
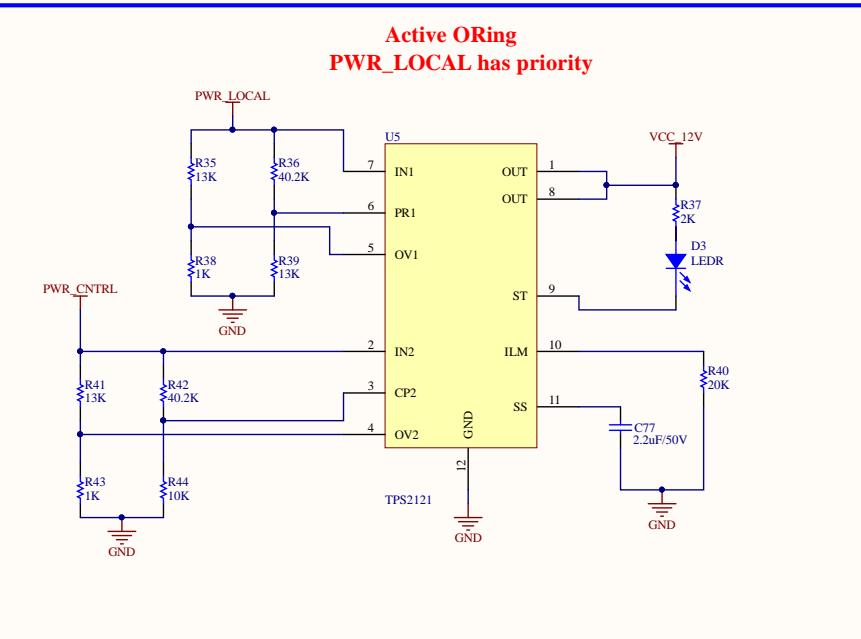
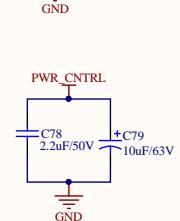
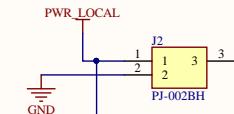


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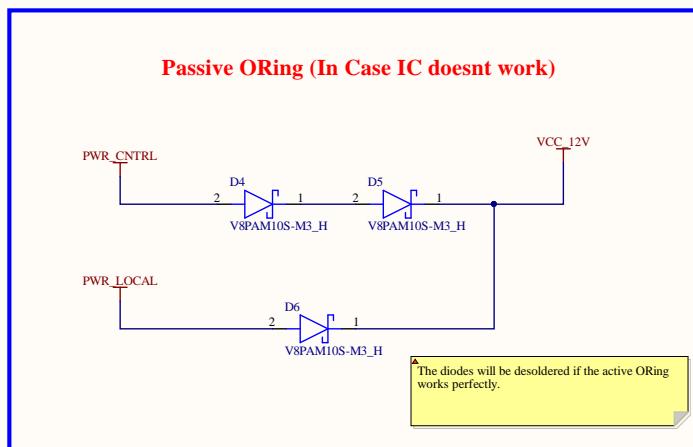
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