

Router_Lint_Report

Initial Lint Process:

Lint File Code:

```
#Liberty files are needed for logical and physical netlist designs
set search_path "."
set link_library " "

set_app_var enable_lint true

configure_lint_setup -goal lint_rtl

analyze -format verilog {../rtl/router_top.v ../rtl/router_fifo.v ../rtl/router_fsm.v ../rtl/router_reg.v
../rtl/router_sync.v}

elaborate router_top

check_lint

report_lint -verbose -file ../report/report_lint_router.txt
```

Lint Process:

```
HarshaVD@mavenserver-RH3:~/VLSI_RN/Verilog_labs/Router_Lint/script
Terminal Sessions View Xserver Tools Games Settings Macros Help
Quick connect...
/home1/BRN47/HarshaVD/VLSI
Name
report_router.bat
report_router.txt
set link_library " "
set_app_var enable_lint true
true
configure_lint_setup -goal lint rtl
#waive lint -tag STARC05-2.5.1.2 -add clock_waive
analyze -format verilog {../rtl/router_top.v ../rtl/router_fifo.v ../rtl/router_fsm.v ../rtl/router_reg.v ../rtl/router_sync.v}
1
elaborate router_top
Doing common elaboration
Final timescale is '1ps/1ps'
Info: Invoking Simon...
Importing Symbol Libraries...
Info: Simon VCS Start
=====
VCS CPU Time(s) :0.08
SIMON CPU Time(s) :0.07
SIMON Total Time(s) :0.02
Peak Memory(MB) :389
=====
Info: Simon VCS Finished
Info: Simon call complete
Info: Exiting after Simon Analysis
[Info] Loading Lint Language Checker starting
Warning:[DB_CANT_LOAD] Invalid library file specified.
Invalid link library file specified. Cannot load link library './'
[Info] Loading Lint Language Checker Finished
Failed to import the "default.u" library because the library files cannot be found in the library paths.
---Any error or warning message, please refer to /home1/BRN47/HarshaVD/VLSI_RN/Verilog_labs/Router_Lint/script/vcst_rtdb/verdi/elabcomLog/libCompiler.log---
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
# Gate Counts
Number of Flat Instances = 1797
Number of Operator = 1797
Number of Libcells = 0
Number of Black-Box Instances = 0
1
check lint
[Info] Running goal lint rtl
[Info] Loading Lint Structural Checker Plugin... Success
Inferring all potential clocks
Inferring all potential resets
1
report_lint -verbose -file ../report/report_lint_router.txt
1
Follow terminal folder
```

Generated Report

Report Summary

Product Info

Name : VC Static Master Shell
Version : T-2022.06 -- May 30, 2022

Report Info

Created : Jun 12, 2024 19:35:07

TopLevelModule: router_top

Management Summary

Stage	Family	Fatals	Errors	Warnings	Infos
LANGUAGE_CHECK	CODING	0	0	0	1
STRUCTURAL_CHECK	CODING	0	1	0	13

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Total		0	1	0	14

Tree Summary

Severity	Stage	Tag	Count
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error	STRUCTURAL_CHECK	STARC05-2.5.1.2	1
info	LANGUAGE_CHECK	ReportPortInfo-ML	1
info	STRUCTURAL_CHECK	RegInputOutput-ML	13
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Total			15

STARC05-2.5.1.2 (1 error/0 waived)

Tag : STARC05-2.5.1.2
Description : Tristate buffer '[Signal]' has logic in enable condition. [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:1
Goal : lint_rtl
FileName : ../../rtl/router_fifo.v
LineNumber : 52
Statement : if(!rstn)
Signal : data_out[7:0]
Module : router_fifo
DesignObjHierarchy : FIFO_0
DrivenByObj
SignalInfo
DesignSignalName : FIFO_0/rstn
FileName : ../../rtl/router_fifo.v
LineNumber : 8

RegInputOutput-ML (13 infos/0 waived)

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:7
Goal : lint_rtl

FileName : ../../rtl/router_top.v
LineNumber : 7
Statement : output vld_out_0,vld_out_1,vld_out_2,err,busy;
Signal : busy
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:8
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 7
Statement : output vld_out_0,vld_out_1,vld_out_2,err,busy;
Signal : vld_out_0
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:10
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 7
Statement : output vld_out_0,vld_out_1,vld_out_2,err,busy;
Signal : vld_out_2
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:11
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 6
Statement : output [7:0]data_out_0,data_out_1,data_out_2;
Signal : data_out_2[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:6
Goal : lint_rtl

FileName : ../../rtl/router_top.v
LineNumber : 5
Statement : input pkt_valid,clock,resetn,read_enb_0,read_enb_1,read_enb_2;
Signal : read_enb_2
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:2
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 5
Statement : input pkt_valid,clock,resetn,read_enb_0,read_enb_1,read_enb_2;
Signal : resetn
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:14
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 6
Statement : output [7:0]data_out_0,data_out_1,data_out_2;
Signal : data_out_0[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:9
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 7
Statement : output vld_out_0,vld_out_1,vld_out_2,err,busy;
Signal : vld_out_1
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:5
Goal : lint_rtl

FileName : ../../rtl/router_top.v
LineNumber : 5
Statement : input pkt_valid,clock,resetn,read_enb_0,read_enb_1,read_enb_2;
Signal : read_enb_1
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:13
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 4
Statement : input [7:0]data_in;
Signal : data_in[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:4
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 5
Statement : input pkt_valid,clock,resetn,read_enb_0,read_enb_1,read_enb_2;
Signal : read_enb_0
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:3
Goal : lint_rtl
FileName : ../../rtl/router_top.v
LineNumber : 5
Statement : input pkt_valid,clock,resetn,read_enb_0,read_enb_1,read_enb_2;
Signal : pkt_valid
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:12
Goal : lint_rtl

FileName : ../../rtl/router_top.v
LineNumber : 6
Statement : output [7:0]data_out_0,data_out_1,data_out_2;
Signal : data_out_1[7:0]
Module : router_top
DesignObjHierarchy : router_top

ReportPortInfo-ML (1 info/0 waived)

Tag : ReportPortInfo-ML
Description : Port Information for top design unit has been generated. For details see report
ReportPortInfo.rpt
Violation : Lint:15
Goal : lint_rtl
FileName :
/home1/BRN47/HarshaVD/VLSI_RN/Verilog_labs/Router_Lint/script/vcst_rtdb/spyglass/vc_lint0/
router_top/VC_GOAL0/spyglass_reports/morelint/ReportPortInfo
LineNumber : 1
Statement : # Comment : Report Top Level Module Port Info

Waiving the STARC05-2.5.1.2 Tag:

Lint File Code:

```
#Liberty files are needed for logical and physical netlist designs
set search_path "."
set link_library " "

set_app_var enable_lint true

configure_lint_setup -goal lint_rtl

waive_lint -tag STARC05-2.5.1.2 -add clock_waive

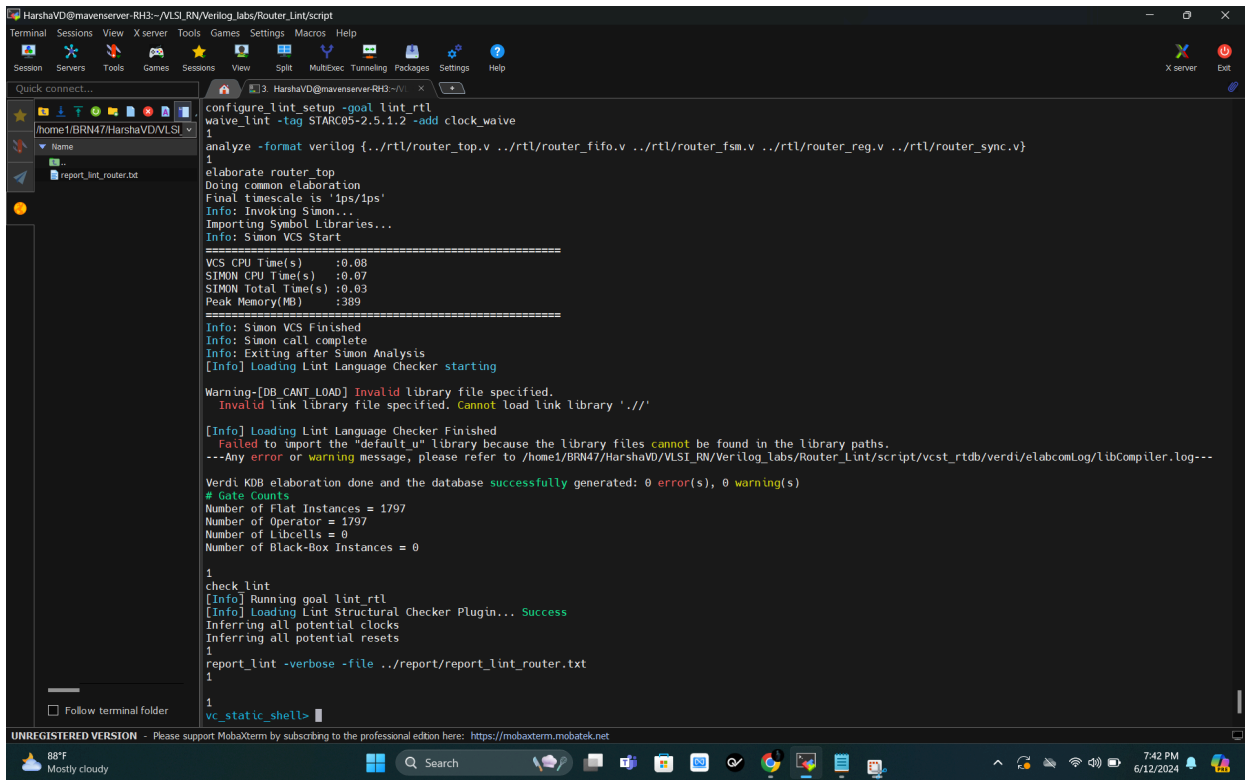
analyze -format verilog {../../rtl/router_top.v ../../rtl/router_fifo.v ../../rtl/router_fsm.v ../../rtl/router_reg.v
../../rtl/router_sync.v}

elaborate router_top

check_lint
```

report_lint -verbose -file ../report/report_lint_router.txt

Lint Process:



Generated Report:

Report Summary

Product Info

 Name : VC Static Master Shell

 Version : T-2022.06 -- May 30, 2022

Report Info

 Created : Jun 12, 2024 10:04:15

 TopLevelModule: router_top

Management Summary

Stage	Family	Fatals	Errors	Warnings	Infos	Waived
LANGUAGE_CHECK	CODING		0	0	0	1 0
STRUCTURAL_CHECK	CODING		0	0	0	10 1
Total		0	0	0	11	1

Tree Summary

Severity	Stage	Tag	Count	Waived
error	STRUCTURAL_CHECK	STARC05-2.5.1.2	0	1
info	LANGUAGE_CHECK	ReportPortInfo-ML	1	0
info	STRUCTURAL_CHECK	RegInputOutput-ML	10	0
Total			11	1

RegInputOutput-ML (10 infos/0 waived)

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:2
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 3
Statement : input resetn,
Signal : resetn
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:7
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 13
Statement : output busy,

Signal : busy
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:6
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 7
Statement : input read_enb_2,
Signal : read_enb_2
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:3
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 4
Statement : input pkt_valid,
Signal : pkt_valid
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:9
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 8
Statement : input [7:0] data_in,
Signal : data_in[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:8
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 14
Statement : output [7:0] data_out_0,

Signal : data_out_0[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:11
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 16
Statement : output [7:0] data_out_2
Signal : data_out_2[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:5
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 6
Statement : input read_enb_1,
Signal : read_enb_1
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:10
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 15
Statement : output [7:0] data_out_1,
Signal : data_out_1[7:0]
Module : router_top
DesignObjHierarchy : router_top

Tag : RegInputOutput-ML
Description : Port '[Signal]' is not registered [Hierarchy: '[DesignObjHierarchy]']
Violation : Lint:4
Goal : lint_rtl
FileName : ./rtl/router_top.v
LineNumber : 5
Statement : input read_enb_0,

Signal : read_enb_0
Module : router_top
DesignObjHierarchy : router_top

ReportPortInfo-ML (1 info/0 waived)

Tag : ReportPortInfo-ML

Description : Port Information for top design unit has been generated. For details see report

ReportPortInfo.rpt

Violation : Lint:15

Goal : lint_rtl

FileName :

/home1/BRN47/HarshaVD/VLSI_RN/Verilog_labs/Router_Lint/script/vcst_rtdb/spyglass/vc_lint0/
router_top/VC_GOAL0/spyglass_reports/morelint/ReportPortInfo

LineNumber : 1

Statement : # Comment : Report Top Level Module Port Info