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CLASS :BSSE SECTION(A)

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SUBJECT : COMPUTER LOGIC DESIGN

ROLL NUMBER : 21

LAB 1

BASIC AND, OR & NOT LOGIC GATES

OBJECTIVE:

- To investigate the behavior of the OR gate using IC & Transistor.
- To investigate the behavior of the AND gate using IC & Transistor.
- To investigate the behavior of the NOT gate using IC & Transistor.

THEORY:

In general logic circuits have one or more inputs and only one output. The circuits respond to various input combinations and a truth table shows this relationship between circuits input combinations and its output. The truth table for a particular circuit explains how the circuit behaves under normal conditions. Familiarization with a logic circuit's truth table is essential to the technologist or technician before he or she can design with or troubleshoot the circuit.

In this experiment three logic circuits are covered: the OR, AND & NOT gates.

The OR operation can be summarized as follows:

1) When any input is 1, the output is also 1.
2) When all inputs are 0, the output is also 0.

The AND operation can be summarized similarly:

1) When any input is 0, the output is also 0.
2) When any input is 1, the output is also 1.

Finally, the NOT operation is said to be complementary.

1) If the input is 0, the output is 1.
2) If the input is 1, the output is 0.

You should recall that the logic levels 0 and 1, have voltage assignments. For TTL circuits a logic 0 can be anywhere from 0 V to +0.8 V, and a logic 1 is in the range of +2.0 V to +5.0.

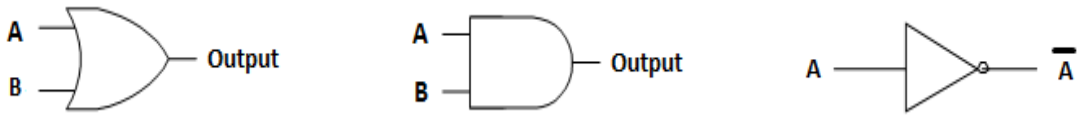
EQUIPMENT / REQUIREMENT:

- 7411 IC AND gate
- 7432 IC OR gate

- 7404 IC NOT gate
- 2 LEDs or Logic Probe
- 6 NPN Transistor
- Breadboard
- 0-5 Volt DC Power Supply

PROCEDURE:

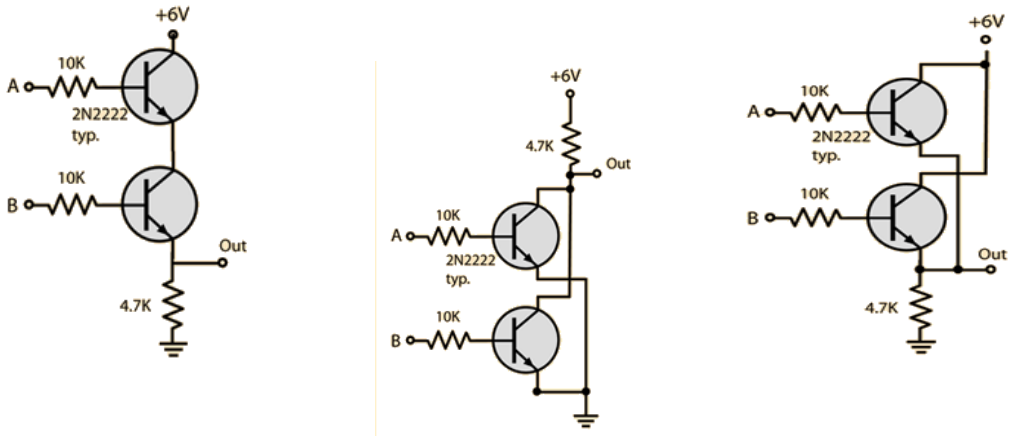
Figure 1.1 shows logic symbols of AND, OR and NOT gates. *Figure 1.2* shows the layouts of AND gate IC (7411), OR gate IC (7432) and NOT gate IC (7404). The pin configuration is also given in the layouts. Construct the circuits with the help of these layouts. Pin no 7 and pin no 14 of each IC is ground and VCC respectively. Apply different inputs and observe the outputs and then compute the truth *tables 1.1, 1.2 and 1.3*.



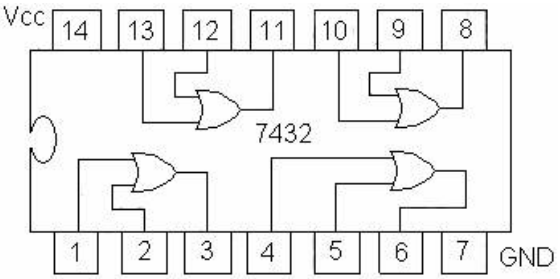
(a) Symbol of OR gate (b) Symbol of AND gate (c) Symbol of NOT gate

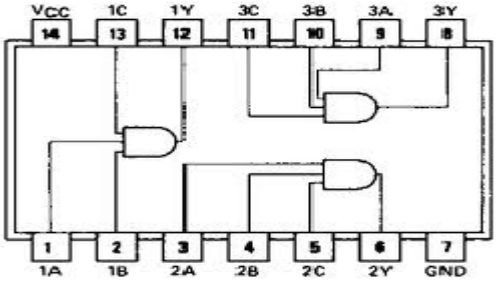
Fig 1.1

Internal Circuits of AND, OR, NOT Gate using Transistor:

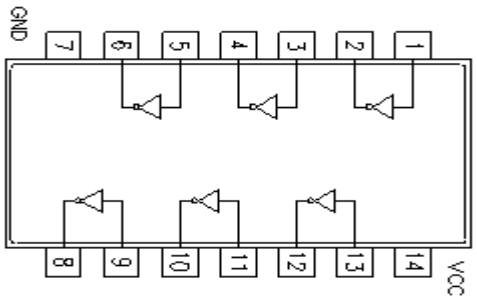


(a) AND gate (b) NOT gate (c) OR gate





(a) 7432 quad 2-input OR gate IC *(b) 7411 3 input AND gate*



(c) 7404 (Hex Inverter) NOT gate IC

Figure 1.2:

OBSERVATION TABLE:

A	B	Q=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Table 1.1

A	B	Q=A*B
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

Table 1.2

A	A'
0	**1**
1	**0**

Table 1.3

QUESTIONS / RESULTS:

1. The output of an OR gate is LOW only when both inputs are off
2. The output of an AND gate is _zero____ whenever any input is LOW.
3. If an OR gate input were accidentally shorted to VCC, the output of the gate would always be high no matter what level the other input level might be.
4. A High Voltage (5volt) stood for a high logic state

Addition Task to be performed:

1. (AB+CD)
2. (A+B.C+D)

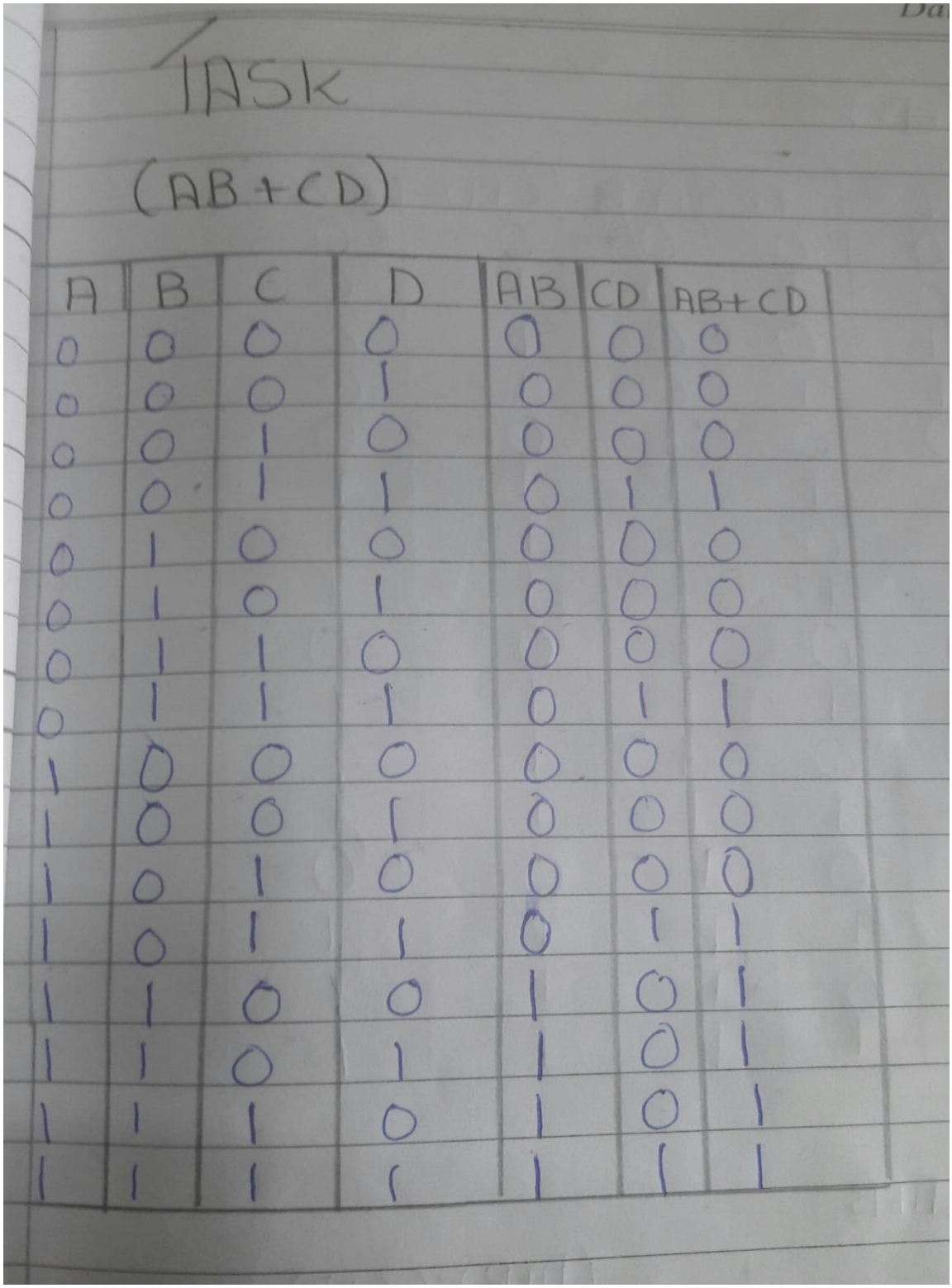
CONCLUSION

AND:AND gate gives high output when both inputs are on.

OR:OR gate gives high output when only one input is on.

NOR:NOR gate inverse the value of input.

TASK 1:

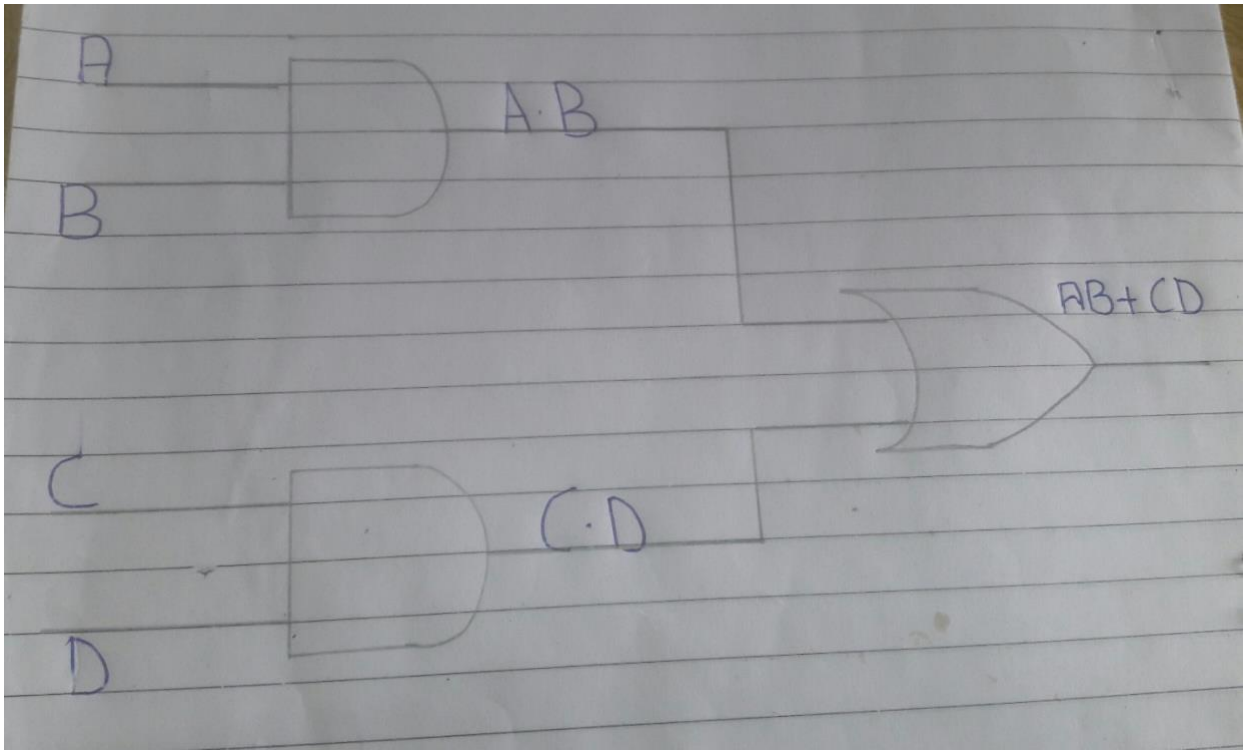


TASK

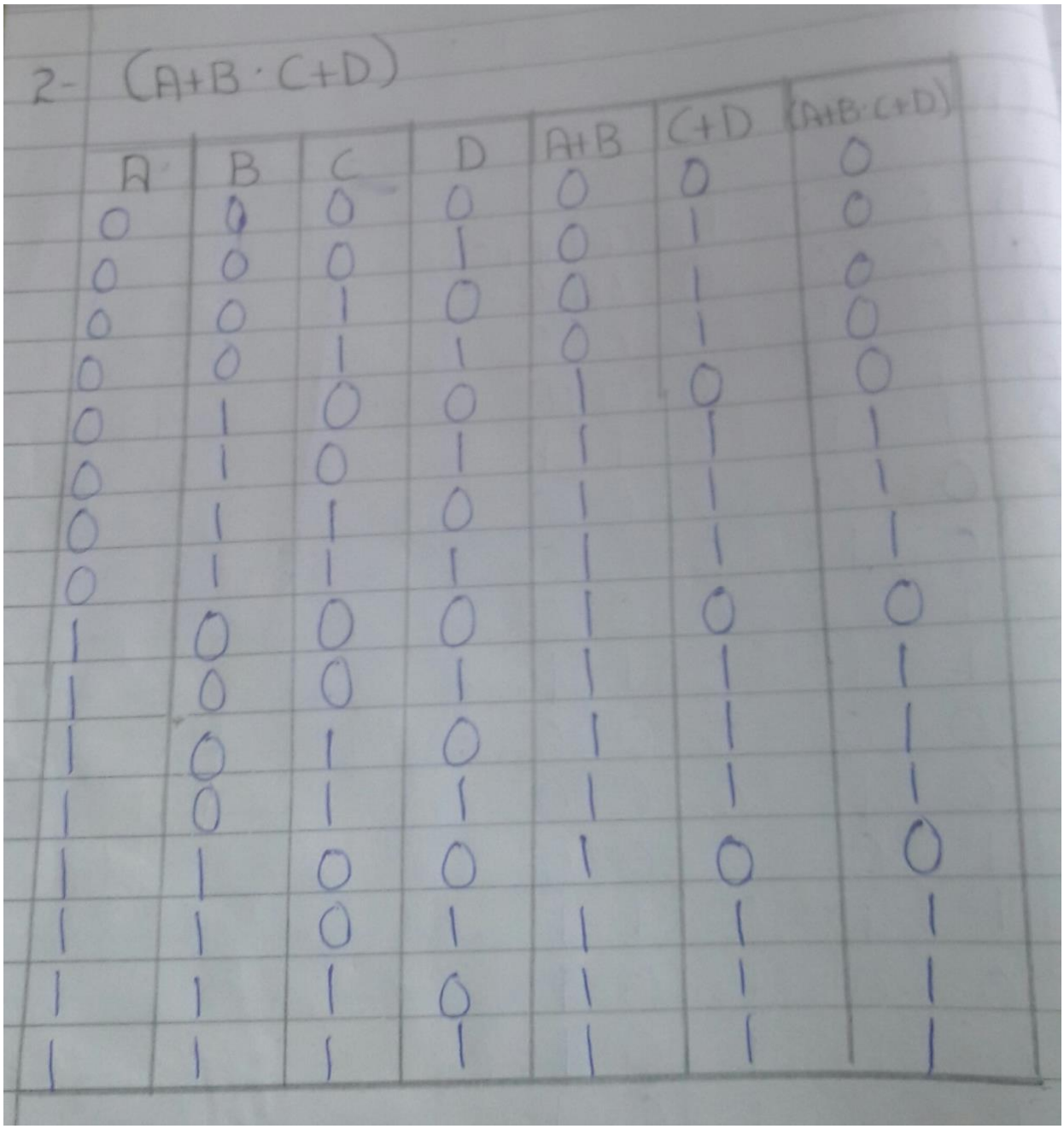
(AB+CD)

A	B	C	D	AB	CD	AB+CD
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	1

DIAGRAM:



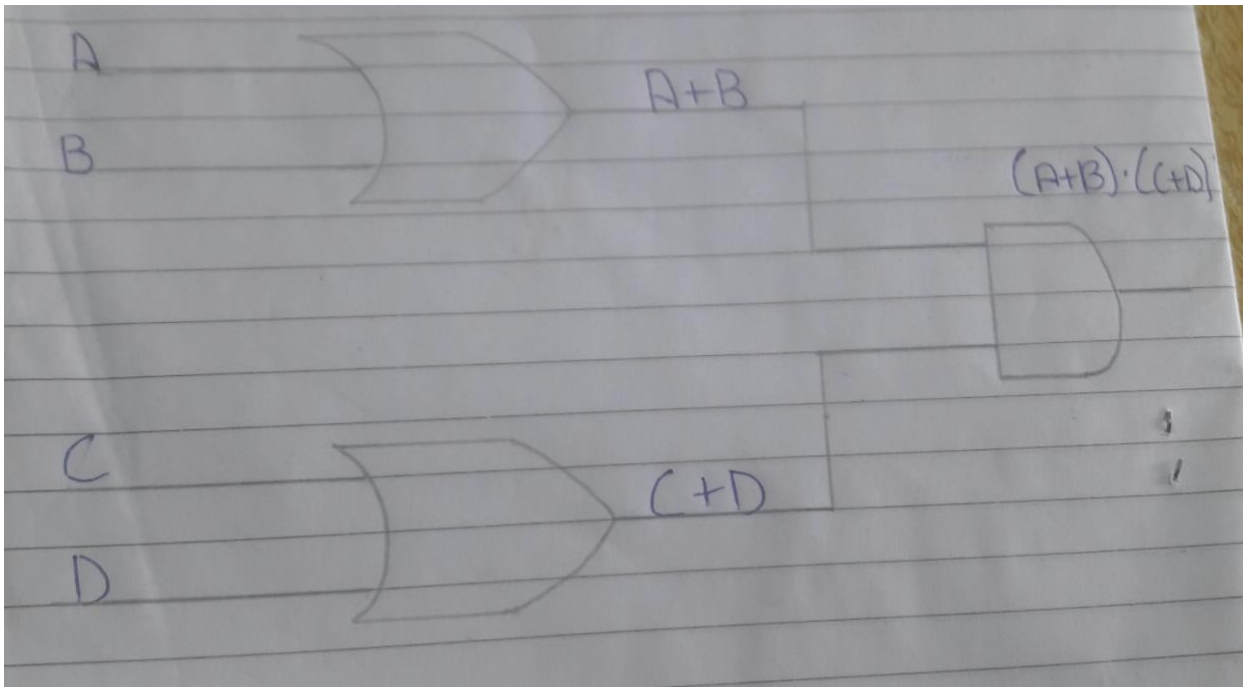
TASK 2:



2- (A+B · C+D)

A	B	C	D	A+B	C+D	(A+B · C+D)
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	1	1	1
0	1	1	0	1	1	1
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	0	0
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

DIAGRAM:



LAB 2

NAND & NOR GATE

OBJECTIVE:

- To investigate the behavior of the NOR gate using IC & Transistor.
- To investigate the behavior of the NAND gate using IC & Transistor.

THEORY:

In Experiment 1, you learned the characteristics of three of the fundamental logic gates: the AND, OR, and NOT. You will now be introduced to two of the remaining logic gates: the NAND and NOR. The NAND and NOR gates are nothing more than inverted AND and OR gates, respectively. That is important, but not the most important thing. The fact that a NAND or a NOR can be used to create all other gates is important, because this fact has made them more popular in use than the others.

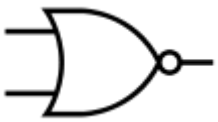
EQUIPMENT / REQUIREMENT:

- 7400 IC
- 7402 IC
- 4 NPN Transistor
- 4 LED or Logic probe
- 0-5 volt DC power supply

PROCEDURE:

Figure 2-1 shows logic symbols of NAND & NOR *Figure 2-2* shows the layouts of NAND gate IC (7400) & NOR gate IC (7402). The pin configuration is also given in the layouts. Construct the circuit with the help of these layouts. Pin no. 7 and Pin no. 14 of each IC is Ground and VCC respectively. Apply different inputs on the given input pins and observe the out puts, and then complete the truth *tables 2-1* and *2-2* of these gates.

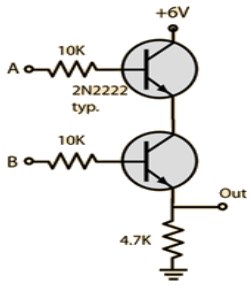
(a) NAND gate Symbol

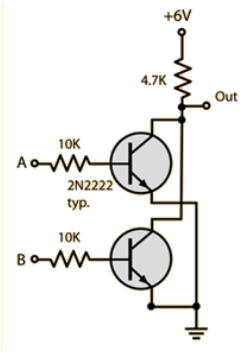


(b) NOR gate Symbol

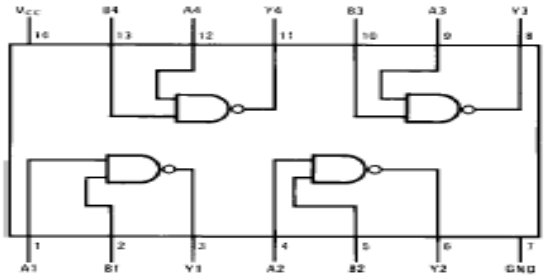
Fig2-1

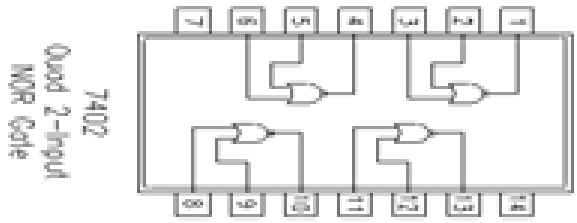
Internal Circuits of NAND, NOR Gate using Transistor





(a) NAND gate ***(b) NOR gate***





(a) IC configuration NAND 7400 gate ***(b) IC Configuration NOR 7402 gate***

Fig 2-2

<u>OBSERVATION TABLE:</u>

A	B	Q=(A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table 2-1 for NOR gate

A	B	Q=(A*B)’
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table 2-2 for NAND gate

QUESTIONS / RESULTS:

5. Why are NAND and NOR gates called universal gates?

ANSWER:THE NAND AND NOR GATES ARE CALLED UNIVERSAL GATE BECAUSE THEY PERFORM ALL THE LOGICAL OPERATIONS OF BASIC GATES LIKE AND,OR,NOT.

2.If the 0 and 1 were inputs for a NAND gate ,what would be the output?

ANSWER:THE OUTPUT WOULD BE HIGH

3.If a signal passing through a gate is inhibited by sending a low into one of the input and the output is light ,the gate is an NAND.

4.What used with an IC , What does the term “Quaid” indicates?

ANSWER: It means the IC contains 4 blocks with same functionality.

5.A high voltage (5 volt) stood for a NAND GATE.

Addition Task to be performed:

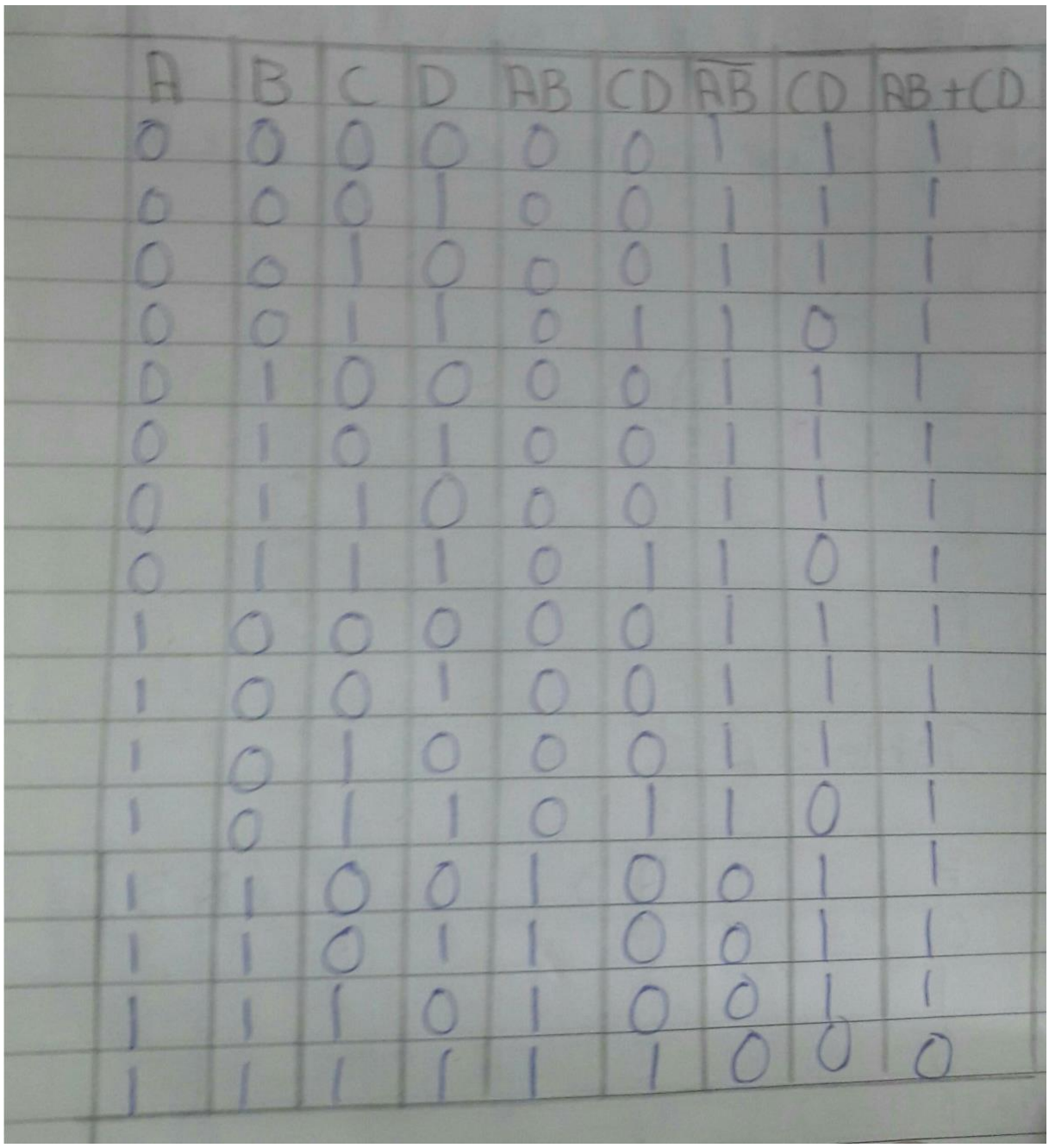
3. Implement OR gate using NAND gate
4. Implement AND, OR gate using NOR gate

CONCLUSION:

NAND: A NAND GATE PRODUCES LOW OUTPUT ONLY WHEN BOTH THE INPUTS ARE ON.

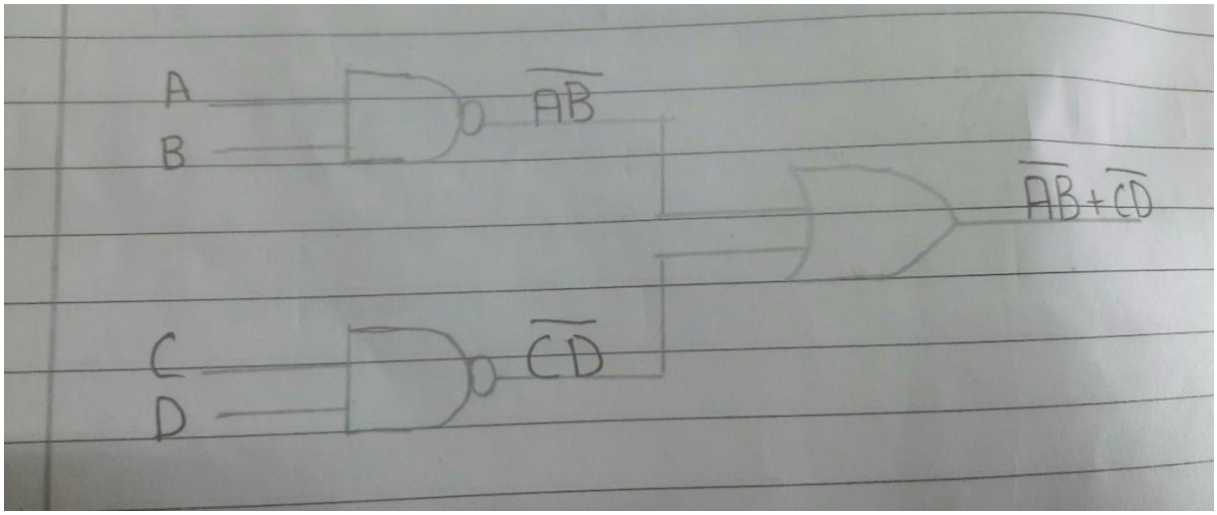
NOR: A NOR GATE PRODUCE HIGH OUTPUT ONLY WHEN BOTH THE INPUTS ARE OFF.

TASK 1:

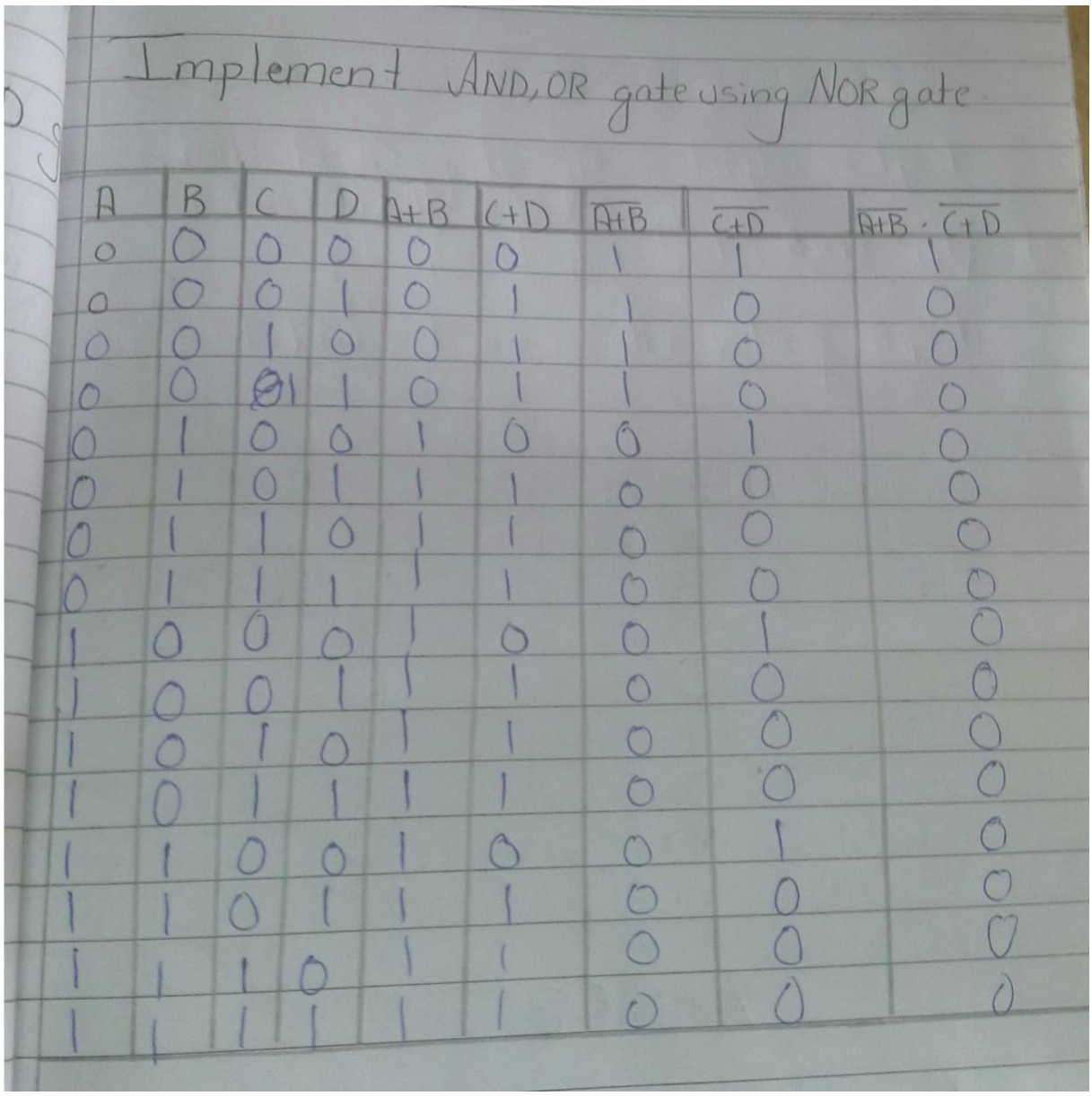


A	B	C	D	AB	CD	$\overline{AB}$	$\overline{CD}$	AB+CD
0	0	0	0	0	0	1	1	1
0	0	0	1	0	0	1	1	1
0	0	1	0	0	0	1	1	1
0	0	1	1	0	1	1	0	1
0	1	0	0	0	0	1	1	1
0	1	0	1	0	0	1	1	1
0	1	1	0	0	0	1	1	1
0	1	1	1	0	1	1	0	1
1	0	0	0	0	0	1	1	1
1	0	0	1	0	0	1	1	1
1	0	1	0	0	0	1	1	1
1	0	1	1	0	1	1	0	1
1	1	0	0	1	0	0	1	1
1	1	0	1	1	0	0	1	1
1	1	1	0	1	0	0	1	1
1	1	1	1	1	1	0	0	0

DIAGRAM:



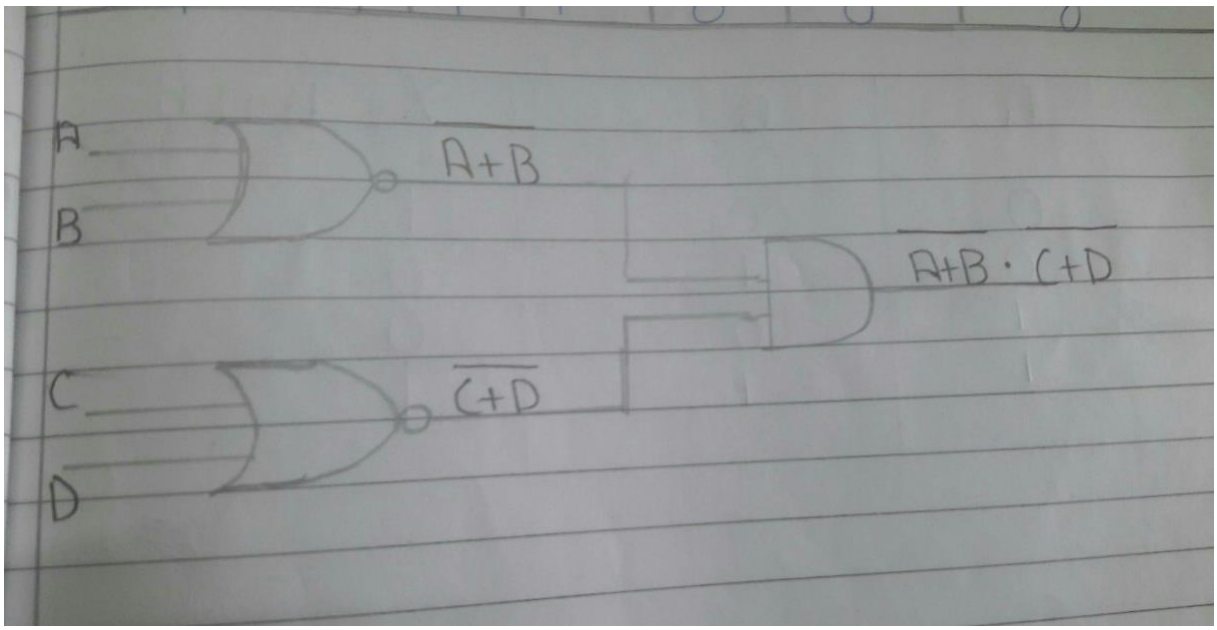
TASK 2:



Implement AND, OR gate using NOR gate.

A	B	C	D	A+B	C+D	$\overline{A+B}$	$\overline{C+D}$	$\overline{A+B} \cdot \overline{C+D}$
0	0	0	0	0	0	1	1	1
0	0	0	1	0	1	1	0	0
0	0	1	0	0	1	1	0	0
0	0	1	1	0	1	1	0	0
0	1	0	0	1	0	0	1	0
0	1	0	1	1	1	0	0	0
0	1	1	0	1	1	0	0	0
0	1	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	0	0	1	1	1	0	0	0
1	0	1	0	1	1	0	0	0
1	0	1	1	1	1	0	0	0
1	1	0	0	1	0	0	1	0
1	1	0	1	1	1	0	0	0
1	1	1	0	1	1	0	0	0
1	1	1	1	1	1	0	0	0

DIAGRAM:



LAB 3

TO STUDY EXCLUSIVE-OR & EXCLUSIVE-NOR GATE

OBJECTIVE:

- To investigate the behavior of the EX-OR
- To investigate the behavior of the EX-NOR

THEORY:

In Experiment 1&2, you learned the characteristics fundamental logic gate. You will now be introduced to two of the remaining logic gates, the EX-OR and EX-NOR. An exclusive OR (XOR) gate is gate with two or more three inputs and one output an output of two inputs XOR assumes a high state if one and only one input assume a high state. This is equivalent to saying that the output is a High if either input X or Y is high exclusively, and low when both are 1 and 0 simultaneously.

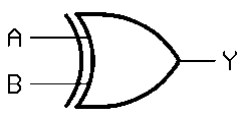
The **Exclusive-NOR Gate** function or Ex-NOR for short, is a digital logic gate that is the reverse or complementary form of the Exclusive-OR function. the output of an Exclusive-NOR gate **ONLY** goes "HIGH" when its two input terminals, A and B are at the "**SAME**" logic level which can be either at a logic level "1" or at a logic level "0".

EQUIPMENT / REQUIREMENT:

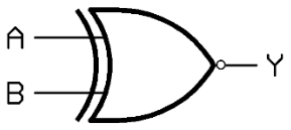
- 7486 IC XOR
- 74266 IC XNOR
- 2 LED or Logic probe
- 0-5 volt DC power supply

PROCEDURE:

Figure 2-1 shows logic symbols of XOR & XNOR *Figure 2-2* shows the layouts of XOR gate IC (7486) & XNOR gate IC (74266).The pin configuration is also given in the layouts. Construct the circuit with the help of these layouts. Pin no. 7 and Pin no. 14 of each IC is Ground and VCC respectively, Apply different inputs on the given input pins and observe the out puts, and then complete the truth *tables 3-1* and *3-2* of these gates.

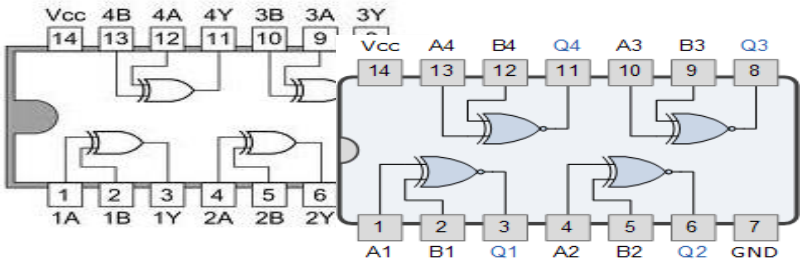


(b) XOR gate Symbol



(b) XNOR gate Symbol

Fig3-1



(a) IC configuration 7486 *(b) IC Configuration 74266*

Fig3-2

OBSERVATION TABLE:

A	B	$X = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

3-1 Truth Table for XOR gate

A	B	$X = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

3-2 Truth Table for XNOR gate

QUESTIONS / RESULTS

6. If the 0 and 1 were inputs for a XOR gate, what would be the output
   ANSWER: THE OUTPUT WOULD BE HIGH.
7. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is LOW, the gate is an **XNOR**.
8. XNOR provides the inverted output of an XOR. **TRUE**.

CONCLUSION:

XOR:XOR GATE GIVES HIGH OUTPUT WHEN BOTH THE INPUT ARE NOT IDENTICAL (BOTH 0'S AND 1'S)

XNOR:XNOR GATE GIVES HIGH OUTPUT WHEN BOTH THE INPUTS ARE IDENTICAL (BOTH 0'S AND 1'S)

LAB 4

BOOLEAN ALGEBRA

OBJECTIVE:

- To verify experimentally some of the Boolean theorems.

THEORY:

Boolean algebra is the mathematics we use to analyze digital gates and circuits. We can use these "Laws of Boolean" to both reduce and simplify a complex Boolean expression in an attempt to reduce the number of logic gates required. *Boolean algebra* is therefore a system of mathematics based on logic that has its own set of rules or laws which are used to define and reduce Boolean expressions. The combinational logic circuits do not have the ability to memorize their past. The result is that combinational logic circuits have no feedback and any changes to the signals being applied to their inputs will immediately have an effect at the output.

PROCEDURE:

Boolean Theorems: Following Boolean theorems table mount a *7404 IC*, a 7408 IC, and a 7432 IC on the circuit board. Connect *VCC* to *+5 V* and GND to power ground on each IC. To verify each theorem, connect the circuit for that theorem. Monitor the output with logic probe and also with LED.

EQUIPMENT / REQUIREMENT:

- 7404IC
- 7408 IC
- 7432 IC
- LED
- 0-5 VOLT DC Power Supply.

BOOLEAN THEORAM:

Idem potency	X + X = X X • X = X
Redundancy Law	*X+X.Y*
Double negation	$\bar{\bar{X}}$ = X
Commutative Law	X + Y = Y+X
Associative laws	X + (Y + Z) = (X + Y) + Z

Distributive laws	X (Y + Z) = XY + XZ
Absorption	X + XY = X
De Morgan's theorem	(X1 + X2 + X3.....) = X1 • X2 • X3..... (X1 • X2 • X3.....) = X1 + X2 + X3.....

RULES OF BOOLEAN ALGEBRA

1. X+0=X
2. X+1=1
3. X.0=0
4. X.1=1
5. X+X=X
6. $X+\overline{X}= X$
7. X.X=X
8. $X.\overline{X}= 0$
9. $\overline{\overline{X}}.X=X$
10. X+XB=A
11. $X+X\overline{B}=X+B$
12. (X+B)(X+C)=X+BC

Verify circuit by using IC's on breadboard.

X	X+0	X+1=1	X.0=0	X.1=1	X+X=X	X+X= X	X.X= X	X.X= 0
0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**
1	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**

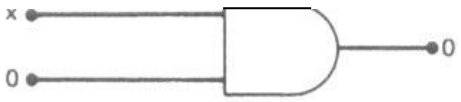
Table 4.1

x	y	Z	X + (Y + Z)	X + XY	*X+X.Y*	x (x + y)
0	**0**	**0**	**0**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**	**0**	**0**
1	**0**	**1**	**1**	**1**	**1**	**1**
1	**1**	**1**	**1**	**1**	**1**	**1**

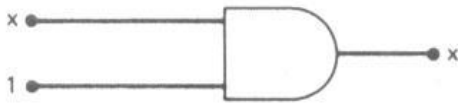
Table 4.2

CIRCUIT IMPLEMENTATION:

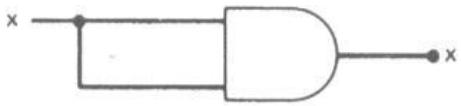
(1) $x \cdot 0 = 0$



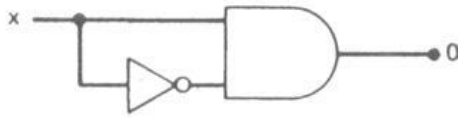
(2) $x \cdot 1 = x$



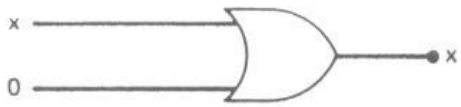
(3) $x \cdot x = x$



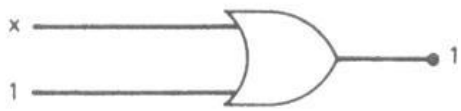
(4) $x \cdot \overline{x} = 0$



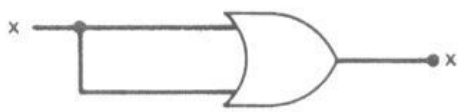
(5) $x + 0 = x$



(6) $x + 1 = 1$



(7) $x + x = x$



(8) $x + \overline{x} = 1$

Task#1: Construct Circuit for Redundancy Law

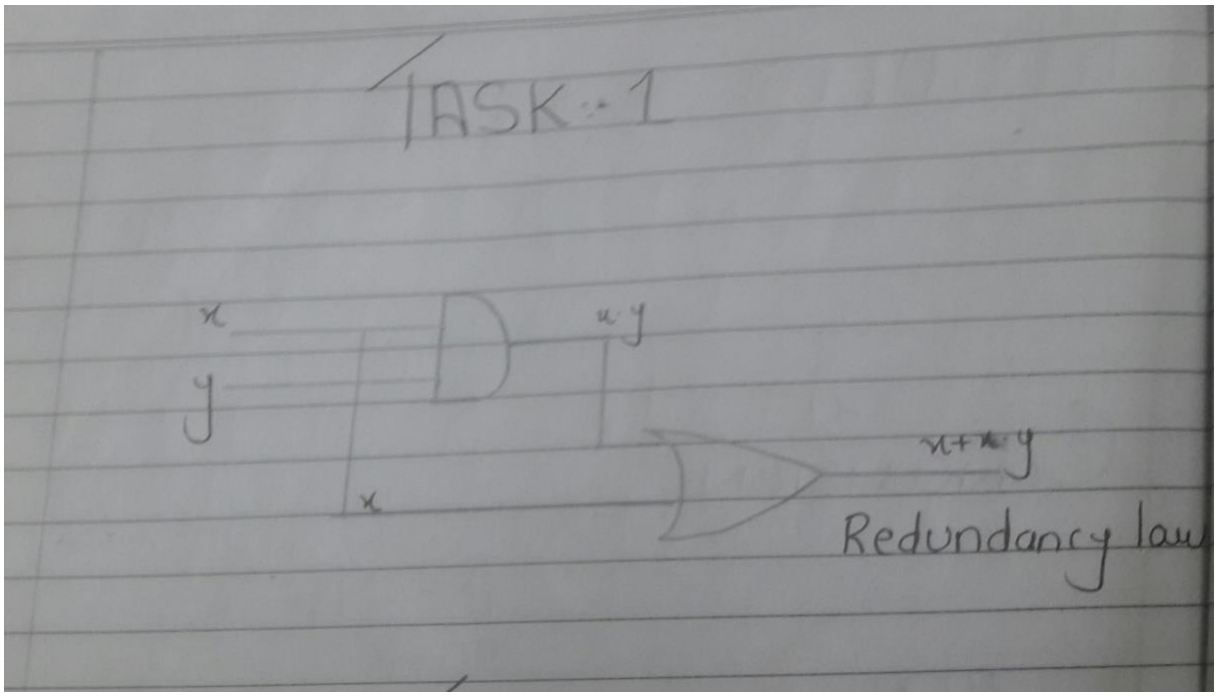
Task#2: Draw logic diagram for x (x + y) and also find out the output x (x + y) =?

Task#3: Construct the circuit for Associative & Absorption theorems and observe the Output.

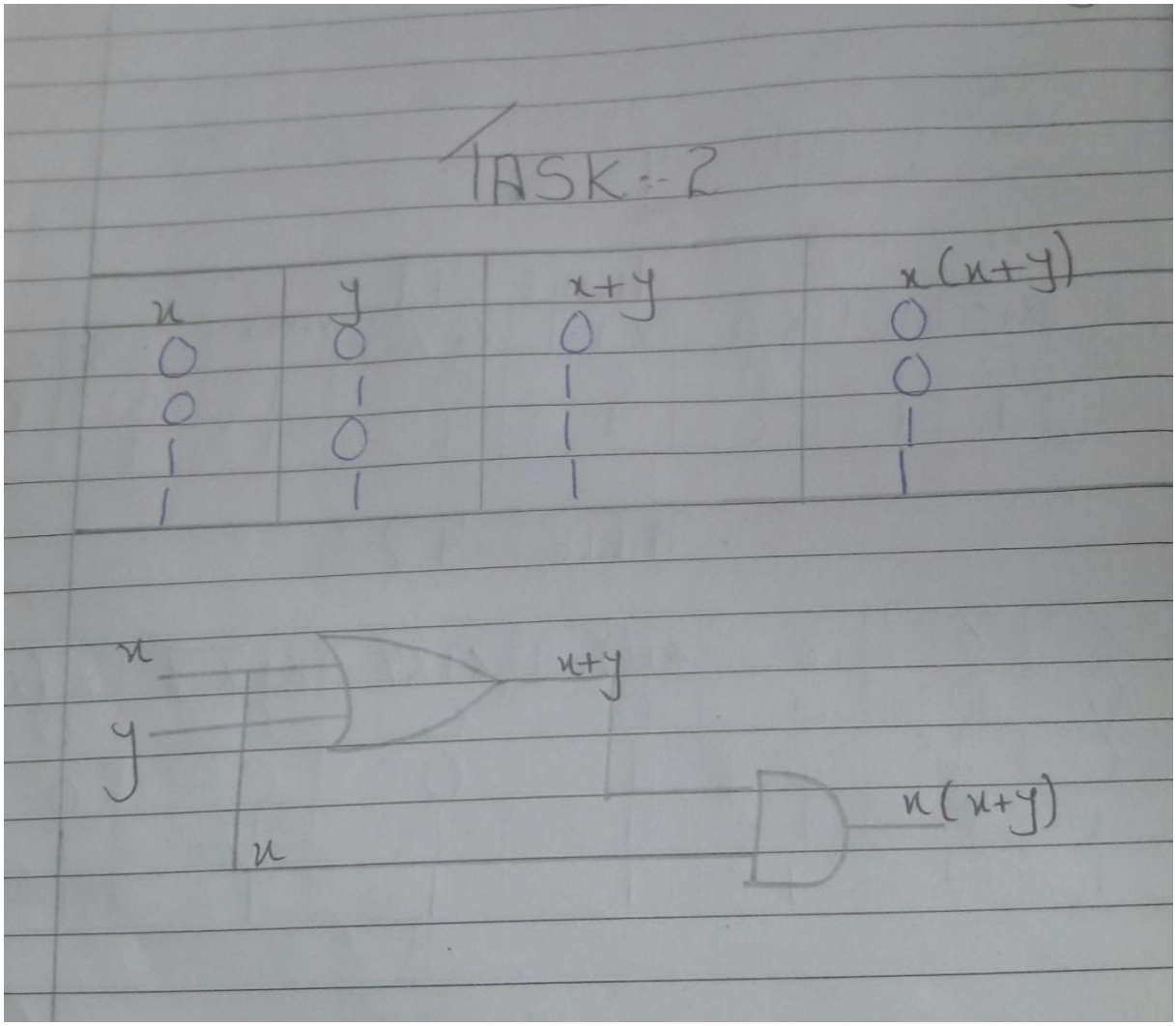
CONCLUSION:

BOOLEAN ALGEBRA IS A BRANCH OF ALGEBRA IN WHICH THE VALUES OF THE VARIABLES ARE THE TRUTH VALUES TRUE AND FALSE USUALLY DENOTED BY 1 AND 0 RESPECTIVELY

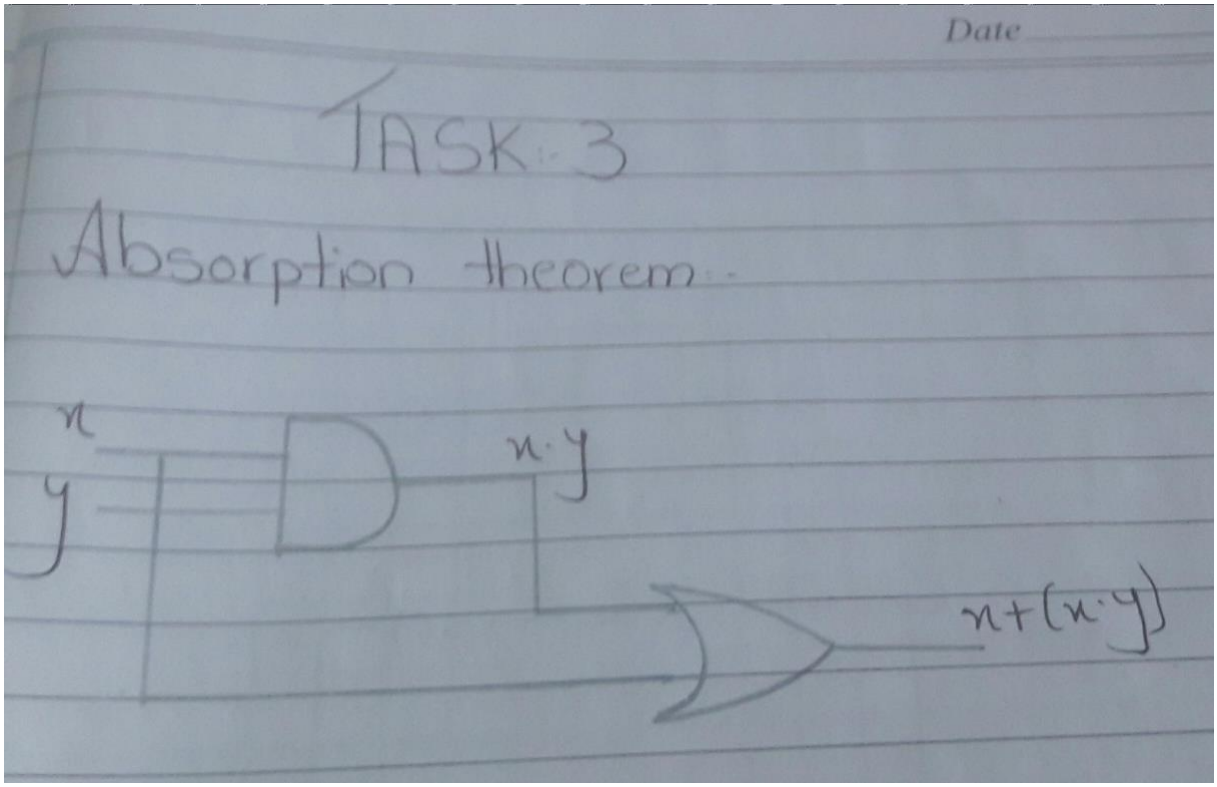
TASK 1:



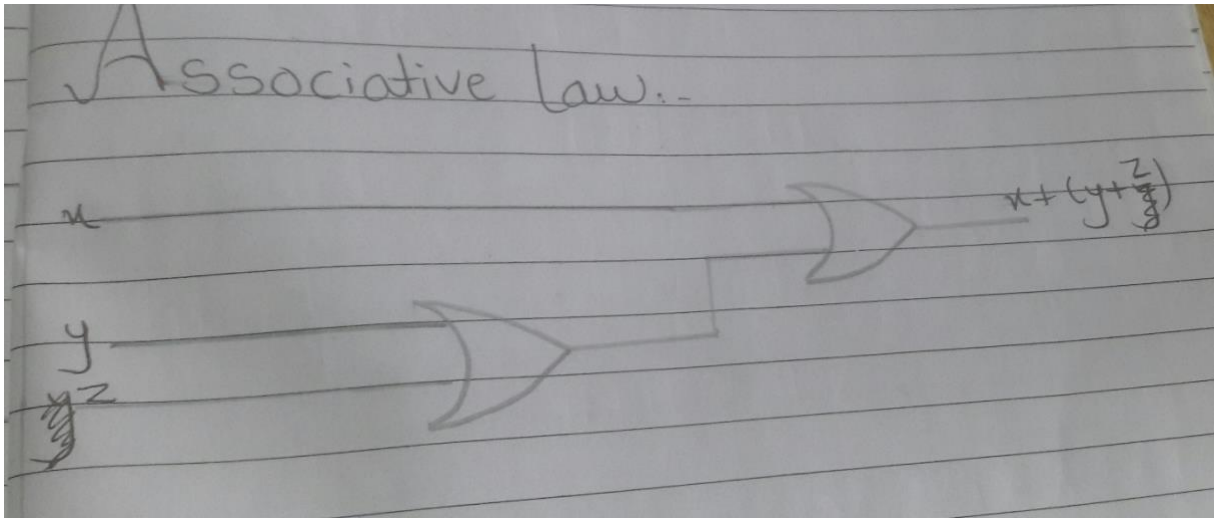
TASK 2:



TASK 3:



Associative law.-



LAB 5

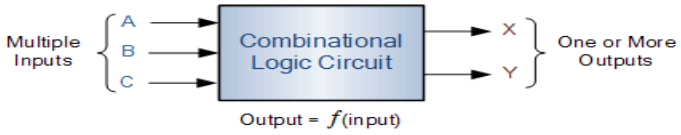
COMBINATIONAL CIRCUITS

OBJECTIVE:

- Implementation of Combinational Circuits.

PROCEDURE:

Combination Circuits: The combinational logic circuits are a type of logic circuits containing only logic gates (AND, OR, XOR, NOT, NAND, NOR) and its output only depends on the current input (do not have memory).



The three main ways of specifying the function of a combinational logic circuit are:

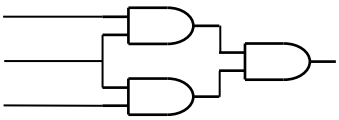
1. **Boolean algebra:** This forms the algebraic expression showing the operation of the logic circuit for each input variable either True or False that result in a logic "1" output.
2. **Truth Table:** A truth table defines the function of a logic gate by providing a concise list that shows all the output states in tabular form for each possible combination of input variable that the gate could encounter.
3. **Logic Diagram:** This is a graphical representation of a logic circuit that shows the wiring and connections of each individual logic gate, represented by a specific graphical symbol that implements the logic circuit.

EQUIPMENT / REQUIREMENT:

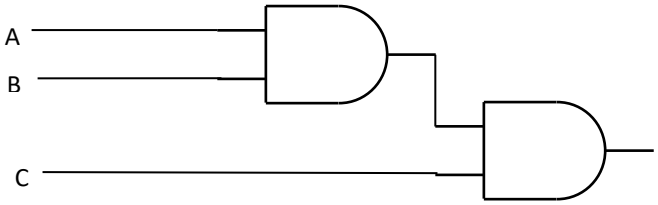
- 7404IC.
- 7408 IC.
- 7432 IC.
- 7400 & 7402 IC
- LED
- 0-5 VOLT DC Power Supply.

COMBINATIONAL LOGIC GATE SCHEMATIC

The circuit in the diagram below uses two-input AND gates to provide a three-input AND gate.



This is one method of producing a three-input AND gate

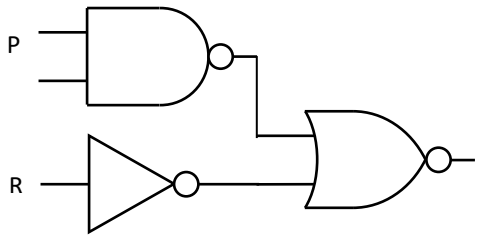


A truth table drawn for both circuits will show the logic function clearly:

C	B	A	O/P
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 5.1

Task#1: Derive the truth table and Boolean expression for the output of the following logic circuits.



R	Q	P	$\overline{P.Q}$	$\overline{R}$	$\overline{P.Q + R}$
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	0	0	1

Task#2*:* Implement circuit for the following equation

$Y=A\overline{B+C}+\overline{D+DE}$

A	B	C	D	E	Output
0	**0**	**0**	**0**	**0**	**1**
0	**0**	**0**	**0**	**1**	**1**
0	**0**	**0**	**1**	**0**	**1**
0	**0**	**0**	**1**	**1**	**1**

0	**0**	**1**	**0**	**0**	**1**
0	**0**	**1**	**0**	**1**	**1**
0	**0**	**1**	**1**	**0**	**1**
0	**0**	**1**	**1**	**1**	**1**
0	**1**	**0**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**1**
0	**1**	**0**	**1**	**0**	**1**
0	**1**	**0**	**1**	**1**	**1**
0	**1**	**1**	**0**	**0**	**1**
0	**1**	**1**	**0**	**1**	**1**
0	**1**	**1**	**1**	**0**	**1**
0	**1**	**1**	**1**	**1**	**1**
1	**0**	**0**	**0**	**0**	**1**
1	**0**	**0**	**0**	**1**	**1**
1	**0**	**0**	**1**	**0**	**1**
1	**0**	**0**	**1**	**1**	**1**
1	**0**	**1**	**0**	**0**	**1**
1	**0**	**1**	**0**	**1**	**1**
1	**0**	**1**	**1**	**0**	**1**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**0**	**0**	**0**	**1**
1	**1**	**0**	**0**	**1**	**1**
1	**1**	**0**	**1**	**0**	**0**
1	**1**	**0**	**1**	**1**	**0**
1	**1**	**1**	**0**	**0**	**0**
1	**1**	**1**	**0**	**1**	**1**
1	**1**	**1**	**1**	**0**	**0**
1	**1**	**1**	**1**	**1**	**0**

CONCLUSION:

COMBINATIONAL LOGIC CIRCUIT ARE MEMORY LESS DIGITAL CIRCUIT WHOSE OUTPUT AT ANY INSTANT IN TIME DEPENDS ONLY ON THE COMBINATIONAL OF ITS INPUT.

LAB 6

HALF ADDER

OBJECTIVE:

- To observe the working of half adder

THEORY:

Half adder: *A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits. The drawback of this circuit is that in case of a multi bit addition, it cannot cater to carry*.

EQUATION FOR HALF ADDER:

$$S = A \oplus B$$
$$C = A \cdot B$$

EQUIPMENT / REQUIREMENT:

- IC 7486
- 7408 IC.
- 7432 IC.
- Breadboard
- LED
- 0-5 VOLT DC Power Supply.

PROCEDURE:

Construct the combinational circuit as diagram given *figure 6.1* after constructing both of these circuits, observe the output and complete the truth table.

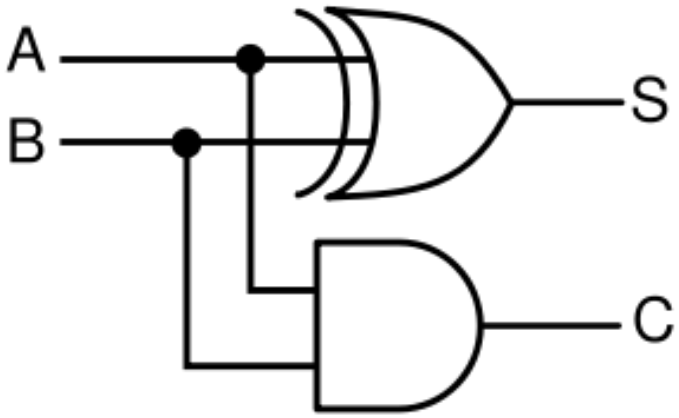


Figure 7.1 half adder circuit

OBSERVATION TABLE:

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 7.1

CONCLUSION:

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value. It has two inputs, called A and B, and two outputs S (sum) and C (carry)

LAB 7

FULL ADDER

OBJECTIVE:

- To observe the working of full adder

THEORY:

Full adder: A full adder is a logical circuit that performs an addition operation on three binary digits. The full adder produces a 'sum' and 'carry' value, which are both binary digits. It can be combined with other full adders or work on its own.

EQUATION FOR FULL ADDER:

$$S = (A \oplus B) \oplus C_i$$
$$C_o = (A \cdot B) + (C_i \cdot (A \oplus B)) = (A \cdot B) + (B \cdot C_i) + (C_i \cdot A)$$

EQUIPMENT / REQUIREMENT:

- IC 7486
- 7408 IC.
- 7432 IC.
- Breadboard
- LED
- 0-5 VOLT DC Power Supply.

PROCEDURE:

Construct the combinational circuit as diagram given figure 7.1. After constructing both of these circuits, observe the output and complete the truth table.

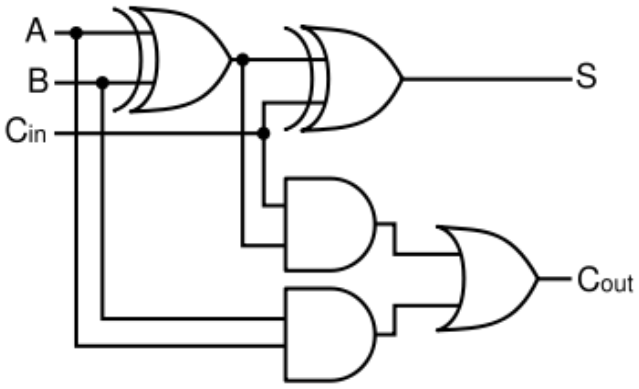


Figure 7.1 Full adder circuit

OBSERVATION TABLE:

A	B	Cī	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 7.1

QUESTIONS / RESULTS:

1. A full adder can be constructed from CONNECTING TWO HALF adders by connecting *A* and *B* to the input of _CARRY OUT___ half adder
2. Full adder performs the arithmetic addition of _3 inputs bits.
3. The HALF adder is one that does not take a carry-in from another adder.

CONCLUSION:

A full adder is a digital circuit that performs addition. ... A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits.

LAB 8

CONCLUSION:

DECODER:The decoder is a circuit used to change the code into a set of signals. The name its self tells the decoder because it has the reverse of encoding. The decoders are very simple to design.

ENCODER: An encoder in digital electronics is a one-hot to binary converter. That is, if there are 2^n input lines, and at most only one of them will ever be high, the binary code of this 'hot' line is produced on the n-bit output lines. A binary encoder is the dual of a binary decoder.