AHSANULLAH UNIVERSITY OF SCIENCE & TECHNOLOGY

Department of EEE

Project Submission

Course No : **EEE 4134**

Course Name : **VLSI-I Lab**

Year : **4th**

Semester : **1st**

Section : **C2**

Project Title : **High Performance 2-bit Magnitude Comparator Using Hybrid Logic Style**

Group Information

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Design of 2 Bit Magnitude Comparator

Abstract:

This project introduces a 2-bit binary Magnitude Comparator design using Conventional CMOS and Pass Transistor Logic. Through simulation and comparison with 5 other designs, the proposed MC demonstrates notable enhancements in speed, power, and Power Delay Product. This improvement positions it as a compelling and efficient alternative to existing Magnitude Comparator designs.

Background:

A 2-bit magnitude comparator is a digital circuit that compares two 2-bit binary numbers to determine their relative magnitudes. It's a fundamental building block in digital systems and is often used in arithmetic and control operations. The primary purpose of a magnitude comparator is to determine which of the two input numbers is greater, equal, or lesser. The operation of a 2-bit magnitude comparator involves comparing each pair of corresponding bits from the two input numbers. In a 2-bit comparator, there are four pairs of bits to compare: the most significant bit (MSB) pair, and then the two pairs of least significant bits (LSBs). The output of the comparator is generally represented using three output lines: one for "greater than," one for "equal," and one for "less than.

Future Aspect:

The 2-bit magnitude comparator could be integrated into larger digital systems and processors, where it forms a crucial component of arithmetic and logic operations. As energy efficiency becomes a more critical concern in digital circuit design, future 2-bit magnitude comparators might be optimized for lower power consumption. Future designs might focus on achieving higher operating speeds for 2-bit magnitude comparators, enabling faster comparison operations in digital systems. This could be achieved through improved transistor technologies, circuit optimizations, and advanced clocking methodologies.

Conclusion:

The research introduces a 2-bit microcontroller (MC) design using PTL (Pass-Transistor Logic) and CCMOS (Complementary CMOS) techniques. The design includes PTL-based VLSI circuits for input terminals and complex VLSI circuits using CCMOS logic for output signals. The implemented design is compared with other MC designs to assess its performance. The results demonstrate notable improvements in power-delay product (PDP) and delay, while still maintaining acceptable power consumption. Consequently, this proposed MC design appears well-suited for contemporary microprocessor design applications.

References

Paper Name : Design of a High-Performance 2-bit Magnitude Comparator Using Hybrid Logic Style

Reference : https://ieeexplore.ieee.org/document/9225524

Data Representation

Truth Table

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

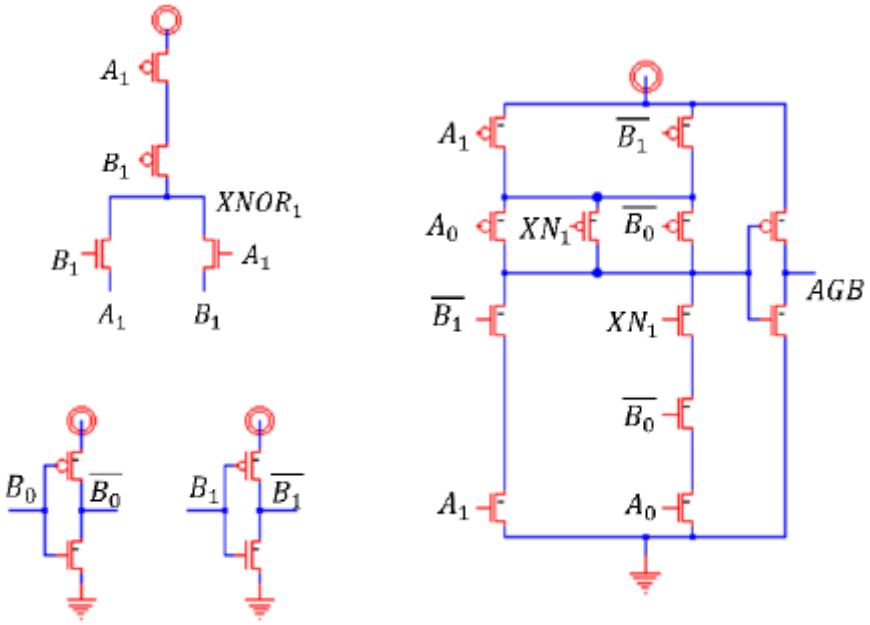
Comparison Table

Circuit	Propagation Delay (pS)	Average Power (µW)	Power Delay Product	Cell Area (μm^2)	No. of Transistors	No. of DRC Errors	No. of LVS Mismatches
A>B	10.03	727.6	7297.828	194.346	20	0	0
A=B	2.93	934.9	2739.257	29.3525	14	0	0
A<B	15.04	554.2	8335.168	87.7965	20	0	0

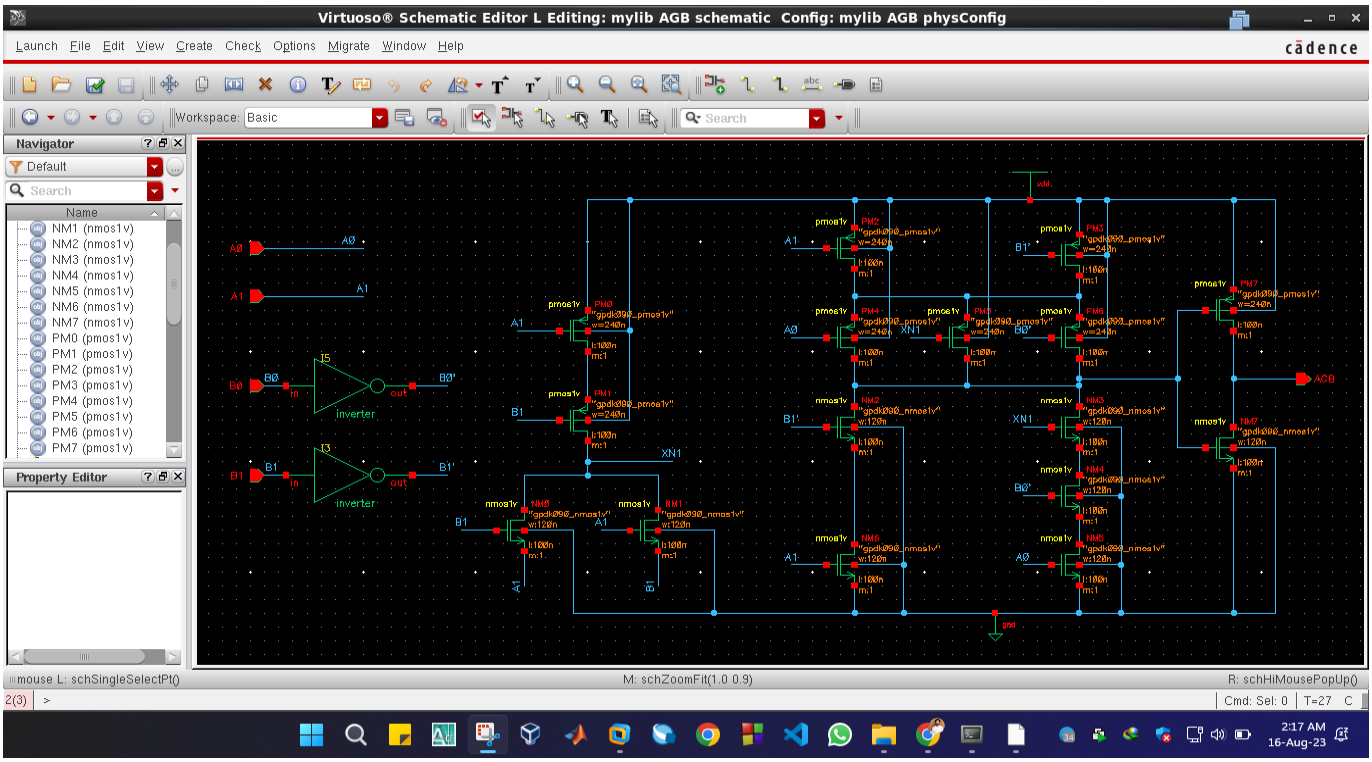
Pictorial Representation

Circuit-1(A>B):

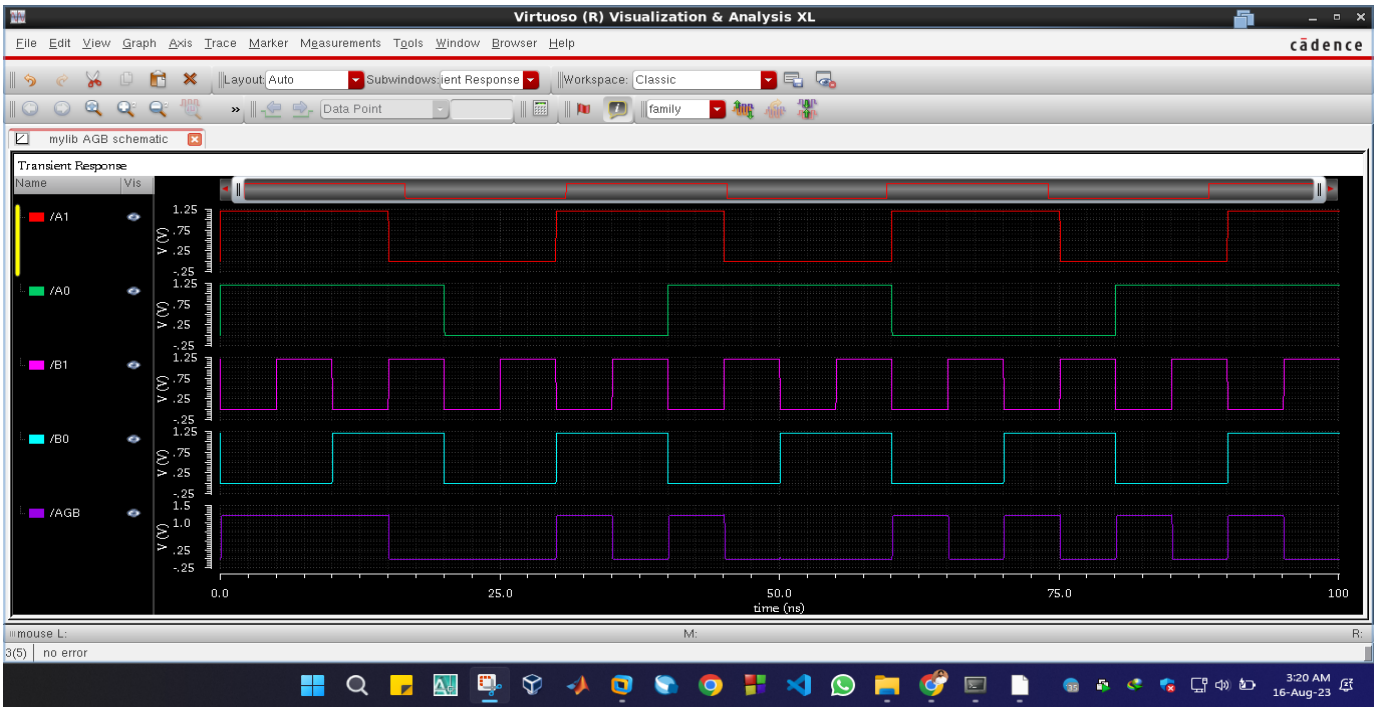
Circuit Diagram:



Schematic:

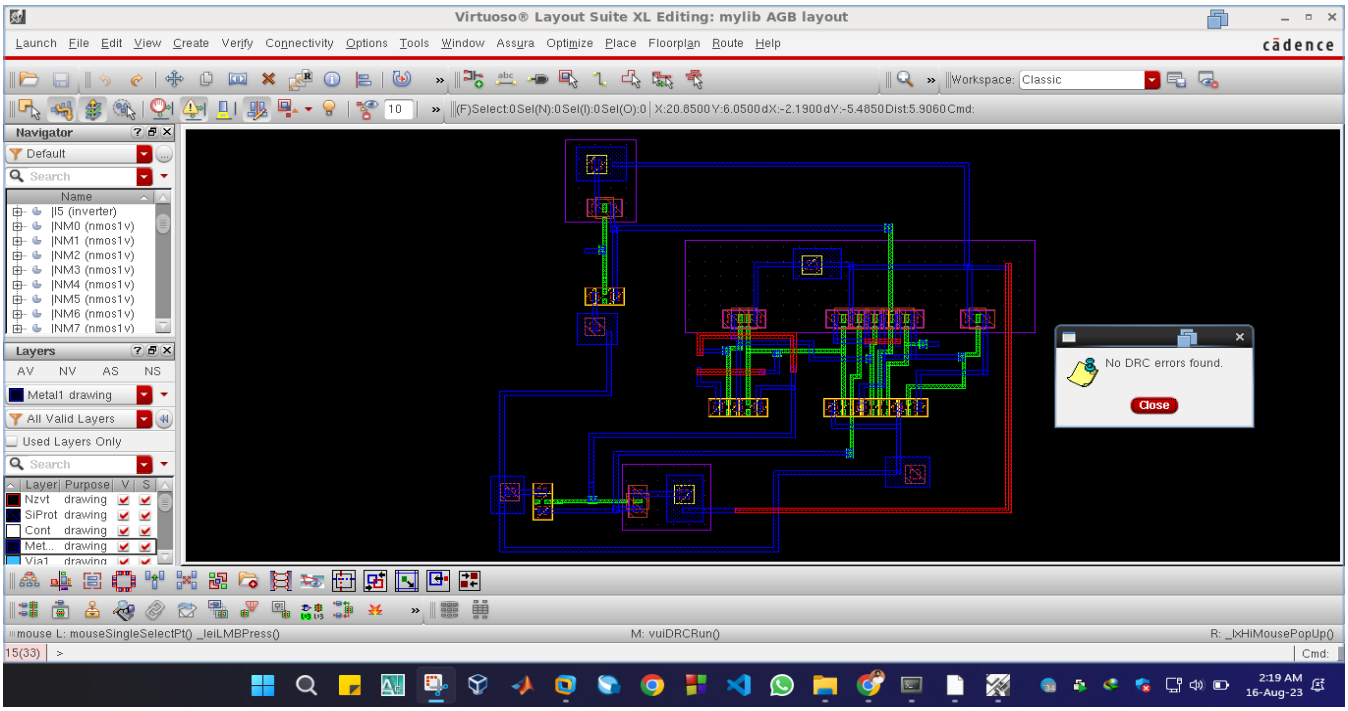


Output with Truth Table:

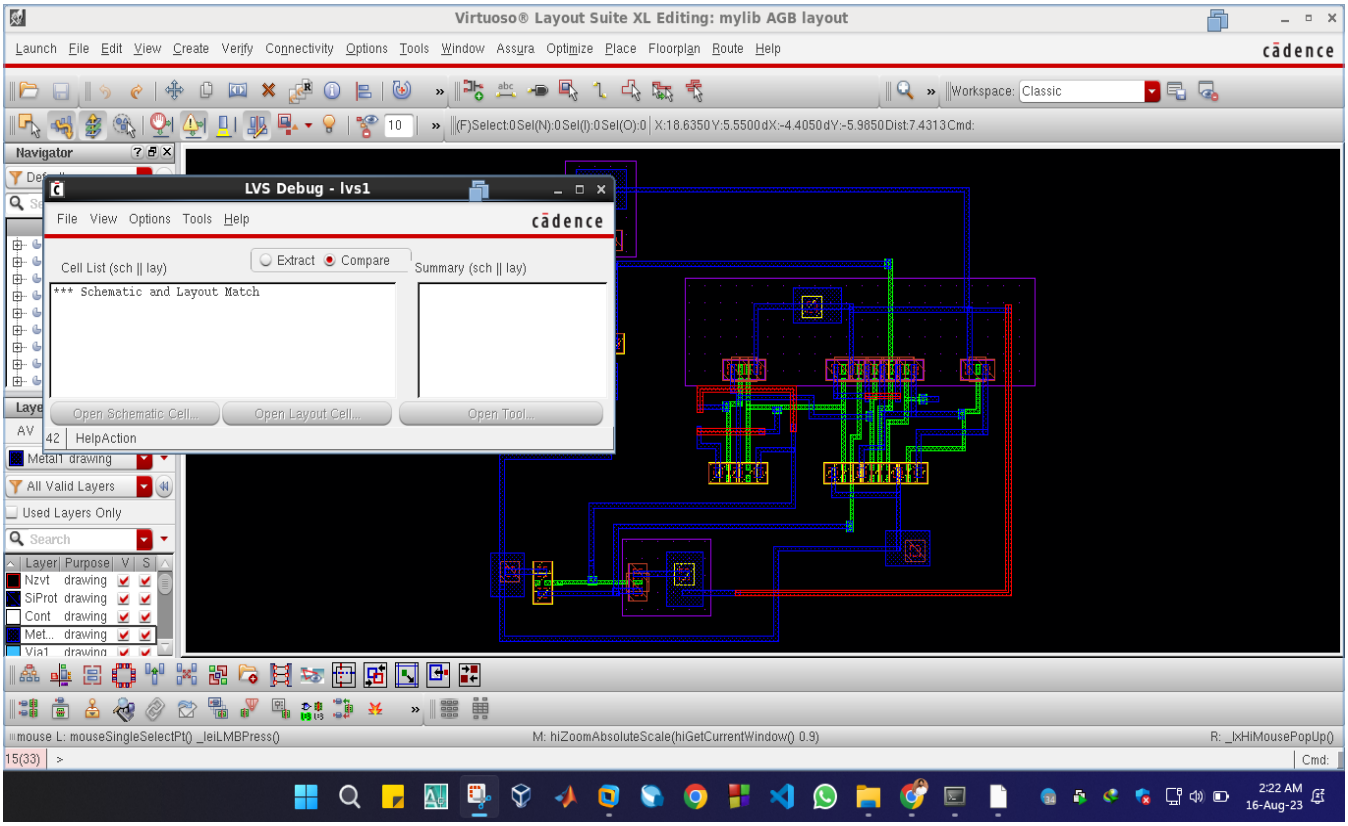


Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Layout with no DRC Error:

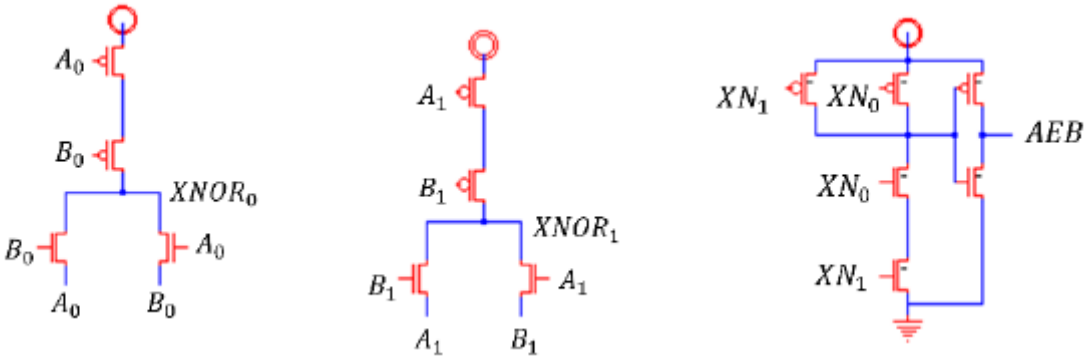


Layout with no LVS mismatch:

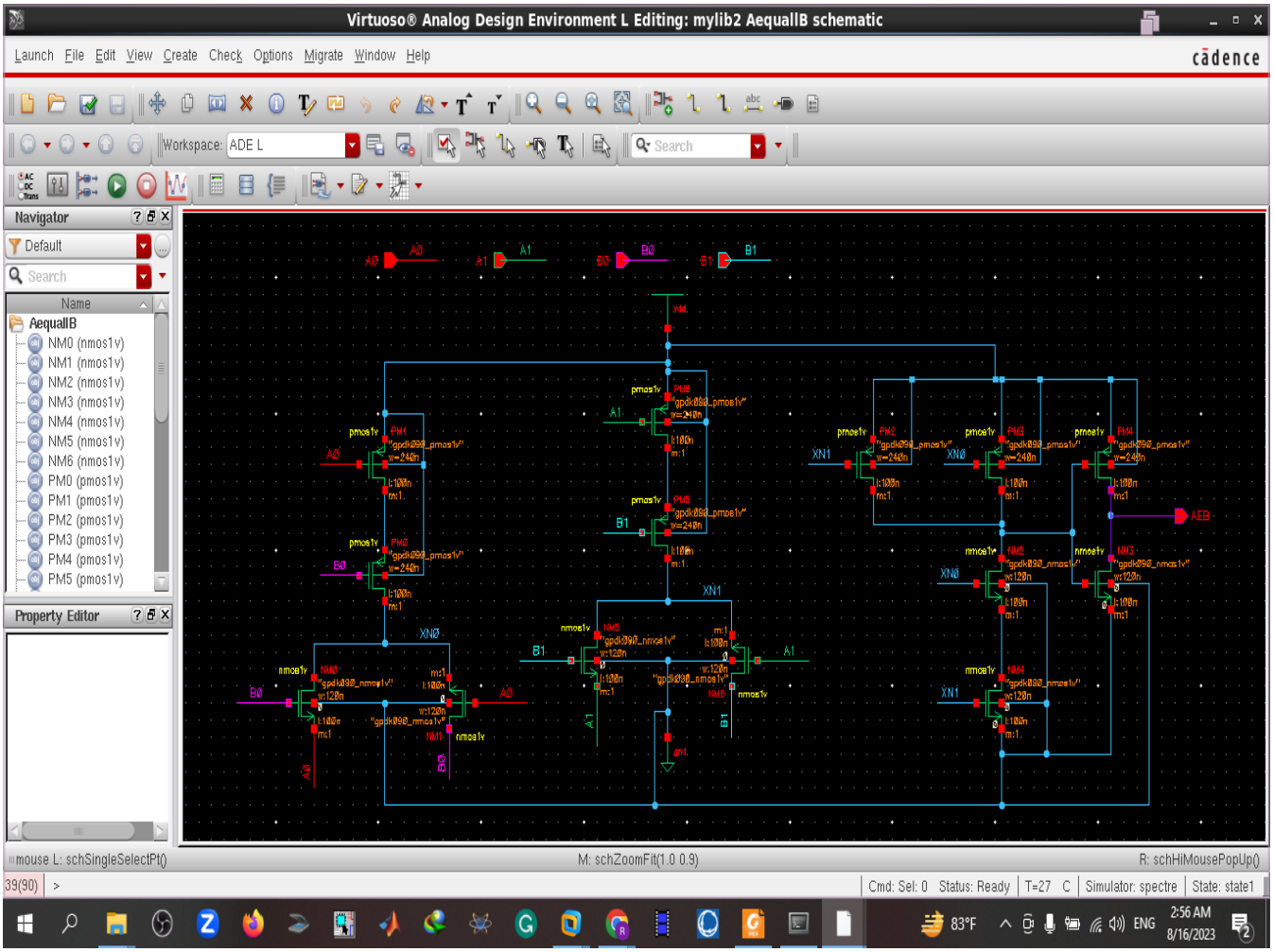


Circuit -2(A=B)

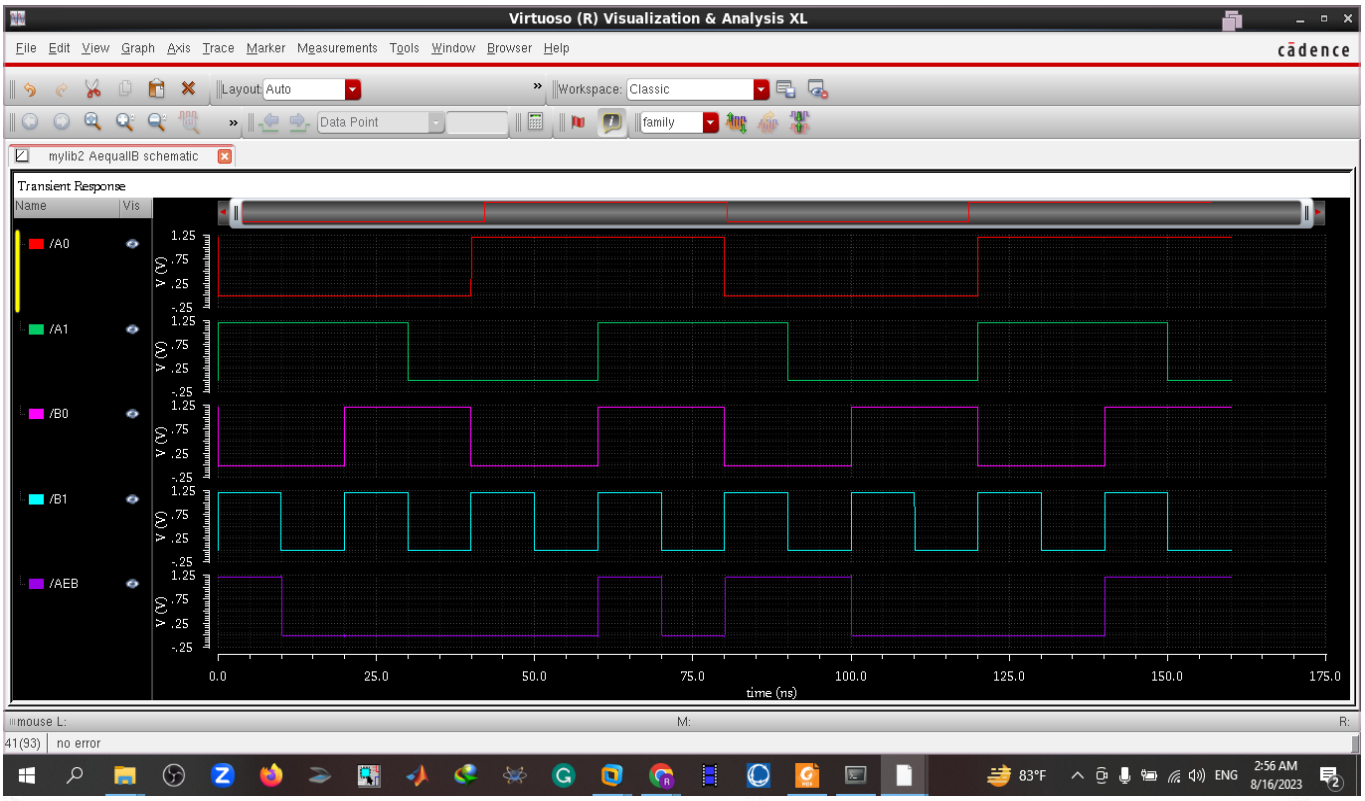
Circuit Diagram:



Schematic:

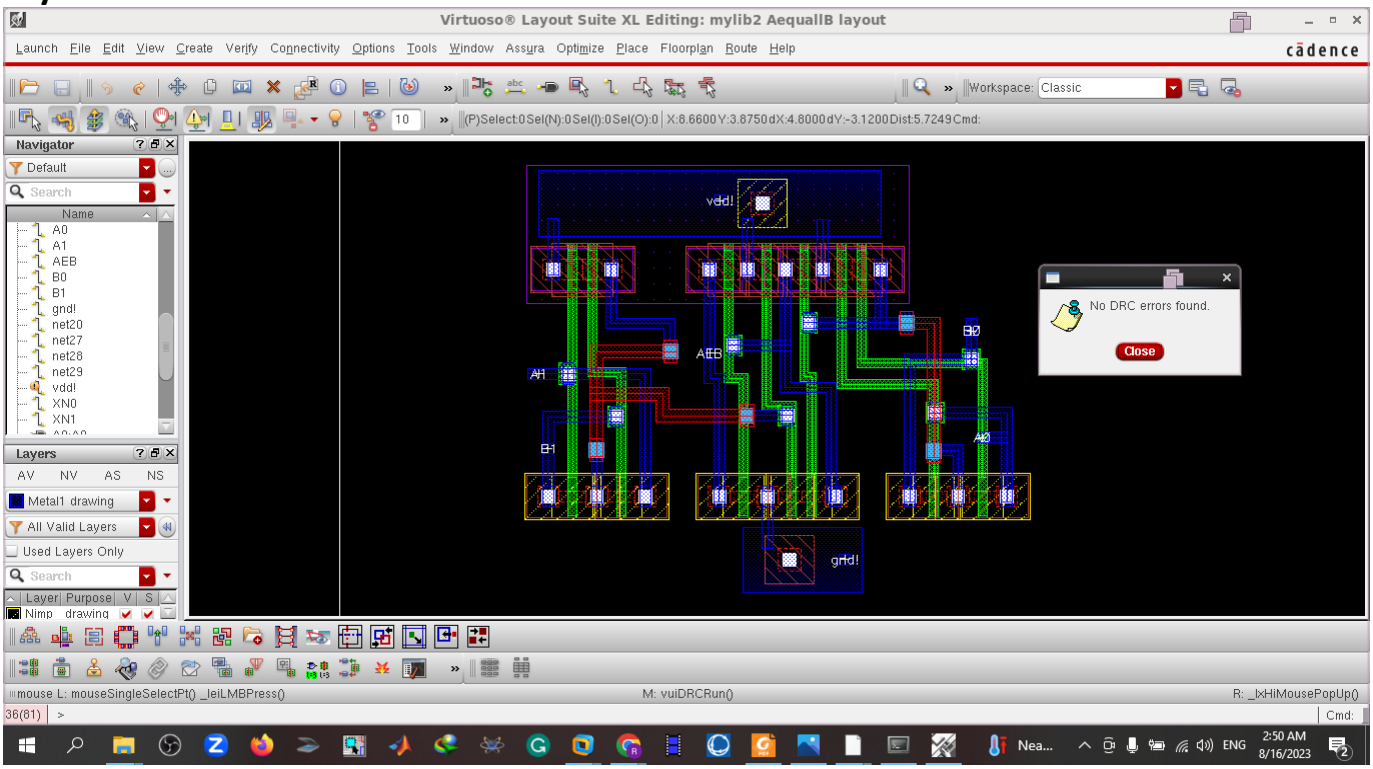


Output with Truth Table:

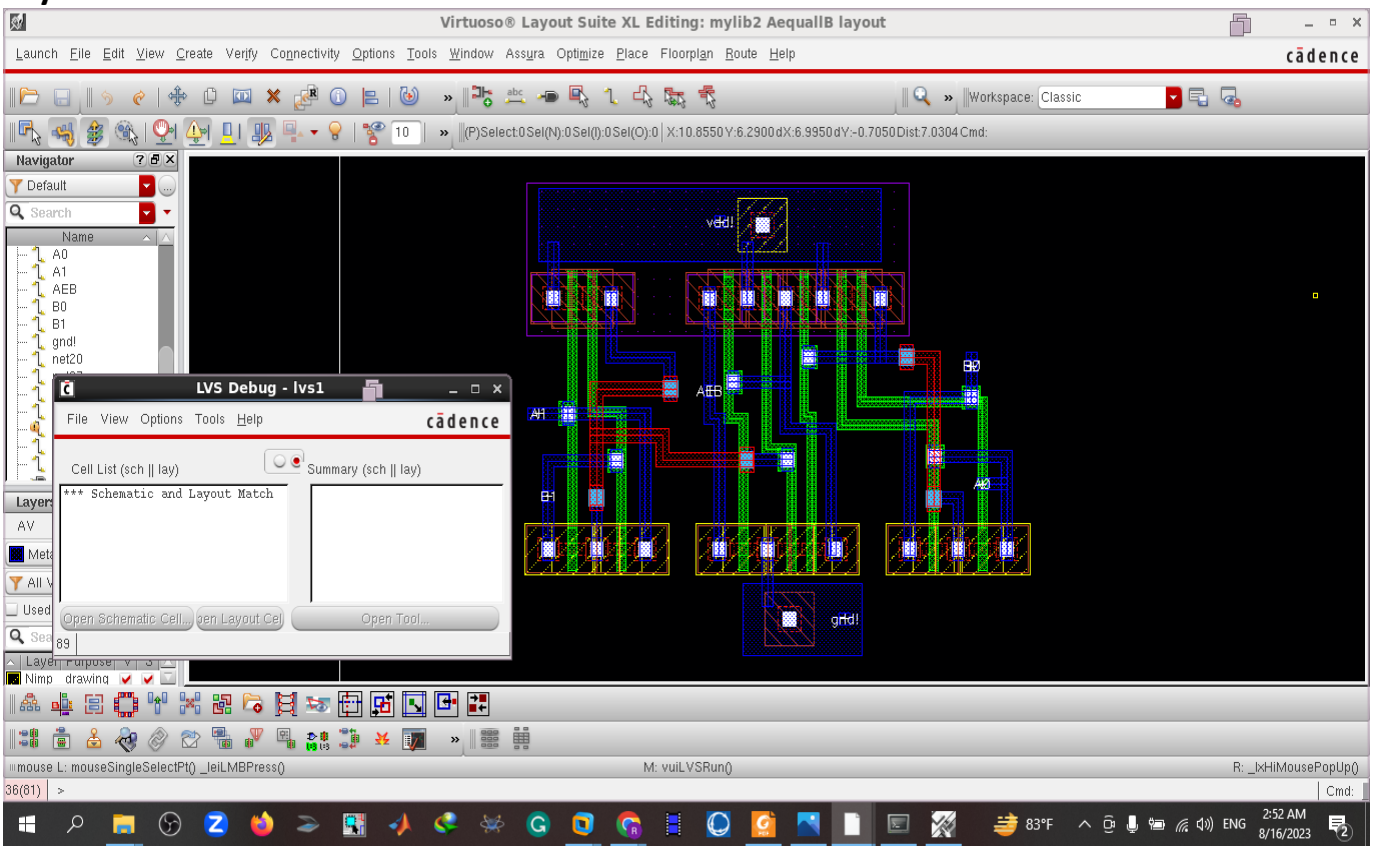


Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Layout with No DRC Error:

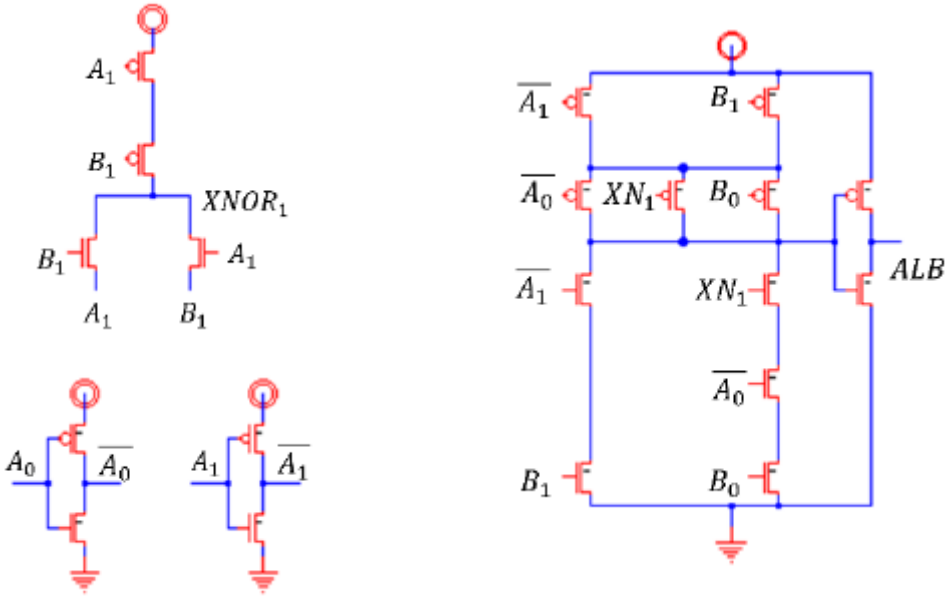


Layout with No LVS Mismatch:

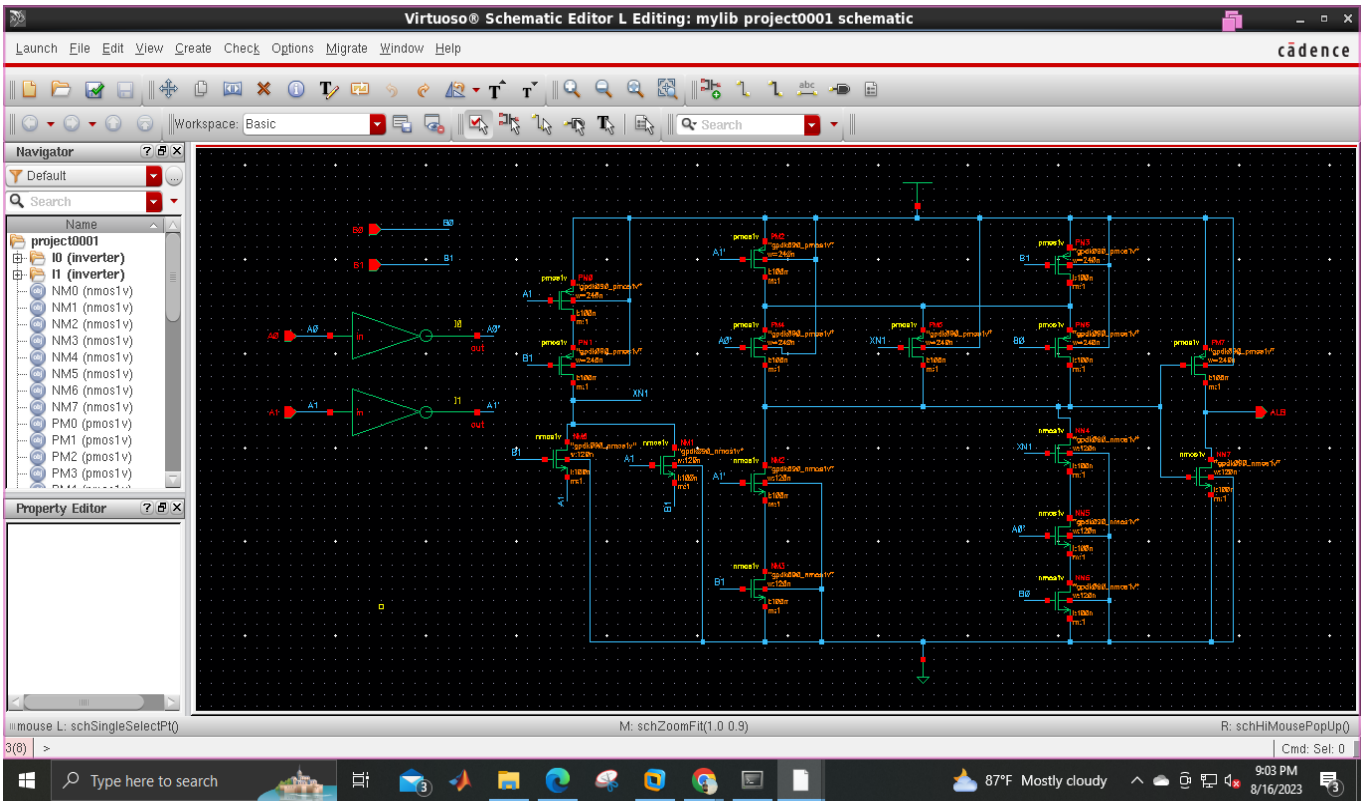


Circuit-3(A<B)

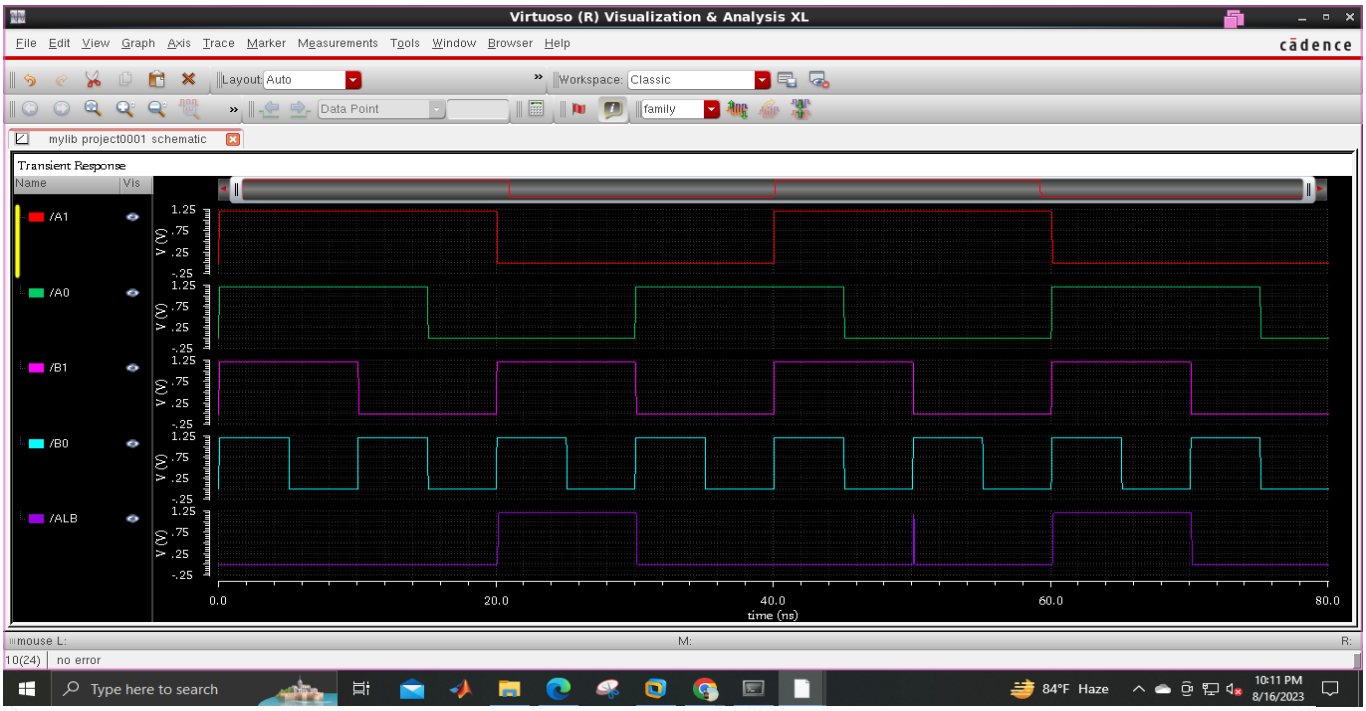
Circuit Diagram:



Schematic:

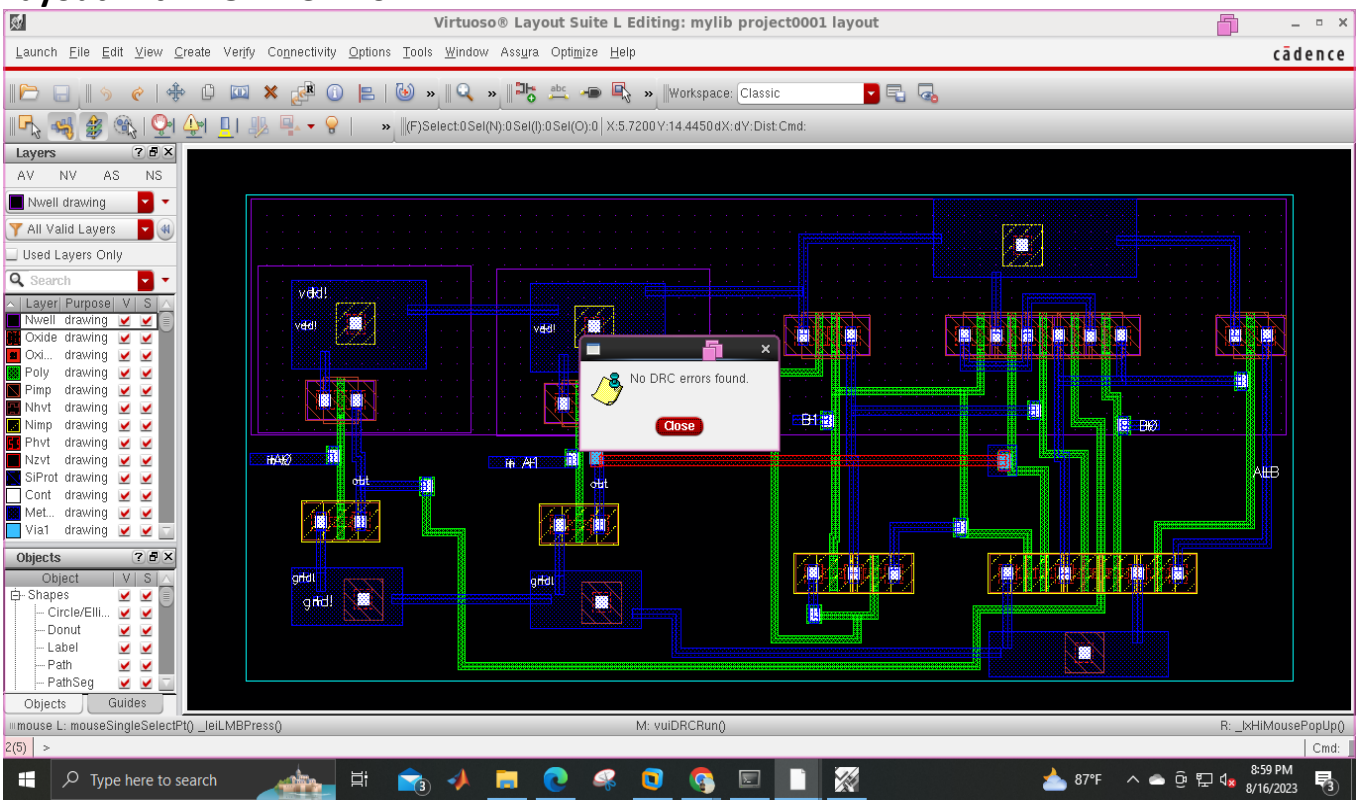


Output with Truth Table:



Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Layout with NO DRC Error:



Layout with NO LVS Mismatch: