HASHIN ISRAQ

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CAREER OBJECTIVE

Highly motivated VLSI aspirant with a passion for transforming innovative ideas into functional chip realities. Proven ability to translate theoretical knowledge into practical solutions through projects and industry training. Seeking to join a team pioneering next-generation VLSI methodologies.

INDUSTRIAL TRAININGS

- **Internship: Analog Circuit Design by Ulkasemi Pvt. Limited (7-Days)**
- **Training (Sessional): System-on-Chip(SoC) Design by Ulkasemi Pvt. Limited**

RELATED PROJECTS

- **System-on-Chip(SoC) Design of Smart Elevator (RTL to GDSII using 45nm Technology)**
  - ✓ RTL Coded and tested using Verilog on ModelSim/Quartus Prime
  - ✓ Designed and analyzed smart elevator fsm using Verilog on Quartus Prime
  - ✓ Synthesis done using cadence genus according to the SDC Constraints
  - ✓ Place and Route(PnR) implemented with proper design constraints, pad cells and corner cells using cadence innovus
  - ✓ Generated STA reports before CTS, after routing and cleared violations using cadence innovus
  - ✓ Performed physical verifications(DRC, LVS, Power Ground(PG) Shorts) and cleared violations using cadence innovus
- **System-on-Chip(SoC) Design of 4-Bit-ALU (using 45nm Technology)**
  - ✓ Implemented Place and Route(PnR) with default design constraints, pad cells and corner cells using cadence innovus
  - ✓ Performed physical verifications(DRC, LVS, Power Ground(PG) Shorts) and cleared violations using cadence innovus
- **High Performance 2-bit Magnitude Comparator Using Hybrid Logic Style (using 90nm Technology)**
  - ✓ Implemented schematic and layout using cadence virtuoso
  - ✓ Performed physical verifications(DRC, LVS) using cadence assura
  - ✓ Compared propagation delay, average power, cell area, transistor count of the comparator

SKILLS

Languages	**:** Bash, Verilog, C, C++, JavaScript, Python, Go
EDA Tools	**:** Cadence virtuoso(Schematic, Layout, Simulation), Cadence genus(Synthesis), Cadence innovus(PnR, STA), ModelSim(RTL Simulation), Quartus Prime(RTL Coding), Silvaco TCAD(SOI Simulation)
Verification Tools	**:** Assura(DRC, LVS), Calibre(DRC, LVS)
Technologies	**:** 45nm, 90nm
Operating Systems	**:** Windows, Linux

RELATED UNDERGRADUATE COURSES

✓ VLSI I, VLSI II	✓ Digital Electronics	✓ Processing and Fabrication Technology
✓ Solid State Device	✓ Computer Architecture	✓ Electrical Properties of Materials

ACADEMIC QUALIFICATIONS

BSc in Electrical and Electronic Engineering Passing Year - 2024
Ahsanullah University of Science and Technology
CGPA - 3.436/4.00

Higher Secondary Certificate Passing Year - 2019
Thakurgaon Government College
GPA - 4.25/5.00

Secondary School Certificate Passing Year - 2017
Thakurgaon Government Boys' High School
GPA - 5.00/5.00

PUBLICATION

SCAPS numerical design of MoSe2 solar cell for different buffer layers
ResearchGate : https://cutt.ly/Veuhqwjs
Semantic Scholar : https://cutt.ly/1egDI7k6

THESIS

Simulation Study of Partially Depleted Silicon on Insulator (SOI) Devices
Supervisor: Dr. Towhid Adnan Chowdhury
Assistant Professor, Department of EEE
Ahsanullah University of Science & Technology

ACTIVITIES

AUST Programming and Informatics Club December 2021-December 2022
Sub-executive Member
- ✓ Designed and Developed Club's Website
- ✓ Organized Events as An Organizer

IEEE AUST Student Branch December 2021-January 2023
General Member
- ✓ Organized Event as A Volunteer

AUST Innovation and Design Club February 2020-February 2024
General Member

TGBHS Bangladesh National Cadet Corps (BNCC) December 2014-March 2017
Former Cadet
- ✓ Completed a Capsule Camp in Dinajpur Government College

INTERESTED AREAS

- VLSI
- Nano Technology

REFERENCES

- Dr. Satyendra Nath Biswas
  Professor, Department of EEE
  Ahsanullah University of Science & Technology
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- Dr. Towhid Adnan Chowdhury
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