Digital System Design

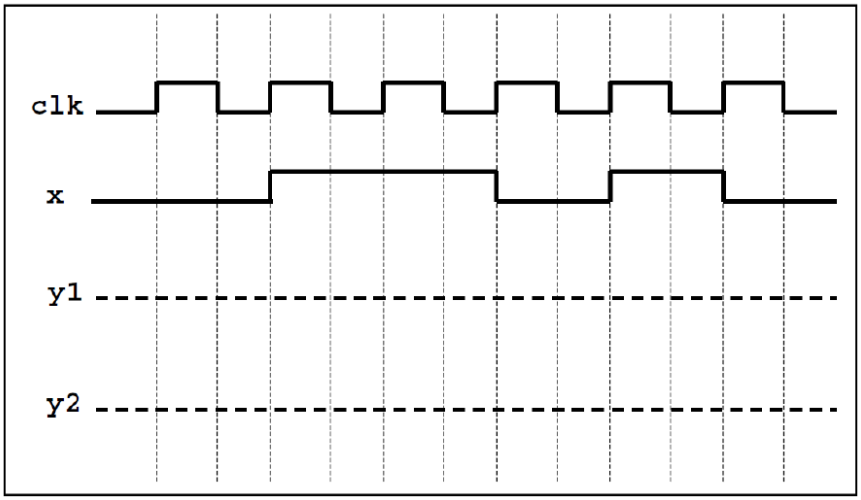
Submission Date: 1st Nov, 2019

Q1: Design a datapath with three 8 bit accumulators. The first accumulator, acc1, adds a 4 bit input data in acc1 in every clock cycle. The second accumulator, acc2, adds the first accumulator in itself, and the third accumulator, acc3, adds the first and second accumulators in itself in every clock cycle. Each accumulator has an asynchronous reset. Draw the RTL level diagram and code the design in RTL Verilog.

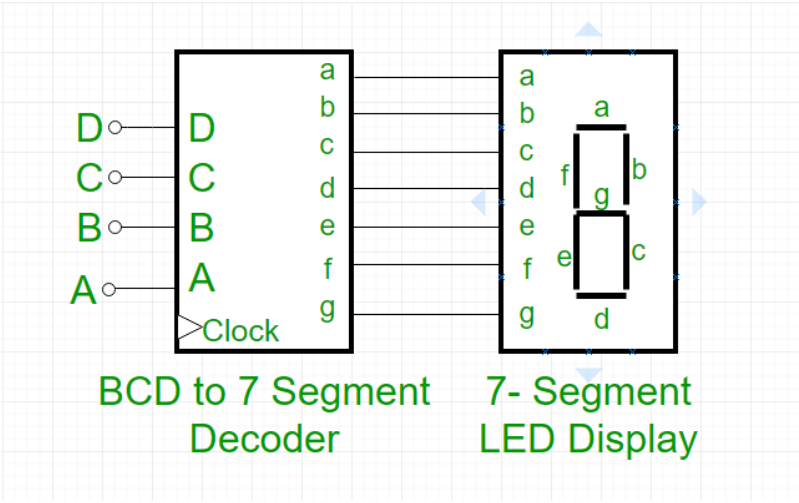
Q2: Exercise question 2.10. Provide an RTL diagram and its relevant code; also test your code using a stimulus. Keep the input and output bit size equal to 4 bits.

Q3: Complete the waveform for the given logic

```
module my_unit(clk, x, y1, y2);
input clk, x;
output y1, y2;
reg y1, y2;
wire w;
assign w = x|(~y1);
always@(posedge clk) y2 <= w;
always@(negedge clk) y1 <=y2;
endmodule
```



Q4: Write RTL Verilog Code for a BCD to 7-segment decoder. The module will accept a BCD number and it should provide bit value to relevant segment so that turn on relevant number can be displayed.
Assume 7-segment to be active low.



NOTE:

- Assignment is a form of learning, please consider this while solving.
- Code should be properly ***indented*** and ***commented***.
- Write your ***code in MODELSIM***, verify it using ***stimulus*** and ***attach output screen shots of your simulation*** in a separate docx file. Code/Screen shots should not be copied, ***in case of copying assignment will not be marked.***
- MODELSIM Projects (VERILOG files and all) along with screen shots of your simulation results should be ***emailed as a single ".rar" file*** on assignments.sajid@gmail.com.
- ***RAR*** file should be ***named*** as ***"YOURNAME_ASSIGN#_DSD"***.
- Subject of your ***email MUST*** be as ***"YOURNAME_ASSIGN#_DSD"***.
- ***VERY IMPORTANT:*** RTL diagrams should either be drawn in VISIO for software submission, for submission in hard form draw the RTL diagrams with your ***HANDS instead of FEET.***