

# MD HASIBUL AMIN

Ph.D. Student | University of South Carolina | Columbia, SC

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🔗 Google Scholar

## EDUCATION

- **University of South Carolina** *Jan 2021-present*  
PhD in Computer Engineering  
Current CGPA: 3.54 out of 4.00  
Research topic: Processing-in-Memory (PIM), Approximate Computing
- **University of South Carolina** *Aug 2022-May 2024*  
MS in Computer Engineering  
CGPA: 3.54 out of 4.00  
Selected Courseworks: Advanced Digital Design, Computer Architecture, Pattern Recognition, Robotics, Analysis of Algorithms
- **Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh** *Feb 2015-Apr 2019*  
Bachelor of Science in Electrical and Electronic Engineering (EEE)  
CGPA: 3.29 out of 4.00  
Research topic: Ab initio study of Carbon Nanotubes  
Thesis title: Ab initio investigation of dopants for ultrahigh conductivities in single wall carbon nanotubes

## RESEARCH EXPERIENCE

- **Graduate Research Student** *Jan 2021-present*  
[Intelligent Circuits, Architectures, and Systems Lab](#), University of South Carolina  
**Supervisor:** Dr. Ramtin Zand, Assistant Professor, University of South Carolina
  - Designed and implemented a hybrid TPU-PIM architecture for 1-bit LLMs, improving computational efficiency and reducing memory bottlenecks [\[link\]](#)  
Heterogeneous Integration LLM Accelerator Efficient LLM
  - Extended the ISA of the RISC-V microarchitecture to support PIM devices as a co-processor using the gem5 simulator system  
Computer Architecture ISA Extension PIM co-processor
  - Developed software-hardware co-design framework for PIM systems based on weight sharing and mixed-precision quantization along with evolutionary search [\[link\]](#) [\[code\]](#)  
Software-hardware co-design NAS for PIM weight-sharing mixed-precision quantization for NN
  - Implemented Verilog RTL and HLS designs for approximate TPU circuits; automated benchmarking with Python and TCL scripts [\[paper\]](#)  
Digital Design Approximate TPU Verilog RTL HLS Design
  - Optimized crossbar circuit performance by modeling interconnect parasitics and analog partitioning [\[paper\]](#)  
Crossbar modeling Interconnect parasitics Partitioning Reliability analysis
  - Built a Python-based SPICE simulation framework for in-memory accelerator circuit analysis [\[paper\]](#)  
Analog PIM Simulation Framework Python scripting SPICE circuit design
- **Undergraduate Research Student** *May 2018-Dec 2019*  
[Nanoscale Simulation, Characterization and Fabrication Lab](#), BUET  
**Supervisor:** Dr. Ahmed Zubair, Professor, Department of EEE, BUET
  - Investigated the effect of various dopants such as  $I_2$ ,  $AuCl_3$  on various carbon nanotube molecules using Density functional theory (DFT) [\[paper\]](#)  
Density Functional Theory Carbon nanotubes Conductivity analysis Dopants

## PROFESSIONAL EXPERIENCE

- **Graduate Research/Teaching Assistant** *Jan 2021-present*  
Department of Computer Science and Engineering, University of South Carolina
- **Lecturer, Department of Electrical and Electronic Engineering** *Jan 2020-May 2020*  
Daffodil International University, Dhaka, Bangladesh

## TECHNICAL SKILLS

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- **Hardware Design:** Verilog, SystemVerilog, HLS
- **Architectural Simulation:** gem5, MNSIM, NeuroSim
- **Programming Languages:** C, C++, Java, Python, MATLAB, TCL
- **EDA Tools:** Cadence Virtuoso, Synopsys Design Compiler, HSPICE
- **Machine Learning:** PyTorch, TensorFlow, Quantization Techniques

## AWARDS AND CERTIFICATIONS

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- IEEE ISCAS 2022 Student Participation Grant *May 2022*
- Deep Learning Specialization Coursera Certificate *Aug 2020*

## SELECTED ACADEMIC PROJECTS

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- Training a transformer-based language model for novel antimicrobial peptide generation *Spring 2024*
- RTL design and FPGA implementation of a 3-stage pipelined RISC-V microarchitecture *Fall 2021*
- RTL design of a 32-bit single-cycle MIPS microarchitecture *Fall 2021*
- Circuit design for a Leaky Integrate-and-Fire (LIF) spiking neuron *Spring 2021*

## PEER REVIEW SERVICE

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- ISCAS-2023, GLSVLSI-2023, MWSCAS-2023, JETCAS *2023*
- ISVLSI-2024, GLSVLSI-2024 *2024*
- ISCAS-2025 *2025*

## SELECTED PUBLICATIONS

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- M. H. Amin, M. Mohammadi, and R. Zand. Multi-objective Neural Architecture Search for In-memory Computing. IEEE Computer Society Annual Symposium on VLSI (ISVLSI '24) *2024*
- Mohammed E Elbitty, Md Hasibul Amin, Hossam Hassan, et al. Design Automation and Quantitative Analysis of Approximate Arithmetic Circuits. TechRxiv. *2024*
- M. H. Amin, M. E. Elbitty, and R. Zand. IMAC-Sim: A Circuit-level Simulator For In-Memory Analog Computing Architectures. In Proceedings of the Great Lakes Symposium on VLSI 2023 (GLSVLSI '23) *2023*
- M. E. Elbitty, B. Reidy, M. H. Amin, and R. Zand. Heterogeneous Integration of In-Memory Analog Computing Architectures with Tensor Processing Units. GLSVLSI '23. *2023*
- M. H. Amin, M. E. Elbitty and R. Zand. Xbar-Partitioning: A Practical Way for Parasitics and Noise Tolerance in Analog IMC Circuits. IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) *2022*
- M. H. Amin, M. Elbitty, M. Mohammadi, R. Zand. MRAM-based Analog Sigmoid Function for In-memory Computing. GLSVLSI '22. *2022*
- M. H. Amin, M. Elbitty and R. Zand. Interconnect Parasitics and Partitioning in Fully-Analog In-Memory Computing Architectures. IEEE International Symposium on Circuits and Systems (ISCAS). *2022*
- M. L. Rahman, M. H. Amin and A. Zubair. Ab initio Theoretical Investigation of Dopants for Ultrahigh Conductivities in Single Wall Carbon Nanotubes. IEEE Region 10 Conference (TENCON). *2019*

## POSTER PRESENTATIONS

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- A Python Framework for SPICE Circuit Simulation of In-Memory Analog Computing Circuits. *2022*  
*IBM-IEEE CAS/EDS - AI Compute Symposium 2022*, IBM Think Lab, NY
- Reliability-Aware Deployment of DNNs on In-Memory Analog Computing Architectures. *2022*  
*IBM-IEEE CAS/EDS - AI Compute Symposium 2022*, IBM Think Lab, NY
- Electronic Structure Study of Halogen and Gold Halide Doped Carbon Nanotubes. *2020*  
*APS March Meeting 2020*, Denver, Colorado