

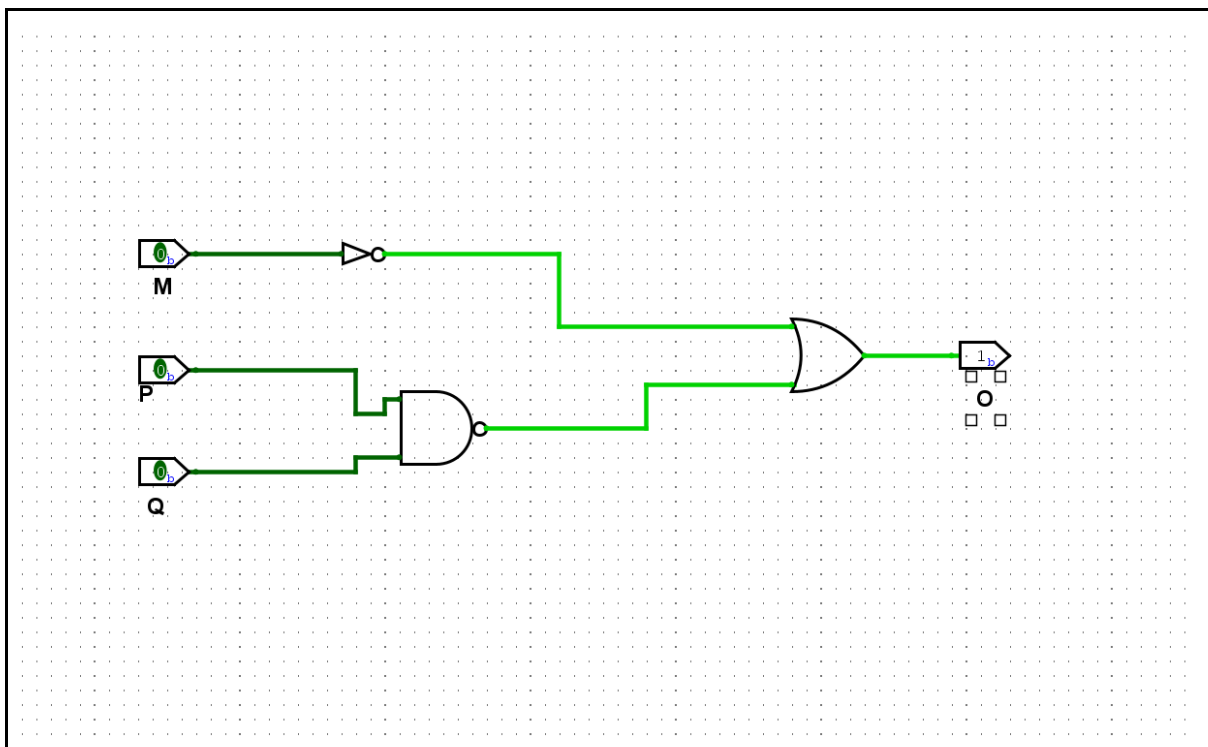
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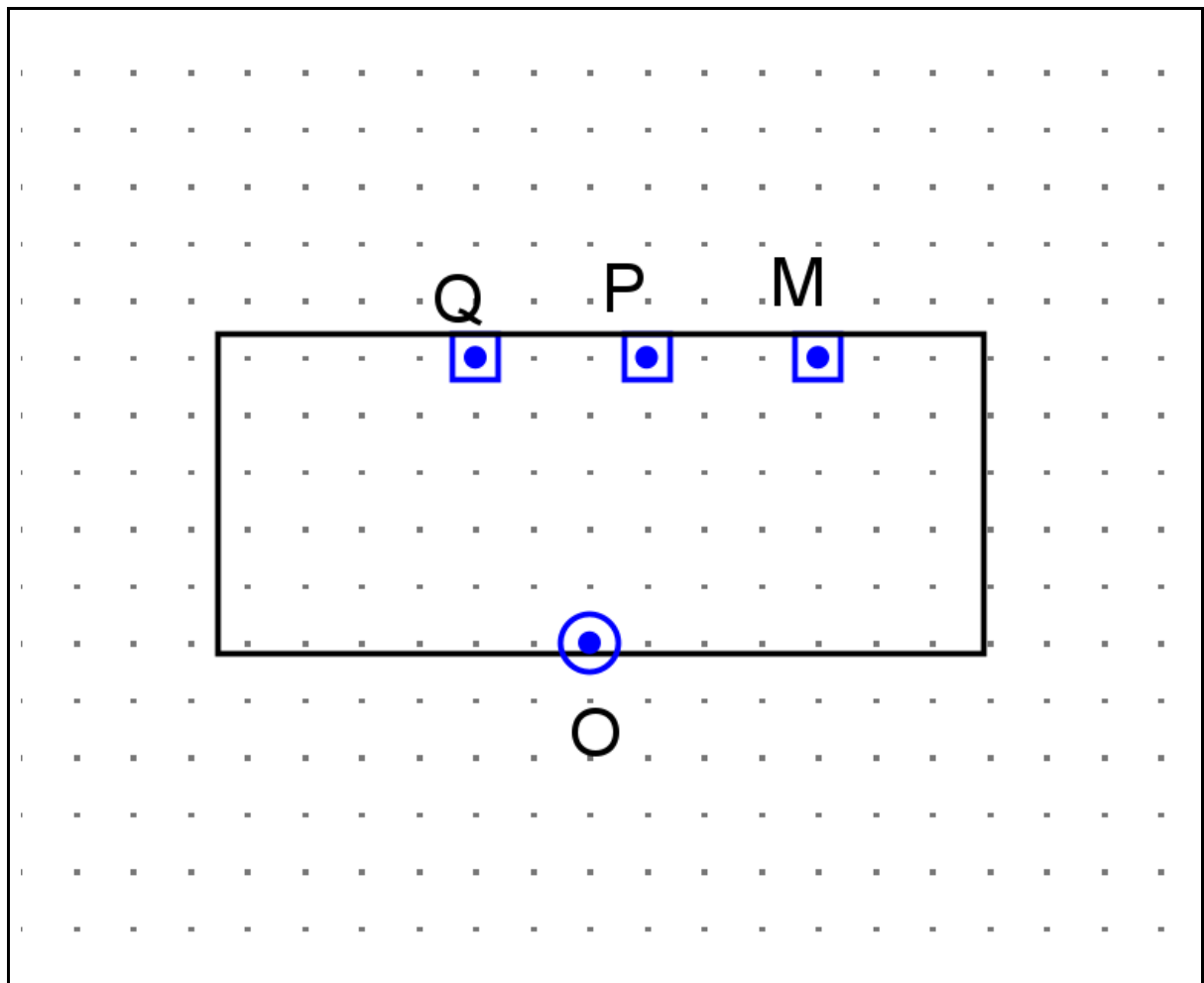
Lab Performance Evaluation 01

Lab Task Q1

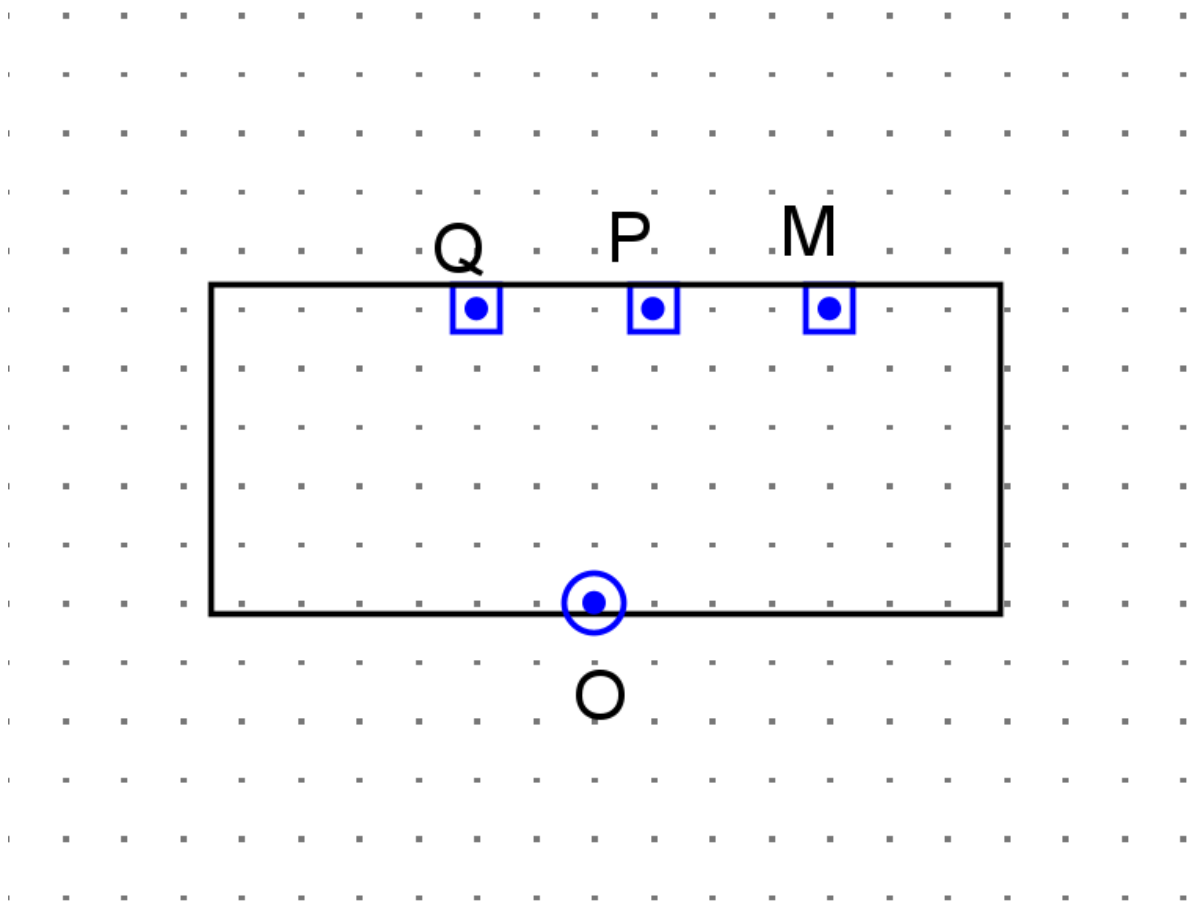
Question: Design a Logic circuit with its Top Level Circuit block (with inputs and outputs pins) with following logic equations: $O = \text{NOT}(M) + \text{NOT}(P.Q)$

Solution (Code/Add all circuits diagrams):





Output/Simulation Result (Screenshot/SnapShot):



Lab Task Q2

Question: Construct an equivalent ARM Assembly Program of following C Program:
//Do not use Register as variable

```
int x = 10;
```

```
if { x = x + 1; } else ( x = x - 2; );
```

Solution (Code/Add all circuits diagrams):

```
PRESERVE8
THUMB

AREA     RESET, DATA, READONLY
EXPORT  __Vectors
```

```

__Vectors
    DCD  0x20001000
    DCD  Reset_Handler
    ALIGN

    AREA  MYCODE, CODE, READONLY

    EXPORT Reset_Handler

Reset_Handler

    ; r1, #0x46a1f1b7
    mov r1,0x20000000
    mov r2, #10
    b eql

eql

    add r2, r2,#1
    str r2,[r1,#1]
    b ex
    str r2, [r1,#0]

    sub r2, r2,#2
    str r2,[r1,#0]

ex
    END

```

Output/Simulation Result (Screenshot/SnapShot):

Register	Value
Core	
R0	0x00000000
R1	0x20000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x20001000
R14 (LR)	0xFFFFFFFF
R15 (PC)	0x00010000
xPSR	0x41000000
Banked	
System	
Internal	
Mode	Thread
Privilege	Privileged
Stack	MSP
States	32763
Sec	0.00273025

Memory 1	
Address:	0x20000000
0x20000000:	00 00
0x2000001A:	00 00
0x20000034:	00 00
0x2000004E:	00 00
0x20000068:	00 00
0x20000082:	00 00
0x2000009C:	00 00
0x200000B6:	00 00

Lab Task Q3

Question:

Solution (Code/Add all circuits diagrams):

Output/Simulation Result (Screenshot/SnapShot):

Lab Task Q[No]

Question:

Solution (Code/Add all circuits diagrams):

Output/Simulation Result (Screenshot/SnapShot):