Overview : The objective of this project is to display a string of characters “ECE212 - 5” on a

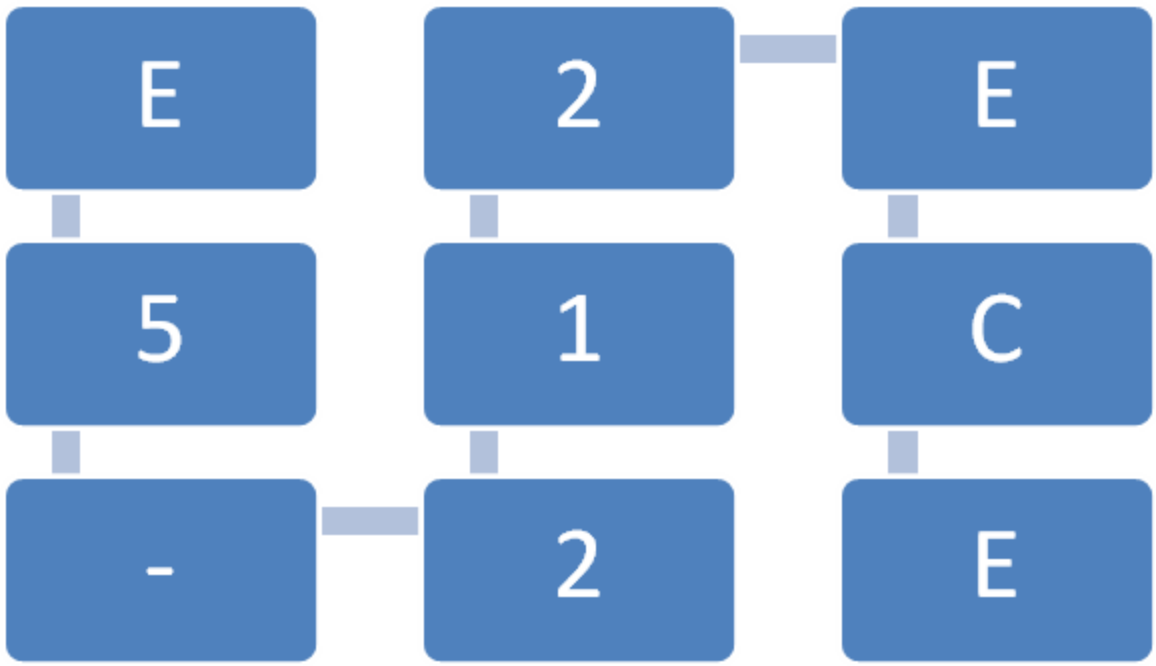
7 segment display using a Sequential Logic Circuit.

This logic circuit is designed in the following forms :

- ➔ JK Flip Flop
- ➔ Trigger Flip Flop
- ➔ Delay Flip Flop

OUTPUT of the Logic: The circuit here will have two options. One to display “5-212ECE” when I0 is pressed. And it will remain in the same state when I1 is pressed. These outputs are shown in a 7 segment display via a combinational logic circuit.

STATE TRANSITION DIAGRAM:



This is known as the MEALY MODEL.

STATE TRANSITION TABLE :

REF	Present State (ABC)	Next State		OUTPUT(F)	
		I=0	I=1	I=0	I=1
0	0	7	0	5	5
1	1	0	1	-	-
2	2	1	2	2	2
3	3	2	3	1	1
4	4	3	4	2	2
5	5	4	5	E	E
6	6	5	6	C	C
7	7	6	7	E	E

STATE ASSIGNMENTS :

REF	PRESENT STATE (ABC)	NEXT STATE		OUTPUT(F)		OUTPUT(on 7 segment display)
		I=0	I=1	I=0	I=1	
0	0 0 0	1 1 1	0 0 0	1 1 0	1 1 0	5
1	0 0 1	0 0 0	0 0 1	0 0 1	0 0 1	E
2	0 1 0	0 0 1	0 1 0	0 1 0	0 1 0	C
3	0 1 1	0 1 0	0 1 1	0 0 1	0 0 1	E
4	1 0 0	0 1 1	1 0 0	0 1 1	0 1 1	2
5	1 0 1	1 0 0	1 0 1	1 0 0	1 0 0	1
6	1 1 0	1 0 1	1 1 0	0 1 1	0 1 1	2
7	1 1 1	1 1 0	1 1 1	1 0 1	1 0 1	-

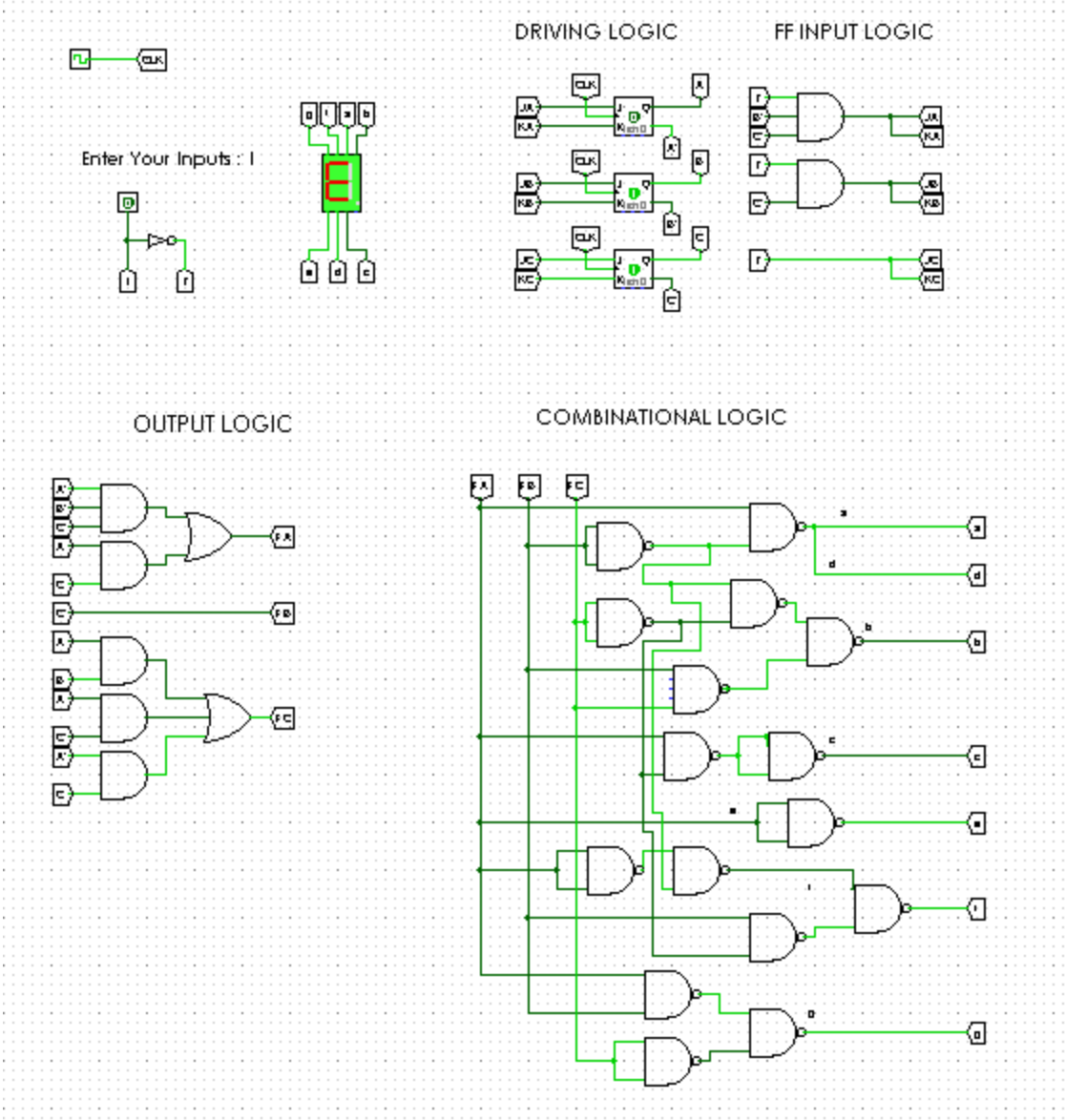
This sequential logic circuit can be performed in various ways. Some of which are using :

1. JK Flip Flop
2. Trigger Flip Flop
3. Delay Flip Flop

All of these are used in a synchronous system, ie. a clock.

JK FLIP FLOP:

The following diagram shows the driving logic , FF input logic, and the output logic.

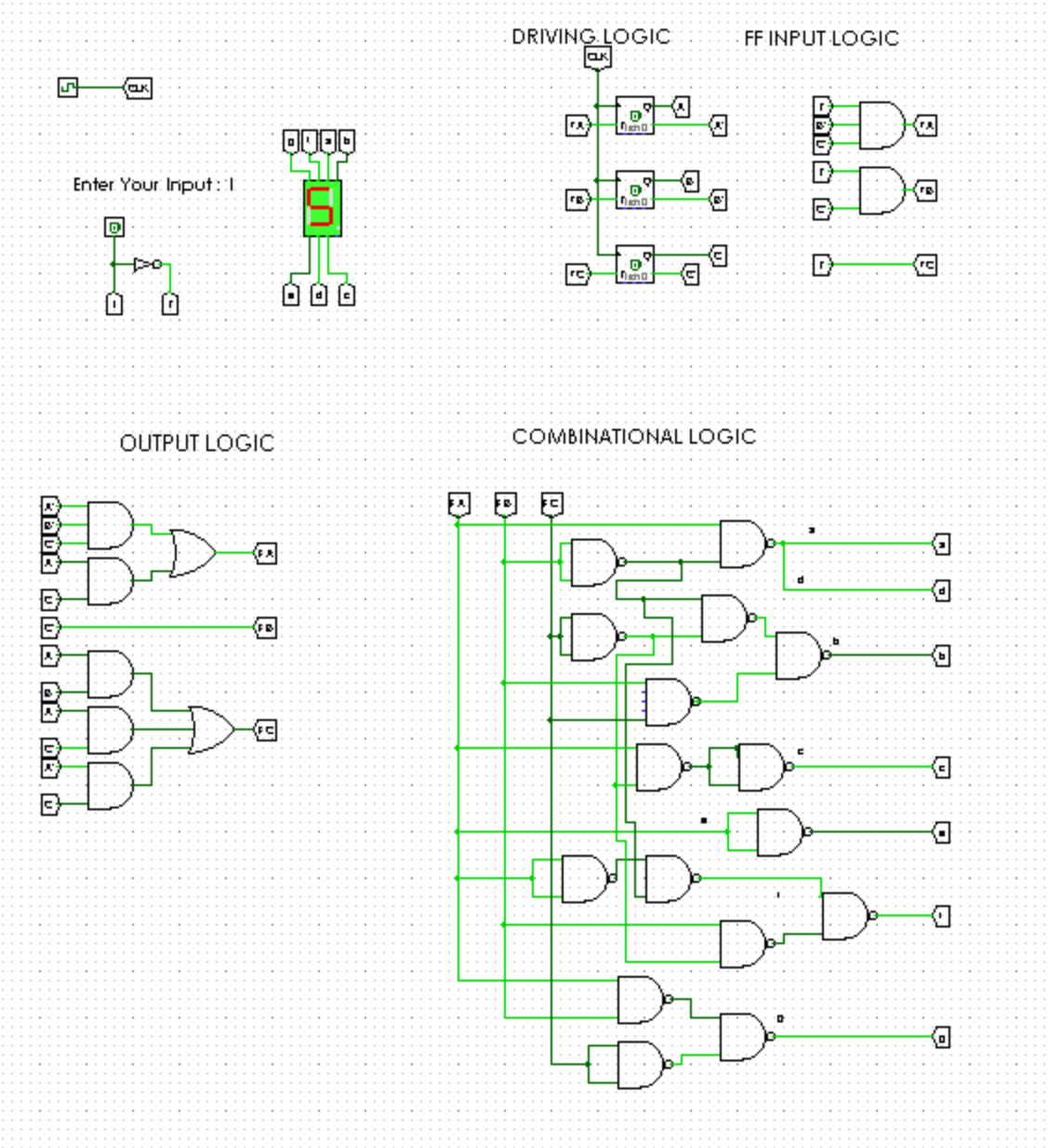


All of these are combined with a combinational logic to get the desired output on the 7 segment display. K Maps for the logics are shown in the next page.

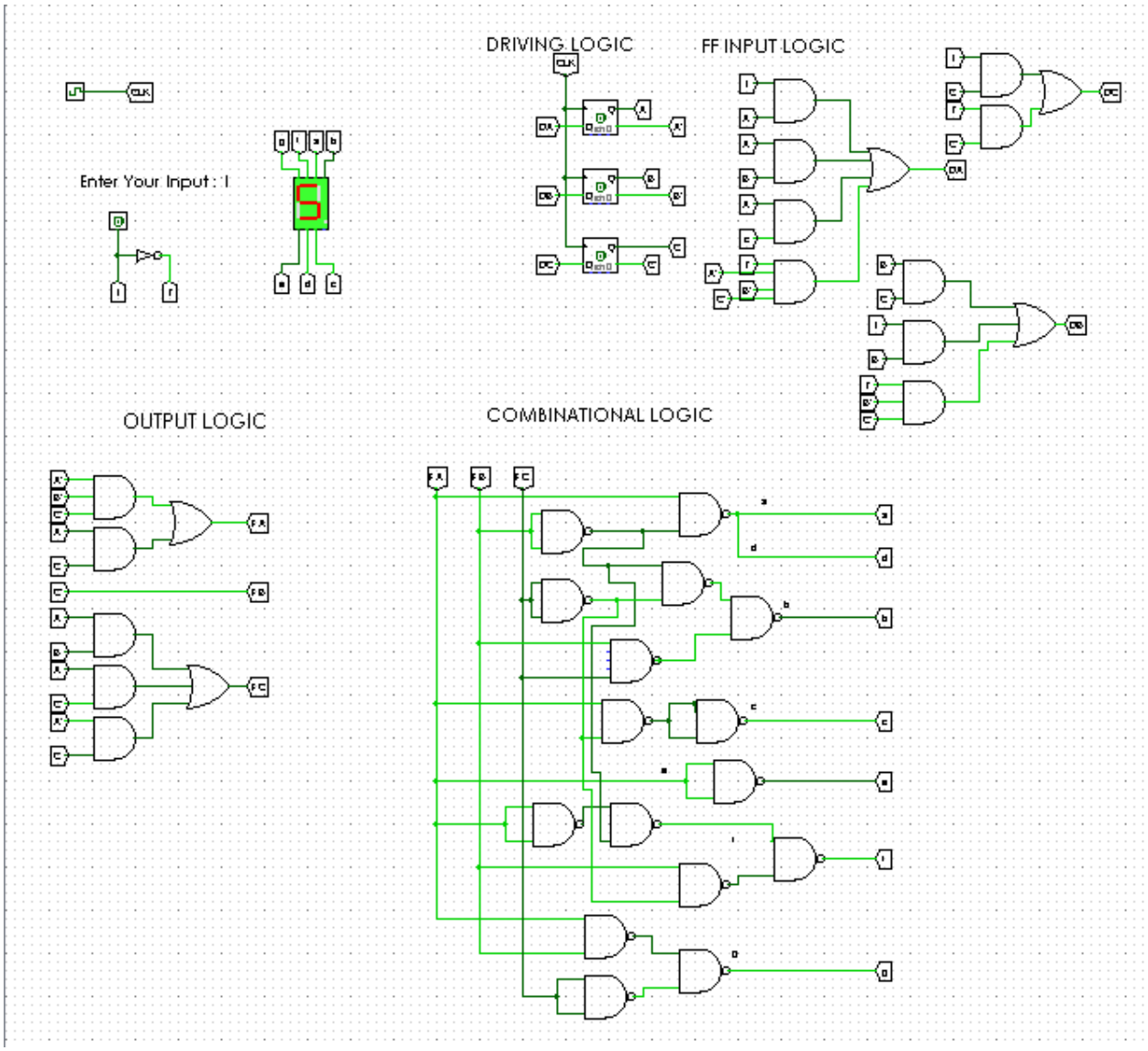
**Other methods are shown in the same format.

Trigger Flip Flop :

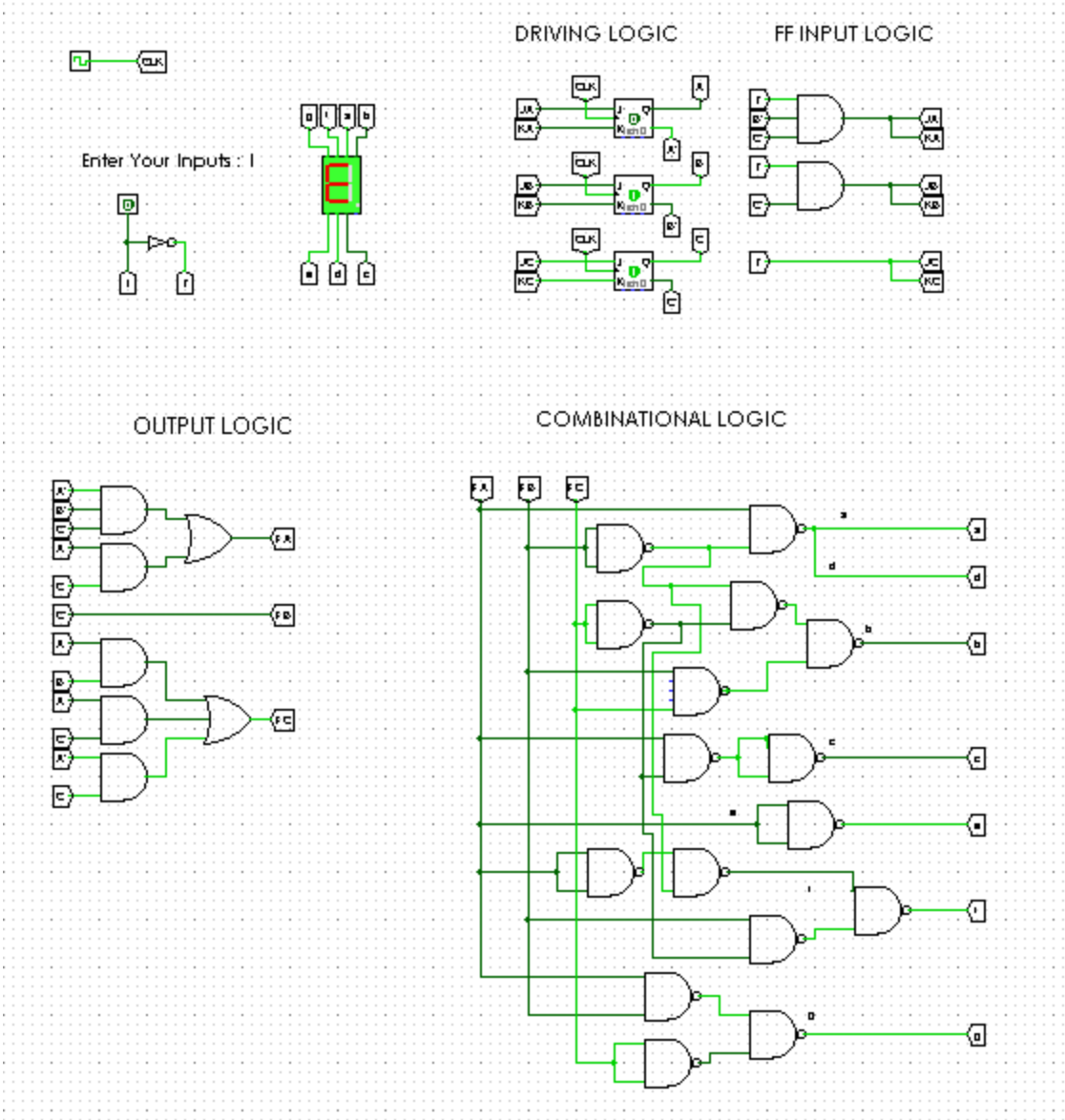
The following diagram shows the driving logic , FF input logic, and the output logic.



DELAY FLIP FLOP :



For our FINAL hardware implementation , we plan to use the following circuit :



THE END