Hasindu Ramanayake

Software Engineer

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EDUCATION

BSc. in Engineering,
Specializing in Computer Engineering (2019)
University of Peradeniya, Sri Lanka

INDUSTRY EXPERIENCE

- **Positions Held**
  - **Staff Engineer at Synopsys (2025-present)**
  - **Senior Engineer at Synopsys (2024-2024)**
  - **Research and Development Engineer II at Synopsys (2022-2024)**
  - **Research and Development Engineer at Synopsys (2019-2021)**
  - **Intern at Synopsys Lanka: 20 weeks (2017 – 2018)**

- **Experience working in large complex software products (Synopsys VC Static Low Power) (4+ years).**
  - VC Static Low Power (VC LP) is a product designed for static low power verification, which is used by large, top tech/Hardware design companies.
  - Learned static low-power, TCL, and UPF from scratch in a short amount of time.
  - Worked for VC LP to maintain the product, complete enhancements, features, and bugs
  - Two patent contributions:
    - https://patents.google.com/patent/US20220075920A1 (*1)
    - https://patents.google.com/patent/US20230072923A1 (*2)
  - Experience collaborating with individuals from diverse countries: India, China, USA

- **Experience in Machine Learning (ML) / Large Language Model (LLM) projects**
  - ML project focused on enhancing validation time within the software development life cycle. The ML model I'm developing recommends benchmarks for specific software changes, enabling the product validation team to expedite the validation process significantly.
  - Experimenting with LLVM and GCC to generate call graphs for large complex production-level code bases

- **Experience in full-stack web development**
  - Currently involved in website development for management, focusing on presenting a visual-based analysis of customer support information from Synopsys tools (JIRA-based ticket data). Additionally, It helps to perform quality analysis and manage tasks based on this analysis.

- **Cross-product working experience**
  - Worked with VC LP and VC Formal teams in a collaborative project. The project was for a high-value customer. In the project we instrumented a power switch model, So VC-Formal can use that model to do formal verification for a design. The project is considered a novelty, considered as a patent inventor (*1)
  - Self-driven personal projects that help to improve and utilize customers' computing resources.
  - Implemented a data collection command to evaluate design complexity, which serves as a valuable benchmark for design complexity evaluation. Subsequently, developed a machine learning model to predict resource allocation for customer designs. This is particularly significant in cloud environments, where customers pay for resources. The application extends its utility to distributed environments, further enhancing its practicality and relevance. (*2)

Experience in small team project management (fast-paced project).
- Worked with VC LP and VC Formality teams in a collaborative project. The project was for a high-value customer.
- Daily contributions were, creating speciation, research on requirements and ideas, quality implementation, and testing
- As for other responsibilities: collaborate with VC Formality principle engineers, work distribution, maintain project requests, and be responsible for on-time delivery.
- As a recognition: promotion to R&D II, got ownership of the project
- **Experience in new product prototyping**
  - Contributed to a new tool/technology for EDA tool debugging to help debug issues in VC LP from customer sites. The project will improve debuggability on customer sites
  - Contribution: Created the data collecting backend, data collection, and design interface APIs to backend, as well as own backend infrastructure.

FINAL YEAR PROJECT(UNDERGRADUATE)

- Power-Aware High-Level Synthesis Flow for Mapping FPGA Designs

PERSONAL PROJECTS

- **Rust**
  - ChatApp, IP tracer CLI, Design Patterns, Learning projects
  - http tcp server with a thread pool

- **C++ Networking/ Backend:**
  - http tcp server, asio client, MMO Server Interface

- **Godot 4**:
  - Classic space game, Classic Flappy Bird, Classic Snake

COMPETITIONS & OTHER ACCOMPLISHMENT

- **Acknowledging & Celebrating Excellence (ACE 2022) Runner up in the "Customer focus" category (Team)**
- **Ideathon finalist:**
  - Ideathon is the hacker-thon organized by Synopsys South Asia to improve innovation in product teams.
- **Code Fest 4.0:**
  - 3rd Place (2022), competition similar to IEEE Xtream.
- **Inter Synopsys Chess Tournament:**
  - Board price and member of the winning chess team
- **University Colours:**
  - 2014/15 , 2016/17

TECHNOLOGIES

Technologies used in professional environments **(6+ years)**
- **Main:** C/C++, Python, Bash, TCL, Perl, Verilog, System Verilog, UPF, CMake
- **Version Control:** Perforce, GitHub
- **Web:** JS, Svelte,Tailwind CSS, HTML, CSS
- **Other:** JIRA

TECHNOLOGIES EXPLORING

- Standalone software development
- Backend server development
- Godot/ Unreal Engine development

OTHER TECHNOLOGIES

I may not have direct professional experience in the following areas,   but I am confident in my ability to acquire proficiency within a reasonable amount of time:
- **General purpose**: Rust, JAVA
- **Web**: Next.js, React.js
- **Cloud**: AWS Services, SQL/ NoSQL databases
- **ML**: Pytorch, Hugging face models, basic ML and LLM
- **Game Dev**: Godot 4, GDScript
- **Frameworks**: Asio Lib, LLVM, CUDA