Hasini Witharana, Security Researcher

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Education

2020 – Present — **Ph.D. University of Florida**, Computer Science.
Thesis title: *Design of Trustworthy Systems using Security Assertions.*
Advisor: *Prof. Prabhat Mishra*

2020 – 2023 — **M.Sc. University of Florida**, Computer Science and Engineering.

2014 – 2018 — **B.Sc. University of Moratuwa Sri Lanka**, Computer Science and Engineering.

Work Experience

2020 – Present — **Research Assistant**, University of Florida.

May 2021 – Aug 2021 — **Security Research Intern**, Intel Corporation, USA.

2019 – 2020 — **Software Engineer**, WSO2, Sri Lanka.

Apr 2018 – Aug 2018 — **Google Summer of Code Contributor**, Apache Foundation, USA.

Jun 2017 – Dec 2017 — **Software Engineering Intern**, WSO2, Sri Lanka.

Skills

Coding — Java, Python, C++, Assembly, LaTeX

Verification — Assertion-Based Security Verification, Test Generation, Quantum Device Verification.

Security — CPU Side-Channel Attacks, Trusted Execution Environments, Pre-Silicon Security.

Misc. — Academic Research, Teaching, Training, Consultation.

Research Publications

Journal Articles

1. H. Witharana, A. Jayasena, A. Whigham, and P. Mishra, "Automated generation of security assertions for rtl models," *ACM Journal on Emerging Technologies in Computing Systems*, 2023.
2. A. Jayasena, B. Kumar, S. Charles, H. Witharana, and P. Mishra, "Network-on-chip trust validation using security assertions," *Journal of Hardware and Systems Security*, 2022.
3. H. Witharana, Y. Lyu, S. Charles, and P. Mishra, "A survey on assertion-based hardware verification," *ACM Computing Surveys (CSUR)*, 2022.
4. H. Witharana, Y. Lyu, and P. Mishra, "Directed test generation for activation of security assertions in rtl models," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2021.

Conference Proceedings

1. H. Witharana, S. Sanjaya, and P. Mishra, "Dynamic refinement of hardware assertion checkers," in *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2023.
2. H. Witharana and P. Mishra, "Speculative load forwarding attack on modern processors," in *Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design*, 2022.

Patent

1. P. Mishra, H. Witharana, and S. Sanjaya, "Dynamic refinement of hardware assertion checkers," U.S. Provisional Patent Application No. 63/489,020, filed March 8 2023.

Other Publications

1. H. Witharana, A. Jayasena, and P. Mishra, *Sequence-based incremental concolic testing of rtl models*, arXiv preprint arXiv:2302.12241, 2023.
2. H. Witharana and P. Mishra, *Scalable assertion-based validation of trusted execution environments*, SRC TECHCON, 2023.
3. H. Witharana and P. Mishra, *Security validation of trusted execution environments*, GOMACTech, 2023.
4. H. Witharana, D. Volya, and P. Mishra, *Quassert: Automatic generation of quantum assertions*, arXiv preprint arXiv:2303.01487, 2023.
5. H. Witharana and P. Mishra, *Side-channel attack on modern processors*, SRC TECHCON, 2022.
6. H. Witharana and P. Mishra, *Automated generation of security assertions*, SRC TECHCON, 2021.
7. H. Witharana and P. Mishra, *Directed test generation for activation of assertions*, SRC TECHCON, 2020.

Miscellaneous Experience

Awards and Achievements

- 2023 — **Gartner Group Graduate Fellowship**, for Outstanding CISE PhD Students (UF).
- 2022 — **Travel Grant**, sponsored by IEEE CEDA to attend ICCAD.
- **Gartner Group Graduate Fellowship**, for Outstanding CISE PhD Students (UF).
- 2020 — **Full Assistantship**, for PhD program in Computer Science (CISE) from University of Florida.
- 2014 — **Merit Scholarship**, to pursue undergraduate studies by the government of Sri Lanka.

Memberships and Certification

- 2022 – Present — **IEEE Student Member**
- 2014 — **Foundation Degree**. Awarded by the Charted Institute of Management Accountants.

Projects

- Sep 2022 - Present — **Compositional Security Verification of Trusted Execution Environments**
  Funding: *Semiconductor Research Corporation (SRC)*
  Role: *Lead Researcher*
- 2022 - 2023 — **Design-for-Debug Architecture for Post-Silicon Security Validation**
  Funding: *National Science Foundation (NSF)*
  Role: *Researcher*
- Jan 2020 - Dec 2022 — **Validation of System-on-Chip Vulnerabilities using Security Assertions**
  Funding: *Semiconductor Research Corporation (SRC)*
  Role: *Lead Researcher*
  Framework: `https://github.com/UFESL/ISV`