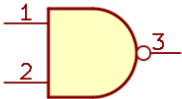# CSCI 463 – Midterm (Fall 2019)

Name: _____ Z-number: _____

Each question has one and only one correct answer. Choose the best possible/most accurate answer for each question.
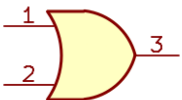
All answers must be given in the context of the lectures and assignments used in the course.
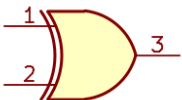
1. What function does this symbol represent?

Ⓐ AND, Ⓑ NAND, Ⓒ OR, Ⓓ NOT, Ⓔ XOR

2. What function does this symbol represent?

Ⓐ AND, Ⓑ NAND, Ⓒ OR, Ⓓ NOT, Ⓔ XOR

3. What function does this symbol represent?

Ⓐ AND, Ⓑ NAND, Ⓒ OR, Ⓓ NOT, Ⓔ XOR
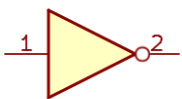
4. What function does this symbol represent?

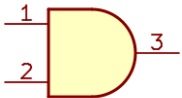

Ⓐ AND, Ⓑ NAND, Ⓒ OR, Ⓓ NOT, Ⓔ XOR

5. What function does this symbol represent?

Ⓐ AND, Ⓑ NAND, Ⓒ OR, Ⓓ NOT, Ⓔ XOR

6. What function does this symbol represent?
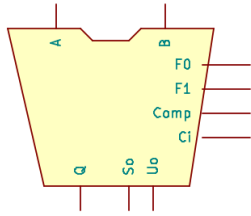
(A) D-latch, (B) Demultiplexer, (C) ALU, (D) Multiplexer, (E) Register

7. What function does this symbol represent?
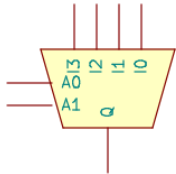
(A) D-latch, (B) Demultiplexer, (C) ALU, (D) Multiplexer, (E) Register

8. What function does this symbol represent?

(A) D-latch, (B) Demultiplexer, (C) ALU, (D) Multiplexer, (E) Register

9. What function does this symbol represent?

(A) D-latch, (B) RS-latch, (C) ALU, (D) Full Adder, (E) Half adder

10. What is the following circuit?

(A) D-latch, (B) RS-latch, (C) ALU, (D) Full Adder, (E) Half adder

11. What is the following circuit?
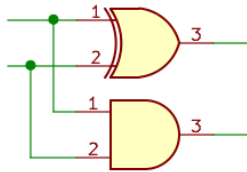
Ⓐ D-latch, Ⓑ RS-latch, Ⓒ ALU, Ⓓ Full Adder, Ⓔ Half adder

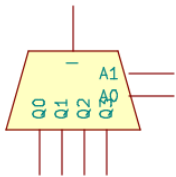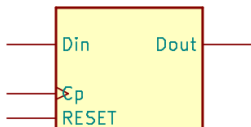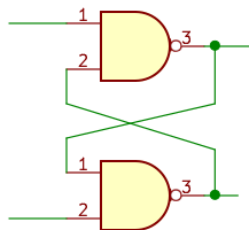**12.** What is the following circuit?
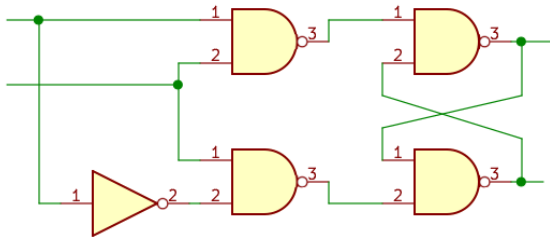
Ⓐ D-latch, Ⓑ RS-latch, Ⓒ ALU, Ⓓ Full Adder, Ⓔ Half adder

13. What is the following circuit?
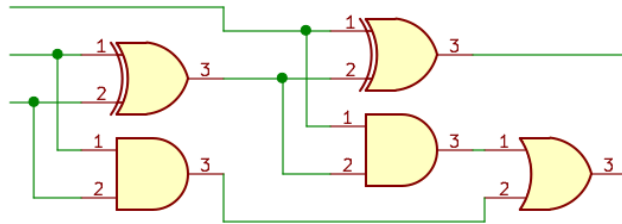
Ⓐ D-latch, Ⓑ RS-latch, Ⓒ ALU, Ⓓ Full Adder, Ⓔ Half adder

14. Which is the truth table for the XOR function?

Ⓐ			Ⓑ			Ⓒ			Ⓓ			Ⓔ		
A	B	Q	A	B	Q	A	B	Q	A	B	Q	A	B	Q
1	1	1	0	0	0	0	0	1	0	0	0	0	0	0
0	1	1	0	1	1	0	1	1	0	1	1	0	1	0
1	0	1	1	0	1	1	0	1	1	0	1	1	0	0
1	1	0	1	1	1	1	1	0	1	1	0	1	1	1

15. Which is the truth table for the OR function?

Ⓐ			Ⓑ			Ⓒ			Ⓓ			Ⓔ		
A	B	Q	A	B	Q	A	B	Q	A	B	Q	A	B	Q
1	1	1	0	0	0	0	0	1	0	0	0	0	0	0
0	1	1	0	1	1	0	1	1	0	1	1	0	1	0
1	0	1	1	0	1	1	0	1	1	0	1	1	0	0
1	1	0	1	1	1	1	1	0	1	1	0	1	1	1

16. Which is the truth table for the NAND function?

A

A	B	Q
1	1	1
0	1	1
1	0	1
1	1	0

B

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

C

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

D

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

E

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

17. What is the clock input used for in those circuits that have one?

(A) To tell time,
(B) To determine when to change its state,
(C) To determine when to change its input,
(D) To disable the output,
(E) To store the demultiplexer output in the ALU

18. Which is the truth table for a full-adder?

A

A	B	Co	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

B

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

C

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

D

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	1	1	1	0
1	1	1	1	0
1	1	1	1	1

E

A	B	Ci	Co	S
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

19. Which is the truth table for a half-adder?

A

A	B	Co	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

B

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

C

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

D

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	1	1	1	0
1	1	1	1	0
1	1	1	1	1

E

A	B	Ci	Co	S
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

20. What is the LSB of the decimal number 1234?

(A) 0, (B) 1, (C) 2, (D) 3, (E) 4

21. What is the LSB of the decimal number 123?

(A) 0, (B) 1, (C) 2, (D) 3, (E) 4

22. What do the signals labeled I0-In do on a multiplexer?

(A) Data inputs, (B) Data outputs, (C) Address inputs, (D) Address outputs, (E) Clock signals

23. What are signals labeled A0-An called on a multiplexer?

(A) Data inputs, (B) Data outputs, (C) Address inputs, (D) Address outputs, (E) Clock signals

24. What do the signals labeled A0-An do on a multiplexer?

   (A) Select which output to enable,
   (B) Select which input to propagate,
   (C) Select which output to disable,
   (D) Select which input to disable,
   (E) Select which boolean function to perform

25. Which signals on a demultiplexer are its inputs?

   (A) A0-An (B) I0-In (C) Q0-Qn (D) Both A and B (E) Both A and C

26. Which signals on a demultiplexer are its outputs?

   (A) A0-An (B) I0-In (C) Q0-Qn (D) Both A and B (E) Both A and C

27. What do the signals labeled F0-Fn do on an ALU?

   (A) Select which output to enable,
   (B) Select which input to propagate,
   (C) Select which arithmetic operation to perform,
   (D) Select which logical operation to perform,
   (E) Both C and D

28. Which circuit can add these two binary numbers: 1101 1100

   (A) RS-latch, (B) Demultiplexer, (C) ALU, (D) Full Adder, (E) Half adder

29. How many full adders are needed to add two signed 8 bit numbers?

   (A) 1, (B) 2, (C) 4, (D) 8, (E) 16

30. What types of clocks are used for registers?

   (A) RS, (B) Level, (C) Edge, (D) Boolean, (E) GPS

31. What is an RS latch used for?

   (A) To reset the ALU,
   (B) To store one bit,
   (C) To store two bits,
   (D) To generate the overflow status,
   (E) To trigger the Multiplexer

32. What is a bus?

   (A) A register,
   (B) To store one bit,
   (C) To store two bits,
   (D) A collection of related signals,
   (E) A collection of unrelated signals

33. Which of the following is true?

   (A) High-level-sensitive latches will retain the input present during the falling edge of the enable signal,
   (B) High-level-sensitive latches allow the output to change multiple times when the enable signal is high,
   (C) Falling-edge-triggered latches retain the input when the clock changes from 1 to 0,
   (D) All of the above
   (E) None of the above

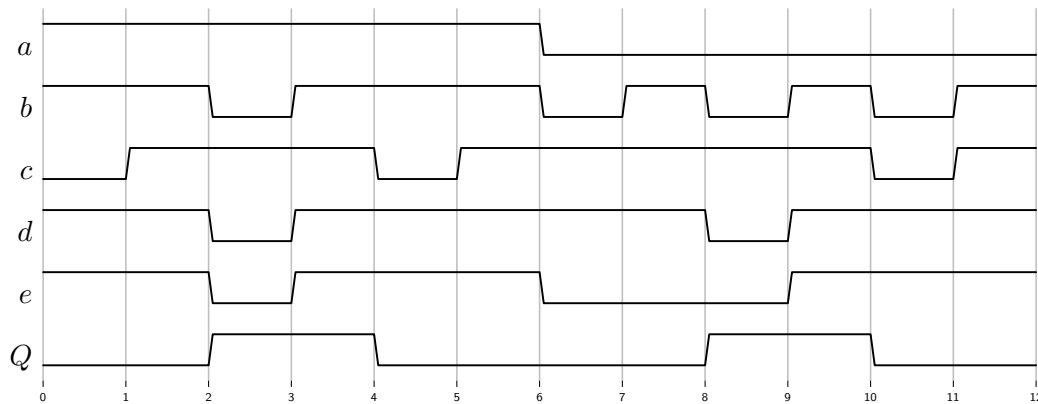The following waveform includes, among other things, the signals of an RS latch whose output is labeled Q:

Figure 1: A Timing Diagram

34. Which signal labeled *a-e* in Figure 1 is the *reset* signal? c

35. Which signal labeled *a-e* in Figure 1 is the *set* signal? d

36. What does overflow mean?

(A) A carry out of the LSB,
(B) A carry into the MSB,
(C) An operation can not fit into the destination register,
(D) A logical operation has no inputs,
(E) A collection of related signals

37. What signifies that an *unsigned* overflow has taken place during an addition?

(A) A carry out of the LSB,
(B) A carry into the MSB,
(C) A carry out of the MSB,
(D) A carry into the LSB that is is different from the carry out of the LSB,
(E) A carry into the MSB that is is different from the carry out of the MSB

38. What signifies that a *signed* overflow has taken place during an addition?

(A) A carry out of the LSB,
(B) A carry into the MSB,
(C) A carry out of the MSB,
(D) A carry into the LSB that is is different from the carry out of the LSB,
(E) A carry into the MSB that is is different from the carry out of the MSB

39. What the hexadecimal value of the binary number 10110001?

(A) 69, (B) C0, (C) 19, (D) C2, (E) B1

40. What the hexadecimal value of the binary number 01101001?

(A) 69, (B) C0, (C) 19, (D) C2, (E) B1

41. What the binary value of the hexadecimal number 22?

(A) 10101010, (B) 11110000, (C) 00000000, (D) 10100101, (E) 00100010

42. What the binary value of the hexadecimal number A5?

(A) 10101010, (B) 11110000, (C) 00000000, (D) 10100101, (E) 00100010

Given the following schematic symbol (that matches that discussed lecture), truth table and waveform diagram (labeled such that time t_0 appears at the far left edge and t_{16} appears at the right):
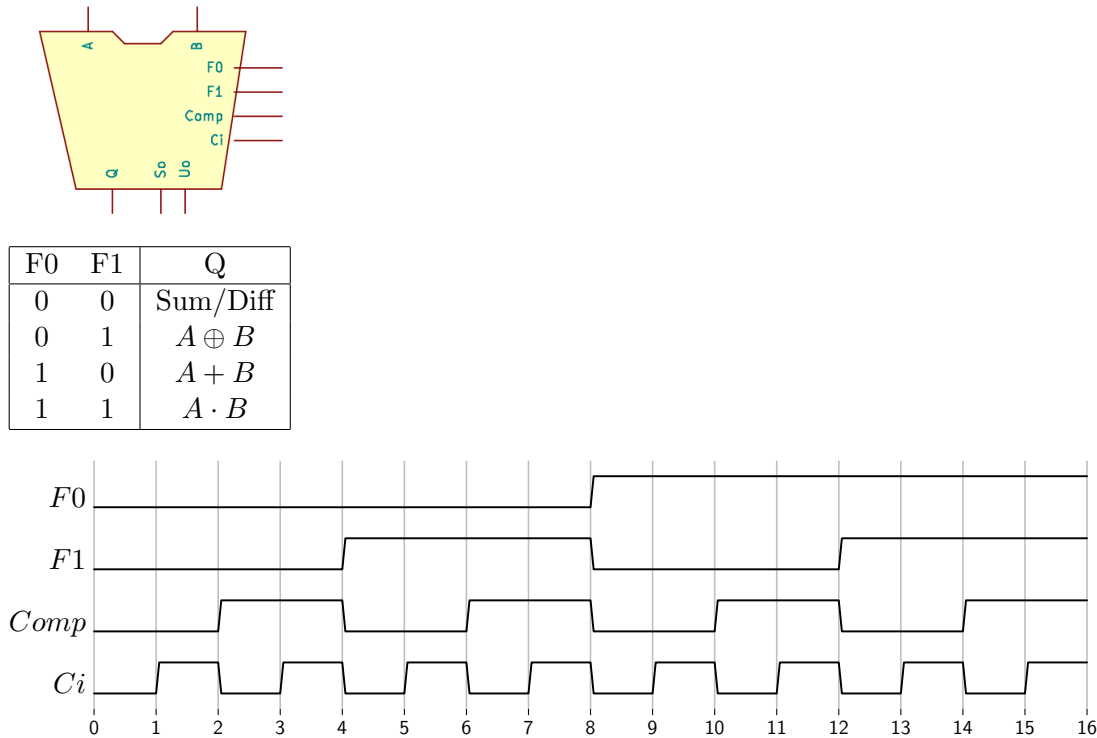

F0	F1	Q
0	0	Sum/Diff
0	1	$A \oplus B$
1	0	$A + B$
1	1	$A \cdot B$

Figure 2: A Timing Diagram

43. What function is being performed between time t_0 and t_1?

    (A) Add, (B) Subtract, (C) XOR, (D) OR, (E) AND

44. What function is being performed between time t_3 and t_4?

    (A) Add, (B) Subtract, (C) XOR, (D) OR, (E) AND

45. What function is being performed between time t_4 and t_5?

    (A) Add, (B) Subtract, (C) XOR, (D) OR, (E) AND

46. What function is being performed between time t_8 and t_9?

    (A) Add, (B) Subtract, (C) XOR, (D) OR, (E) AND

47. What function is being performed between time t_{12} and t_{13}?

    (A) Add, (B) Subtract, (C) XOR, (D) OR, (E) AND

48. What function is being performed between time t_{13} and t_{14}?

    (A) Add, (B) Subtract, (C) XOR, (D) OR, (E) AND

49. What function is being performed between time t_5 and t_6?

    (A) $A \oplus B$, (B) $\overline{A} \cdot B$, (C) $A \cdot B$, (D) $A \cdot \overline{B}$, (E) $A + \overline{B}$

50. What function is being performed between time t_{14} and t_{15}?

    (A) $A \oplus B$, (B) $\overline{A} \cdot B$, (C) $A \cdot B$, (D) $A \cdot \overline{B}$, (E) $A + \overline{B}$